Achieve Ultra-Low Latency for High-Frequency Trading Applications

What You Will Learn

Cisco and Emulex have introduced an innovative low-latency design using the Cisco Nexus® 3548 Switch, a full-featured Ethernet switch offering network latencies of less than 250 nanoseconds, and Emulex's OneConnect Network Xceleration solution leveraging OneConnect OCe12000-D high performance 10GbE network adapter and FastStack DBL powered by Myricom, to reduce host-stack latency by more than 80 percent compared to non-optimized operation.

High-Frequency Trading Overview

High-frequency trading (HFT) applications have brought immense profitability to financial markets over the past few years, making them a popular investment tool for investment firms.

HFT applications support the rapid turnover of positions through the use of sophisticated trading algorithms, which process hundreds of trades in fractions of a second on the basis of changing market conditions. HFT strategies are characterized by a high number of trades and a low average gain per trade. Instead of holding positions for weeks or even months with the goal of generating a few percentage points in return per trade, HFT managers perform multiple trades each minute, gaining a return of a fraction of a percentage point per trade. Positions are often held for an extremely short time, with no positions remaining at the end of the day.

The faster a trading application responds to market signals - completing an analysis, arriving at a decision, and sending a market order - the higher the chances of getting an order filled. The ratio of order fills to orders that are not filled is a common metric for gauging the success a given algorithm and infrastructure.

At the time of this writing, many high-frequency traders implement trading applications that attempt to reach a trade decision in less than 100 microseconds. Achieving such low latency requires an optimized end-to-end trading infrastructure: OS, networking stack, application, and network components. Two such critical components are discussed in this document: the TCP stack and switch fabric.

Optimizing Server-Side Latency

With traditional network APIs, the kernel is involved in almost every network communication. Although this model provides a convenient and well-defined level of abstraction for applications in the HFT market, it presents a tremendous performance bottleneck when latency is a critical design consideration.

Emulex's kernel bypass offering framework for HFT environments, called FastStack DBL, provides network acceleration capability, using a networking stack (TCP or User Datagram Protocol [UDP]) that is implemented in a user library, to which the application links. The FastStack DBL library and its associated networking stack intercept network operations from the application and then manage them entirely in the user space, bypassing the kernel, which significantly improves latency and response-time performance.

FastStack DBL is designed for cases in which target latencies, response time, and jitter could not otherwise be achieved by the OS protocol stack and scheduling policies. In addition to latency, trade accuracy is also playing an important role in HFT environments. That is why firms engaged in high frequency trading are also leveraging Emulex FastStack Sniffer10G to optimize the performance of their trading algorithms. FastStack Sniffer10G provides 100 percent lossless packet capture and injection capability at line rate. This enables developers to run modeling scenarios from captured market data and refine HFT algorithms. The combination of FastStack DBL and FastStack Sniffer10G not only helps to ensure lower trade latency, but also increase trade accuracy.

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Optimizing Network Latency

Trading organizations also need to consider how to decrease the network-component-induced latency. Many HFT designs have already co-located their trading equipment near that of the financial exchange in order to minimize signal propagation latency. Further optimization is needed, however, to reduce latency for packets traversing the switch infrastructure. The Cisco Nexus 3548 offers this optimization by achieving latencies of less than 250 nanoseconds for all workloads - layer 2 and layer 3, unicast and multicast, regardless of features enabled. Cisco *Algo Boost* silicon technology, a core component of the Nexus 3548, pairs ultra low latency with a rich feature set which is essential for running a trading infrastructure, including active buffer monitoring, Network Address Translation (NAT), Switched Port Analyzer (SPAN), and robust Layer 3 capabilities. For more information, refer to http://www.cisco.com/go/nexus3000.

Test Methodology

Any latency metric must consider the standalone latency of each component - in this case, the Cisco 3548 and the Emulex network interface card (NIC) - as well as the latency incurred with multiple components combined. Typically, latency is measured with traditional test equipment (IXIA or Spirent); however, that measure may not reflect the latency from the application's viewpoint. To measure latency that can be easily understood as well accurately measured in microseconds or nanoseconds, this test used a utility developed by Emulex running on the trading servers themselves.

The Emulex FastStack DBL *tcp_pingpong* utility is a pure socket-layer application that bounces TCP or UDP packets from one host to another host and prints latency results in microseconds. It sends a packet, waits for it to receive a response, then sends another packet. It records the length of time between sending a packet and receiving a response and divides by 2 for the half-round-trip latency. It repeats this for a certain number of iterations (the default is 10000, but can be changed). The results presented here are the average time for the packet transfers in microseconds. For each packet transfer, 100,000 packets were sent.

Server Configuration

Two Cisco UCS® C240 M3 Rack Servers were used: one as a server, and the other as a client. Table 1 shows the configuration of the servers. The switch used was the Cisco Nexus 3548.

Table 1: Server Configuration for Tests

Component	Specification
CPU	2 x 2.90-GHz Intel Xeon processor E5-2690
RAM	96 GB (12 x 8GB DDR3-1600-MHz RDIMM ECC)
Hard drive	2 x 1 terabyte (TB) 7.2K RPM
NIC	Emulex OCE12102-DX 10GE adapter
OS	Red Hat Linux 6.2

For more information about the Cisco Nexus 3548, refer to http://www.cisco.com/go/nexus3000.

Latency Results

Solution Latency

Cisco® switching along with the Emulex FastStack DBL network acceleration software delivers 80 percent improvement in latency. Figure 1 compares the results of tests running the Cisco Nexus 3548 and FastStack DBL with the results of tests running the Cisco Nexus 3548 without FastStackDBL.

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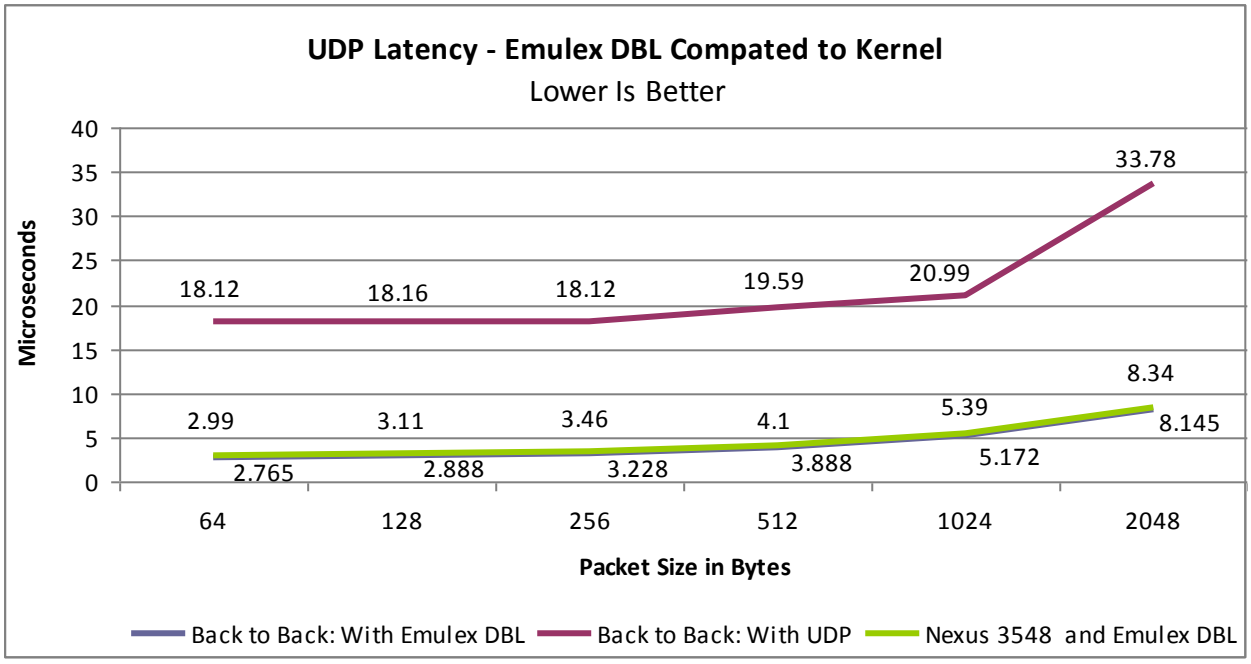
Table 2: Latency Tests

Topology	Used Emulex FastStack DBL?
Back to back	No
Back to back	Yes
With Cisco Nexus 3548	Yes

Figure 1: Latency Results: With the test set listed in Table 2



This latency can be improved by fine-tuning the application and the OS. Fine-tuning was not done for these tests.

After the application and OS are tuned, network latency should be considered. Steps to reduce latency by milliseconds include moving closer to the exchange and decreasing the length of the cable being used. When optimizing at this level, microseconds are too large a measure for latency reduction; instead, the focus is on savings in nanoseconds.

Saving Nanoseconds with Cisco Nexus 3548

Switch latency is derived by subtracting the latency of two Emulex NICs back-to-back from the latency of two Emulex NICs connected through a Nexus 3548. Figure 2 shows the latency of the Cisco Nexus 3548 Switch with the FastStackDBL utility tcp_pingpong. Figure 2 also shows the latency achieved when using a feature called Warp mode, where latency can be improved by upto 20% without impacting any critical features. For further details on Warp mode please visit the Cisco Nexus 3000 homepage at http://www.cisco.com/go/nexus3000.

Table 3: Latency Tests

Topology	Used Emulex FastStack DBL?
Back to back	Yes
With Cisco Nexus 3548	Yes
With Cisco Nexus 3548 (Warp Mode)	Yes

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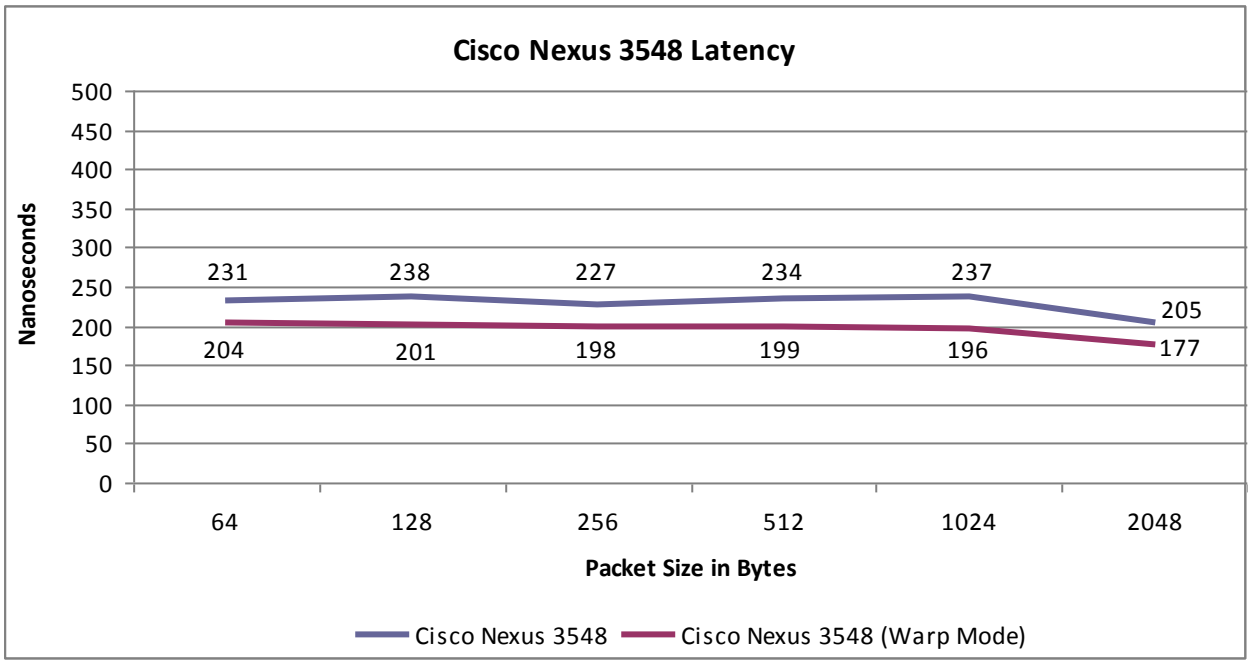
Figure 2: Cisco Nexus 3548 Latency



Conclusion

Latency is a critical consideration in the HFT market. This document shows how to achieve network latencies of less than 250 nanoseconds with the Cisco Nexus 3548, and how to lower server stack latency by up to 80 percent with FastStack DBL. There may be other considerations and tuning that can help reduce latency even more. Please contact your Cisco or Emulex representative for more information.

About Emulex

Emulex, the leader in converged networking solutions, provides enterprise-class connectivity for servers, networks and storage devices within the data center. Emulex's Fibre Channel host bus adapters, 10Gb Ethernet network interface cards, Ethernet-based converged network adapters, controllers, embedded bridges and switches, and connectivity management software are proven, tested and trusted by the world's largest IT environments. Emulex solutions are used and offered by the industry's leading server and storage OEMs including, Apple, Cisco, Dell, EMC, Fujitsu, Hitachi, Hitachi Data Systems, HP, Huawei, IBM, LSI, Lenovo, NEC, Oracle, NetApp, Samsung and ZTE. More information about Emulex (NYSE:ELX) is available at http://www.Emulex.com.

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For More Information

For more information on Emuelx FastStack DBL and FastStack Sniffer10G, please visit:

- http://www.emulex.com/products/network-xceleration-nx-solutions/faststack-dbl/overview.html
- http://www.emulex.com/products/network-xceleration-nx-solutions/faststack-sniffer10g/overview.html

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