



## CHAPTER 6

# Overview of the ATM SPAs

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This chapter provides an overview of the release history, features, and MIB support for the ATM SPAs on the Cisco ASR 1000 Series Aggregation Services Routers. This chapter includes the following sections:

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# Release History

Release	Modification
Cisco IOS XE Release 2.5	<p>The following SPA support was introduced on the Cisco ASR 1000 Series Routers in Cisco IOS XE Release 2.5:</p> <ul style="list-style-type: none"> <li>• 1-Port Clear Channel OC-12 ATM SPA</li> </ul> <p>The following new feature support was introduced for the ATM SPAs in Cisco IOS XE Release 2.5:</p> <ul style="list-style-type: none"> <li>• Access Node Control Protocol (ANCP)</li> <li>• ATM Multipoint Subinterfaces</li> <li>• ATM PVC Ranges</li> <li>• CISCO-PPPOE-MIB</li> <li>• Local Template-Based ATM PVC Provisioning</li> <li>• Point-to-Point Protocol Over Ethernet Over ATM (PPPoEoA)</li> <li>• PPPoE Connection Throttling</li> </ul> <p>In addition to the “<a href="#">Configuring the ATM SPAs</a>” chapter in this guide, see also the new features list for Cisco IOS XE Release 2.5 for more details about these features at:</p> <p><a href="http://www.cisco.com/en/US/products/ps9587/products_feature_guides_list.html">http://www.cisco.com/en/US/products/ps9587/products_feature_guides_list.html</a></p>
Cisco IOS XE Release 2.3	Initial release for the 1-Port Clear Channel OC-3 ATM SPA and 3-Port Clear Channel OC-3 ATM SPA for Cisco ASR 1000 Series Routers.

## Supported Features

This section provides a list of some of the primary features supported by the ATM hardware and software:

- [Basic Features, page 6-2](#)
- [SONET/SDH Error, Alarm, and Performance Monitoring, page 6-3](#)
- [Layer 2 Features, page 6-4](#)
- [Layer 3 Features, page 6-4](#)
- [High Availability Features, page 6-6](#)

## Basic Features

- Bellcore GR-253-CORE SONET/SDH compliance (ITU-T G.707, G.783, G.957, G.958)
- Interface-compatible with other Cisco ATM adapters

**Note**

The ATM SPA is functionally similar to other ATM port adapters on the Cisco ASR 1000 Series Routers, but because it is a different card type, the configuration for the slot is lost when you replace an existing ATM port adapter with an ATM SPA in a SIP.

- RFC 2684: *Multiprotocol Encapsulation over ATM Adaptation Layer 5* (formerly RFC 1483).
- Supports permanent virtual circuits (PVCs)
- IEEE 802.1QinQ
- ATM adaptation layer 5 (AAL5) for data traffic.
- Uses small form-factor pluggable (SFP) optical transceivers, allowing the same ATM SPA hardware to support multimode (MM), single-mode intermediate (SMI), or single-mode long (SML) reach, depending on the capabilities of the SPA.
- ATM section, line, and path alarm indication signal (AIS) cells, including support for F4 and F5 flows, loopback, and remote defect indication (RDI).
- Operation, Administration, and Maintenance (OAM) cells.
- Online insertion and removal (OIR) of individual ATM SPAs from the SIP, as well as OIR of the SIPs with ATM SPAs installed.

## SONET/SDH Error, Alarm, and Performance Monitoring

- Fiber removed and reinserted
- Signal failure bit error rate (SF-BER)
- Signal degrade bit error rate (SD-BER)
- Signal label payload construction (C2)
- Path trace byte (J1)
- Section Diagnostics:
  - Loss of signal (SLOS)
  - Loss of frame (SLOF)
  - Error counts for B1
  - Threshold crossing alarms (TCA) for B1 (B1-TCA)
- Line Diagnostics:
  - Line alarm indication signal (LAIS)
  - Line remote defect indication (LRDI)
  - Line remote error indication (LREI)
  - Error counts for B2
  - Threshold crossing alarms for B2 (B2-TCA)
- Path Diagnostics:
  - Path alarm indication signal (PAIS)
  - Path remote defect indication (PRDI)
  - Path remote error indication (PREI)

- Error counts for B3
- Threshold crossing alarms for B3 (B3-TCA)
- Loss of pointer (PLOP)
- New pointer events (NEWPTR)
- Positive stuffing event (PSE)
- Negative stuffing event (NSE)
- The following loopback tests are supported:
  - Network (line) loopback
  - Internal (diagnostic) loopback
- Supported SONET/SDH synchronization:
  - Local (internal) timing (for inter-router connections over dark fiber or wavelength division multiplexing [WDM] equipment)
  - Loop (line) timing (for connecting to SONET/SDH equipment)
  - +/- 4.6 ppm clock accuracy over full operating temperature

## Layer 2 Features

- Supports the following encapsulation types:
  - AAL5SNAP (LLC/SNAP)
  - AAL5MUX (VC multiplexing)
  - AAL5NLPID
- Supports the following ATM traffic classes and per-VC traffic shaping modes:
  - Constant bit rate (CBR) with peak rate
  - Unspecified bit rate (UBR) with peak cell rate (PCR)
  - Non-real-time variable bit rate (VBR-nrt)
  - Variable bit rate real-time (VBR-rt)




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**Note** ATM shaping is supported, but class queue-based shaping is not.

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- ATM multipoint connections (beginning in Cisco IOS XE Release 2.5)
- ATM point-to-point connections
- Explicit Forward Congestion Indication (EFCI) bit in the ATM cell header
- AToM VP and VC Mode Cell Relay support
- RFC 2225, *Classical IP and ARP over ATM* (obsoletes RFC 1577)

## Layer 3 Features

- ATM over MPLS (AToM) in AAL0 VC and VP mode

- No limitation on the maximum number of VCs per VPI, up to the maximum number of 4,096 total VCs per interface (so there is no need to configure this limit using the **atm vc-per-vp** command, which is required on other ATM SPAs)
- OAM flow connectivity using OAM ping for segment or end-to-end loopback
- PVC multicast (Protocol Independent Multicast [PIM] dense and sparse modes)
- PVC ranges (beginning in Cisco IOS XE Release 2.5)
- Supports oversubscription by default
- Routing protocols:
  - Border Gateway Protocol (BGP)
  - Enhanced Interior Gateway Routing Protocol (EIGRP)
  - Interior Gateway Routing Protocol (IGRP)
  - Integrated Intermediate System-to-Intermediate System (IS-IS)
  - Open Shortest Path First (OSPF)
  - Routing Information Protocol version 1 and version 2 (RIPv1 and RIPv2)

## High Availability Features

- Route Processor Redundancy (RPR)
- OSPF Nonstop Forwarding (NSF)
- Stateful Switchover (SSO)

## Restrictions

- The ATM SPAs in the Cisco ASR 1000 Series Routers do not support APS reflector and reflector channel modes. (These modes require a facing path terminating element [PTE], which is typically a Cisco ATM switch.)
- The ATM SPAs in the Cisco ASR 1000 Series Routers do not support a data path on the main interface. Data is only supported in subinterface configuration.
- Link Fragmentation and Interleaving (LFI) processing is not supported.
- Integrated Local Management Interface (ILMI) is not supported.
- Multipoint subinterfaces are not supported in releases prior to Cisco IOS XE Release 2.5.
- Routed Bridge Encapsulation Subinterface Grouping is not supported.
- For best performance, we recommend the following maximums:

### Releases Prior to Cisco IOS XE Release 2.5

In releases before Cisco IOS XE Release 2.5, an absolute maximum of 1,000 (1K) configured VCs per ATM SPA (1,000 [1K] per interface) with the following recommended limitations:

- A recommended maximum number of 1,000 PVCs on all point-to-point subinterfaces for all ATM SPAs in a SIP.
- A recommended maximum number of 1,024 PVCs using service policies for all ATM SPAs in a SIP.

### Cisco IOS XE Release 2.5 and Later

Beginning in Cisco IOS XE Release 2.5, the following recommended limits are supported:

- 4,000 VCs per interface
- 12,000 VCs per SPA
- 32,000 VCs per system (Cisco ASR 1000 Series Router)



**Note** These limits are flexible and depend on all factors that affect performance in the router, such as processor card, type of traffic, and so on.

- A maximum number of 4,000 PVCs configured with Modular QoS CLI (MQC) policy maps.
- In the default configuration of the transmit path trace buffer, the ATM SPA does not support automatic updates of remote host name and IP address (as displayed by the **show controllers atm** command). This information is updated only when the interface is shut down and reactivated (using the **shutdown** and **no shutdown** commands). Information for the received path trace buffer, however, is automatically updated.

- For ATM SPAs on the Cisco ASR1000 series routers, ISSU from releases prior to Cisco IOS XE Release 2.5.0 to Cisco IOS XE Release 2.5.0, or from Cisco IOS XE Release 2.5.0 to a release prior to Cisco IOS XE Release 2.5.0, is not supported. If you want to perform ISSU in this environment, you must first remove the configuration from the ATM SPAs on the router, and then shut down the SPAs using the **shutdown** command prior to running the ISSU process.

## Supported MIBs

The following MIBs are supported in Cisco IOS XE Release 2.3 and later releases for the ATM SPAs on the Cisco ASR 1000 Series Routers.

- ATM-MIB
- CISCO-AAL5-MIB
- CISCO-ATM-EXT-MIB
- CISCO-CLASS-BASED-QOS-MIB
- CISCO-ENTITY-ALARM-MIB
- CISCO-ENTITY-EXT-MIB
- CISCO-ENTITY-FRU-CONTROL-MIB
- CISCO-ENTITY-ASSET-MIB
- CISCO-ENTITY-SENSOR-MIB
- CISCO-IETF-PW-MIB
- CISCO-IETF-PW-MPLS-MIB
- CISCO-IF-EXTENSION-MIB
- CISCO-MQC-MIB
- CISCO-PPPOE-MIB (beginning in Cisco IOS XE Release 2.5)
- CISCO-SONET-MIB
- ENTITY-MIB
- ENTITY-SENSOR-MIB
- IF-MIB
- MIB-II
- MPLS-CEM-MIB
- OLD-CISCO-CHASSIS-MIB
- SONET-MIB

For more information about MIB support on a Cisco ASR 1000 Series Routers, refer to the *Cisco ASR 1000 Series Aggregation Services Routers MIB Specifications Guide*, at the following URL:

<http://www.cisco.com/en/US/docs/routers/asr1000/mib/guide/asr1kmib.html>

To locate and download MIBs for selected platforms, Cisco IOS releases, and feature sets, use Cisco MIB Locator found at the following URL:

<http://tools.cisco.com/ITDIT/MIBS/servlet/index>

If Cisco MIB Locator does not support the MIB information that you need, you can also obtain a list of supported MIBs and download MIBs from the Cisco MIBs page at the following URL:

<http://www.cisco.com/public/sw-center/netmgmt/cmtk/mibs.shtml>

To access Cisco MIB Locator, you must have an account on Cisco.com. If you have forgotten or lost your account information, send a blank e-mail to [cco-locksmith@cisco.com](mailto:cco-locksmith@cisco.com). An automatic check will verify that your e-mail address is registered with Cisco.com. If the check is successful, account details with a new random password will be e-mailed to you. Qualified users can establish an account on Cisco.com by following the directions found at this URL:

<http://www.cisco.com/register>

## SPA Architecture

This section provides an overview of the data path for the ATM SPAs, for use in troubleshooting and monitoring. [Figure 6-1](#) shows the data path for ATM traffic as it travels between the ATM optical connectors on the front panel of the ATM SPA to the backplane connector that connects the SPA to the SIP.

**Figure 6-1** ATM SPA Data Architecture



**Note**

LFI processing is not supported on the Cisco ASR 1000 Series Routers.

## Path of Cells in the Ingress Direction

The following steps describe the path of an ingress cell as it is received from the ATM network and converted to a data packet before transmission through the SIP to the router's processors for switching, routing, or further processing:

1. The SONET/SDH framer device receives incoming cells on a per-port basis from the SPA's optical circuitry. The actual number of optical ports depends on the model of ATM SPA on the Cisco ASR 1000 Series Routers.
2. The SONET/SDH framer removes the SONET overhead information, performs any necessary clock and data recovery, and processes any SONET/SDH alarms that might be present. The framer then extracts the 53-byte ATM cells from the data stream and forwards each cell to the ATM segmentation and reassembly (SAR) engine using one channel per physical port supported by the SPA.

3. The SAR engine receives the cells from the framer and reassembles the cells into the original packets, temporarily storing them in a per-port receive buffer until they can be forwarded (using one channel per physical port) to the field-programmable gate array (FPGA). The SAR engine discards any cells that have been corrupted in transit.

The SAR also sends in-band Event Based Flow Control (EBFC) and Weighted Random Early Detection (WRED) statistic packets to the FPGA using two additional channels.

4. The FPGA receives the packets from the SAR engine and forwards them to the host processor (using one channel per physical port) for further routing, switching, or additional processing. The FPGA also collects the traffic statistics for the packets that it passes.

## Path of Packets in the Egress Direction

The following steps describe the path of an egress packet as the SPA receives it from the router through the SIP and converts it to ATM cells for transmission on the ATM network:

1. The FPGA receives the packets from the host processor (using one channel per physical port) and stores them in its packet buffers until the SAR engine is ready to receive them. The ATM shim header is replaced by the appropriate canonical header for the SAR and the whole packet is forwarded to the SAR.

The FPGA also collects the traffic statistics for the packets that it passes, and any errored packets are flagged and forwarded to the SAR. The FPGA uses two channels to forward traffic to the SAR: one for AAL5 traffic and one for cell unbundling traffic.

2. The SAR engine receives the packets from the FPGA and supports multiple CBWFQ queues to store the packets until they can be fully segmented. If any errored data is detected, it is dropped within the SAR. The SAR engine performs the necessary WRED queue admission and CBWFQ QoS traffic scheduling on its queues before segmenting the packets into ATM cells and shaping the cells into the SONET/SDH framer. The SAR controls all of the traffic shaping and will drop traffic as necessary due to congestion. The ATM cells are transmitted to the SONET/SDH framer using one channel per physical port.
3. The SONET/SDH framer receives the cells from the SAR engine, optionally adds a header check sequence (HCS) and scrambles the cell, and then inserts each cell into the SONET payload, adding the necessary clocking, SONET overhead, and alarm information. The framer also inserts idle cells as needed to fill the payload. The framer then transmits the payload along with the SONET frame complete with all the appropriate section, line and path overhead.
4. The optical port conveys the optical data onto the physical layer of the ATM network.

## Displaying the SPA Hardware Type

To verify the SPA hardware type that is installed in your Cisco ASR 1000 Series Routers, use the **show interfaces**, or **show controllers** commands. A number of other **show** commands also provide information about the SPA hardware.

Table 6-1 shows the hardware description that appears in the **show interfaces** command output for each ATM SPA that is supported on the Cisco ASR 1000 Series Routers:

**Table 6-1 ATM SPA Hardware Descriptions in show interfaces Command**

SPA	Description in show interfaces Command
SPA-1XOC3-ATM-V2	“Hardware is SPA-1XOC3-ATM-V2”
SPA-3XOC3-ATM-V2	“Hardware is SPA-3XOC3-ATM-V2”
SPA-1XOC12-ATM-V2	“Hardware is SPA-1XOC12-ATM-V2”

## Example of the show interfaces Command

The following example shows output from the **show interfaces atm** command on a Cisco ASR 1000 Series Routers with an ATM SPA installed in the second subslot of a SIP that is installed in slot 0:

```
Router#show interfaces atm 0/2/2
ATM0/2/2 is up, line protocol is up
  Hardware is SPA-3XOC3-ATM-V2, address is 001a.3044.7522 (bia 001a.3044.7522)
  MTU 4470 bytes, sub MTU 4470, BW 149760 Kbit, DLY 80 usec,
    reliability 255/255, txload 1/255, rxload 1/255
  Encapsulation ATM, loopback not set
  Keepalive not supported
  Encapsulation(s): AAL5 AAL0
  4095 maximum active VCs, 1 current VCCs
  VC Auto Creation Disabled.
  VC idle disconnect time: 300 seconds
  4 carrier transitions
  Last input never, output 00:04:11, output hang never
  Last clearing of "show interface" counters never
  Input queue: 0/375/0/0 (size/max/drops/flushes); Total output drops: 0
  Queueing strategy: fifo
  Output queue: 0/40 (size/max)
  5 minute input rate 0 bits/sec, 0 packets/sec
  5 minute output rate 0 bits/sec, 0 packets/sec
    5 packets input, 540 bytes, 0 no buffer
    Received 0 broadcasts (0 IP multicasts)
    0 runts, 0 giants, 0 throttles
    0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored, 0 abort
    5 packets output, 540 bytes, 0 underruns
    0 output errors, 0 collisions, 1 interface resets
    0 output buffer failures, 0 output buffers swapped out
```

## Example of the show controllers Command

The following example shows output from the **show controllers atm** command on a Cisco ASR 1000 Series Routers with an ATM SPA installed in the second subslot of a SIP that is installed in slot 0:

```
Router# show controllers atm 0/2/2
Interface ATM0/2/2 (SPA-3XOC3-ATM-V2[0/2]) is up
  Framing mode: SONET OC3 STS-3c
SONET Subblock:
SECTION
  LOF = 0          LOS   = 1          BIP(B1) = 0
LINE
  AIS = 0          RDI   = 1          FEBE = 55          BIP(B2) = 0
PATH
  AIS = 0          RDI   = 1          FEBE = 21          BIP(B3) = 0
```

```
LOP = 1          NEWPTR = 0          PSE = 0          NSE = 0

Active Defects: None
Active Alarms:  None
Alarm reporting enabled for: SF SLOS SLOF B1-TCA B2-TCA PLOP B3-TCA

ATM framing errors:
  HCS (correctable):  0
  HCS (uncorrectable): 0

APS
not configured
COAPS = 0          PSBF = 0
State: PSBF_state = False
Rx(K1/K2): 00/00  Tx(K1/K2): 00/00
Rx Synchronization Status S1 = 00
S1S0 = 00, C2 = 13
PATH TRACE BUFFER : STABLE

BER thresholds:  SF = 10e-3  SD = 10e-6
TCA thresholds:  B1 = 10e-6  B2 = 10e-6  B3 = 10e-6

Clock source:  line
```

