# Active and Standby Control Card States During a WAN Switch Software Upgrade

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 **Caution:** The information in this document is based on a BPX switch software upgrade from version 9.2.40 to version 9.3.36, and is designed only to illustrate how control card states change during an upgrade.

## Introduction

This document explains the states that Broadband Control Cards (BCCs) pass through during a Switch Software (SWSW) upgrade, and uses an upgrade from 9.2.40 to 9.3.36 on a BPX as an example. The Card State, RAM, ROM, and BRAM fields all reflect the values displayed for a selected Controller Card by the **dspcds** command. The Primary and Secondary **dsprevs** command output fields reflect the values displayed by the **dsprevs** command. The switch software upgrade commands described in this document require SuperUser login and password. Briefly, the entire switch software upgrade process consists of a sequence of three commands that you can execute from the command line interface (CLI):

1. **loadrev** ***target_software_version nodename***

   **Note:** This command is commonly referred to as the "first loadrev".

2. **runrev** ***target_software_version nodename***

   **Note:** This command is commonly referred to as the "runrev". The SuperUser needs to log back in to use the final, next, command.

3. **loadrev** ***target_software_version nodename***

   **Note:** This command is commonly referred to as the "second loadrev".

Each of the three commands represents a significant amount of activity for the active and standby controller cards. The first **loadrev** command precipitates the largest number of state changes.

# Prerequisites

## Requirements

Readers of this document should refer to and be knowledgeable of the following for complete details on how to safely execute their planned upgrade:

- The applicable WAN Switch Software Release Notes
- WAN Switch Software Upgrade Planner
- WAN Switch Software Upgrade Script

## Components Used

The information in this document is based on these software and hardware versions:

- SWSW 9.2.40
- SWSW 9.3.36

The information in this document was created from the devices in a specific lab environment. All of the devices used in this document started with a cleared (default) configuration. If your network is live, make sure that you understand the potential impact of any command.

## Conventions

For more information on document conventions, refer to the Cisco Technical Tips Conventions.

# BCC States Before the Upgrade Begins

This table shows the BCC states before the start of the upgrade from 9.2.40 to version 9.3.36:

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|

| | | | | | | |
|---|---|---|---|---|---|---|
| BCC slot 7 | Active | 9.2.40 | 9.2.40 | 9.2.40 | Running 9.2.40 | — |
| BCC slot 8 | Standby | 9.2.40 | 9.2.40 | 9.2.40 | — | — |

# BCC States During the First loadrev Command

This table shows the BCC states after the SuperUser uses the **loadrev 9.3.36** ***nodename*** command:

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | Active | 9.2.40 | 9.2.40 | 9.2.40 | Running 9.2.40 | Unavailable 9.3.36 |
| BCC slot 8 | Standby | 9.2.40 | 9.2.40 | 9.2.40 | — | — |

**Note:** If the BPX does not locate switch software version 9.3.36, the **dsprevs** command output screen displays `Unavailable 9.3.36` until the **loadrev 9.2.40** ***nodename*** command is issued to restore the secondary image.

Once version 9.3.36 is found in a neighbor switch, a connected StrataView (SVlite), or a Cisco WAN Manager (CWM) workstation, the active BCC ROM is cleared and programmed with version 9.3.36. You can use the **dspdnld** command monitor the ROM erasure and the version 9.3.36 load. The **dsprevs** command output screen transitions from `Unavailable` to `Downloading` when the ROM is erased and ready to accept the 9.3.36 image.

This table shows that the ROM is erased:

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | Active | 9.2.40 | — | 9.2.40 | Running 9.2.40 | Unavailable 9.3.36 |
| BCC slot 8 | Standby | 9.2.40 | 9.2.40 | 9.2.40 | — | — |

This table shows that version 9.3.36 is loading into the ROM:

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | Active | 9.2.40 | — | 9.2.40 | Running 9.2.40 | Downloading 9.3.36 |
| BCC slot 8 | Standby | 9.2.40 | 9.2.40 | 9.2.40 | — | — |

Once version 9.3.36 is downloaded to the active BCC ROM, it is then downloaded to the standby BCC RAM (DRAM and Configuration). This causes two separate state changes during which the standby BCC in slot 8 is automatically removed from the BPX twice. During this stage, the standby BCC Boot ID field is blank until version 9.3.36 is successfully downloaded to the RAM. You can use the **dspdnld** command to monitor the image load to the standby BCC DRAM.

The next three tables show the state transitions of the standby BCC as it is removed from the BPX the first time.

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | Active | 9.2.40 | 9.3.36 | 9.2.40 | Running 9.2.40 | Loaded 9.3.36 |
| BCC slot 8 | Removed | — | — | — | — | — |

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | Active | 9.2.40 | 9.3.36 | 9.2.40 | Running 9.2.40 | Loaded 9.3.36 |
| BCC slot 8 | DnLder | — | 9.2.40 | 9.2.40 | — | — |

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | Active | 9.2.40 | 9.3.36 | 9.2.40 | Running 9.2.40 | Loaded 9.3.36 |
| BCC slot 8 | DnLding | — | 9.2.40 | 9.2.40 | — | — |

This table shows the card states when version 9.3.36 is successfully downloaded:

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | Active | 9.2.40 | 9.3.36 | 9.2.40 | Running 9.2.40 | Loaded 9.3.36 |
| BCC slot 8 | DnLded | — | 9.2.40 | 9.2.40 | — | — |

This table shows that the standby BCC is then removed a second time:

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|

| | | | | | | |
|---|---|---|---|---|---|---|
| BCC slot 7 | Active | 9.2.40 | 9.3.36 | 9.2.40 | Running 9.2.40 | Loaded 9.3.36 |
| BCC slot 8 | Removed | — | — | — | — | — |

This table shows that the standby BCC database is then reformatted according to the required structure for version 9.3.36:

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | Active | 9.2.40 | 9.3.36 | 9.2.40 | Running 9.2.40 | Upgrading 9.3.36 |
| BCC slot 8 | Upgrading | — | 9.2.40 | 9.2.40 | — | — |

The first **loadrev** command is now complete. This table shows the BCC states as they should appear:

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | Active | 9.2.40 | 9.3.36 | 9.2.40 | Running 9.2.40 | Upgraded 9.3.36 |
| BCC slot 8 | Upgraded | 9.3.36 | 9.2.40 | 9.2.40 | — | — |

# BCC States During the runrev

After you use the **runrev** command, version 9.3.36 is executed and running on the BCC in slot 8. The **switchcc** command is used by the **runrev** command process to transition to the BCC in slot 8 with the upgraded database. After the **runrev** command is successfully executed, the SuperUser must log back into the BPX. The BCC in slot 7 still has the database associated with version 9.2.40. This allows version 9.2.40 to be restored to the BPX using the **runrev 9.2.40** ***nodename*** command. After the command is issued, the BPX is running switch software version 9.3.36, and upgrade verification tests can then be performed.

**Note:** While the BCC in slot 7 is in the locked state, any network configuration changes, such as adding a connection, are not communicated to the BCC. This places the BPX at risk for a database inconsistency if the node experiences a fault on the BCC in slot 8. The length of time a switch spends in the locked state should be kept to the minimum required to accomplish network upgrade verification tests. Refer to Network Characteristics Cannot Be Modified When IGX 8400 and BPX 8600 Nodes Are Unreachable for more information.

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|

| | | | | | | |
|---|---|---|---|---|---|---|
| BCC slot 7 | Locked | 9.2.40 | 9.3.36 | 9.2.40 | — | — |
| BCC slot 8 | Active | 9.3.36 | 9.2.40 | 9.3.36 | Running 9.3.36 | Loaded 9.2.40 |

# BCC States During the Second loadrev

The second **loadrev** command, also known as "Unlocking the Processors", is the final step in the upgrade to 9.3.36. When you use the **loadrev 9.3.36** ***nodename*** command, the ability to revert back to 9.2.40 is lost. This is indicated by the absence of version 9.2.40 in the **dsprevs** command output screen. Any subsequent downgrade requires the **clrallcnf** command to correct any inconsistencies in the BCC database brought on by the different memory structure of the older release. During the second **loadrev** command, version 9.3.36 is downloaded into the RAM (DRAM and Configuration) of the BCC in slot 7. During this process, the BCC in slot 7 is automatically removed from the BPX. You can use the **dspdnld** command to monitor the image load into the BCC DRAM in slot 7. The second **loadrev** command also completes the 9.3.36 image load into the ROM of the BCC in slot 8.

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | DnLder | — | 9.3.36 | 9.3.36 | — | — |
| BCC slot 8 | Active | 9.3.36 | — | 9.3.36 | Running 9.3.36 | — |

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | DnLded | 9.3.36 | 9.3.36 | 9.3.36 | — | — |
| BCC slot 8 | Active | 9.3.36 | — | 9.3.36 | Running 9.3.36 | — |

This table shows that the BCC in slot 7 is removed to prepare for the `Standby` status:

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | Removed | — | — | — | — | — |
| BCC slot 8 | Active | 9.3.36 | — | 9.3.36 | Running 9.3.36 | — |

This table shows that the standby BCC database is updating:

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | Update | 9.3.36 | 9.3.36 | 9.3.36 | — | — |
| BCC slot 8 | Active | 9.3.36 | — | 9.3.36 | Running 9.3.36 | — |

After the standby BCC in slot 7 is updated, the active BCC in slot 8 downloads version 9.3.36 into ROM. This table shows that the upgrade to 9.3.36 is now complete:

| Controller Card | Card State | RAM | ROM | BRAM | Primary dsprevs Output | Secondary dsprevs Output |
|---|---|---|---|---|---|---|
| BCC slot 7 | Standby | 9.3.36 | 9.3.36 | 9.3.36 | — | — |
| BCC slot 8 | Active | 9.3.36 | 9.3.36 | 9.3.36 | Running 9.3.36 | — |

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|---|
| Network Infrastructure: WAN Routing and Switching |

# Related Information

- **Cisco WAN Switching Solutions - Cisco Documentation**
- **Guide to New Names and Colors for WAN Switching Products**
- **Software Center - WAN Switching Software**
- **Technical Support - Cisco Systems**