



ONS 15454 Timing Issues

[TAC Notice: What's Changing on TAC Web](#)

Document ID: 15234

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Introduction

There are several common issues that arise when you configure timing on the Cisco ONS 15454. This document explains these issues and provides an example of a timing best practice that you can use in a four-node ONS 15454 network. This document covers these areas:

- [BITS backplane pins for external timing references](#)
- [Timing alarm types](#)
- [Timing concepts](#)
- [Simple Timing Topology Lab setup](#)
- [Best Practice Timing Topology Lab setup](#)
- [Timing configuration screen for external timing](#)
- [Alarms screen when configuring external timing](#)
- [Timing configuration screen for line timing](#)
- [Alarms screen when configuring line timing](#)
- [Timing topology changes when a ring is broken](#)
- [Using alarm screens to explain timing topology resynchronization](#)
- [Using alarm screens to explain timing topology recovery \(reversion\)](#)

Use this document with the [Setting Up ONS 15454 Timing](#) section of the Cisco ONS 15454 User Documentation. The lab setup used is based on the network shown in the user documentation. However, this document can also be used as a standalone configuration and troubleshooting guide.

Note: It is necessary to set the Synchronous Optical Network (SONET) timing parameters for each ONS 15454. Timing can be set to either the external, line, or mixed node. In most ONS 15454 networks, one node is set to external, and the other nodes are set to line. The external node accepts its timing from a Building Integrated Timing Supply (BITS) source wired to the BITS backplane pins. The BITS source, in turn, gets its timing from a Primary Reference Source (PRS), such as a Stratum 1 (ST1) clock or Global Positioning Satellite (GPS) signal. The line nodes accept their timing from optical carrier cards. For protection, up to three timing references can be identified. These are typically two BITS level or line-level sources and an internal reference. The internal reference is the Stratum 3 (ST3) clock provided on every ONS 15454 Timing Communication and Control (TCC) card.

[Table 1](#) shows the clock accuracy and why we are an ST3. When the ONS 15454 goes into holdover

and is timing from its own internal clock, the timing source must be within the timing tolerance for a minimum of 24 hours.

Table 1 – Clock Accuracy

Stratum Accuracy	Adjustment Range	Pull-In-Range	Stability	Time To First Frame Slip
1 1 x	10-11	NA	NA	72 days
2 1.6 x	10-8	Must be able to synchronize to clock with accuracy of $\pm 1.6 \times 10^{-8}$ 1 x	10-10/day	14 days
3E 4.6 x	10-6	Must be able to synchronize to clock with accuracy of $\pm 4.6 \times 10^{-6}$ 1 x	10-8/day	17 hours
3 4.6 x	10-6	Must be able to synchronize to clock with accuracy of $\pm 4.6 \times 10^{-6}$ 3.7 x	10-7/day	23 minutes
SONET Minimum Clock 20 x	10-6	Must be able to synchronize to clock with accuracy of $\pm 20 \times 10^{-6}$	Not specified	Not specified
4E 32 x	10-6	Must be able to synchronize to clock with accuracy of $\pm 32 \times 10^{-6}$	Same as Accuracy	Not specified
		Must be		

4 32 x	10-6	able to synchronize to clock with accuracy of $\pm 32 \times 10^{-6}$	Same as Accuracy	Not specified
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Prerequisites

Requirements

There are no specific requirements for this document.

Components Used

This document is not restricted to specific software and hardware versions.

Conventions

For more information on document conventions, see the [Cisco Technical Tips Conventions](#).

Timing Concepts

A common mistake is to think that the timing reference is controlled from an ONS 15454 node to its adjacent node. This is not true. Each node independently accepts its own timing reference from one of three sources:

- The BITS Input pins on the ONS 15454 backplane.
- An optical carrier card installed in the ONS 15454.
- The internal ST3 clock on the TCC/TCC+/TCC2 card.

If the timing comes from the BITS Input pins, the ONS 15454 has to be set for external timing. If the timing comes from an optical carrier card, the ONS 15454 has to set for line timing. The default timing source is the internal ST3 clock. The ONS 15454 can be set for either external, line, mixed, or internal timing. The ONS 15454 times all of its interfaces by the timing source that it accepts.

Note: DS-1s delivered over traffic links are not suitable BITS sources. The primary reason for this is that SONET compensation for off-frequency DS-1s results in jitter because controlled slips are not performed.

Mixed Mode Timing

In external timing mode, the Reference List options include two BITS sources and the internal clock. In line timing mode the Reference List options include all optical ports and the internal clock. With mixed mode timing, both external and line timing sources can be included in the synchronization Reference List. Exercise caution when you use mixed mode timing because it can result in inadvertent timing loops. The CTC screen below shows how mixed mode timing is provisioned.

Note: The Reference List includes both BITS and optical ports as timing sources.

Internal (Free-Running) Synchronization

The ONS 15454 has an internal clock in the TCC/TCC+/TCC2 that is used to track a higher quality reference. In the event of node isolation, the clock provides holdover timing or a free-running clock source. The internal clock is a certified ST3 clock with enhanced capabilities that match the Stratum 3E specifications for:

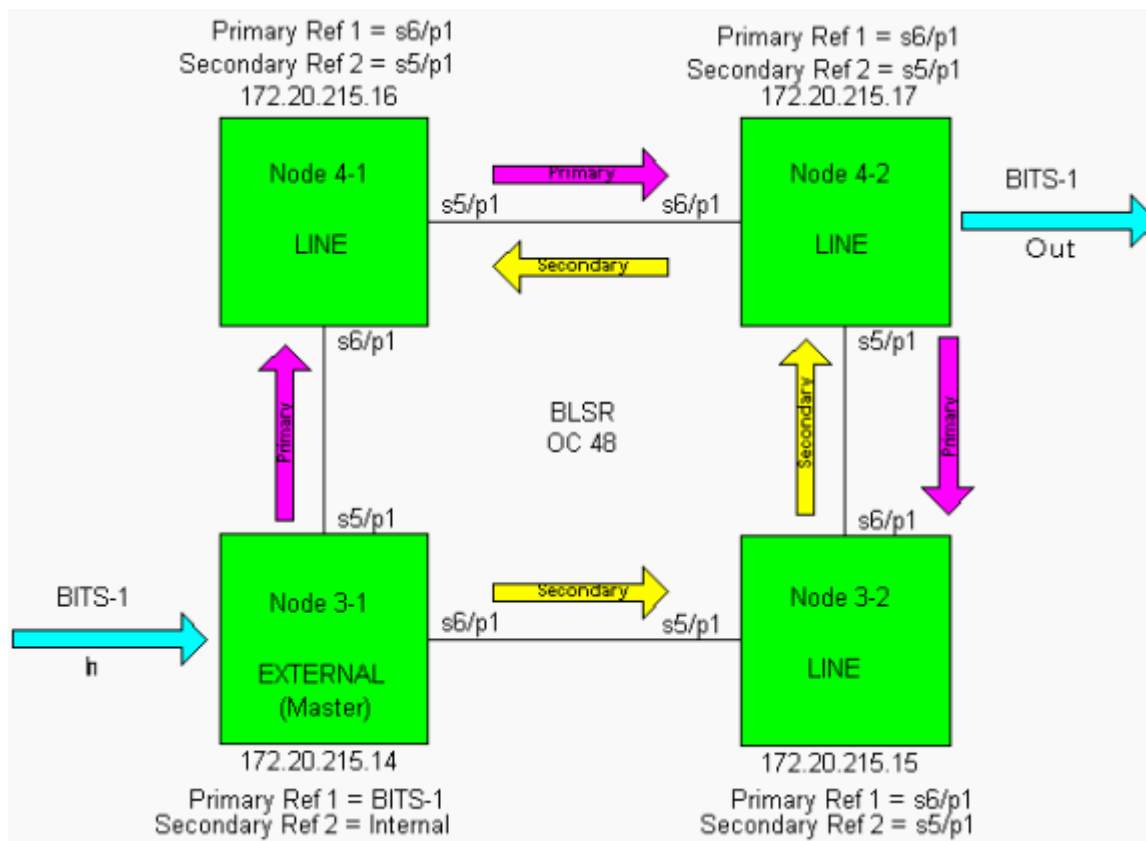
- Free-run accuracy.
- Holdover frequency drift.
- Wander tolerance.
- Wander generation.
- Pull-in and hold-in.
- Reference locking/settling time.
- Phase transient (tolerance and generation).

A typical example of line timing is when ports on each node of the ring are configured to be primary and secondary timing references for other nodes in the ring. The primary timing reference is then accepted in one direction around the ring, and the secondary timing reference is accepted in the opposite direction.

Here is a best practice recommendation when line timing:

Configure primary timing clockwise around the ring, and secondary timing counterclockwise around the ring. [Figure 1](#) shows the timing topology:

Figure 1 – Timing Topology Diagram



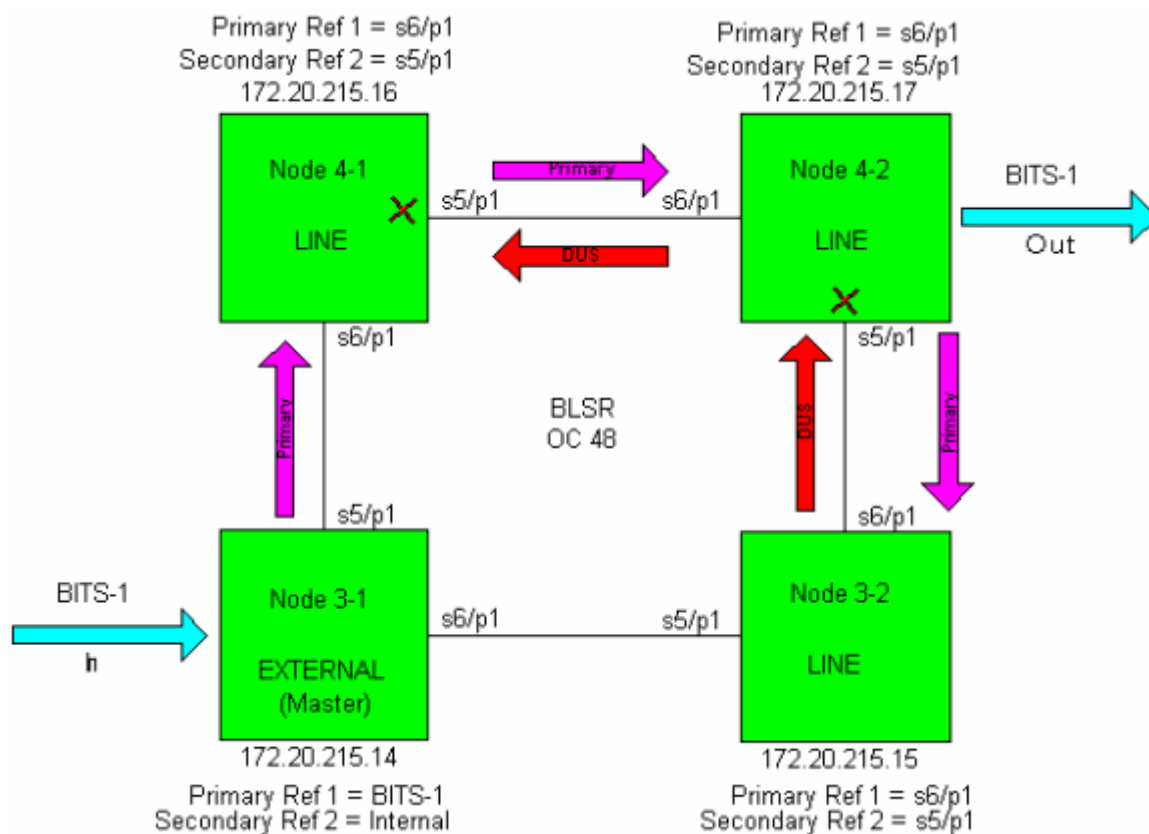
In the above timing topology diagram, Node 3-1 accepts the external ST1 reference on its BITS 1 pins. Node 3-1 can be thought of as the master from which the other nodes that use line timing, accept their primary and secondary timing reference in a clockwise or counterclockwise direction respectively.

Another equally valid timing topology, however, would be to have each of the above four nodes timed from separate ST1 primary timing references on their backplane BITS pins.

Note: Daisy-chaining of BITS sources is not supported. In other words, one BITS source is not used to time multiple nodes from the same wire wrap pins. Each timing line card from timing sources typically provides pin outputs to one set of Timing Inputs. It is recommended that a protect card or another timing line card be used for the other BITS Input for redundancy and timing protection.

If the ONS 15454 performs line timing, and accepts its primary timing reference from one of its optical cards, it sends back a "Don't Use for Synchronization (DUS)" SSM message on that optical card in the opposite direction. [Figure 2](#) represents this scenario (this is not automatic; it must be selected on the line card). This is the preferred method of timing with the use of the DUS, as checked on the line card.

Figure 2 – Timing With the Use of the DUS



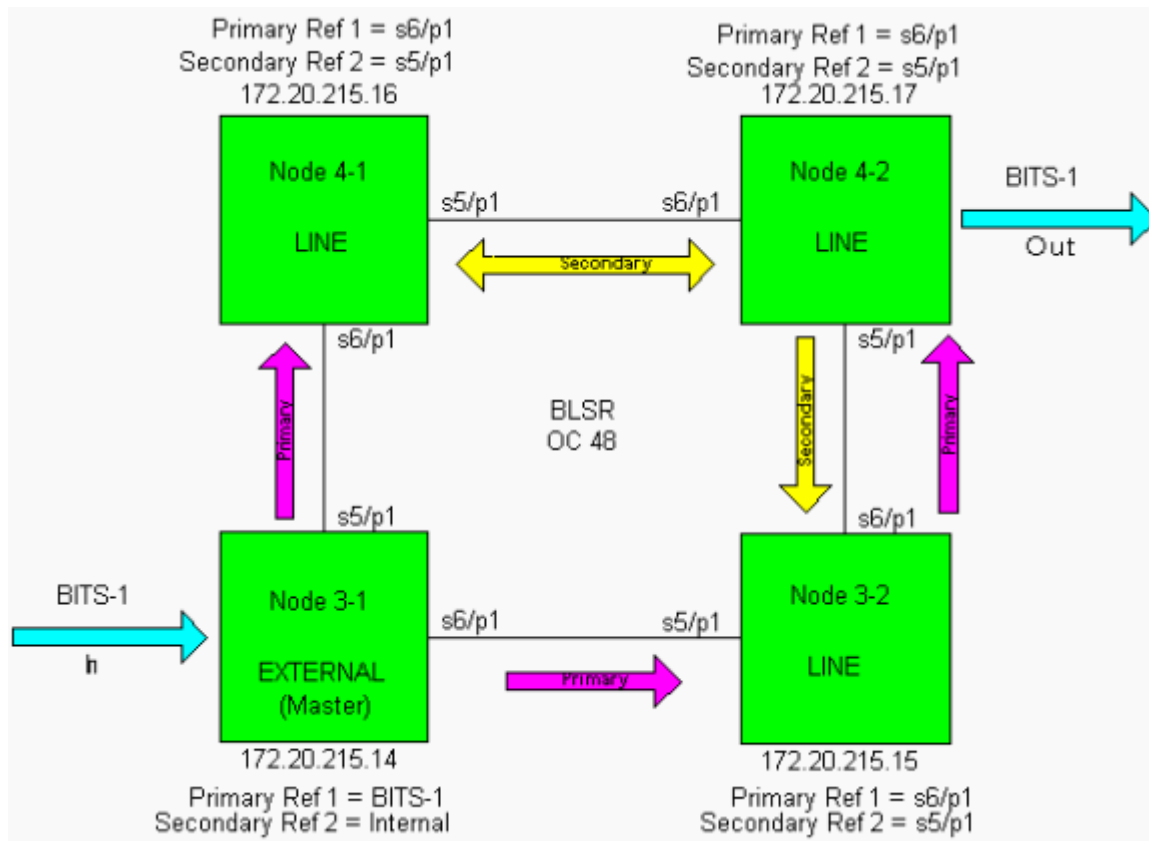
The DUS SSM message is because, if the ONS 15454 accepted its primary timing reference from the same interface from which its opposite node accepted the primary timing reference, the same timing reference would circle from one ONS 15454 to the other ONS 15454. This would result in a timing loop. Node 3-1 does not receive a DUS SSM message because, it externally times from its backplane BITS pins, as opposed to line timing.

To be precise, Node 3-1 must show a DUS SSM message on slot 5, port 1 because that interface provides line timing for adjacent Node 4-1. It does not report the DUS SSM message, however, because slot 5 is not one of the primary, secondary, or third timing references on Node 3-1 (Node 3-1 timing references are BITS 1, BITS 2, and internal). Similarly, if you were to remove the secondary timing references (slot 5) from Nodes 4-1 and 4-2, the DUS SSM messages that you have there would disappear.

The DUS SSM messages are logged in the active alarms screen within the Cisco Transport Controller (CTC). The logged DUS SSM messages allow you to verify the timing topology. You can use them to check the direction from which each ONS 15454 accepts its timing.

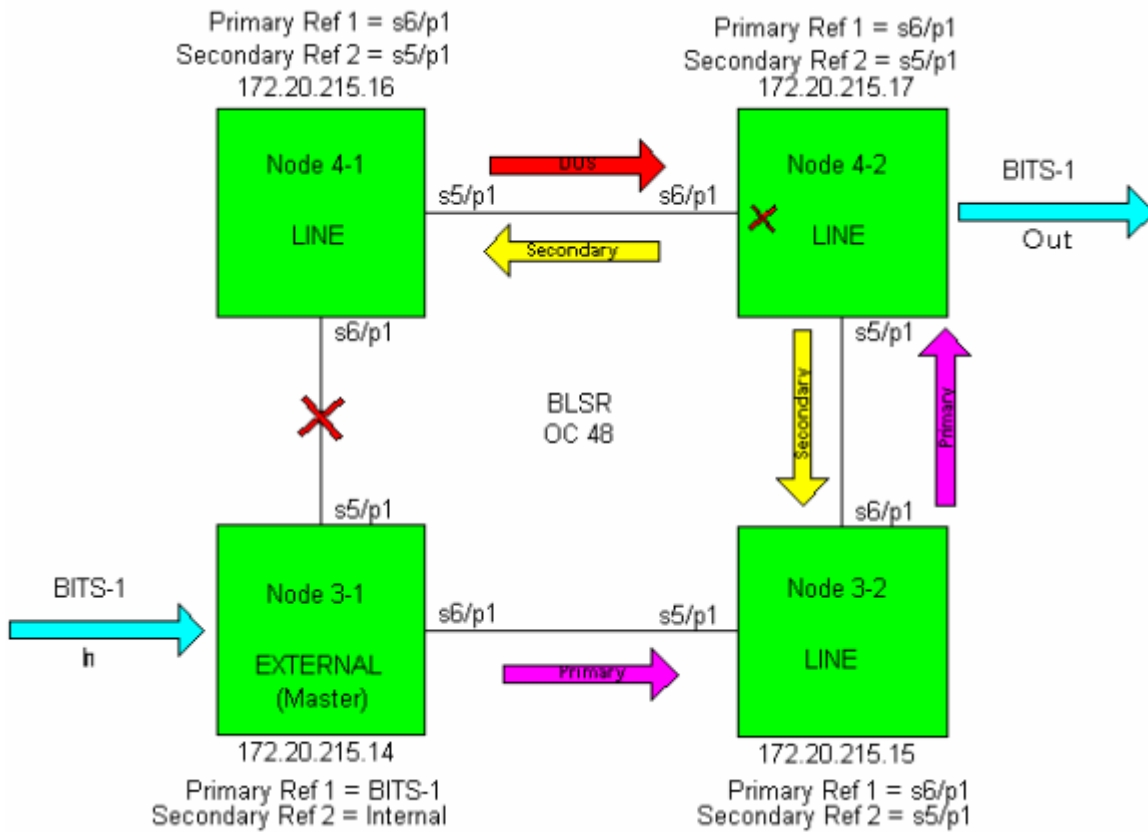
The clockwise primary timing reference and counter-clockwise secondary timing reference timing topology appears logical and simple to comprehend. However, to check what happens if you turned one of the three-line timed nodes primary timing reference around to be accepted from the opposite direction, take Node 4-2. Instruct the node that its primary timing reference must now be accepted from Node 3-2, as opposed to its current Node 4-1, as shown in [figure 3](#):

Figure 3 – Primary Timing Reference Accepted From Node 3-2



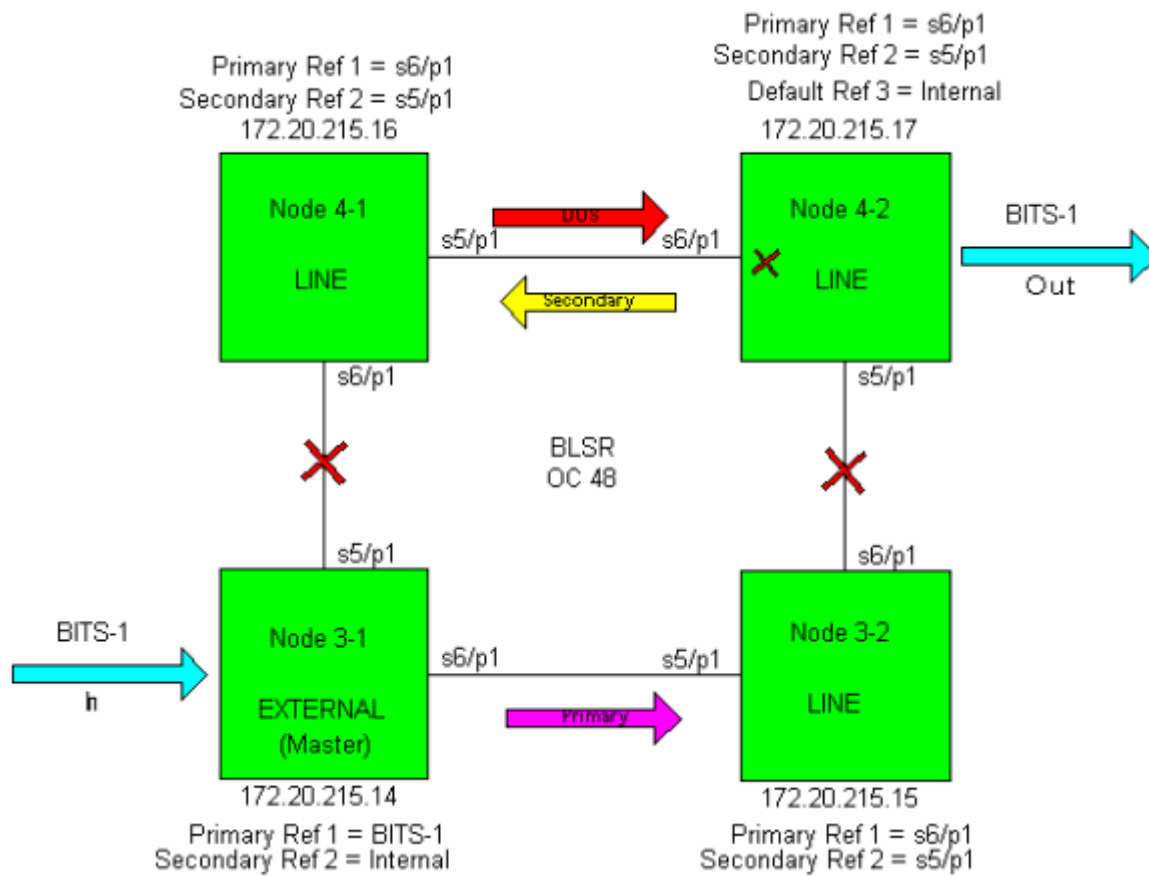
Although, in [figure 3](#), each of the three-line timed nodes are able to accept a primary and secondary timing reference, this timing topology is not as easy to understand. In addition, there seems to be a timing loop between Node 4-1 and Node 4-2. If Node 4-1 lost its primary timing reference, and had to use its secondary timing reference, check whether there would be a timing loop. This is where the importance of the DUS SSM message comes in, as shown in [figure 4](#):

Figure 4 – The Importance of the DUS SSM Message



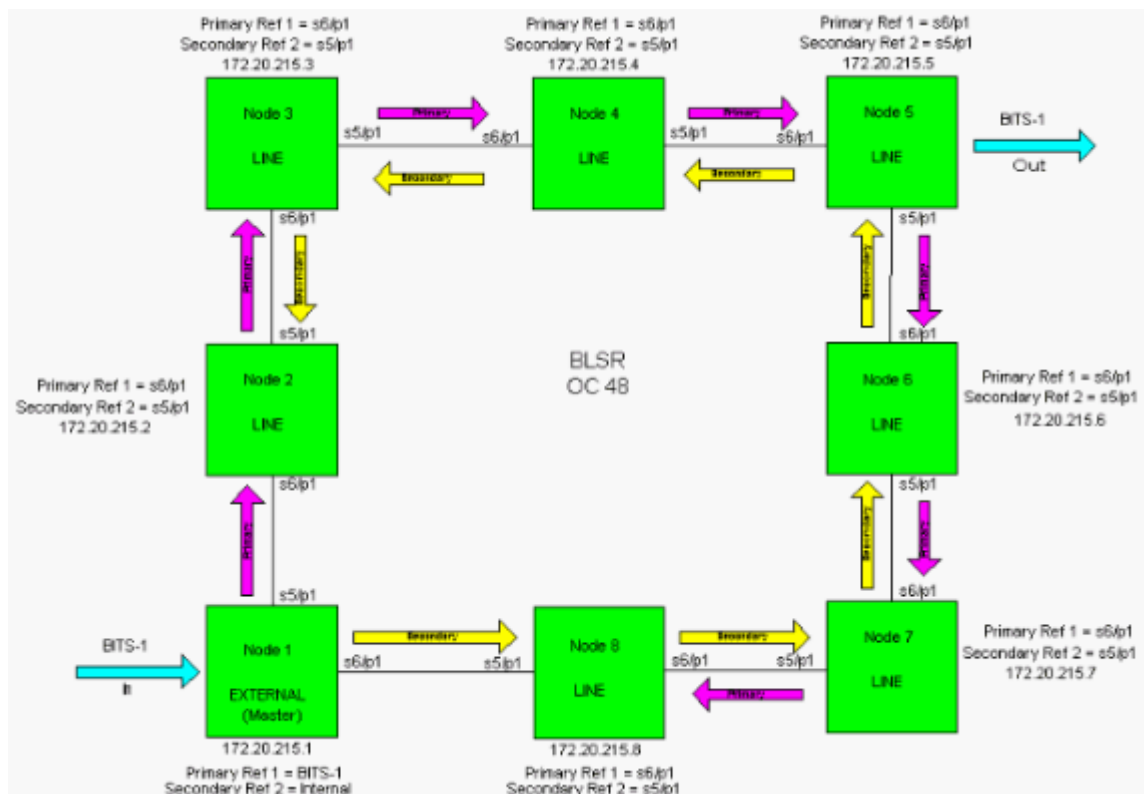
Instead of a timing loop due to Node 4-1 that uses its secondary timing reference, a DUS SSM message is sent, to tell Node 4-2 not to use this interface for a timing reference. If Node 4-2 now lost its primary timing reference, it would be forced to accept the default timing reference of its internal ST3E clock, as opposed to its secondary timing reference from Node 4-1, as shown in [figure 5](#):

Figure 5 – Default Timing Reference of the Internal ST3E Clock



However, now the question arises about why this complex timing topology must be used, when a more easily understandable clockwise primary timing reference and anti-clockwise secondary timing reference topology can be used. To answer this question, let us expand the above network into a larger topology, as shown in [figure 6](#):

Figure 6 – When the Network is Expanded into a Larger Topology

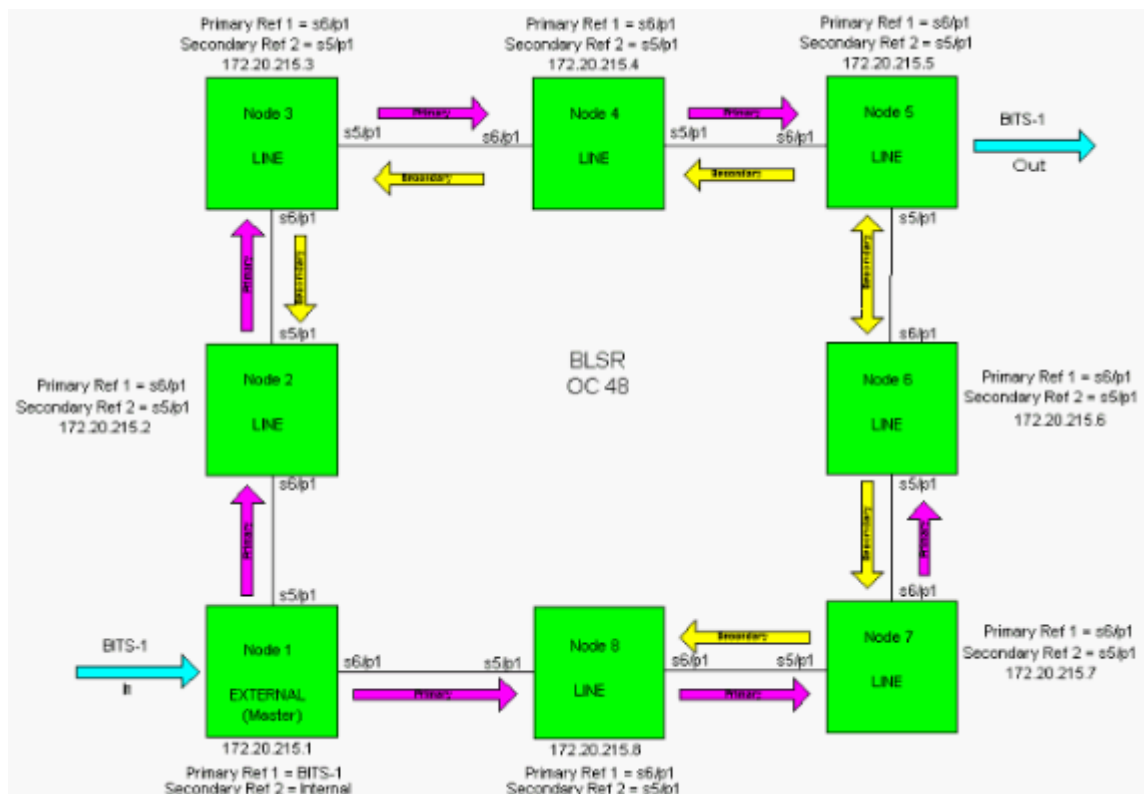


In the above eight node Bidirectional Line Switching Ring Optical Carrier (BLSR OC 48) ring, each node accepts its primary timing reference in a clockwise direction, and its secondary timing reference in an anti-clockwise direction.

The problem with this timing topology is that by the time the primary timing reference is accepted by Node 8, it has been regenerated six times. In large networks when the primary timing reference has to be line timed round the entire ring, timing problems such as slips can occur.

A solution to this is to ensure that the primary timing reference is accepted in both directions around the ring. This means that the primary timing reference only has to travel halfway around the ring, as shown in [figure 7](#):

Figure 7 – The Primary Timing Reference Travels Halfway Around the Ring



In [figure 7](#), the primary timing reference only needs to be accepted halfway around the ring. Also, you can see that if any of the links between the nodes are broken, they are still able to accept a secondary timing reference.

Timing is a complex subject and a complete discussion on it is beyond the scope of this document. However, this section tries to provide a basic explanation of the concepts behind timing on the ONS 15454.

Synchronization Modes

Based on the network condition, the ONS 15454 operates in one of these synchronization modes:

- Normal Mode:** The system clock is synchronized to a reference source. The output frequency of the clock is the same as the input reference frequency over the long term. The Sync LED on the TCC/TCC+/TCC2 and XC/XCVT/XC10G card indicates Normal Mode.
- Fast Start Mode:** Used for fast 'pull-in' of a reference clock, Fast Start is active when the internal reference frequency is offset from the external reference clock. If the frequency is offset by more than 2 ppm (parts per million) in every 30 seconds (called the "wander threshold"), the secondary reference source will be selected. The node will revert back to the primary reference source when it is within the specified threshold (for example, +/- 15 ppm). During the switching process, the internal clock will be in Fast Start mode. Fast Start is sometimes referred to as the "Acquire State".
- Holdover Mode:** The ONS 15454 goes into Holdover when the last available reference is lost and the node is synchronized to that reference for more than 140 seconds. During this period, the internal clock is held at the last known value of the Phase Lock Loop (PLL) parameters when the node is still synchronized to the reference clock. If the holdover frequency value is corrupted, the ONS 15454 will switch to Free Run mode.

- **Free Run Mode:** The ONS 15454 is considered to be in Free Run mode when operates on its own internal clock. Free-run accuracy for the ONS 15454 and most SONET nodes is ST3. The minimum accuracy for any SONET node must be better than SONET Minimum Clock (SMC), which is +/- 20 ppm.

Use the BITS Backplane Pins for External Timing References

The ONS 15454 backplane supports two BITS clock pin fields. The first four BITS pins, rows 3 and 4, support output and input from the first external timing device. The last four BITS pins, rows 1 and 2, perform the identical functions for the second external timing device. See [table 2](#) for the pin assignments for the BITS timing pin fields.

Table 2 – Pin Assignments for the BITS Timing Pin Fields

External Device	Contact	Tip and Ring	Function
First External Device	A3 (BITS 1 Out)	Primary ring (-)	Output to external device
	B3 (BITS 1 Out)	Primary tip (+)	Output to external device
	A4 (BITS 1 In)	Secondary ring (-)	Input from external device
	B4 (BITS 1 In)	Secondary tip (+)	Input from external device
Second External Device	A1 (BITS 2 Out)	Primary ring (-)	Output to external device
	B1 (BITS 2 Out)	Primary tip (+)	Output to external device
	A2 (BITS 2 In)	Secondary ring (-)	Input from external device
	B2 (BITS 2 In)	Secondary tip (+)	Input from external device

Figure 8 – BITS In and Out

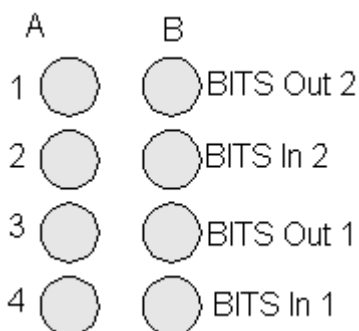
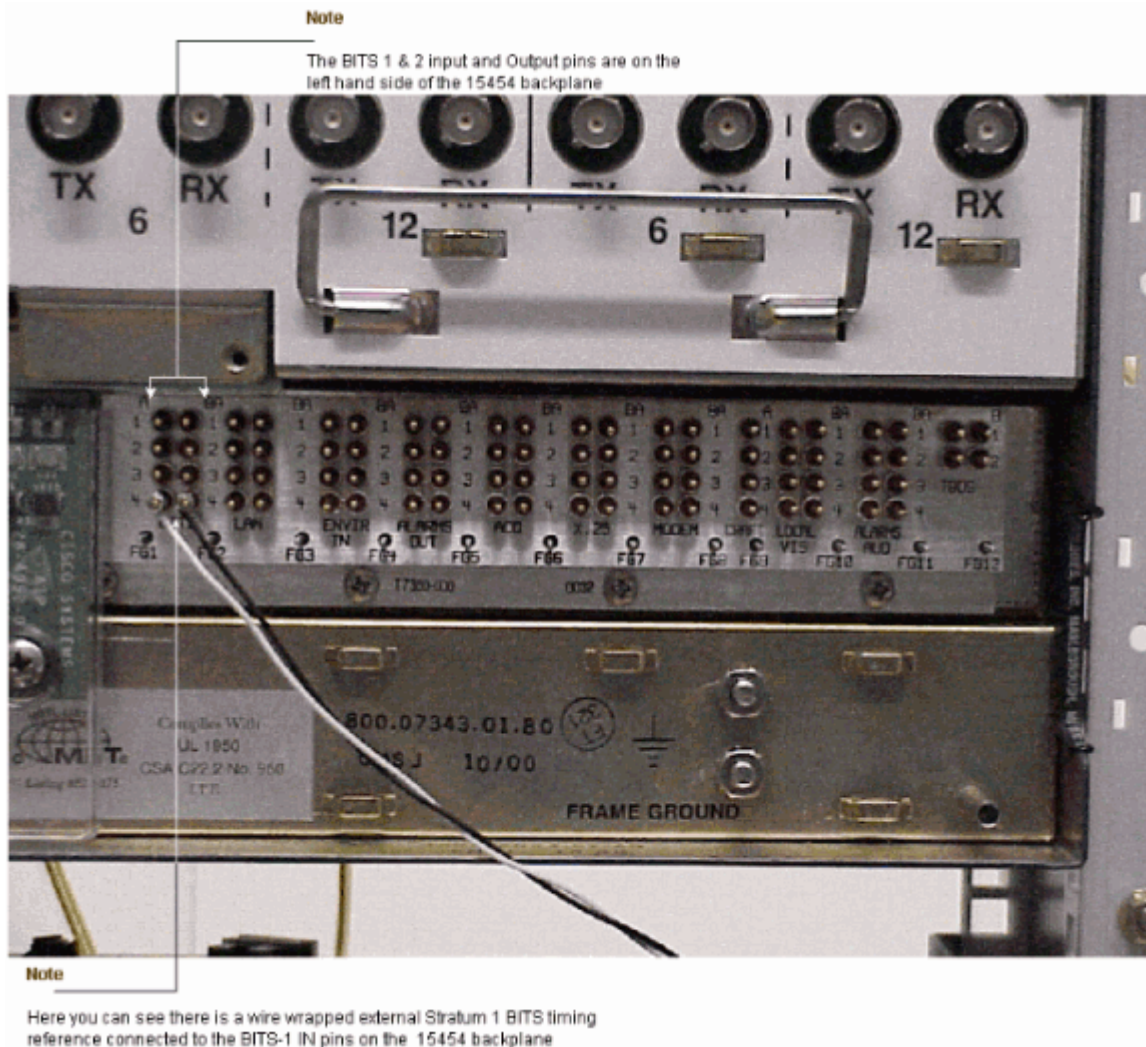


Figure 9 – The 15454 Backplane



Understand the Timing Alarms

The ONS 15454 uses an active alarm screen that displays various alarms to provide a summary of the current status. All timing conditions appear in blue to indicate that although they appear as alarms in older operating software, they must be treated as non-critical event notification messages or conditions.

When a timing event notification (such as a change in the timing topology) happens, new timing event notification alarms appear in blue, and the old timing event notification alarms expire and turn to white. They are then removed when the alarm display screen is refreshed.

A summary of the timing event notification type codes is shown in this section.

Figure 10 – The BITS-1 Type Code

BITS-1

The BITS 1 type code indicates that the BITS 1 interface on the ONS 15454 generates the timing event notification.

Figure 11 – The BITS-2 Type Code

BITS-2

The BITS 2 type code indicates that the BITS 2 interface on the ONS 15454 generates the timing event notification.

Figure 12 – The SYNC-NE Type Code**SYNC-NE**

The SYNC-NE type code indicates that the synchronization on the TCC card generates the timing event notification for the ONS 15454.

Figure 13 – The FAC-6-X-Y Type Code**FAC-X-Y**

The FAC-6-X-Y type code indicates that the facility on slot X, port Y generates the timing event notification for the ONS 15454.

Figure 14 – The SYNC-BITS 1 Type Code**SYNC-BITS1**

The SYNC-BITS 1 type code indicates that the synchronization on the TCC card generates the timing event notification for the BITS 1 interface.

Figure 15 – The SYNC-BITS 2 Type Code**SYNC-BITS2**

The SYNC-BITS 2 type code indicates that the synchronization on the TCC card generates the timing event notification for the BITS 2 interface.

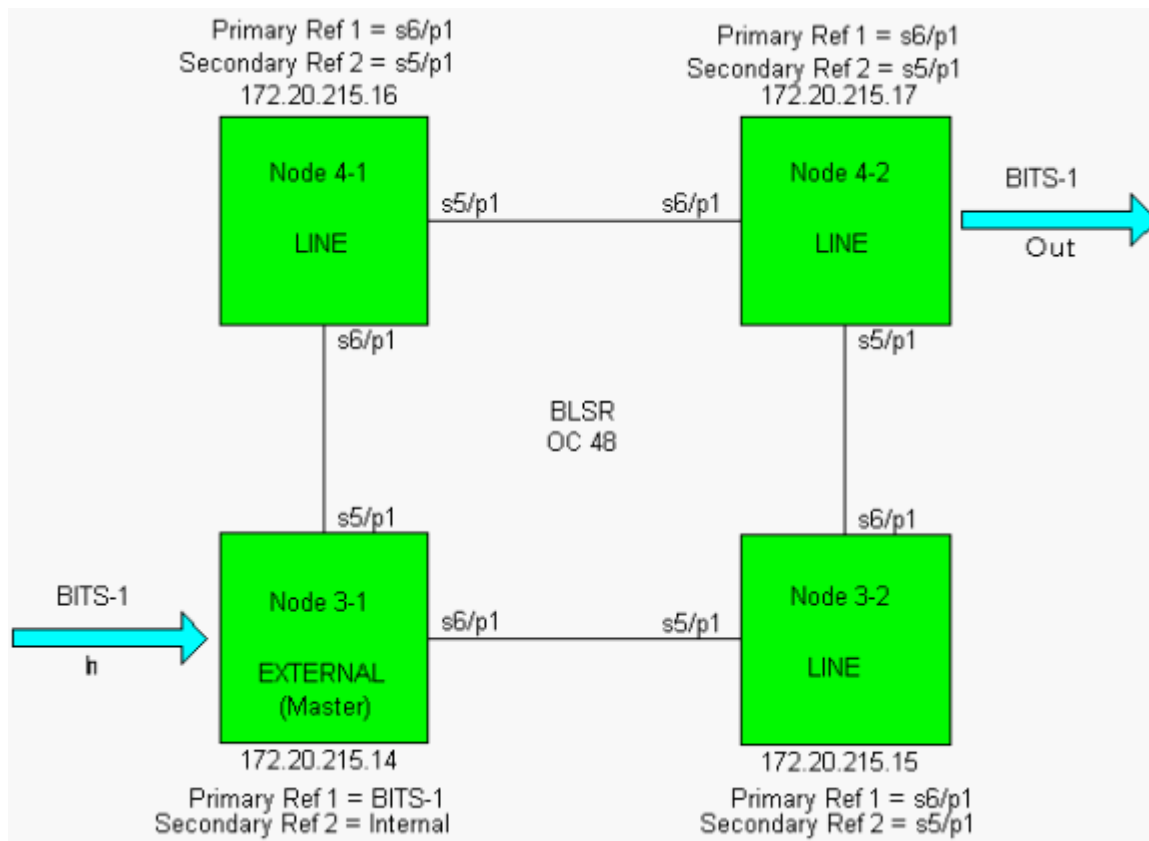
Best Practice Timing Topology Lab Setup

In the lab setup below, we demonstrate a typical timing setup for the ONS 15454. It is based on a lab setup that consists of four ONS 15454 nodes in a BLSR OC 48 ring. It shows how one node accepts a BITS 1 external timing reference. It also shows how the node that acts as the master uses line timing for the other nodes in the ring to accept their clockwise primary timing reference and synchronize themselves from it.

The lab setup shows that the ring is deliberately broken, and indicates how the nodes accept the anti-clockwise secondary timing reference to recover and resynchronize their timing. The ring is then repaired, and the nodes resynchronize their timing back to accept the clockwise primary timing reference.

The network topology used in the lab setup is shown in [figure 16](#):

Figure 16 – Best Practice Timing Topology Lab Setup



The same timing topology is shown through the CTC network view in [figure 17](#). All nodes that are line timing are shown synchronized to accept their clockwise primary timing reference.

Figure 17 – The CTC Network View

The screenshot shows the CTC interface with a network map and an Alarms table. The network map displays four nodes: Node 3-1 (green), Node 4-1 (orange), Node 4-2 (orange), and Node 3-2 (green), connected in a ring topology. The Alarms table below shows a list of events with columns for Date, Node, Type, Slot, Port, Sev, ST, SA, Cond, and Description. The entry for Node 4-2 at 01/02/70 13:42:10 is highlighted in yellow, indicating a 'Loss of Signal' event.

Date	Node	Type	Slot	Port	Sev	ST	SA	Cond	Description
01/02/70 14:05:05	Node 3-1	BITS-1			NA	R		PR3	Primary Reference Source - Stratum 1 Traceable
01/02/70 14:05:05	Node 3-1	S'YNC-NE			NR	R		SWTOPRI	Synchronization Switch To Primary reference
01/02/70 14:05:05	Node 3-1	S'YNC-NE			NR	R		PR3	Primary Reference Source - Stratum 1 Traceable
01/01/70 18:23:04	Node 3-2	FAC 5-1	5	1	NA	R		PR3	Primary Reference Source - Stratum 1 Traceable
01/01/70 15:23:35	Node 3-2	S'YNC-NE			NR	R		PR3	Primary Reference Source - Stratum 1 Traceable
01/02/70 13:55:45	Node 3-2	FAC 6-1	6	1	NA	R		PR3	Primary Reference Source - Stratum 1 Traceable
01/02/70 12:55:55	Node 3-2	S'YNC-NE			NR	R		SWTOPRI	Synchronization Switch To Primary reference
01/01/70 18:01:10	Node 4-1	S'YNC-NE			NR	R		PR3	Primary Reference Source - Stratum 1 Traceable
01/01/70 18:01:10	Node 4-1	FAC 6-1	6	1	NA	R		PR3	Primary Reference Source - Stratum 1 Traceable
01/01/70 15:06:10	Node 4-1	S'YNC-NE			NR	R		SWTOPRI	Synchronization Switch To Primary reference
01/01/70 15:05:20	Node 4-1	FAC 5-1	5	1	NA	R		DUS	Don't Use for Synchronization
01/02/70 13:42:10	Node 4-2	BITS-1			NA	R		LOG	Loss of Signal
01/02/70 13:42:10	Node 4-2	S'YNC-NE			NR	R		PR3	Primary Reference Source - Stratum 1 Traceable
01/02/70 13:54:20	Node 4-2	FAC 6-1	6	1	NA	R		PR3	Primary Reference Source - Stratum 1 Traceable
01/02/70 13:54:31	Node 4-2	S'YNC-NE			NR	R		SWTOPRI	Synchronization Switch To Primary reference
01/02/70 13:54:41	Node 4-2	FAC 5-1	5	1	NA	R		DUS	Don't Use for Synchronization

Externally Timing the First Node

The first node to be configured for timing is Node 3-1. Use the CTC interface to navigate to the timing screen through the **Provisioning > Timing** tabs. The ONS 15454 can accept its timing either from the line (one of the optical cards) or from an external BITS 1 source. Specify **external** for the timing mode. When you specify external, Node 3-1 is instructed to use the BITS backplane pins to accept its primary timing source.

In the timing configuration example shown in [figure 18](#), the NE Reference REF 1 field is set to **BITS 1**. This instructs Node 3-1 to use the BITS 1 IN backplane pins to accept its primary timing reference. The BITS 1 STATE field is placed **In Service (IS)** to enable the BITS 1 pins.

When Node 3-1 initializes, it uses its BITS 1 IN backplane pins as its primary timing reference source. If it cannot use the BITS 1 backplane pins, it accepts its secondary timing reference from the internal ST3 clock that runs on the TCC card. If this fails, it accepts its third timing reference, which is again the internal ST3 clock.

If Node 3-1 initializes to accept the secondary or third timing source, but at a later time its primary timing source becomes available, Node 3-1 switches to accept its synchronization from it. This is because, the **revertive** option is selected in the configuration screen. A reversion time of **five** minutes is set, which is the time that Node 3-1 waits for its primary timing reference to become available to switch to accept it.

If Node 3-1 uses the BITS 1 pins as its primary timing reference source, all of the interface cards in Node 3-1 will be timed by an ST1 clock. Otherwise, Node 3-1 uses its secondary or third timing reference, and all of the interface cards will be timed by an ST3 clock.

For a complete description of the options available from the timing configuration screen, refer to the

[Setting Up ONS 15454 Timing](#) section of the ONS 15454 User Documentation.

Figure 18 – Configuration Example Where the First Node is Externally Timed

The figure illustrates the configuration of an ONS 15454 node for external timing. At the top, a diagram shows two columns of ports labeled A and B. Column A contains ports 1, 2, 3, and 4. Column B contains BITS Out 2, BITS In 2, BITS Out 1, and BITS In 1. Arrows indicate connections: port 1 to BITS Out 2, port 2 to BITS In 2, port 3 to BITS Out 1, and port 4 to BITS In 1.

Below the diagram are two notes:

- Note:** Revertive if ticked tells the 15454 to revert back to its primary timing source when it becomes available again. The reversion time is the time the 15454 will stay on the secondary timing source before reverting back to its primary.
- Note:** Set to external if timing comes from external BITS source wired to the BITS IN backplane pins. Set to line if timing comes from an Optical Carrier card.

The main part of the figure is a screenshot of the CTC (Cisco Transport Controller) configuration interface. The 'Timing' tab is active, showing the following settings:

- General Timing:**
 - Timing Mode: External
 - EDM Message Set: Generation 1
 - Quality of BER: R23 w DUB
 - Reverse Reversion Time: 1 min
- BITS Facilities:**
 - BITS-1:**
 - State: 0
 - Coding: B8Z5
 - Flaming: EBF
 - Eye Monitoring: Enabled
 - AM Threshold: 100
 - BITS-2:**
 - State: 008
 - Coding: B8Z5
 - Flaming: EBF
 - Eye Monitoring: Enabled
 - AM Threshold: 100
- Reference Lists:**
 - Ref 1:
 - NE Reference: BITS 1
 - BITS-1 Out: None
 - BITS-2 Out: None
 - Ref 2:
 - NE Reference: Internal Clock
 - BITS-1 Out: None
 - BITS-2 Out: None
 - Ref 3:
 - NE Reference: External Clock
 - BITS-1 Out: None
 - BITS-2 Out: None

At the bottom, another note states: "Up to three timing references can be specified. If timing mode is external then options are BITS-1, BITS-2 or internal. If timing mode is line then the nodes working optical cards are displayed." A final note says: "Used to specify the timing source for equipment wired to the BITS OUT backplane pins. Usually used with line nodes. As we are not using the BITS OUT pins on this node nothing is specified."

Alarms for Externally Timing the First Node

When you configure Node 3-1 to accept an external BITS 1 timing reference, three alarms are generated, as shown in [figure 19](#). To view these alarms through the CTC interface, navigate to the alarms screen through the **Alarms** tab. The alarms indicate that Node 3-1:

- detected an ST1 Traceable PRS.
- successfully switched to it.

- is incoming on the BITS 1 backplane pins.

Note: The severity of the alarms is all Not Reported (NR) or Not Alarmed (NA). This indicates that the alarms are informational only.

Figure 19 – Three Alarms Generated When the First Node is Externally Timed

Note

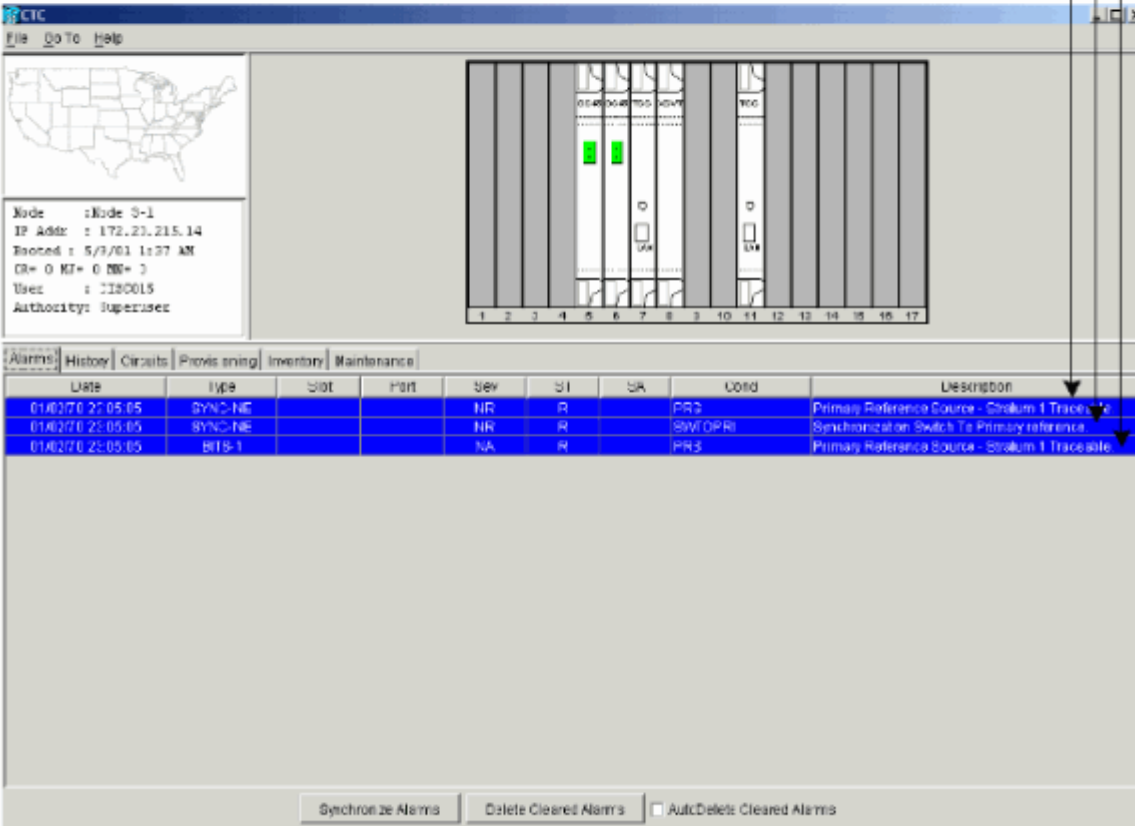
The third alarm tells you interface on the 15454 where it is detecting the Stratum 1 traceable. In this case it is the BITS-1 pins on the 15454 backplane. The severity is NA (Not alarmed).

Note

The second alarm indicates that the 15454 is has recognised that the Stratum 1 traceable matches its primary reference source and is switching to it. The severity is NR (Not Reported).

Note

The first alarm indicates that a Stratum 1 traceable primary reference source has been detected by the 15454. The severity is NR (Not Reported).



Date	Type	Slot	Port	Sev	SI	SR	Code	Description
01/02/00 23:05:05	SYNC-NE			NR	R		PR3	Primary Reference Source - Stratum 1 Traceable
01/02/00 23:05:05	SYNC-NE			NR	R		SW(OPR)	Synchronization Switch To Primary reference
01/02/00 23:05:05	BITS-1			NA	R		PR3	Primary Reference Source - Stratum 1 Traceable

Synchronize Alarms Delete Cleared Alarms AutoDelete Cleared Alarms

Line Timing the Second Node

The next node configured for timing is Node 3-2. Use the CTC interface to navigate to the timing screen through the **Provisioning - Timing** tabs. Specify **line** for the timing mode. When you specify line, Node 3-2 is instructed to look at the optical card in slot 6 to accept its primary timing reference, and slot 5 to accept its secondary timing reference.

In the timing configuration screen, the NE Reference REF 1 field has been set to **slot 6, port 1**. This is where you instruct Node 3-2 to look at the 125 microsecond SONET packets on the OC 48 optical card in slot 6 to find its primary timing source.

The NE Reference REF 2 field has been set to **slot 5, port 1**. This is where you instruct Node 3-2 to

look at the 125 microsecond SONET packets on the OC 48 optical card in slot 5 to find its secondary timing source.

When Node 3-2 initializes, it uses the OC 48 card in slot 6 to accept its primary timing reference. If it cannot use this OC 48 card, it accepts its secondary timing reference from the OC 48 card in slot 5. If both primary and secondary timing sources cannot be accepted, Node 3-2 accepts its third timing reference from the internal ST3 clock running on the TCC card.

If Node 3-2 accepts its secondary or third timing source to initialize, but at a later time the primary timing reference becomes available, Node 3-2 switches to accept it. This is because, the **revertive** option is selected in the configuration screen. A reversion time of **five** minutes is set, which is the time that Node 3-2 waits from its primary timing reference to become available to switch to accept it.

If Node 3-2 accepts its primary timing reference, all interface cards in Node 3-2 are timed by the OC 48 card in slot 6. If Node 3-2 accepts its secondary timing reference, all interface cards are timed by the OC 48 card in slot 5. Otherwise, all interface cards are timed by the internal ST3 clock.

For a complete description of the options available from the timing configuration screen, refer to the [Setting Up ONS 15454 Timing](#) section of the ONS 15454 User Documentation.

Figure 20 – Configuration Example When Second Node is Line Timed

Note
Set to line if timing comes from an Optical carrier card as opposed to an external BITS source

Note
Here we specifying that the 125 microsecond long SONET packets incoming on Slot 5, port 1 are going to act as our secondary timing reference

Note
Here we specifying that the 125 microsecond long SONET packets incoming on Slot 6, port 1 are going to act as our primary timing reference

s6/p1

Node 3-2
LINE

172.20.215.15
Ref 1 = s6/p1
Ref 2 = s5/p1

s5/p1

Alarms for Line Timing the Second Node

When you configure Node 3-2 for line timing, four alarms are generated, as shown in [figure 21](#). To view these alarms from the CTC interface, navigate to the alarms screen through the **Alarms** tab. From the alarms, it can be inferred that:

- Node 3-2 successfully switched to a ST1 Traceable PRS.
- ST1 Traceable PRS available on slot 6, port 1.

- Node 3-2 has detected a ST1 Traceable PRS.
- ST1 Traceable PRS available on slot 5, port 1.

Note: The severity of the alarms is all NR or NA. This indicates that the alarms are informational only.

Figure 21 – Alarms Generated When the Second Node is Line Timed

Note
The fourth alarm indicates that a Stratum 1 traceable primary reference source is being used on Interface Slot 5, Port 1. The severity is NR (Not Reported).

Note
The third alarm indicates that a Stratum 1 traceable primary reference source has been detected by Node 3-2. The severity is NR (Not Reported).

Note
The second alarm indicates that a Stratum 1 traceable primary reference source is being used on Interface Slot 6, Port 1. The severity is NR (Not Reported).

Note
The first alarm indicates that Node 3-2 has recognized that the Stratum 1 traceable OC-48 card on Slot 6, port 1 matches its primary reference source and is switching to it. The severity is NR (Not Reported).

The screenshot shows the CTC interface for Node 3-2. The rack diagram displays slots 1 through 17, with slots 5 and 6 highlighted in green. The Alarms table below shows the following entries:

Date	Type	Slot	Port	Sev	DI	SA	Card	Description
01/02/00 22:55:59	SYNC-NE			NR	R		SWTQPR	Synchronization Switch To Primary Reference.
01/02/00 22:55:45	FAC-S-T	6	1	NA	R		PRS	Primary Reference Source - Stratum 1 Traceable.
01/02/00 01:23:35	SYNC-NE			NR	R		PRS	Primary Reference Source - Stratum 1 Traceable.
01/02/00 01:23:04	FAC-S-T	5	1	NA	R		PRS	Primary Reference Source - Stratum 1 Traceable.

Line Timing the Third Node

The next node configured for timing is Node 4-1. Use the CTC interface to navigate to the timing screen through the **Provisioning - Timing** tabs. Specify **line** for the timing mode. When you specify line, Node 4-1 is instructed to look at the Optical Card in slot 6 to accept its primary timing reference, and slot 5 to accept its secondary timing reference.

In the timing configuration screen the NE Reference REF 1 field is set to **slot 6, port 1**. This is where you instruct Node 4-1 to look at the 125 microsecond SONET packets on the OC 48 optical card in slot 6 to find its primary timing source.

The NE Reference REF 2 field has been set to **slot 5, port 1**. This is where you instruct Node 4-1 to look at the 125 microsecond SONET packets on the OC 48 optical card in slot 5 to find its secondary timing source.

When Node 4-1 initializes, it uses the OC 48 card in slot 6 to accept its primary timing reference. If it cannot use this OC 48 card, it accepts its secondary timing reference from the OC 48 card in slot 5. If both primary and secondary timing sources cannot be accepted, Node 4-1 accepts its third timing reference from the internal Stratum 3 clock running on the TCC card.

If Node 4-1 initializes accepting its secondary or third timing source, but at a later time the primary timing reference becomes available, Node 4-1 switches to accept it. This is because, the **revertive** option is selected in the configuration screen. A reversion time of **five** minutes is set, which is the time that Node 4-1 will wait for its primary timing reference to become available to switch to accept it.

If Node 4-1 accepts its primary timing reference, all interface cards in Node 4-1 are timed by the OC 48 card in slot 6. If Node 4-1 accepts its secondary timing reference, all interface cards are timed by OC 48 card in slot 5. Otherwise, all interface cards are timed by the internal ST3 clock.

For a complete description of the options available from the timing configuration screen, refer to the [Setting Up ONS 15454 Timing](#) section of the ONS 15454 User Documentation.

Figure 22 – Configuration Example When Third Node is Line Timed

Note
Set to line if timing comes from an Optical carrier card as opposed to an external BITS source

Note
Here we specifying that the 125 microsecond long SONET packets incoming on Slot 6, port 1 are going to act as our primary timing reference

Note
Here we specifying that the 125 microsecond long SONET packets incoming on Slot 5, port 1 are going to act as our secondary timing reference

Ref 1 = s6/p1
Ref 2 = s5/p1
172.20.215.16

Node 4-1
LINE

s5/p1 ←

→ s6/p1

Alarms for Line Timing the Third Node

The same alarms are reported for Node 4-1 as for Node 3-2 with the exception of the DUS SSM message. This alarm is important, because it allows you to recognize the timing topology within your network. If an ONS 15454 is line timing and uses a particular incoming circuit on an optical card as its primary timing reference, it will send a DUS SSM message back down that interface in order to prevent timing loops.

Note: This may or may not happen. The DUS SSM message will only be sent when you have checked that feature under the **Provisioning** tab of the line card. You must do this in order to send the DUS SSM message.

Refer to the [Timing Topology Changes When the Ring Is Broken](#) section of this document for more

information.

Figure 23 – Alarms Generated When the Third Node is Line Timed

Note

The fourth alarm indicates that a Stratum 1 traceable primary reference source has been detected by Node 4-1. The severity is NR (Not Reported).

Note

The third alarm indicates that a Stratum 1 traceable primary reference source is being used on Interface Slot 6, Port 1. The severity is NA (Not Alarmed).

Note

The second alarm indicates that Node 4-1 has recognised that the Stratum 1 traceable OC-48 card on Slot 6, port 1 matches its primary reference source and is switching to it. The severity is NR (Not Reported).

Note

The first alarm indicates that the next hop Node 4-2 is using the output from interface Slot 5, Port 1 as its line timing reference. If a 15454 uses a particular Optical Card as its primary timing reference it sends back a DUS (Don't Use for Synchronisation) alarm in order to prevent timing loops. The severity is NA (Not Alarmed).

Date	Type	Slot	Port	Sev	ST	SA	Cond	Description
01/01/73 15:00:20	FAC 5-1	5	1	NA	R		DUS	Don't Use for Synchronisation
01/01/73 15:00:10	SYNC-NE			NR	R		SWT(SPR)	Synchronization Switch to Primary reference
01/01/73 15:01:10	FAC 6-1	6	1	NA	R		PRS	Primary Reference Source - Stratum 1 Traceable
01/01/73 15:01:10	SYNC-NE			NR	R		PRS	Primary Reference Source - Stratum 1 Traceable

Line Timing and Providing a BITS OUT Timing Reference on the Fourth Node

The last node configured is Node 4-2. Use the CTC interface to navigate to the timing screen through the **Provisioning > Timing** tabs. Specify **line** for the timing mode. When you specify line, Node 4-2 is instructed to look at the Optical Card in slot 6 to accept its primary timing reference, and the optical card in slot 5 to accept its secondary timing reference.

The BITS OUT pins and the ONS 15454 itself have separate fields where you specify the timing references that you want to use. These fields are explained here:

- The BITS 1 OUT, REF 1 field is set to **slot 6, port 1**. This instructs Node 4-2 to accept the 125 microsecond SONET packets on the OC 48 optical card in slot 6 as its primary timing

reference for the BITS 1 OUT pins on the backplane.

- The BITS 1 OUT, REF 2 field is set to **slot 5, port 1**. Again, this instructs Node 4-2 to accept the 125 microsecond SONET packets on the OC 48 optical card in slot 5 as its secondary timing reference for the BITS 1 OUT pins on the backplane.
- The BITS 1 STATE field is placed **IS** to enable the BITS 1 pins.
- The NE Reference REF 1 field is set to **slot 6, port 1**. This is where you instruct Node 4-1 to look at the 125 microsecond SONET packets on the OC 48 optical card in slot 6 to find its primary timing source.
- The NE Reference REF 2 field is set to **slot 5, port 1**. This is where you instruct Node 4-1 to look at the 125 microsecond SONET packets on the OC 48 optical card in slot 5 to find its secondary timing source.

When Node 4-2 initializes, it uses the OC 48 card in slot 6 to accept its primary timing reference. If it cannot use this OC 48 card, it accepts its secondary timing reference from the OC 48 card in slot 5. If both primary and secondary timing sources cannot be accepted, Node 4-2 accepts its third timing reference from the internal ST3 clock running on the TCC card.

If Node 4-2 initializes accepting its secondary or third timing source, but at a later time the primary timing reference becomes available, Node 4-2 switches to accept it. This is because the **revertive** option is selected in the configuration screen. A reversion time of **five** minutes is set, which is the time that Node 4-2 waits for its primary timing reference to become available to switch to accept it.

If Node 4-2 accepts its primary timing reference, all interface cards in Node 4-2 are timed by the OC 48 card in slot 6. If Node 4-2 accepts its secondary timing reference, all interface cards are timed by OC-48 card in slot 5. Otherwise, all interface cards are timed by the internal ST3 clock.

For a complete description of the options available from the timing configuration screen, refer to the [Setting Up ONS 15454 Timing](#) section of the ONS 15454 User Documentation.

Figure 24 – Example for the Fourth Node When it is Line Timed and Provided a BITS Out Reference

Note
Set to line if timing comes from an Optical carrier card as opposed to an external BITS source

Note
Here we specifying that the 125 microsecond long SONET packets incoming on Slot 6, port 1 are going to act as our primary timing reference

Note
Here we specifying that the 125 microsecond long SONET packets incoming on Slot 5, port 1 are going to act as our secondary timing reference

Note
Here we placing the BITS-1 interface in service so that we can provide timing to equipment wired to the BITS-1 OUT pins on the Node 4-2's backplane

Note
Here we are specifying that the 125 microsecond long SONET packets incoming on Slot 5, port 1 are to act as our primary timing reference for the BITS-1 OUT interface

Note
Here we are specifying that the 125 microsecond long SONET packets incoming on Slot 6, port 1 are to act as our secondary timing reference for the BITS-1 OUT interface

Ref 1 = s6/p1
Ref 2 = s5/p1
172.20.215.17

Node 4-2
LINE

s6/p1 → BITS-1 Out → s5/p1

A: 1 BITS Out 2, 2 BITS In 2
B: 3 BITS Out 1, 4 BITS In 1

Alarms for Line Timing and Providing a BITS OUT Timing Reference On the Fourth Node

For Node 4-2, a DUS SSM message is again seen as the next hop Node 3-2 is line timing and uses interface slot 5, port 1 as a primary timing reference. If an ONS 15454 uses a particular optical card as a timing reference, it sends a DUS SSM message back down that interface in order to prevent timing loops. Refer to the [Timing Topology Changes When the Ring Is Broken](#) section of this

document for more information.

A Loss Of Signal (LOS) alarm for the BITS 1 backplane pins is also seen. This is because although the BITS 1 backplane pins have been put into service, there is no equipment physically wire wrapped to those pins. In other words, there is no incoming signal on the BITS 1 IN backplane pins.

Figure 25 – Alarms Generated for the Fourth Node

Note

The third alarm indicates that Node 4-2 has recognised that the Stratum 1 traceable OC-48 card on Slot 6, port 1 matches its primary reference source and is switching to it. The severity is NR (Not Reported).

Note

The second alarm indicates that the next hop Node 3-2 connected to interface Slot 5, Port 1 is using it as a timing reference. If a 15454 uses a particular Optical Card as a primary timing reference it sends back a DUS (Don't Use for Synchronisation) alarm in order to prevent timing loops. The severity is NA (Not Alarmed).

Note

The first alarm indicates that Node 4-2 has previously recognised a BITS 1 secondary timing reference and has switched to it.

Date	Type	Slot	Port	Sev	ST	SA	Cond	Description
01/02/79 04:57:51	SYNC-BITS1	6	1	NR	R	SWTOSRC		Synchronization Switch To Second reference.
01/02/79 13:54:41	FAC-S-1	5	1	NA	R	DUS		Don't Use for Synchronization
01/02/79 13:54:31	SYNC-NE	6	1	NR	R	SWTOSRC		Synchronization Switch To Primary reference.
01/02/79 13:54:26	FAC-S-1	6	1	NA	R	PRS		Primary Reference Source - Stratum 1 Traceable.
01/02/79 13:42:18	SYNC-NE	6	1	NR	R	PRS		Primary Reference Source - Stratum 1 Traceable.
01/02/79 13:42:18	BITS-1	6	1	MJ	R	LOS		Loss of Signal

Note

The fourth alarm indicates that a Stratum 1 traceable primary reference source is being used on interface Slot 6, Port 1. The severity is NA (Not Alarmed).

Note

The fifth alarm indicates that a Stratum 1 traceable primary reference source has been detected by Node 4-2. The severity is NR (Not Reported).

Note

The sixth alarm indicates a Loss Of Signal (LOS) on the BITS-1 backplane pins. This is because although we have put the BITS 1 pins into service there is nothing physically attached to the pins, i.e. there is no incoming signal. The severity is MJ (Major).

Synchronize Alarms Delete Cleared Alarms AutoDelete Cleared Alarms

The four node ONS 15454 lab setup is now complete. There are four nodes configured in an OC 48 BLSR ring topology. Node 3-1 acts as the master. It supplies the ST1 timing reference through its incoming BITS 1 IN backplane pins.

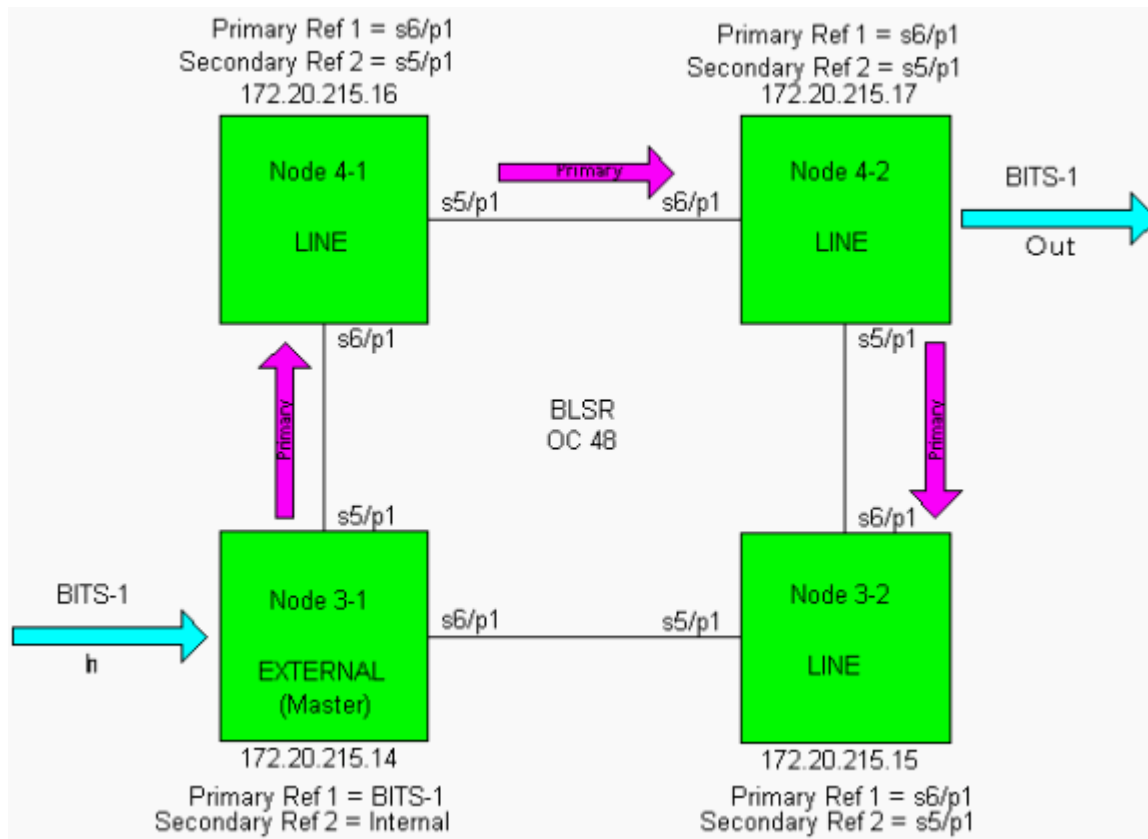
The other three nodes in the ring are each line timing from Node 3-1. In addition, Node 4-2 supplies an ST1 timing reference through its BITS 1 OUT backplane pins.

We have a simple timing topology with the primary timing reference accepted clockwise around the ring, and the secondary timing reference accepted anti-clockwise around the ring.

Timing Topology Changes when the Ring Is Broken

In the lab setup, the ring is stable with the PRS accepted clockwise around the ring, as shown in [figure 26](#):

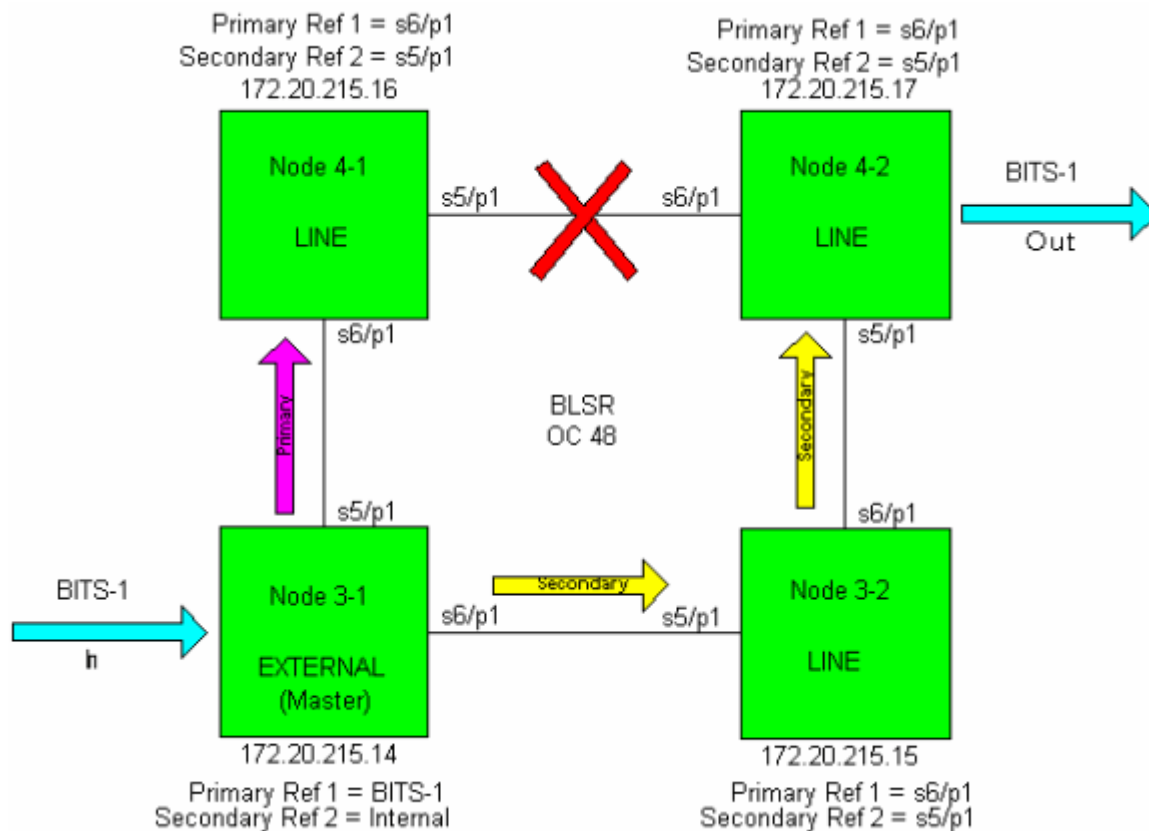
Figure 26 – PRS Accepted Clockwise Around the Ring



The ring will now be deliberately broken. To do so, disconnect the OC 48 link between Node 4-1 and Node 4-2. The next section uses alarm screens to explain how the ring recovers.

[Figure 27](#) shows what the resynchronized timing topology of the ring looks like after the link between Node 4-1 and Node 4-2 is broken.

Figure 27 – Topology When Link Between Node 4-1 and Node 4-2 is Broken



Node 3-1 still accepts the ST1 primary timing reference through the BIT 1 pins on its backplane. This is because Node 3-1 externally times, and does not line time, it is unaffected by the break in the ring.

Node 4-1 is upstream from the fiber break, and therefore can still accept the clockwise primary timing reference.

Node 4-2 is downstream from the fiber break, and has been forced to switch to accept the anti-clockwise secondary timing reference.

Node 3-2 is also downstream from the fiber break, and has also been forced to accept the anti-clockwise secondary timing reference.

Use the Alarm Screens to Explain Timing Topology Changes

Before you attempt to understand the timing changes on the individual nodes after the ring is broken, you must look at the network level CTC view of the changed timing topology.

Figure 28 – Modified Timing Topology

Alarms History Circuits

Date	Node	Type	Slot	Port	Dev	ST	SA	Cond	Description
01/03/70 14:05:05	Node 3-1	BITS-1			NA	R		PRS	Primary Reference Source - Stratum 1 Traceable
01/03/70 14:05:06	Node 3-1	SYNC-NE			NR	R		SWTOPRI	Synchronization Switch To Primary reference
01/03/70 14:05:06	Node 3-1	SYNC-NE			NR	R		PRS	Primary Reference Source - Stratum 1 Traceable
01/03/70 14:23:04	Node 3-2	FAC-S-1	5	1	NA	R		PRS	Primary Reference Source - Stratum 1 Traceable
01/03/70 05:16:07	Node 3-2	SYNC-NE			NR	R		SWTOSEC	Synchronization Switch To Second reference
01/03/70 05:16:07	Node 3-2	SYNC-NE			NR	R		PRS	Primary Reference Source - Stratum 1 Traceable
01/03/70 05:16:07	Node 3-2	FAC-B-1	6	1	NA	R		DUB	Don't Use for Synchronization
01/03/70 14:01:10	Node 4-1	SYNC-NE			NR	R		PRS	Primary Reference Source - Stratum 1 Traceable
01/03/70 14:01:10	Node 4-1	FAC-S-1	5	1	NA	R		PRS	Primary Reference Source - Stratum 1 Traceable
01/03/70 14:06:10	Node 4-1	SYNC-NE			NR	R		SWTOPRI	Synchronization Switch To Primary reference
01/03/70 07:26:33	Node 4-1	FAC-S-1	5	1	NA	R		DUB	Don't Use for Synchronization
01/03/70 07:26:35	Node 4-1	FAC-S-1	5	1	CR	R	<input checked="" type="checkbox"/>	ASL	Alarm Indication Signal - Line
01/03/70 07:26:36	Node 4-1	SYNC-NE			MN	R		SYNCSEC	Loss of timing on secondary synchronization link
01/03/70 07:26:37	Node 4-1	FAC-S-1	5	1	MU	R		EOC	SDCC termination failure
01/03/70 13:42:10	Node 4-2	BITS-1			MU	R	<input checked="" type="checkbox"/>	LOS	Loss of Signal
01/03/70 05:16:45	Node 4-2	SYNC-NE			MN	R		SYNCPRI	Loss of timing on primary synchronization link
01/03/70 05:16:45	Node 4-2	SYNC-DTC1			MN	R		SYNCPRI	Loss of timing on primary synchronization link
01/03/70 05:16:53	Node 4-2	FAC-S-1	5	1	NA	R		PRS	Primary Reference Source - Stratum 1 Traceable
01/03/70 05:16:53	Node 4-2	SYNC-NE			NR	R		SWTOSEC	Synchronization Switch To Second reference
01/03/70 05:16:53	Node 4-2	SYNC-NE			NR	R		PRS	Primary Reference Source - Stratum 1 Traceable
01/03/70 05:16:53	Node 4-2	SYNC-BITS1			NR	R		SWTOSEC	Synchronization Switch To Second reference
01/03/70 05:16:55	Node 4-2	FAC-B-1	6	1	MN	R		EOC	SDCC termination failure

Synchronize Alarms Delete Cleared Alarms AutoDelete Cleared Alarms

Now, look at the individual nodes in turn.

Timing Topology Changes for the First Node

As previously stated, each ONS 15454 has three timing sources, primary, secondary, and third. Node 3-1 is configured for external timing and accepts its timing references from these:

- **Primary** – The BITS 1 pins on the ONS 15454 backplane.
- **Secondary** – The internal ST3 clock on the TCC card.
- **Third** – The internal ST3 clock on the TCC card.

With this configuration, Node 3-1 is unaffected by the break in the ring as its primary timing reference source is connected directly onto its BITS 1 IN backplane pins. As [figure 29](#) shows, Node 3-1 remains unchanged.

Figure 29 – Alarm Screen Indicating that Node 3-1 is Unchanged

Note

The third alarm tells you interface on the 15454 where it is detecting the Stratum 1 traceable. In this case it is the BITS-1 pins on the 15454 backplane. The severity is NA (Not alarmed).

Note

The second alarm indicates that the 15454 has recognised that the Stratum 1 traceable matches its primary reference source and is switching to it. The severity is NR (Not Reported).

Note

The first alarm indicates that a Stratum 1 traceable primary reference source has been detected by the 15454. The severity is NR (Not Reported).

Date	Type	Slot	Port	sev	SI	SA	Cond	Description
01/02/00 21:05:05	SYNC-NE			NR	R		PR3	Primary Reference Source - Stratum 1 Traceable
01/02/00 21:05:05	SYNC-NE			NR	R		SWTOPRI	Synchronizat on Switch To Primary reference
01/02/00 21:05:05	BITS-1			NA	R		PR3	Primary Reference Source - Stratum 1 Traceable

Buttons: Synchronize Alarms, Delete Cleared Alarms, AutoDelete Cleared Alarms

Timing Topology Changes for the Second Node

Node 3-2 is configured for line timing, and accepts its timing references from these:

- **Primary** – The slot 6, port 1 Optical Carrier OC 48 line card.
- **Secondary** – The slot 5, port 1 Optical Carrier OC 48 line card.
- **Third** – The internal ST3 clock on the TCC card.

With this configuration, Node 3-2 is affected by a break in the ring. This is because it accepts its timing from the primary timing reference source coming clockwise around the ring across a break that is introduced into the ring.

Node 3-2 detects a loss of its primary timing source, and switches to its secondary timing source.

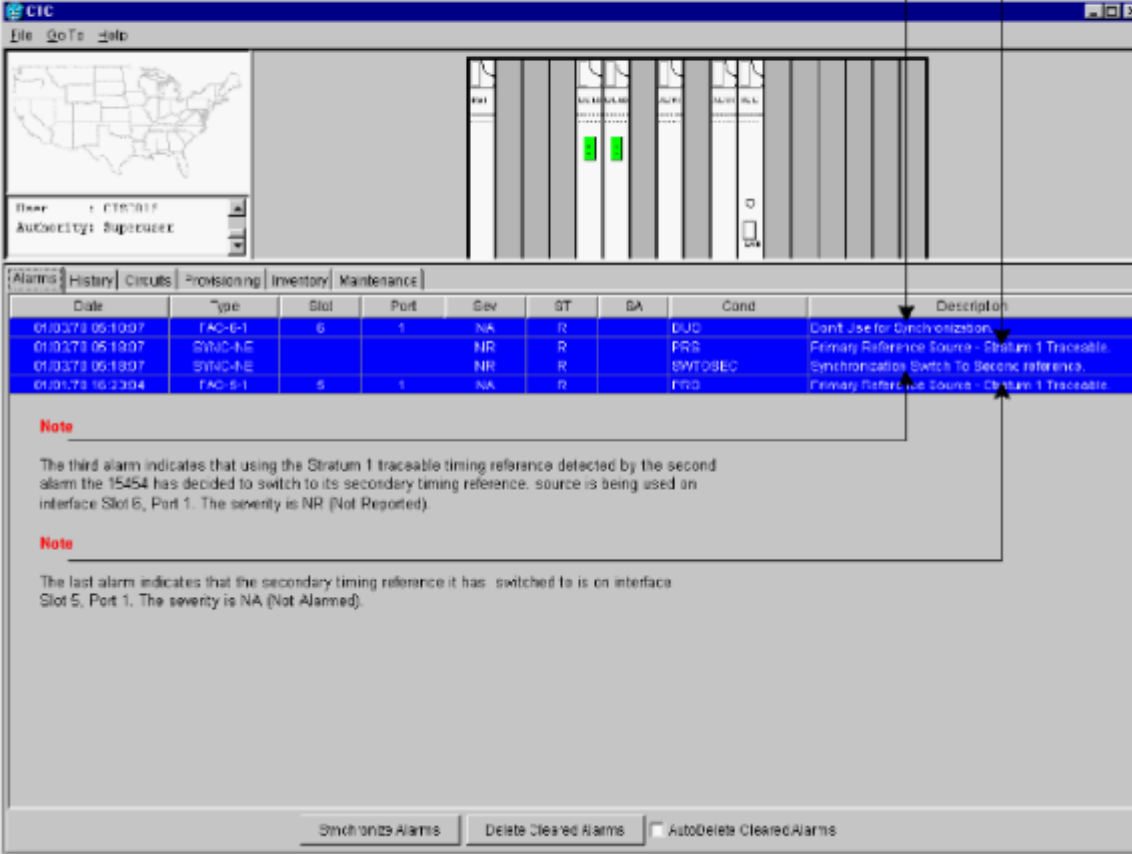
Figure 30 – Node 3-2 Detects a Loss of its Primary Timing Source

Note

The second alarm indicates that Node 3-2 has detected a Stratum 1 traceable timing reference source. The severity is NR (Not Reported).

Note

The first alarm indicates that due to change in the timing topology caused by the break in the ring, the next hop Node 4-2 is now using the output from interface Slot 6, Port 1 as its line timing reference. If a 15454 uses a particular Optical Card as its primary timing reference it sends back a DUS (Don't Use for Synchronization) alarm in order to prevent timing loops. The severity is NA (Not Alarmed).



The screenshot shows the 'Alarms' window in the Cisco ONS 15454 interface. It features a table with columns for Date, Type, Slot, Port, Sev, ST, SA, Cond, and Description. The table contains three entries related to timing synchronization. Below the table, there are two 'Note' sections providing context for the alarms. The first note explains that the first alarm is triggered by a ring break, causing Node 4-2 to use Slot 6, Port 1 as its primary timing reference. The second note states that the second alarm is triggered because Node 3-2 has detected a Stratum 1 traceable timing reference source. The table entries are as follows:

Date	Type	Slot	Port	Sev	ST	SA	Cond	Description
01/03/73 05:10:07	TAC-E-1	6	1	NA	R		DUC	Can't Use for Synchronization
01/03/73 05:10:07	SYNC-NE			NR	R		PRS	Primary Reference Source - Stratum 1 Traceable
01/03/73 05:10:07	SYNC-NE			NR	R		SWTOSBC	Synchronizes Switch To Second reference
01/01/73 16:23:04	TAC-E-1	5	1	NA	R		PRS	Primary Reference Source - Stratum 1 Traceable

Note

The third alarm indicates that using the Stratum 1 traceable timing reference detected by the second alarm the 15454 has decided to switch to its secondary timing reference. source is being used an interface Slot 6, Port 1. The severity is NR (Not Reported).

Note

The last alarm indicates that the secondary timing reference it has switched to is on interface Slot 5, Port 1. The severity is NA (Not Alarmed).

Buttons at the bottom: Synchronize Alarms, Delete Cleared Alarms, AutoDelete Cleared Alarms

Timing Topology Changes for the Third Node

Node 4-1 is configured for line timing, and accepts its timing references from these:

- **Primary** – The slot 6, port 1 Optical Carrier OC 48 line card.
- **Secondary** – The slot 5, port 1 Optical Carrier OC 48 line card.
- **Third** – The internal ST3 clock on the TCC card.

With this configuration, Node 4-1 is affected by the break in the ring. This is because it accepts its timing from the primary timing reference that comes clockwise around the ring from Node 3-2 before the break that is introduced into the ring. However, alarms are reported for the break in the ring.

Figure 31 – Alarms Reported for the Break in the Ring

Note

Indicates that the OC-48 Optical Card in slot 5 has detected an Alarm Indication Signal (AIS) in the SONET overhead. The severity is CR (Critical).

Note

Indicates that Node 4-1 can no longer synchronise with its secondary timing source. The severity is MN (Minor).

Note

Indicates that the OC-48 Optical Card in slot 5 has lost its Data Communication Channel (DCC). The severity is MJ (Major).

Date	Type	Slot	Port	Sev	ST	SA	Cond	Description
01/02/79 07:29:37	FAC-5-1	5	1	MJ	R		ECC	SDCC termination failure
01/02/79 07:29:38	SYNC-NE			MN	R		SYNCSEC	Loss of timing on secondary synchronization link
01/02/79 07:29:39	FAC-5-1	5	1	CR	R	<input checked="" type="checkbox"/>	AIS-L	Alarm Indication Signal - Line
01/02/79 07:29:33	FAC-5-1	5	1	NA	R		DUS	Don't Use for Synchronization
01/01/79 16:36:10	SYNC-NE			NR	R		SWTDRP	Synchronization switch to Primary reference
01/01/79 16:31:10	FAC-5-1	5	1	NA	R		PRS	Primary Reference Source - Stratum 1 Traceable
01/01/79 16:31:10	SYNC-NE			NR	R		PRS	Primary Reference Source - Stratum 1 Traceable

Note

Indicates that next hop Node 4-2 is using the output from Slot 5, Port 1 as its line timing reference if a 15454 uses an Optical Card as its primary timing reference it sends back a DUS (Don't Use for Synchronization) alarm in order to prevent timing loops. The severity is NA (Not Alarmed).

Note

Indicates that Node 4-1 has recognised that the Stratum 1 traceable OC-48 card on Slot 5, port 1 matches its primary reference source and is switching to it. The severity is NR (Not Reported).

Note

Indicates that a Stratum 1 traceable primary reference source is being used on interface Slot 5, Port 1. The severity is NA (Not Alarmed).

Note

Indicates that a Stratum 1 traceable primary reference source has been detected by Node 4-1. The severity is NR (Not Reported).

Synchronize Alarms Delete Cleared Alarms AutoDelete Cleared Alarms

Timing Topology Changes for the Fourth Node

Node 4-2 is configured for line timing, and accepts its timing references from these:

- **Primary** – The slot 6, port 1 Optical Carrier OC 48 line card.
- **Secondary** – The slot 5, port 1 Optical Carrier OC 48 line card.
- **Third** – The internal ST3 clock on the TCC card.

With this configuration, Node 4-2 is affected by the break in the ring and switches to its secondary timing source. This is because it accepts its timing from the primary timing reference that comes clockwise around the ring from Node 3-2 across the break that is introduced into the ring. Alarms are also reported for the break in the ring.

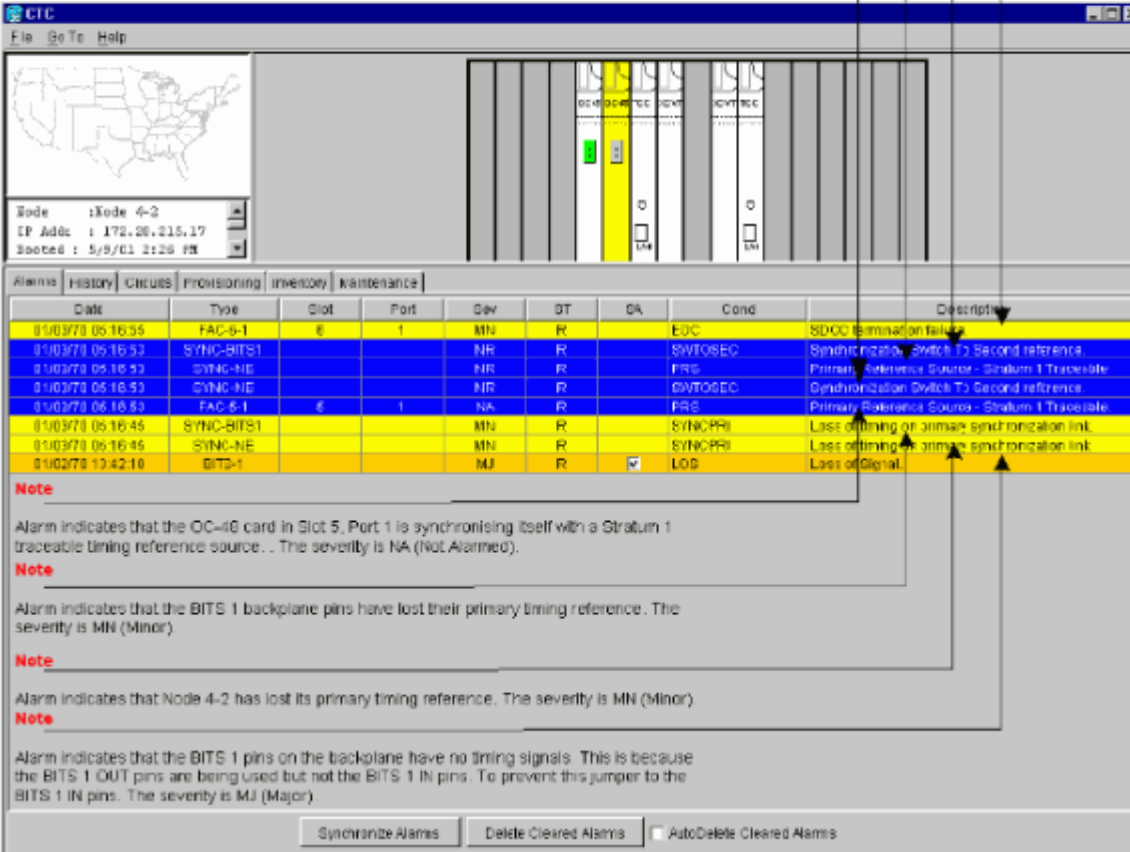
Figure 32 – Node 4-2 Affected by the Break in the Ring

Note
Alarm indicates that Node 4-2 has lost its Data Communication channel (DCC). The severity is NR (Not Reported).

Note
Alarm indicates that the BITS 1 pins on the backplane have switched to their secondary timing reference. The severity is NR (Not Reported).

Note
Alarm indicates that Node 4-2 is synchronising itself with a Stratum 1 traceable timing reference source. The severity is NR (Not Reported).

Note
Alarm indicates that Node 4-2 has switched to its secondary timing reference on Slot 5, Port 1. The severity is NR (Not Reported).



Date	Type	Slot	Port	Dev	ST	DA	Cond	Description
01/03/73 05:16:55	FAC-S-1	5	1	MN	R		EDC	SDCC termination failure
01/03/73 05:16:53	SYNC-BITS1			NR	R		SWTOSCC	Synchronization Switch To Second reference
01/03/73 05:16:53	SYNC-NE			NR	R		PRS	Primary Reference Source - Stratum 1 Traceable
01/03/73 05:16:53	SYNC-NE			NR	R		SWTOSCC	Synchronization Switch To Second reference
01/03/73 05:16:53	FAC-S-1	5	1	NA	R		PRS	Primary Reference Source - Stratum 1 Traceable
01/03/73 05:16:45	SYNC-BITS1			MN	R		SYNCPRI	Last of timing on primary synchronization link
01/03/73 05:16:45	SYNC-NE			MN	R		SYNCPRI	Last of timing on primary synchronization link
01/02/73 13:42:10	BITS-1			MJ	R		LOG	Last of Signal

Note
Alarm indicates that the OC-48 card in Slot 5, Port 1 is synchronising itself with a Stratum 1 traceable timing reference source. The severity is NA (Not Alarmed).

Note
Alarm indicates that the BITS 1 backplane pins have lost their primary timing reference. The severity is MN (Minor).

Note
Alarm indicates that Node 4-2 has lost its primary timing reference. The severity is MN (Minor).

Note
Alarm indicates that the BITS 1 pins on the backplane have no timing signals. This is because the BITS 1 OUT pins are being used but not the BITS 1 IN pins. To prevent this jumper to the BITS 1 IN pins. The severity is MJ (Major).

Synchronize Alarms Delete Cleared Alarms AutoDelete Cleared Alarms

Timing Topology Recovery (Reversion)

In the lab set, each node had the **revertive** option selected in the CTC timing configuration screen. When you select this option, the node is instructed that if it loses its primary timing reference and has to switch, it must accept either the secondary or third timing reference. If it later recovers its primary timing reference, it can switch back to accept it.

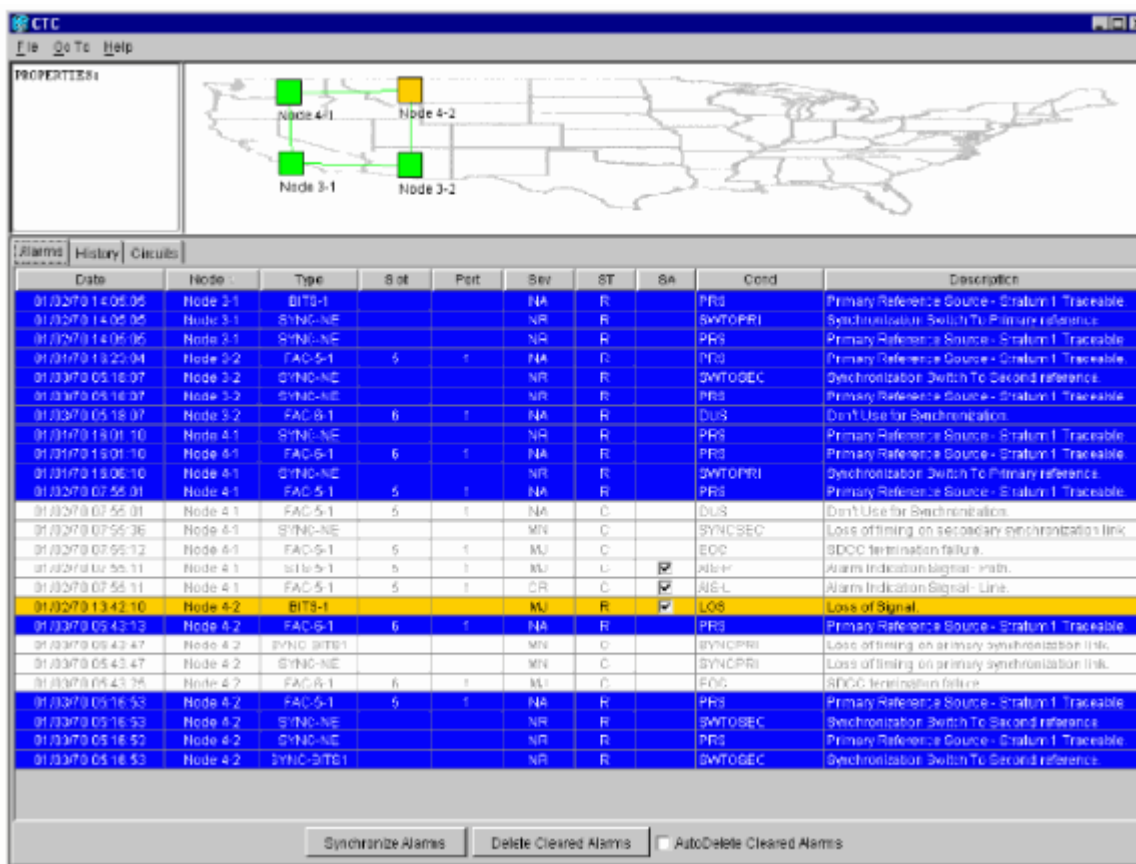
Each node also had their reversion timer set to **five** minutes. The reversion timer specifies how long after a node regains its primary timing reference it waits before it switches back to accept it.

The fiber break in the lab setup is now repaired. The nodes recognize that the break is repaired, but do not change their timing topologies until after the reversion timers have expired. After five minutes, the reversion timers expire, and the timing topology reverts to its original state with each node accepting the ST1 primary timing reference coming clockwise round the ring from the BITS 1 pins on Node 3-2.

[Figure 33](#) shows the CTC network view of the timing topology three minutes after the fiber break has been repaired. The nodes have detected that the fiber break has been repaired, but still have two

minutes to wait before their reversion timers expire.

Figure 33 – CTC Network View of the Timing Topology 3 Minutes After the Fiber Break is Repaired



The messages above have been sorted by node. All the MN (Minor), MJ (Major), and CR (Critical) alarms caused by the fiber break between Node 4-1 and Node 4-2 are now white. This indicates that Node 4-1 and Node 4-2 have detected that the fiber break has been repaired.

In addition, the DUS SSM message on Node 4-1 is also white. This is because Node 4-2 accepts its secondary timing reference from Node 3-2, and sends DUS back to Node 3-2. Although Node 4-2 now has a valid primary timing reference incoming from Node 4-1 over the repaired fiber link, it does not switch back to accept it until the reversion timer has expired.

Normally, an ONS 15454 will only send back DUS on the interface on which it accepts its timing.

[Figure 34](#) shows the screen just after the five minute reversion timer has expired.

Figure 34 – The 5-Minute Reversion Timer has Expired

Date	Node	Type	Snt	Port	Svc	RT	RA	Cond	Description
01/02/70 14:05:05	Node 3-1	BITS-1			NA	R	PRS		Primary Reference Source - Stratum 1 Traceable
01/02/70 14:05:05	Node 3-1	SYNC-NE			NR	R	SWTOPRI		Synchronization Switch To Primary reference
01/02/70 14:05:05	Node 3-1	SYNC-NE			NR	R	PRS		Primary Reference Source - Stratum 1 Traceable
01/02/70 15:22:04	Node 3-2	FAC 5-1	5	1	NA	R	PRS		Primary Reference Source - Stratum 1 Traceable
01/02/70 05:16:07	Node 3-2	SYNC-NE			NR	R	PRS		Primary Reference Source - Stratum 1 Traceable
01/02/70 05:48:50	Node 3-2	FAC 6-1	6	1	NA	C	DUS		Don't Use for Synchronization
01/02/70 05:50:00	Node 3-2	SYNC-NE			NR	R	SWTOPRI		Synchronization Switch To Primary reference
01/02/70 05:50:00	Node 3-2	SYNC-NE			NR	C	SWTOSEC		Synchronization Switch To Second reference
01/02/70 05:48:50	Node 3-2	FAC 6-1	6	1	NA	R	PRS		Primary Reference Source - Stratum 1 Traceable
01/02/70 15:01:10	Node 4-1	SYNC-NE			NR	R	PRS		Primary Reference Source - Stratum 1 Traceable
01/02/70 15:01:10	Node 4-1	FAC 6-1	6	1	NA	R	PRS		Primary Reference Source - Stratum 1 Traceable
01/02/70 15:06:10	Node 4-1	SYNC-NE			NR	R	SWTOPRI		Synchronization Switch To Primary reference
01/02/70 07:55:36	Node 4-1	SYNC-NE			MR	C	SYNCCDC		Loss of timing on secondary synchronization link
01/02/70 08:06:26	Node 4-1	FAC 5-1	5	1	NA	C	PRS		Primary Reference Source - Stratum 1 Traceable
01/02/70 08:06:26	Node 4-1	FAC 5-1	5	1	NA	R	DUS		Don't Use for Synchronization
01/02/70 07:55:12	Node 4-1	FAC 5-1	5	1	MU	C	EOC		SDCC termination failure
01/02/70 07:55:11	Node 4-1	STS-5-1	5	1	MU	C	AIS-P		Alarm Indication Signal - Path
01/02/70 07:55:11	Node 4-1	FAC 5-1	5	1	CR	C	AIS-L		Alarm Indication Signal - Line
01/02/70 13:43:10	Node 4-2	BITS-1			MU	R	LOS		Loss of Signal
01/02/70 03:42:13	Node 4-2	FAC 6-1	6	1	NA	R	PRS		Primary Reference Source - Stratum 1 Traceable
01/02/70 05:48:36	Node 4-2	SYNC-NE			NR	C	SWTOSEC		Synchronization Switch To Second reference
01/02/70 05:48:46	Node 4-2	FAC 5-1	5	1	NA	C	PRS		Primary Reference Source - Stratum 1 Traceable
01/02/70 05:48:46	Node 4-2	FAC 5-1	5	1	NA	R	DUS		Don't Use for Synchronization
01/02/70 05:48:36	Node 4-2	SYNC-NE			NR	C	SWTOSEC		Synchronization Switch To Second reference
01/02/70 05:48:36	Node 4-2	SYNC-NE			NR	R	SWTOPRI		Synchronization Switch To Primary reference
01/02/70 05:48:36	Node 4-2	SYNC-NE			NR	R	SWTOPRI		Synchronization Switch To Primary reference
01/02/70 05:43:47	Node 4-2	SYNC-STS1			MR	C	SYNCPRI		Loss of timing on primary synchronization link
01/02/70 05:43:47	Node 4-2	SYNC-NE			MR	C	SYNCPRI		Loss of timing on primary synchronization link
01/02/70 05:43:25	Node 4-2	FAC 6-1	6	1	MU	C	EOC		SDCC termination failure
01/02/70 05:16:53	Node 4-2	SYNC-NE			NR	R	PRS		Primary Reference Source - Stratum 1 Traceable

The messages above have been sorted by node. Here are the messages for each node in turn:

- **Node 3-1** – Remains unchanged because it accepts its primary timing reference from its BITS 1 pins it is unaffected by the timing topology changes.
- **Node 3-2** – Lost its primary timing reference source when the fiber break occurred. This is because it was downstream from the clockwise primary timing reference from Node 3-1. It had to switch to accept its secondary timing reference coming anti-clockwise from Node 3-1. In addition, Node 4-2 had to change to its secondary timing reference because it was also downstream of the fiber break. Node 4-2 accepted its secondary timing reference provided anti-clockwise from Node 3-2.

The first alarm that is white for Node 3-2 is DUS. This is because Node 4-2 has switched to use its clockwise primary timing reference and no longer uses the anti-clockwise secondary timing reference from Node 3-2. Normally, an ONS 15454 only sends back DUS on the interface from which it accepts its timing.

The second alarm that is white for Node 3-2 is SWTOSEC (Switch To Secondary). This is because Node 3-2 has now detected and switched back to use its primary timing reference.

- **Node 4-1** – The only timing alarm that is white for Node 4-1 is PRS for FAC 5-1 (Facility). This is because Node 4-2 now uses the primary timing reference that comes clockwise around the ring that Node 4-1 sends. Because it accepts this timing reference it sends a DUS is back. Hence, Node 4-1 can no longer use this interface as a timing reference. Normally, an ONS 15454 only sends back DUS on the interface from which it accepts its timing.
- **Node 4-2** – The first two timing alarms (SWTOSEC and PRS) that are white were issued when it switched to accept its secondary timing source from Node 3-2. Because Node 4-2 has

now switched back to accept its primary timing reference these alarms are now white.

The third timing alarm (SWTOSEC) that is white was from the BITS 1 interface on Node 4-2, to state that it had switched to its secondary timing reference. Because the BITS 1 interface on Node 4-2 has now also switched back to its primary timing source, this message is now white.

The last two timing alarms (SYNCPRI) that are white come from Node 4-2 itself and the BITS 1 interface. This indicates that they had both lost their primary timing reference. Because the primary timing reference has now been restored, these messages are now white.

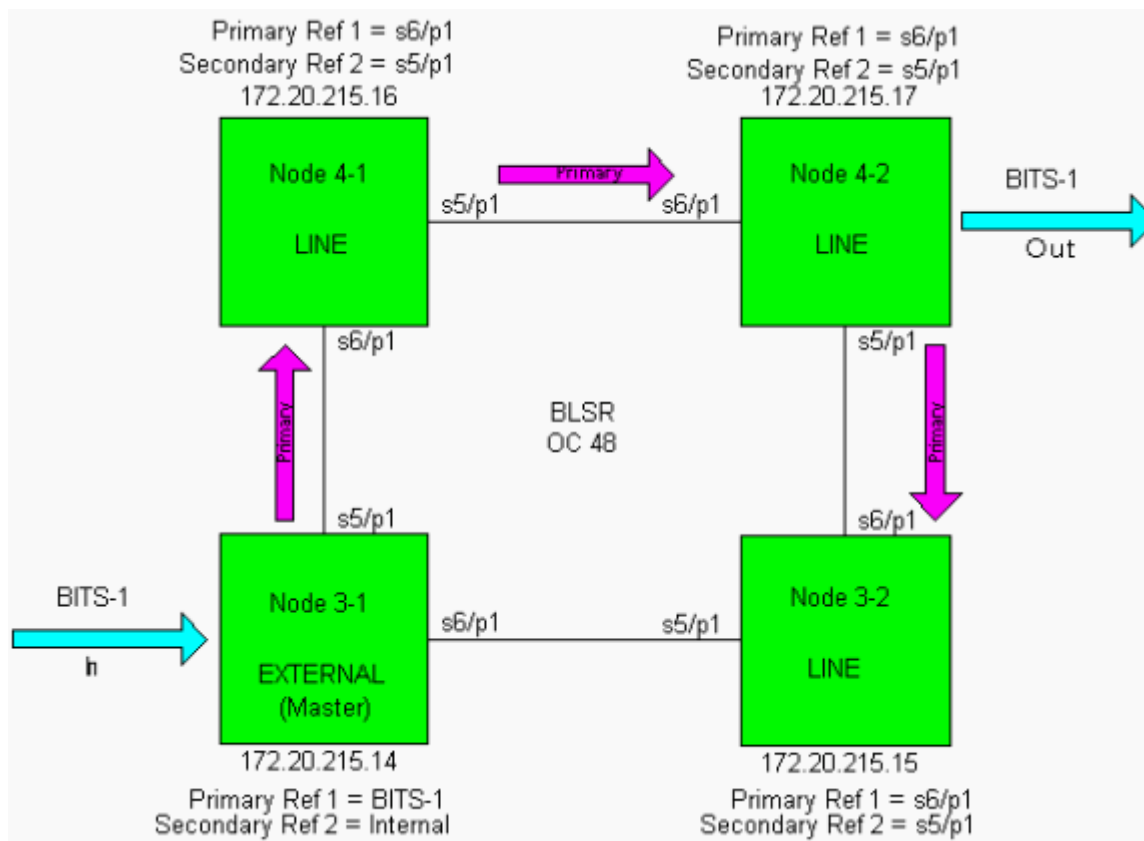
[Figure 35](#) shows the final active alarm screen after all the alarms have been cleared.

Figure 35 – The Final Active Alarm Screen

Date	Node	Type	Ref	Port	Rev	RT	RA	Coord	Description
01/02/70 14:05:36	Node 3-1	BITS-1			NA	R	PR3		Primary Reference Source - Stratum 1, Traceable
01/02/70 14:05:36	Node 3-1	SYNCPRI			NR	R	SWTOPRI		Synchronization Switch To Primary reference.
01/02/70 14:05:36	Node 3-1	SYNCPRI			NR	R	PR3		Primary Reference Source - Stratum 1, Traceable
01/02/70 14:05:34	Node 3-2	FAC-S-1	5	1	NA	R	PR3		Primary Reference Source - Stratum 1, Traceable
01/02/70 05:18:37	Node 3-2	SYNCPRI			NR	R	PR3		Primary Reference Source - Stratum 1, Traceable
01/02/70 05:48:50	Node 3-2	FAC-B-1	6	1	NA	R	PR3		Primary Reference Source - Stratum 1, Traceable
01/02/70 05:50:30	Node 3-2	SYNCPRI			NR	R	SWTOPRI		Synchronization Switch To Primary reference.
01/02/70 14:01:10	Node 4-1	SYNCPRI			NR	R	PR3		Primary Reference Source - Stratum 1, Traceable
01/02/70 14:01:10	Node 4-1	FAC-B-1	6	1	NA	R	PR3		Primary Reference Source - Stratum 1, Traceable
01/02/70 14:00:10	Node 4-1	SYNCPRI			NR	R	SWTOPRI		Synchronization Switch To Primary reference.
01/02/70 04:00:26	Node 4-1	FAC-B-1	5	1	NA	R	DUS		Don't Use for Synchronization.
01/02/70 13:42:10	Node 4-2	BITS-1			NA	R	LOS		Loss of Signal.
01/02/70 05:16:53	Node 4-2	SYNCPRI			NR	R	PR3		Primary Reference Source - Stratum 1, Traceable
01/02/70 05:43:13	Node 4-2	FAC-B-1	6	1	NA	R	PR3		Primary Reference Source - Stratum 1, Traceable
01/02/70 05:48:26	Node 4-2	SYNCPRI			NR	R	SWTOPRI		Synchronization Switch To Primary reference.
01/02/70 03:46:36	Node 4-2	SYNCPRI			NR	R	SWTOPRI		Synchronization Switch To Primary reference.
01/02/70 05:46:46	Node 4-2	FAC-S-1	5	1	NA	R	DUS		Don't Use for Synchronization.

Here, we can see that the timing topology has reverted to its original configuration, wherein each node accepts the primary timing reference clockwise around the ring.

Figure 36 – Each Node Accepts the Primary Timing Reference Clockwise Around the Ring



Timing Alarms/Conditions and Troubleshooting Timing (software level dependent)

This section describes timing alarms and conditions. It also provides tips and procedures to troubleshoot or solve them.

FRNGSYNC

Free run synchronization (FRNGSYNC) is a major, service affecting error.

The reporting ONS 15454 is in free run synchronization mode. External timing sources have been disabled and the node uses its internal clock, or the ONS 15454 has lost its designated BITS timing source.

To clear the FRNGSYNC, complete these steps:

1. If the ONS 15454 is configured to operate from its own internal clock, disregard this alarm.
2. If the ONS 15454 is configured to operate off an external timing source, verify that the BITS timing source is valid. Common problems with a BITS timing source include reversed wiring and bad timing cards.

FSTSYNC

Fast Start Synchronization (FSTSYNC) is a minor, non-service affecting alarm.

FSTSYNC mode means the ONS 15454 chooses a new timing reference. The previous timing reference has failed. This alarm disappears after approximately 30 seconds. This is an informational

alarm.

HLDOVERSYNC

Holdover Synchronization (HLDOVERSYNC) is a major, service affecting alarm.

Loss of the primary/secondary timing reference raises the HLDOVERSYNC alarm. Timing reference loss occurs when line coding on the timing input is different than the configuration on the ONS 15454. It also usually occurs during the selection of a new node reference clock. This alarm indicates that the ONS 15454 has gone into holdover and is using the ONS 15454 internal reference clock, which is a ST3-level timing device. The alarm clears when primary or secondary timing is reestablished.

To clear the HLDOVERSYNC, complete these steps:

1. Check for additional alarms that relate to timing.
2. Reestablish a primary and secondary timing source according to local site practice.

LOF (TCC+)

Loss of Frame (LOF) (TCC+) is a major, service affecting alarm.

A port on the TCC+ BITS input detects a LOF on the incoming BITS timing reference signal. LOF indicates that the receiving ONS 15454 has lost frame delineation in the incoming data.

Note: The procedure assumes that the BITS timing reference signal functions properly. It also assumes the alarm does not appear during node turn-up.

To clear the LOF on the TCC+, complete these steps:

1. Verify that the line framing and line coding match between the BITS input and the TCC+.
2. In CTC, note the slot and port reporting the alarm.
3. Find the coding and framing formats of the external BITS timing source. This should be in the user documentation for the external BITS timing source or on the timing source itself.
4. Click the **Provisioning** > **Timing** tabs to display the General Timing screen.
5. Verify that Coding matches the coding of the BITS timing source (either B8ZS or AMI).
6. If the coding does not match, click **Coding** to reveal a menu. Choose the appropriate coding. For more information refer to these sections:
 - o Page 36 of the Cisco ONS 15454 Troubleshooting and Reference Guide
 - o Page 78 of 12576-01 June 2001 Alarm Troubleshooting for PalmOS
7. Verify that Framing matches the framing of the BITS timing source (either ESF or SF [D4]).
8. If the framing does not match, click **Framing** to reveal the menu. Choose the appropriate framing.

Note: On the timing subtab, the B8ZS coding field is normally paired with ESF in the Framing field, and the AMI coding field is normally paired with SF (D4) in the Framing field.

9. If the alarm does not clear when the line framing and line coding match between the BITS input and the TCC+, replace the TCC+ card.

Note: When you replace a card with an identical type of card, you do not need to make any changes to the database.

STU

Synchronization Traceability Unknown (STU) is not alarmed.

The STU alarm occurs when the reporting node is timed to a reference that does not support Synchronous Status Messaging (SSM). SSM is a SONET protocol that communicates information about the quality of the timing source. SSM messages are carried on the S1 byte of the SONET line layer. SSM enables SONET devices to automatically choose the highest quality timing reference and to avoid timing loops. The ONS 15454 supports SSM. This alarm indicates that the reporting node has SSM enabled but the timing source does not support SSM, or the reporting node does not have SSM enabled but the timing source supports SSM.

To clear the STU, complete these steps:

1. Click the **Provisioning > Timing** tabs.
2. If Sync Messaging is checked, clear the selection. If Sync Messaging is not selected, check the box.
3. Click **Apply**.

SWTOPRI

Switched to Primary (SWTOPRI) is not alarmed.

The ONS 15454 has switched to the primary timing source (reference 1). The ONS 15454 uses three ranked timing references. The timing references are typically two BITS-level or line-level sources and an internal reference.

Note: This is a condition and not an alarm. It is for information only and does not require you to troubleshoot.

SWTOSEC

Switched to Secondary (SWTOSEC) is not alarmed. For more information, refer to these sections:

- Page 56 of the Cisco ONS 15454 Troubleshooting and Reference Guide
- Page 78 of 12576-01 June 2001 Alarm Troubleshooting for PalmOS

The ONS 15454 has switched to the secondary timing source (reference 2). The ONS 15454 uses three ranked timing references. The timing references are typically two BITS-level or line-level sources and an internal reference.

To clear the SWTOSEC, lookup and troubleshoot alarms related to failures of the primary source, such as the SYNCPRI alarm.

SWTOTHIRD

Switched to Third (SWTOTHIRD) is not alarmed.

The ONS 15454 has switched to the third timing source (reference 3). The ONS 15454 uses three ranked timing references. The timing references are typically two BITS-level or line-level sources and an internal reference.

To clear the SWTOTHIRD, lookup and troubleshoot alarms related to failures of the primary and secondary reference source, such as the SYNCPRI and SYNCSEC alarms.

SYNCPRI

Loss of Timing on Primary Reference (SYNCPRI) is a minor, non-service affecting alarm.

A SYNCPRI alarm occurs when the ONS 15454 loses the primary timing source (reference 1). The ONS 15454 uses three ranking timing references. The timing references are typically two BITS-level or line-level sources and an internal reference. If SYNCPRI occurs, the ONS 15454 should switch to its secondary timing source (reference 2). This switch also triggers the SWTOSEC alarm.

To clear the SYNCPRI on the TCC+ Card, complete these steps:

1. From the card view for the reporting TCC+ card, click the **Provisioning** > **Timing** tabs.
2. Check the current configuration for the REF-1 of the NE Reference.
3. If the primary reference is a BITS input, follow the procedure in the "LOS (OC-N)" section on page 41.
4. If the primary reference clock is an incoming port on the ONS 15454, check the **primary reference clock**.

SYNCSEC

SYNCSEC is a minor, non-service affecting alarm.

For more information, refer to these sections:

- Page 57 of the Cisco ONS 15454 Troubleshooting and Reference Guide
- Alarm Troubleshooting for Palm OS 78-12576-01 June 2001

A Loss of Timing on Secondary Reference alarm occurs when the ONS 15454 loses the secondary timing source (reference 2). The ONS 15454 uses three ranked timing references. The timing references are typically two BITS-level or line-level sources and an internal reference. If SYNCSEC occurs, the ONS 15454 should switch to the third timing source (reference 3) to obtain valid timing for the ONS 15454. This switch also triggers the SWTOTHIRD alarm.

To clear the SYNCSEC on the TCC+ Card, complete these steps:

1. From the card view for the reporting TCC+ card, click the **Provisioning > Timing** tabs.
2. Check the current configuration of the REF-2 for the NE Reference.
3. If the secondary reference is a BITS input, follow the procedure in the "LOS (OC-N)" section on page 41.
4. If the secondary timing source is an incoming port on the ONS 15454, check the secondary timing source.

SYNCTHIRD

SYNCTHIRD is a minor, non-service affecting alarm.

A Loss of Timing on Third Reference alarm occurs when the ONS 15454 loses the third timing source (reference 3). The ONS 15454 uses three ranking timing references. The timing references are typically two BITS-level or line-level sources and an internal reference. If SYNCTHIRD occurs and the ONS 15454 uses an internal reference for source three, then the TCC+ card may have failed. The ONS 15454 often reports either FRNGSYNC or HLDOVERSYNC after SYNCTHIRD.

To clear the SYNCTHIRD on the TCC+ Card, complete these steps:

1. From the card view for the reporting TCC+ card, click the **Provisioning > Timing** tabs.
2. Check the current configuration of the REF-3 for the NE Reference.
3. If the third timing source is a BITS input, follow the procedure in the "LOS (OC-N)" section on page 41.
4. If the third timing source is an incoming port on the ONS 15454, check the timing source.
5. If the third timing source uses the internal ONS 15454 timing, perform a software reset on the TCC+ card:
 - a. Display the CTC node view.
 - b. Position the cursor over the slot reporting the alarm.
 - c. Right-click and choose **RESET CARD**.
6. If this fails to clear the alarm, physically reset the TCC+ card.
7. If the reset fails to clear the alarm, replace the TCC+ card.

For more information, refer to:

- Chapter Two of Cisco ONS 15454 Troubleshooting Guide - Release 4.1.x and Release 4.5 (Alarm Troubleshooting).

Note: When you replace a card with an identical type of card, you do not need to make any changes to the database.

Timing Wallchart

Use this [PDF wallchart](#) for more information on timing.

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How do I stop this warning! - Dec 9, 2004
Protection in VPLS - Draft - Dec 1, 2004

Related Information

- [ONS 15454 User Documentation v2.2.1 - Setting Up Timing](#)
- [ONS 15454 Installation and Operations Guide v3.0 - Setting Up Timing](#)
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