

Troubleshooting Clocking Issues on the PA–A2

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Introduction

Network clocking defines the process of recovering clocking from a physical interface connected to your network and then using this clock source to generate the transmit clock for other physical interfaces configured for a network–derived transmit clock source. We configure a network clocking policy to ensure that the network–derived physical interfaces all are synchronized to the same external timing reference.

The PA–A2 port adapter for the 7200 series supports three sources of network clocking:

- Receive clock on the ATM WAN uplink port
- T1/E1 CBR interfaces
- Local reference oscillator used to run the T1/E1 framers

Use the **network–clock–select <priority>** configuration command to select ports for network clock extraction. Up to four ports can be chosen for clock extraction. Use the **show network–clocks** command to view these ports and their configured priority.

When using a physical interface as the network clock source, your router may report a change in the current clock source via a log and/or console message depending on your router's logging configuration.

The purpose of this document is to review network clocking on the PA–A2 and provide information to help troubleshoot clocking issues.

Before You Begin

Conventions

For more information on document conventions, see the Cisco Technical Tips Conventions.

Prerequisites

There are no specific prerequisites for this document.

Components Used

This document is not restricted to specific software and hardware versions.

Understanding the Framer Crystal Oscillator

The PA–A2 electronics includes a reference crystal oscillator that runs the T1/E1 framers. This reference oscillator provides a Stratum 4 clock source. Note that Stratum defines the accuracy of a clock source. Typically, telcos provide clock source with Stratum 1 or 2 accuracy.

Oscillators built around quartz crystals can be extremely accurate and stable. In a crystal oscillator circuit, an AC signal is applied through a crystal slab, causing the crystal to vibrate. The thickness of the crystal slab determines the resonant frequency or the specific frequency at which the oscillator is most willing to vibrate.

Selecting Clock Sources

When the port adapter is initializing, the current clock source is set to the local oscillator used to run the T1/E1 framers. The router then checks the up/down status of all physical ports on the PA–A2. Depending on the configuration, it selects an active physical port with the highest priority level as the current transmit clock source for network–derived interfaces. This so–called derived clock is distributed to other ports on the PA–A2 that are configured to use network–derived clocking as the transmit clock.

Use the following two configuration commands on the PA–A2 to create a network clock selection policy.

- **network–clock–select** – Specifies one or more clock sources that serve as a transmit clock on interfaces configured for network–derived clocking using the **ces dsx1 clock source network–derived** command on the CBR interfaces or the default atm clock internal on the ATM port.
- **ces dsx1 clock source** – Specifies for an individual interface which clock source to use as a transmit clock. The following two options are available on the PA–A2:
 - ◆ *Network–derived* – Interface uses the clock source specified by the **network–clock–select** statement. Use the **show network–clock** command to find out which clock source is being used.
 - ◆ *Loop–timed* – Interface uses the clock source received on the same interface. This mode can be used when connecting to a device with a very accurate clock source.

Let's look at this process step by step.

1. Review the list of currently configured network clock sources with the **show network–clocks** command.

```
7200-2.4#show network-clocks
Priority 1 clock source: not configured
Priority 2 clock source: not configured
Priority 3 clock source: not configured
Priority 4 clock source: not configured
Priority 5 clock source: Local oscillator
Current clock source:Local oscillator, priority:5
```

2. Use the **network-clock-select** command to configure a network clock source. In this example, we specify CBR port 2/0.

```
7200-2.4(config)#network-clock-select ?
<1-4> priority
```

```
7200-2.4(config)#network-clock-select 1 ?
ATM ATM interface
CBR Constant Bit Rate
```

```
7200-2.4(config)#network-clock-select 1 cbr 2/0
```

3. Confirm your configuration change with the **show network-clocks** command.

```
7200-2.4#show network-clocks
Priority 1 clock source: CBR2/0 UP
Priority 2 clock source: not configured
Priority 3 clock source: not configured
Priority 4 clock source: not configured
Priority 5 clock source: Local oscillator
Current clock source:CBR2/0, priority:1
```

Note: We will take this recovered clock source and feed it into the Phase-Locked Loop (PLL), which corrects any frequency drifts and maintains the accuracy of the clock source.

4. Configure a CBR port to be network-derived with the **ces dsx1 clock source network-derived** command.

```
7200-2.4(config-if)#ces dsx1 clock source ?
loop-timed Configure the Transmit clock timing to loop
network-derived Configure the Transmit clock to be derived from the Network
```

5. Confirm your setting with the **show ces interface cbr** command.

```
7200-2.4#show ces int cbr 2/0
Interface: CBR2/0 Port-type:T1-DCU
IF Status: DOWN Admin Status: UP
Channels in use on this port:
LineType: ESF LineCoding: B8ZS LoopConfig: NoLoop
SignalMode: NoSignalling XmtClockSrc: network-derived
DataFormat: Structured AAL1 Clocking Mode: Synchronous LineLength: 0_110
LineState: Up
Errors in the Current Interval:
PCVs 0 LCVs 0 ESs 0 SESs 0 SEFSs 0
UASs 0 CSSs 0 LESs 0 BESSs 0 DMs 0
Errors in the last 24Hrs:
PCVs 0 LCVs 1 ESs 0 SESs 0 SEFSs 0
UASs 0 CSSs 0 LESs 0 BESSs 0 DMs 0
Input Counters: 0 cells, 0 bytes
Output Counters: 0 cells, 0 bytes
```

Network-Derived Clocking

On the PA-A2, specify network-derived clocking with one of the following commands depending on the interface type:

- ATM – Leave the default configuration of internal clocking. Use the **no atm clock internal** command to specify transmit timing from the line and the equivalent of loop-timed clocking. Use the **show atm interface atm** command to confirm the configured transmit clock source.

```
7200-2.4#show atm int atm 2/0
Interface ATM2/0:
AAL enabled: AAL5 , Maximum VCs: 2047, Current VCCs: 2
```

```
Maximum Transmit Channels: 256
Max. Datagram Size: 4516
PLIM Type: SONET - 155000Kbps, TX clocking: LINE
988 input, 988 output, 0 IN fast, 0 OUT fastVBR-NRT : 2500
Avail bw = 152500
Config. is ACTIVE
```

- CBR – Use the **ces dsx1 clock source** command.

```
7200-2.4(config-if)#ces dsx1 clock source ?
    loop-timed      Configure the Transmit clock timing to loop
    network-derived Configure the Transmit clock to be derived from the Net
```

Note that although the configuration commands differ for the two port types, the functionality is the same. The router runs through the **network-clock-select** statements and finds the highest-priority clock source. If this source remains stable for one minute, the router uses this source for network-derived interfaces. If no sources remain stable or are configured, the router defaults to using the framer oscillator.

Understanding PLL

Before we discuss how to troubleshoot network clock faults, we first need to understand what a PLL is.

A phase-locked loop (PLL) is an electronic circuit that synchronizes itself to an external "reference" signal. It locks itself onto the phase or onto the average frequency of the incoming signal, dynamically tracks it, and outputs a related but more useful version. Among the typical applications of a PLL in digital circuits are synchronizing a system to a single clock source and jitter filtering (removing phase noise).

The PA-A2 uses a PLL chip to provide hardware support for accurate clocking distribution. The adapter feeds the selected clock source into the PLL, which locks onto and tracks the clock source. In turn, this high quality, locked clock is fed to the network clock interfaces to provide interface timing. In other words, the crystal oscillator generates the carrier frequency, and the PLL helps it stay in phase.

When conditions lead to a cutover between clock sources, the PLL minimizes network clocking disruptions with a relatively smooth cutover and minimal loss.

Troubleshooting Clock Faults

In rare circumstances, the router reports a network clock switchover or a change in the current clock source. In general, there are two methods of determining whether or not the selected clock source is of sufficient quality and whether or not to initiate a network clock switchover:

- Loss of activity detection – Simply monitors the *up/down* state of the physical interface from which the network clock is being extracted.
- Loss of lock detection – Uses a PLL to monitor the quality of the selected clock. If the *quality* is not acceptable, the selected clock source is declared down, and the next available active clock source is selected.

The following sections discuss these switchover reasons in greater detail.

Loss of Activity Detection

All systems with network-derived clock sources support loss of activity detection, in which the system simply monitors the up/down state of the physical interface from which the network clock is being extracted. The clock failure is detected when the port driver detects loss of signal or loss of frame.

In other words, any time that a physical port transitions from up to down or down to up state, the system checks whether that port is configured as a network clock source. If so, then the system calls the appropriate software functions to bring the network clock source up or down. A clock source must be up for 1 minute for any revertive action to take effect and for the router to make this source the new current source.

The configured clock sources are searched after one of the following occurs:

- Change in up/down status of physical port
- Loss of lock by PLL
- Configuration change to the network clock sources

If a higher preference clock source becomes available and stays active for more than one minute, then the network clock source is switched over to the higher preference clock.

If the current network clock source fails, then the next available active clock source with the highest preference is selected as the network clock source. If none of the configured clock sources are active, then the PA–A2's framer crystal oscillator is used as the network clock source.

Loss of Lock Detection

A PLL plays an important role in ensuring accurate clocking. In an LS1010 with an FC1 and in other systems without a PLL, there is no loss of lock detection. The system considers a given clock source to be good or bad simply based on whether the physical port from which the network clock is being extracted is up or down. Systems with a PLL are capable of detecting loss of lock and initiate an automatic switchover to a secondary clock source.

To detect an out of lock or loss of lock condition, the system polls a PLL/alarm register at a regular interval. If the PLL goes out of lock, then the system invokes a series of routines that leads to searching through the configured network clock sources in order of priority to select the highest active clock source.

We see the following message when the PLL detects loss of lock:

```
1w4d: %NETWORK_CLOCK_SYNCHRONIZATION-4-NETCLK_PLL_LOST_LOCK:  
Network clock Wan-uplink PLL lost lock - clock source failed.
```

Understanding Clock Distribution Across PAs

An ATM switch supports the ability to distribute clock across modules. In other words, we extract a clock source from a physical port, and we make it the system clock or global clock.

On the 7200 VXR series, this capability requires special multiservice interchange (MIX) interconnections on the midplane, to which the I/O controller, port adapters, power supplies, and network processing engine connect directly. The MIX interconnections provide the ability to switch DS–0 time slots between multichannel T1 or E1 interfaces, much like a digital cross–connect or an add–drop multiplexer. These interconnections also enable a network clock from one port to be sent to another other port on the port adapter or to other adapters using the MIX bus. In data mode, each port can be configured as a separate clock source.

Only select port adapters with specific MIX support can derive clocking from another port adapter. The PA–A2 and PA–A3 are not MIX–enabled. Port adapters that are MIX–enabled include PA–MCX–2TE1, PA–MCX–4TE1, PA–VXB and the PA–VXC , and the PA–MCX.

Thus, clock distribution takes place within the PA–A2 only. The highest priority active source in the PA–A2 supplies clocking to all other interfaces on the same card that require network clock synchronization services.

Related Information

- **Bellcore GR-1244-CORE – Clocks for the Synchronized Network: Common Generic Criteria**
 - **SONET & T1: Architectures for Digital Transport Networks", Black and Waters, Prentice Hall**
 - **Network Clock Select Command**
 - **More ATM Information**
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