

# Calculating ATM Cell Rates on a Circuit Emulation Virtual Circuit

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## Introduction

### Prerequisites

- Requirements
- Components Used
- Conventions

### Understand ATM Cell Format With AAL1

### Understand the Pointer Byte

### Understand Partial Fill

### Sample Scenarios of Changing the Cell Rate

- Example One: Standard Configuration with Unstructured CES
- Example Two: Structured CES without Partial Fill or CAS
- Example Three: Structured CES with Partial Fill
- Example Four: Structured CES with Partial Fill and CAS

### Related Information

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## Introduction

The **show ces circuit interface cbr** command on a Campus ATM switch displays detailed circuit information for a circuit emulation service (CES) connection on a constant bit rate (CBR) interface. Among the values displayed are the cell rate and bit rate, as shown in this sample output:

```
Switch#show ces circuit interface cbr 0/0/1 1
Circuit:Name CBR0/0/1:1, Circuit-state ADMIN_UP / Interface CBR0/0/1,
Circuit_id 1, Port-Type T1, Port-State UP
Port Clocking network-derived, aall Clocking Method CESIWF_AAL1_CLOCK_SYNC
Channel in use on this port: 1-24
Channels used by this circuit: 1-12
Cell-Rate: 2043, Bit-Rate 768000
cas OFF, cell_header 0x4100 (vci = 1040)
Configured CDV 2000 usecs, Measured CDV unavailable
De-jitter: UnderFlow unavailable, OverFlow unavailiable
ErrTolerance 8, idleCircuitdetect OFF, onHookIdleCode 0x0
state: VcActive, maxQueueDepth 42, startDequeueDepth 25
Partial Fill: 47, Structured Data Transfer 288
Active SoftVC
Src:atm addr 47.0091.8100.0000.0061.705a.cd01.4000.0c80.0034.10 vpi 0, vci 1040
Dst:atm addr 47.0091.8100.0000.0060.5c71.2001.4000.0c80.1034.10
```

The calculated cell rate varies with the number of configured timeslots for the circuit, as well as whether the partial fill and channel associated signalling (CAS) options are enabled.

This document clarifies the formula that CBR interfaces that support CES use to calculate the displayed the cell rate. This is performed by first illustrating the format of an ATM cell that uses ATM Adaptation Layer 1 (AAL1) and block sizes greater than one byte with structured CES.

# Prerequisites

## Requirements

There are no specific requirements for this document.

## Components Used

This document is not restricted to specific software and hardware versions.

## Conventions

Refer to Cisco Technical Tips Conventions for more information on document conventions.

# Understand ATM Cell Format With AAL1

CES uses the CBR service class and AAL1 to emulate a constant bit rate connection, such as T1 or E1. ITU-T Recommendation I.363.1 defines AAL1.

An ATM cell that uses AAL1 at the AAL sublayer "robs" a byte from the 48-byte payload field of the cell for an AAL1 header. This robbed byte consists of two subfields: the sequence number (SN) field and the sequence number protection (SNP) field. In turn, each subfield consists of its own subfields that provide timestamps, sequence numbers and other bits to adapt the asynchronous nature of ATM to the synchronous Layer 1. The ATM network uses these bits to help resolve problems with cell delay variation, cell misinsertion, and cell loss.

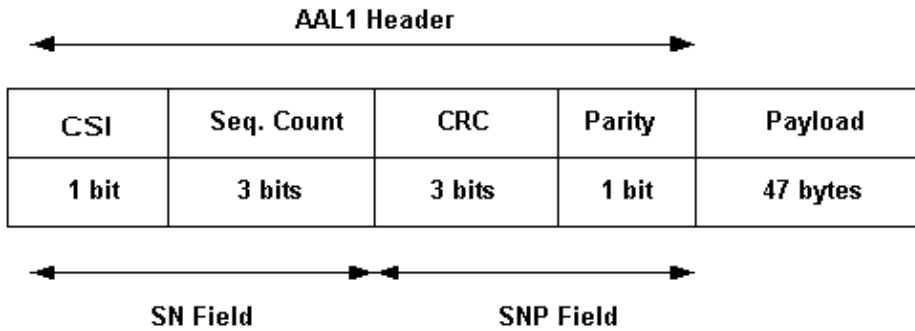
AAL1 transfers data in two modes:

- Structured Maps one or more T1 or E1 digital signal level 0 (DS-0) time slots to an ATM permanent virtual circuit (PVC). Each DS-0 time slot or channel represents a single Nx64 circuit that can transmit CBR data at a rate of 64 kbps. For example, many video codecs operate at Nx64 kbps rates. Structured mode allows you to configure each video codec to have a subset of the T1 bandwidth.
- Unstructured Maps the entire T1 or E1 bandwidth or all DS-0 time slots to an ATM PVC.

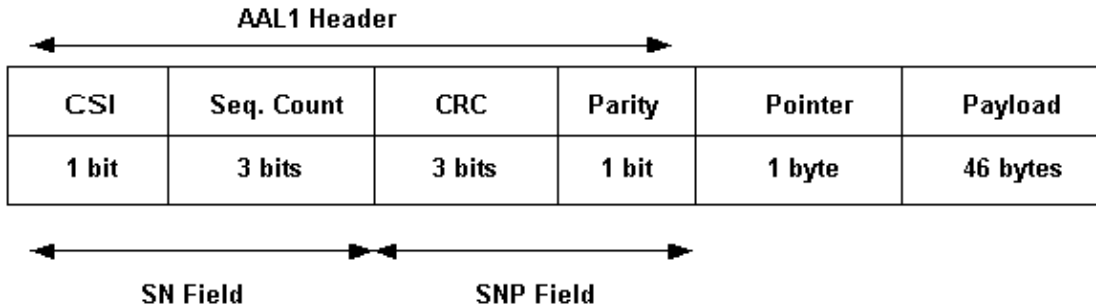
Both modes use the AAL1 header byte. In addition, structured mode also robs another byte for use as a pointer byte, which depends on the block size. This is discussed in the next section.

These diagrams illustrate the difference between unstructured and structured AAL1 cells:

## Unstructured Protocol Data Unit (PDU) Format



**Structured PDU Format**



**Note:** The pointer byte is used when the block size in the payload field is greater than one byte.

Field	Description
<b>Sequence Number Field</b>	
Convergence Sublayer Indication (CSI)	<p>Carries one of two sets of information, which depends on the PDU:</p> <ul style="list-style-type: none"> <li>Odd-numbered PDUs Conveys timing information, specifically the four bits of a synchronous residual timestamp (SRTS). Using one bit in only odd-numbered PDUs means it takes eight PDUs to convey a single time stamp. This information, together with the common ATM network clock, makes it possible to reconstruct the original clock sequence at the receiver side. If SRTS is not used, the value of this field is set to zero.</li> <li>Even-numbered PDUs Indicates whether the frame is structured or unstructured. If structured, Cisco requires an additional byte of overhead every eight cells when the block size inside the payload field is greater than one byte. This byte is known as the pointer byte.</li> </ul>

Sequence Count	Supports a modulo-8 counter to identify mis-sequenced, misinserted and missing ATM cells.
<b>Sequence Number Protection Field</b>	
cyclic redundancy check (CRC)-3	Protects important timing and sequencing information carried in the CSI and sequence count.
Parity	Provides additional protection against bit errors in the AAL1 header. Covers the first seven bits of the header, that CSI, sequence count, and CRC-3.

## Understand the Pointer Byte

Structured AAL1 uses fixed-length blocks of data. Each block consists of some number of octets to support multiple user voice channels within a virtual circuit (VC). A payload pointer is necessary in structured service since the AAL1 block is larger than one octet.

The actual layout of the Nx64 kbps data within the blocks depends on the type of signalling.

- Common channel signalling Encode Nx64 without signalling involves the collection of one octet from each timeslot and then grouping them in sequence.
- Channel associated signalling Each AAL1 block is divided into two sections. The first carries the Nx64 kbps payload, while the second carries the signalling bits. The payload part of the structure is one multiframe in length, Nx24 octets for DS-1 and Nx16 octets for E1.

Use of both the structured mode with the pointer byte and channel associated signalling affects the CES cells-per-second formula. Therefore, this affects the number of cells needed to send a certain kbps worth of traffic across the ATM PVC.

**Note:** With unstructured mode, the mapping function simply maps every bit between the AAL1 layer and the T1 or E1 CBR port.

## Understand Partial Fill

A digitized voice sample is normally one byte, although many voice codecs do use less bandwidth. Refer to Voice over IP – Per Call Bandwidth Consumption for more information. The collection of enough bytes, such as voice samples, to fill an ATM cell introduces cell payload assembly delay on the transmission end. The CES recommendation of the ATM Forum allows the source ATM interface, known as the CES interworking function (IWF), to transmit only partially filled cells and use dummy octets in the unused byte positions in order to reduce such delay.

Issue the **ces circuit {id} timeslots {slot ids} partial-fill {bytes}** command to set the number of bytes in each partially filled cell. Note that partial fill reduces delay at the expense of a higher cell rate, as seen in the example scenarios in the next section.

# Sample Scenarios of Changing the Cell Rate

Now that you understand the concepts explained in this document, this section shows how partial fill and CAS affect the cell rate in relation to the bit rate based on the number of T1 timeslots. When you read through the example scenarios, consider these points:

- Cell rates are derived by the division of the required user octet-rate by the number of user octets carried per cell. In other words, the cell rate generally is calculated with a formula that uses 47 bytes per cell, not the full 53 bytes.
- AAL1 robs a further byte from the 48-byte payload portion for an AAL1 header. See ITU-T Recommendation I.363.1 for the format of the header.
- During a cycle of every eight consecutive cells, structured CES introduces another byte for the AAL1 structure pointer if the block size is greater than one octet, which leaves 46 payload bytes per cell.
- Partial fill means that the CES IWF does not wait for the full number of one-octet voice samples, but rather sends partially-filled cells to reduce transmit delay.

**Note:** All of the formulas described in the example scenarios come directly from the CES v2 Recommendation , which you can download without charge from the ATM Forum website.

These example scenarios use an LightStream 1010 ATM switch with a four-port T1 CES port adapter module (PAM) and Cisco IOS® Software Release 12.0(16). In these formulas, PCR stands for peak cell rate and CLP stands for cell loss priority.

## Example One: Standard Configuration with Unstructured CES

T1 Formulas:

- $PCR (CLP=0+1) = 1544 \text{ kbits per second user data} = 4107 \text{ cells per second}$
- $4107 \text{ cells per second} > (1.544 \times 106 \text{ bits per second} + 130 \text{ ppm}) / (47 \text{ AAL1 octets/cell} \times 8 \text{ bits/octet})$

E1 Formulas:

- $PCR (CLP=0+1) = 2048 \text{ kbit/s user data} = 5447 \text{ cells per second}$
- $5447 \text{ cells per second} > (2.048 \times 106 \text{ bits per second} + 50 \text{ ppm}) / (47 \text{ AAL1 octets/cell} \times 8 \text{ bits/octet})$

This example shows that the CES PAM in fact uses the above formula and a cells per second rate of 4107 for the full T1.

```
ls1010-2#show ces circuit interface cbr 3/0/3 0
Circuit: Name example1, Circuit-state ADMIN_UP / oper-state UP Interface
CBR3/0/3, Circuit_id 0, Port-Type T1, Port-State UP
Port Clocking network-derived, aall Clocking Method CESIWF_AAL1_CLOCK_SYNC
Channel in use on this port: 1-24
Channels used by this circuit: 1-24
Cell-Rate: 4107, Bit-Rate 1544000
cas OFF, cell_header 0xC100 (vci = 3088)
Configured CDV 2000 usecs, Measured CDV unavailable
De-jitter: UnderFlow 240436, OverFlow 0
ErrTolerance 8, idleCircuitdetect OFF, onHookIdleCode 0x0
state: VcAlarm, maxQueueDepth 823, startDequeueDepth 435
Partial Fill: 47, Structured Data Transfer 0
HardPVC
src: CBR3/0/3 vpi 0, vci 3088
Dst: ATM2/0/0 vpi 0, vci 100
interface CBR3/0/3
```

```

no ip address
no ip directed-broadcast
ces circuit 0 circuit-name example1
ces pvc 0 interface ATM2/0/0 vpi 0 vci 100

```

**Note:** Although unstructured mode is explicitly configured, the **ces aall service structured** command does not appear in the running configuration because this mode is the default.

## Example Two: Structured CES without Partial Fill or CAS

Formula:

- $(8000 \times N) / 46.875$

N is the number of 64 kbps timeslots.

In this example, a structured CES circuit with 10 Nx64 kbps timeslots is configured. Look at the calculated cell rate:  $8000 \times 10 / 46.875 = 1707$ , which the switch further rounds up to 1708.

```

ls1010-2(config-if)#ces aall service structured
Changing to Structured deletes Unstructured circuit 0 proceed? [confirm]
ls1010-2(config-if)#ces circuit 1 timeslots 1-5,11-15 circuit-name example2
ls1010-2#show ces circuit interface cbr 3/0/3 1
Circuit: Name example2, Circuit-state ADMIN_UP / oper-state DOWN Interface
CBR3/0/3, Circuit_id 1, Port-Type T1, Port-State UP
Port Clocking network-derived, aall Clocking Method CESIWF_AAL1_CLOCK_SYNC
Channel in use on this port: 1-5,11-15
Channels used by this circuit: 1-5,11-15
Cell-Rate: 1708, Bit-Rate 640000
cas OFF, cell_header 0xC100 (vci = 3088)
Configured CDV 2000 usecs, Measured CDV unavailable
De-jitter: UnderFlow unavailable, OverFlow unavaliabile
ErrTolerance 8, idleCircuitdetect OFF, onHookIdleCode 0x0
state: VcInactive, maxQueueDepth 0, startDequeueDepth 0
Partial Fill: 47, Structured Data Transfer 10
Passive SoftVC
Src: atm addr 47.0091.8100.0000.0060.3e5a.8f01.4000.0c81.803c.10 vpi 0, vci 3088
Dst: atm addr default

```

## Example Three: Structured CES with Partial Fill

Formula:

- $(8000 \times N) / K$

K is the number of octets filled per cell, that is the partial cell value.

If you keep the same circuit as Example Two and simply change the partial fill value to 20, note that the bit rate stays the same, and the cell rate increases significantly from 1708 to 4002. The reason for this is that partial fill means the CES hardware creates a cell when it accumulates just 20 bytes of payload (typically voice samples), rather than 47 bytes.

```

ls1010-2(config-if)#ces circuit 1 timeslots 1-5,11-15 partial-fill ?
<20-47> Number of octets in each AAL1 Cell
ls1010-2(config-if)#ces circuit 1 timeslots 1-5,11-15 partial-fill 20
ls1010-2#show ces circuit interface cbr 3/0/3 1
Circuit: Name example2, Circuit-state ADMIN_UP / oper-state DOWN Interface

```

```

CBR3/0/3, Circuit_id 1, Port-Type T1, Port-State UP
Port Clocking network-derived, aall Clocking Method CESIWF_AAL1_CLOCK_SYNC
Channel in use on this port: 1-5,11-15
Channels used by this circuit: 1-5,11-15
Cell-Rate: 4002, Bit-Rate 640000
cas OFF, cell_header 0xC100 (vci = 3088)
Configured CDV 2000 usecs, Measured CDV unavailable
De-jitter: UnderFlow unavailable, OverFlow unavaliable
ErrTolerance 8, idleCircuitdetect OFF, onHookIdleCode 0x0
state: VcInactive, maxQueueDepth 0, startDequeueDepth 0
Partial Fill: 20, Structured Data Transfer 10
Passive SoftVC
Src: atm addr 47.0091.8100.0000.0060.3e5a.8f01.4000.0c81.803c.10 vpi 0, vci 3088
Dst: atm addr default

```

## Example Four: Structured CES with Partial Fill and CAS

The formula for structured CES with partial cell fill, N = even, K = the number of AAL1 user octets filled is:

- $8000 \times [N \times 49 / 48] / K$

Refer to Section 5.1 of the CES v2 Recommendation for other formulas, which includes those for E1 and J2 framing.

**Note:** Before you enable CAS, issue the **ces dsx1 signalmode robbedbit** command in order to enable so-called robbed-bit signalling to carry the ABCD signalling bits.

```

ls1010-2(config-if)#ces circuit 1 cas
CAS requires: dsx1 signalmode robbedbit on CBR3/0/3
ls1010-2(config-if)#ces dsx1 signalmode robbedbit
ls1010-2#show ces circuit interface cbr 3/0/3 1
Circuit: Name example2, Circuit-state ADMIN_UP / oper-state DOWN Interface
CBR3/0/3, Circuit_id 1, Port-Type T1, Port-State UP
Port Clocking network-derived, aall Clocking Method CESIWF_AAL1_CLOCK_SYNC
Channel in use on this port: 1-5,11-15
Channels used by this circuit: 1-5,11-15
Cell-Rate: 4096, Bit-Rate 640000
cas ON, cell_header 0xC100 (vci = 3088)
Configured CDV 2000 usecs, Measured CDV unavailable
De-jitter: UnderFlow unavailable, OverFlow unavaliable
ErrTolerance 8, idleCircuitdetect OFF, onHookIdleCode 0x0
state: VcInactive, maxQueueDepth 0, startDequeueDepth 0
Partial Fill: 20, Structured Data Transfer 245
Passive SoftVC
Src: atm addr 47.0091.8100.0000.0060.3e5a.8f01.4000.0c81.803c.10 vpi 0, vci 3088
Dst: atm addr default

```

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## Related Information

- [ATM Technology Support Pages](#)
  - [Technical Support & Documentation – Cisco Systems](#)
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