

Table of Contents

<u>When Should Scrambling Be Enabled on ATM Virtual Circuits?</u>	1
<u>Document ID: 10412</u>	1
<u>Introduction</u>	1
<u>Prerequisites</u>	2
<u>Requirements</u>	2
<u>Components Used</u>	2
<u>Conventions</u>	2
<u>Understanding Scrambling</u>	2
<u>How Do I Enable Scrambling?</u>	3
<u>Understanding the atm scrambling cell-payload Command</u>	3
<u>Understanding the atm ds3-scramble and atm e3-scramble Commands</u>	4
<u>Understanding the scrambling-payload Command</u>	4
<u>Known Issue: atm scrambling cell-payload Disabled on Reload</u>	5
<u>Scrambling on ATM Switch Routers</u>	5
<u>ATM Scrambling on Packet Over SONET Links</u>	5
<u>Does Scrambling Make ATM Links Secure?</u>	5
<u>Related Information</u>	6

When Should Scrambling Be Enabled on ATM Virtual Circuits?

Document ID: 10412

Introduction

Prerequisites

- Requirements
- Components Used
- Conventions

Understanding Scrambling

How Do I Enable Scrambling?

- Understanding the atm scrambling cell-payload Command
- Understanding the atm ds3-scramble and atm e3-scramble Commands
- Understanding the scrambling-payload Command

Known Issue: atm scrambling cell-payload Disabled on Reload

Scrambling on ATM Switch Routers

ATM Scrambling on Packet Over SONET Links

Does Scrambling Make ATM Links Secure?

Related Information

Introduction

ATM is both a layer-2 protocol and a protocol stack, similar to the way in which IP is a layer-3 protocol and a protocol stack. The ATM Reference Model table illustrates the protocol stack for ATM.

ATM Reference Model	
Higher Layers	
ATM Adaptation Layer (AAL)	Convergence Sublayer (CS) Segmentation and Reassembly (SAR) Sublayer
ATM Layer	Generic flow control (GFC) Cell header creation and verification Cell virtual path identifier (VPI) and virtual channel identifier (VCI) translation Cell multiplex and demultiplex
Physical Layers	
Transmission Convergence (TC) Sublayer	Header error control (HEC) generation and verification Cell delineation

	Cell-rate decoupling
	Transmission adaptation
Physical Medium Dependent (PMD) Sublayer	Bit timing (time recover)

Line coding for physical medium

The physical layer consists of two sublayers. The upper half of the physical layer is the TC sublayer, which implements such functions as cell scrambling and unscrambling, cell delineation, and HEC generation and verification.

The purpose of this document is to review the benefits of scrambling and the different commands used to enable scrambling on ATM interfaces, depending on the physical layer interface module (PLIM).

Prerequisites

Requirements

There are no specific requirements for this document.

Components Used

This document is not restricted to specific software and hardware versions.

The information in this document was created from the devices in a specific lab environment. All of the devices used in this document started with a cleared (default) configuration. If your network is live, make sure that you understand the potential impact of any command.

Conventions

For more information on document conventions, refer to the Cisco Technical Tips Conventions.

Understanding Scrambling

Scrambling is designed to randomize the pattern of 1s and 0s carried in ATM cells or in the physical layer frame. Randomizing the digital bits can prevent continuous, non-variable bit patterns; in other words, long strings of all 1s or all 0s. Several physical layer protocols rely on transitions between 1s and 0s to maintain clocking.

One problem symptom that can be a good candidate for scrambling is link flaps, which occur when particular files cross an ATM link. Such files may be producing such a long string of all 1s or all 0s.

If you choose to enable cell-payload scrambling, ensure that both ends of a virtual channel (VC) are configured with the same scrambling setting. Note that most ATM interfaces do not include a default scrambling statement in the configuration. For example, with the PA-A3-T3 port adapter, only a non-default setting of `cell-payload scrambling enabled` will appear in the configuration. In contrast, a scrambling statement always appears in the configuration for an NM-4T1-IMA network module.

How Do I Enable Scrambling?

Cisco IOS® Software supports three commands to enable scrambling on router ATM interfaces:

- **atm scrambling cell-payload** All other ATM interface hardware (except the PA-A1).
- **atm ds3-scramble** Digital signal level 3 (DS-3) ATM interfaces only.

Note: DS-3 interfaces now use the **atm scrambling cell-payload** command for equivalent functionality.

- **payload-scrambling** 600 and 3600 inverse multiplexing over ATM (IMA) network modules only.

The following sections discuss each of these commands in further detail.

Understanding the atm scrambling cell-payload Command

Most ATM interfaces on Cisco routers support the **atm scrambling cell-payload** command. Use the **show atm interface atm** command to confirm the scrambling settings.

```
router(config-if)# atm scrambling ?

cell-payload  SONET in cell payload scrambling mode
sts-stream    SONET in sts-stream scrambling mode

7200-1# show atm interface atm 3/0

Interface ATM3/0:
AAL enabled:  AAL5 , Maximum VCs: 4096, Current VCCs: 1
Maximum Transmit Channels: 0
Max. Datagram Size: 4528
PLIM Type: SONET - 155000Kbps, TX clocking: LINE
Cell-payload scrambling: ON
sts-stream scrambling: ON
0 input, 0 output, 0 IN fast, 0 OUT fast, 0 out drop
  Avail bw = 155000
Config. is ACTIVE
```

That output shows that the Synchronous Optical Network (SONET) interfaces support two levels of scrambling. The first level, sts-stream scrambling mode, is required by the GR-253 standard of the International Telecommunication Union Telecommunication Standardization Sector (ITU-T). It uses a $1 + x^6 + x^7$ algorithm and scrambles all but the first row of the section overhead of the SONET frame. Consider this definition of the use of sts-stream scrambling in section 5.1.3 of GR-253:

SONET optical interface signals use binary line coding and therefore must be scrambled to assure an adequate number of transitions (0s to 1s and 1s to 0s) for such purposes as line rate clock recovery at the receiver. SONET electrical interface signals use line codes that assure adequate transitions; however, they are also scrambled for consistency between the electrical and optical interfaces. The scrambler shall be reset to '1111111' on the most-significant bit of the byte following the Z0 byte in the Nth STS-1 (in other words, the byte following the last Z0 byte). The scrambler shall run continuously from that bit on throughout the remainder of the STS-N frame. Note that the framing bytes (A1 and A2), the Section Trace byte (J0), and the Section Growth (Z0) bytes are not scrambled.

The second level of scrambling, cell-payload scrambling, is optional and is defined in ITU-T I.432, section 4.5.3. It uses a polynomial of $1 + x^{43}$. Cell-payload scrambling randomizes the bits in only the payload portion of an ATM cell and leaves the 5-byte header unscrambled. Cell-payload scrambling is designed to ensure successful ATM cell delineation, which is the process of recognizing the start of each new cell.

Cisco – When Should Scrambling Be Enabled on ATM Virtual Circuits?

In summary, it is important to understand that SONET-level or sts-stream scrambling must be enabled on every SONET device. Cell-payload scrambling can be enabled or disabled with a configuration command.

Note that the Cisco IOS Software command line presents an option to disable sts-stream scrambling. Although this command is accepted, it does not actually disable this level of scrambling. CSCdu17082 will remove this command in a future release.

Understanding the atm ds3-scramble and atm e3-scramble Commands

Line-coding protocols on DS-3 and E3 interfaces can benefit from scrambling. Specifically, scrambling helps to ensure accurate clock recovery on the receiving ATM interface.

Originally, Cisco IOS Software used the **ds3-scramble** and **atm ds3-scramble** commands on DS-3 interfaces and the **atm e3-scramble** command on E3 interfaces. In Cisco IOS Software Release 12.2, these commands are hidden and when configured will appear as **atm scrambling cell-payload** in the configuration.

```
Router# show atm interface atm 2/0/0

ATM interface ATM2/0/0:
AAL enabled: AAL5, Maximum VCs: 4096, Current VCCs: 12
Max. Datagram Size:4528, MIDs/VC: 1024
PLIM Type:DS3 - 45Mbps, Framing is C-bit ADM,
DS3 lbo: short, TX clocking: LINE
Scrambling: OFF
227585 input, 227585 output, 0 IN fast, 0 OUT fast
Config. is ACTIVE
```

Understanding the scrambling-payload Command

The IMA network module for the 2600 and 3600 router series supports the **scrambling-payload** command. Cisco IOS Software Release 12.0(5)T and 12.0(5)XK introduced support for the IMA module and for this command.

By default, payload scrambling is off for T1 links and on for E1 links. The default binary 8-zero substitution (B8ZS) line coding for T1 links normally is sufficient for proper cell delineation. The scrambling setting must match the far end.

Use the **show atm interface atm** or **show controller atm** commands to view the status of scrambling on your IMA interfaces.

```
router# show controller atm 0/2

Interface ATM0/2 is administratively down
Hardware is ATM T1

!--- Output suppressed.

SAR Scheduling channels: -1 -1 -1 -1 -1 -1 -1 -1
Part of IMA group 3
Link 2 IMA Info:
  group index is 1
  Tx link id is 2, Tx link state is unusableNoGivenReason
  Rx link id is 99, Rx link state is unusableFault
  Rx link failure status is fault,
  0 tx failures, 3 rx failures
Link 2 Framer Info:
```

Cisco – When Should Scrambling Be Enabled on ATM Virtual Circuits?

```
framing is ESF, line code is B8ZS, fdl is ANSI
cable-length is long, Rcv gain is 26db and Tx gain is 0db,
clock src is line, payload-scrambling is disabled, no loopback
```

Known Issue: atm scrambling cell-payload Disabled on Reload

ATM network processor modules for the 4x00 router series use the **atm scrambling cell-payload** command to configure payload scrambling. CSCds42723 resolves a condition in which the router removes the payload scrambling command and enters a `no scrambling` statement in the running configuration upon reload.

Note: The default scrambling state on these modules is `no scrambling`.

Scrambling on ATM Switch Routers

The LS1010 and Catalyst 8500 series of ATM switches support both modes of SONET scrambling. Both modes are enabled by default on SONET interfaces.

```
ls1010# show controllers atm 12/0/3

IF Name: ATM12/0/3      Chip Base Address: A8E0E000
Port type: OC3         Port rate: 155 Mbps      Port medium: SM Fiber
Port status:Good Signal Loopback:None      Flags:8308
TX Led: Traffic Pattern RX Led: Traffic Pattern
TX clock source: network-derived
Framing mode: sts-3c
Cell payload scrambling on
Sts-stream scrambling on
```

Cell-payload scrambling is disabled by default on DS-3 interfaces and is enabled by default for E3 interfaces.

Use the **show controllers atm** command to confirm any configuration changes to these default settings.

ATM Scrambling on Packet Over SONET Links

Packet over SONET (POS) interfaces support ATM-style payload scrambling over the synchronous payload envelope (SPE) portion of a SONET frame to ensure sufficient bit-transition density. Such scrambling is off by default and is enabled with the **pos scramble-atm** command.

```
Router(config)# interface pos 3/0

Router(config-if)# pos scramble-atm
```

Note: Scrambling changes the value of the C2 byte in the path overhead. The two values are **16** for scrambling enabled and **CF** for scrambling disabled. Scrambling does not change the C2 byte when used with ATM over SONET links.

Does Scrambling Make ATM Links Secure?

Cell scrambling does not provide security. Use it to randomize the data pattern carried over a virtual connection. For secure ATM connections, consider implementing security at a higher layer or using an encryptor.

Cisco – When Should Scrambling Be Enabled on ATM Virtual Circuits?

Related Information

- [ATM \(Asynchronous Transfer Mode\) Support Pages](#)
 - [Tools and Utilities – Cisco Systems](#)
 - [Technical Support – Cisco Systems](#)
-

All contents are Copyright © 1992–2005 Cisco Systems, Inc. All rights reserved. Important Notices and Privacy Statement.

Updated: May 11, 2005

Document ID: 10412
