CHAPTER 3

Processor Switch Module

Overview

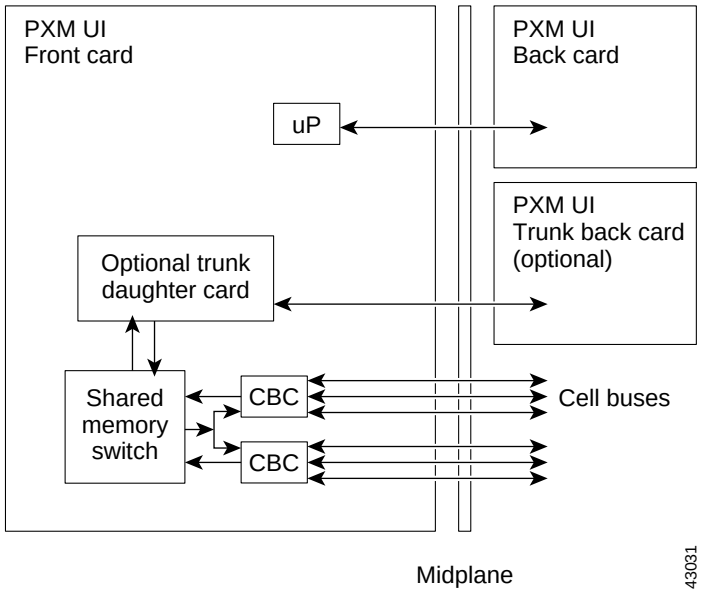
The Processor Switch Module (PXM1) provides the switching fabric in the MGX 8250 universal chassis. This PXM allows Cisco customers to scale the switch focus and capacity to 1.2 GBps (PXM1). The PXM1 combines the functions of the processor, the switch fabric, and broadband ports into a single module.

The MGX 8250 supports both shared memory and cross-point switching technologies to optimize costs for narrowband requirements. Although the backplane is always 45 GBps-capable, the customer can choose to deploy a 1.2 GBps-shared memory fabric (PXM1) to support the narrowband Service Modules. The PXM1 provides 1.2 GBps of nonblocking bandwidth.

The switch fabric (PXM1) provides up to 1.2 GBps of nonblocking ATM switching along with an integrated hard disk for statistical and management features and an ATM multicast engine.

Figure 3-1 shows the hardware architecture of the PXM1.

Figure 3-1 PXM1 Architecture



PXM1 Functions

The PXM1 performs the following functions:

- **Shelf Management**—The PXM1 is responsible for monitoring and controlling the card modules.
- **Switches Cells**—

  The PXM houses the shared-memory switch that sends and receives ATM cells from the network trunk and Service Modules.
- **Bus Master**—

  All ATM cells created by the Service Modules are sent to the PXM card to be switched to other Service Modules or the attached ATM network. The PXM is responsible for managing the flow of cells on the cell bus.
- **Network Management**—Network management devices (such as Cisco WAN Manger workstation, PC, and dumb terminals) communicate directly with the PXM.
- **Stores Service Modules Configuration and Firmware Images**—Copies of the configuration database and firmware images for each installed Service Module is stored on the PXM on a PCM-CIA disk drive.
- **Shelf Timing**—The PXM is responsible for extracting a clock signal from either an external clock source or the trunk to the ATM network. The PXM propagates the timing signals across the switch's timing bus**.**
- **Measures Environmental Alarms**—Chassis temperature and fan and power supply status are monitored by the PXM.
- **Local Alarm Notification**—Local major and minor alarms are reported by the PXM front card LEDs and by the dry contact relays on the PXM-UI back card.

Hot-Standby Redundancy

The PXM1 and all inputs (cell bus and trunk interfaces) support configuration for 1:1 hot-standby redundancy. Each PXM1 supports two active back cards.The upper level back card provides the BITS synchronization interfaces and the OAM interfaces while the lower back card provides the trunk interfaces. Both the active and redundant PXM1 are able to access either pair of the PXM back cards, which eliminates the necessity of a PXM1 switchover if either of the back cards should fail.

The midplane supports full OC-12c bandwidth to each trunk back card. The PXM1 trunk back cards also support cross-coupling between trunk interfaces for SONET APS 1+1 redundancy support.

All local connections go through QE0 and each local connection consumes two GLCNs (one for each direction). QE0 supports 32K GLCNs for a total of 16K *local* connections that can be supported in hardware.

From a hardware perspective, the PXM 1 can support up to 32K connections.

PXM1 Front Card Support

The PXM1 front cards supports the following components.

- +500MB hard drive
- High-speed SAR interface into the fabric
- Cell bus control and arbitration
- Multicast engine

PXM1 Back Card Support

PXM1 back cards provide high-speed (T3, OC-3, OC-12) native ATM interfaces that can be configured as ATM UNI ports or trunks. The interfaces are cost-optimized for trunking. Cross-coupling signals are provided between the lower back cards to allow Automatic Protection Switching (APS). The PXM1 supports two back cards.

User Interface Back Cards (Upper)

The upper User Interface cards support the followingports and interfaces.

- User and Management Interface
  - EIA/TIA-232 control port
  - EIA/TIA-232 maintenance port
  - 10BaseT Ethernet port
- Network synchronization for the shelf
  - T1/E1 BITS synchronization port
  - Stratum-4E clocking
  - Stratum-3 clocking (optional)
- Central office–compatible major/minor alarm interface
  - DB-15 connector
  - Major Alarm Audio
  - Major Alarm Visual
  - Minor Alarm Visual

PXM-UI Back Card (Standard)

The PXM-UI back card provides user access to the following interfaces:

- Ethernet port
- RS232 maintenance port
- RS232 control port
- T1/E1 timing reference ports
- Audio and visual alarm interface port

PXM-UI-S3 back card (optional)

The PXM-UI-S3 is an optional card that provides external Stratum-3 clocking. This back card provides user access to the following interfaces:

- Ethernet port
- RS232 Maintenance port
- RS232 Control port
- External T1/E1 timing reference ports
- Audio and visual alarm interface port

Trunking Back Cards (Lower)

The lower back cards on PXM1 support three types of trunking daughter cards with the following ATM interfaces:

- Two-port T3/E3
- Four-port OC-3c/STM-1
- One-port OC-12/STM-4

The PXM1 back cards provide user accessible interfaces for the uplink trunks and for management and alarm interfaces.

Uplink Back Cards (Lower)

The uplink back cards provide line drivers for the uplink interface. The following interfaces are provided:

- 2 T3 ports, BNC connectors
- 2 E3 ports, BNC connectors
- 4 OC-3 multimode port, SC connectors
- 4 OC-3 single mode intermediate reach ports, SC connectors
- 4 OC-3 single mode long reach ports, SC connectors
- 1 OC-12 single mode intermediate reach port, SC connectors
- 1 OC-12 single mode long reach port, SC connectors

Warning **A mismatch between the type of uplink back card and the PXM1 will generate a major alarm.**

Table 3-1 lists the PXM1 modules.

Table 3-2 provides the interface characteristics.

Table 3-1 Cisco MGX 8250 Processor Switch Modules

PXM1	Card
PXM1-2-T3E3	T3/E3 ports
PXM1-4-155	4 155-Mbps ports
PXM1-622	1 622-Mbps port
PXM1-UI	PXM user interface BC-PXM1
PXM-UI-S3	PXM user interface BC-Stratum-3, PXM1, PXM45
MGX-BNC-2E3	2-port E3 back card, BNC connectors
MGX-BNC-2T3	2-port T3 back card, BNC connectors
MGX-MMF-4-155	4-port 155-Mbps back card, MMF, SC connectors
MGX-SMFIR-4-155	4-port 155-Mbps back card, SMF-IR, SC connectors
MGX-SMFLR-4-155	4-port 155-Mbps back card, SMF-LR, SC connectors
MGX-SMFIR-1-622	1-port 622-Mbps back card, SMF-IR, FC connectors
MGX-SMFLR-1-622	1-port 622-Mbps back card, SMF-LR, FC connectors

Table 3-2 Interface Physical Characteristics

Characteristic	T3 (DS3)	E3 (34 Mbps)
Line Rate	44.736 Mbps, 20 ppm	34.368 Mbps, 20 ppm
Line Code	B3ZS	HDB3
Cell Transfer Rate	96,000 cells/sec	80,000 cells/sec
Framing	ANSI T1.107, T1.107a	ITU-T G.804, G.832
Signal Level	TA-TSY-00077 TA-TSY-000773 TA-TSY-000772	ITU-T-G.703
Connector	Locking	Locking
Cell Mapping	PLLP, Direct	PLLP, Direct

Bandwidth

The PXM1 provides 1.2 GBps of nonblocking bandwidth.

Cell Bus Access

The cell bus is a Poll-Request-Grant bus. The polling algorithm is based on round-robin servicing. The granting is based on a programmable rate factor for the device.

For example, if a Service Module has been guaranteed 45 Mbps of bandwidth, the priority of the device will be increased whenever the grant rate of that device falls below the guaranteed rate. This priority is increased until the minimum rate is achieved.

The eight cell buses are grouped into two groups (CB1–4, 5–8).

- Group 1 covers slots on the left side of the chassis (slots 1–6, 17–22).
- Group 2 covers the right side of the chassis (slots 9–14, 25–30).
- Excess bandwidth is proportionally shared among all devices within the same group.

When the cell buses are running at double speed, each cell bus is guaranteed 160 Mbps bandwidth. The excess bandwidth is shared proportionally among all devices within the same group. Therefore, it is important to *not* set the total guaranteed bandwidth for either the left or right side to more than 640 Mbps.

Processor (IDT 4700)

The IDT 4700 processor module provides the following basic features:

- Clock speed—200 MHz internal, 50 MHz external
- Flash— 2 MB
- DRAM—28 MB
- Secondary Cache—512 KB
- BRAM—128 KB

System Environment Monitoring

The following system environmental parameters are monitored and logged by the PXM1:

- 48 VAC power supply status
- 5V and 3.3V on-board power status
- Cooling fan revolution
- Enclosure temperature

Minor and major alarms will be generated when one or more environmental parameters are out of range.

Clocking

Clocking is provided via the PXM user interface back cards. The PXM-UI card is the standard card and provides Stratum-4 clocking. The optional PXM-UI-S3 back card also provides Stratum-3 clocking.

External References

The PXM1 supports a minimum of two external timing references on separate physical interfaces. These are provisioned as the active (*act*) and alternate (*alt*). The terms *act* and *alt* are interchangeable depending on which reference is active and providing timing reference for the system. The system also provides a DS1 reference for external timing in D4 (SF) format. At least two DS1 synchronization references, as specified in Bellcore GR-1244-CORE, Section 3.4, can be configured.

Clock Switchover

The currently selected clock source is constantly monitored by the hardware to ensure that it is within tolerance. If a failure in the selected clock is detected, the hardware gracefully switches over to the specified secondary clock source.

When both external timing references fail, the MGX 8250 can operate in self-timing, or free-running mode, using an internal clock (refer toBellcore GR-1244-CORE, Section 3.4.1).

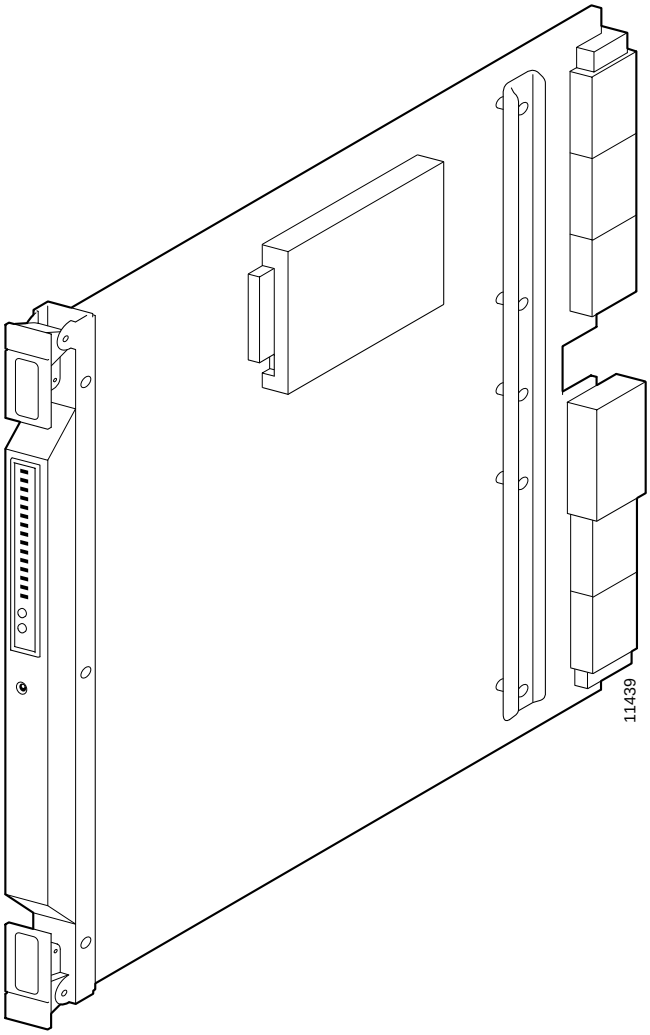
For example, if both the primary and secondary sources fail, the hardware will automatically output the internally generated clock. The system automatically switches back the primary clock once it is within tolerance.

Regardless of whether the clock switchover is initiated by the user or by the hardware, the switchover meets the Accunet T1.5 Maximum Time Interval Error (MTIE) Specification.

Alarm Circuit and Indicators (Front Card LEDs)

PXM1 provides connectors for external audio and visual alarms . The PXM1 monitors ACO and History push-buttons located in the front card faceplate. The following LED indicators are also located on the PXM1 front card faceplate as shown in Figure 3-2.

Figure 3-2 PXM1 LEDs



The front card LEDS are as follows.

- **Card**
  Active (green)
  Standby (yellow)
  Fail (red)
- **LAN activity**
  Flashing green

- **Node alarm**
  Major alarm (red)
  Minor alarm (yellow)
- **Node Power Supply**
  DC OK A (green/red)
  DC OK B (green/red)
- **Alarm History**
  ACO
  History
- **Port Interface (per port)**
  Active and OK (green)
  Active and local alarm (red)
  Active and remote alarm (yellow)
  Inactive (no light)

Storage

The PXM1 provides three types of nonvolatile storage:

- **Flash**
  Flash memory is used to store boot code for the processor. The boot code can be upgraded in the field by a software download.
- **Hard drive**
  The PXM hard drive is a 2.5 inch, 2.2 GB IDE drive. Configuration information and code for the PXM and Service Modules are stored on the drive. This information can be updated during system operation or by user download.
- **Battery backed up RAM (BRAM)**
  The BRAM is used to store bookkeeping information for the card. Stored information includes:
  - Identifiers such as board hardware revision, serial number, and PCB part number.
  - MAC address of the PXM.
  - Hard drive parameters such as number of heads and cylinder size.

  The BRAM also acts as a temporary cache. If the hard drive fails for any reason, log information created immediately before the failure can be stored in the BRAM for further analysis.

Physical Interfaces

The physical interfaces include:

- Clock Switchover.
- Optical Interfaces.
- Physical Layer T3/E3 Interface.
- Physical Layer OC-3c/STM-1 Interface.
- Physical Layer OC-12c/STM-4 Interface.
- ATM Layer.

Optical Interfaces

The optical transceivers in the PXM1 interfaces are compliant with ITU-T G.957. The dispersion tolerances according to G.957 are as follows.

- STM-1 Intermediate Reach (S-1.1)

  Maximum dispersion in the optical path is 96 ps/nm
- STM-1 Long Reach (L-1.1)

  Maximum dispersion in the optical path is 185 ps/nm
- STM-4 Intermediate Reach (S-4.1)

  Maximum dispersion in the optical path is 74 ps/nm
- STM-4 Long Reach (L-4.1)

  Maximum dispersion in the optical path is 109 ps/nm

The modulation used in all PXM1 optics is direct built-in electroabsortion modulator in standard temperature range (0 to 70°C). The types of laser sources for the different PXM1 interfaces are

- OC-3 IR: Fabry-Perot
- OC-3 LR: Fabry-Perot
- OC-12 IR: Fabry-Perot
- OC-12 LR: DFB

Physical Layer T3/E3 Interface

The T3/E3 interface provides

- Two T3/E3 ports
- Compliance with ATM Forum UNI specification versions 3.0 and 3.1
- 1:1 PXM1 redundancy
- Both PLCP and HEC direct mapping for T3; HEC direct mapping for E3

Physical Layer OC-3c/STM-1 Interface

The OC-3c/STM-1 interface provides

- Four OC-3c/STM-1 (155.520 Mbps) ports
- Trunk or port interface mode
- Cell transfer rate of 353,208 cells per second
- Compliance with SONET standards (Bellcore GR-253-CORE and ANSI T1.105)
- Compliance with SDH standards (ITU-T G.707, G.708, G.709, G.957, and G.958)
- 1:1 PXM1 redundancy
- SONET APS
- Linear APS

Physical Layer OC-12c/STM-4 Interface

The OC-12c/STM-4 interface provides:

- One OC-12c/STM-4 (622.08 Mbps) port
- Cell transfer rate of 1,412,832 cells per second
- Compliance with SONET standards (Bellcore GR-253-CORE, TR-TSY-000020, ANSI T1.105)
- Compliance with SDH standards (ITU-T G.707, G.708, G.709, G.957, G.958)
- 1:1 PXM1 redundancy
- SONET APS

ATM Layer

The ATM layer is configurable for trunk and public or private UNI applications. It is conformant to ATM Forum UNI Specification V3.0, 3.1, ITU-T I.361 and I.432 Specifications, and it supports virtual circuit connections (VCCs) and virtual path connections (VPCs) per ATM Forum UNI Specification V3.1 and ITU-T I.371.