验证在CEF的ASR9000 VQI分配

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简介

本文在聚合服务路由器9000 (ASR9K)的思科快速转发(CEF)描述如何验证虚拟队列索引(VQIs)和适当地分配他们。

背景信息

为了信息包能转发从一个接口到另一个在ASR9K，信息包必须横断结构。没有在ASR9K的本地交换。信息包如何从一个接口虽则有别的？这通过分配到每个接口的使用是实现的VQIs。这样结构知道哪个线路卡(LC)和路由信息包的网络处理器(NP)。

有时虽则，和一旦CSCvc83681 ，错误的VQI也许分配，并且数据流可以是黑洞在路由器里面。

验证VQI分配

请参见此部分为了验证VQI分配。

首先，请识别入口，并且流、来源和目的地网络协议(IP)地址的输出接口，与显示**detail命令CEF的<prefix>**。

这帮助确定哪LCs需要查看对VQI分配。

这是源地址：

```
RP/0/RSP0/CPU0:ASR9006-H#show cef 123.29.62.12 detail
Tue May  1 10:54:50.356 EDT
123.29.62.12/32, version 325561, internal 0x1000001 0x0 (ptr 0x76a07a40) [1], 0x0 (0x73ffbf50),
0xa28 (0x75e3133c)
Updated May  1 10:26:51.592
remote adjacency to TenGigE0/1/0/5
Prefix Len 32, traffic index 0, precedence n/a, priority 1
 gateway array (0x74bff484) reference count 3, flags 0x68, source lsd (5), 1 backups
               [2 type 5 flags 0x8401 (0x7216f3d0) ext 0x0 (0x0)]
 LW-LDI[type=5, refc=3, ptr=0x73ffbf50, sh-ldi=0x7216f3d0]
 gateway array update type-time 1 May  1 10:26:51.592
LDI Update time May  1 10:26:51.592
LW-LDI-TS May  1 10:26:51.592
  via 10.94.1.182/32, TenGigE0/1/0/5, 6 dependencies, weight 0, class 0 [flags 0x0]
   path-idx 0 NHID 0x0 [0x7181cfc4 0x0]
   next hop 10.94.1.182/32
   remote adjacency
    local label 24088      labels imposed {86}
```

```
  via 10.94.1.150/32, TenGigE0/1/0/7, 6 dependencies, weight 0, class 0 [flags 0x0]
   path-idx 1 NHID 0x0 [0x7181d018 0x0]
   next hop 10.94.1.150/32
   remote adjacency
    local label 24088      labels imposed {86}


   Load distribution: 0 1 (refcount 2)

   Hash  OK  Interface                 Address
   0     Y   TenGigE0/1/0/5            remote
   1     Y   TenGigE0/1/0/7            remote
```

这是目的地地址：

```
RP/0/RSP0/CPU0:ASR9006-H#show cef 123.29.62.1 detail
Tue May  1 10:53:14.531 EDT
123.29.62.1/32, version 334286, internal 0x1000001 0x0 (ptr 0x74bf1a04) [1], 0x0 (0x73ffbeb0),
0xa20 (0x75e310d4)
Updated May  1 10:53:12.459
remote adjacency to TenGigE0/0/0/2
Prefix Len 32, traffic index 0, precedence n/a, priority 1
 gateway array (0x74c025ec) reference count 27, flags 0x68, source lsd (5), 1 backups
               [19 type 4 flags 0x8401 (0x7216f390) ext 0x0 (0x0)]
 LW-LDI[type=1, refc=1, ptr=0x73ffbeb0, sh-ldi=0x7216f390]
 gateway array update type-time 1 Apr 30 17:03:05.246
LDI Update time Apr 30 17:03:05.246
LW-LDI-TS Apr 30 17:03:05.247
  via 10.94.0.10/32, TenGigE0/0/0/2, 4 dependencies, weight 0, class 0 [flags 0x0]
   path-idx 0 NHID 0x0 [0x7181ce20 0x7181d06c]
   next hop 10.94.0.10/32
   remote adjacency
    local label 24012      labels imposed {ImplNull}
  via 10.94.2.9/32, TenGigE0/0/0/3, 4 dependencies, weight 0, class 0 [flags 0x0]
   path-idx 1 NHID 0x0 [0x7181ce74 0x7181d0c0]
   next hop 10.94.2.9/32
   remote adjacency
    local label 24012      labels imposed {ImplNull}


   Load distribution: 0 1 (refcount 19)

   Hash  OK  Interface                 Address
   0     Y   TenGigE0/0/0/2            remote
   1     Y   TenGigE0/0/0/3            remote
```

从这些输出，您看到LC 1是入口LC和LC 0是出口LC，两个有两个端口为了负载平衡数据流。

其次，您需要识别多少NPs是在入口和出口LC与**show controller np端口所有位置<LC>**命令。

入口LC有8 NPs ：

```
RP/0/RSP0/CPU0:ASR9006-H#show controller np ports all loc 0/1/CPU0
Tue May  1 10:56:57.996 EDT

               Node: 0/1/CPU0:
----------------------------------------------------------------

NP Bridge Fia                      Ports
-- ------ --- -----------------------------------------------------
0  --     0   TenGigE0/1/0/0 - TenGigE0/1/0/2
```

```
1  --     0   TenGigE0/1/0/3 - TenGigE0/1/0/5
2  --     1   TenGigE0/1/0/6 - TenGigE0/1/0/8
3  --     1   TenGigE0/1/0/9 - TenGigE0/1/0/11
4  --     2   TenGigE0/1/0/12 - TenGigE0/1/0/14
5  --     2   TenGigE0/1/0/15 - TenGigE0/1/0/17
6  --     3   TenGigE0/1/0/18 - TenGigE0/1/0/20
7  --     3   TenGigE0/1/0/21 - TenGigE0/1/0/23
```

出口LC有2 NPs ：

```
RP/0/RSP0/CPU0:ASR9006-H#show controller np ports all loc 0/0/cPU0
Tue May  1 10:55:27.661 EDT

               Node: 0/0/CPU0:
----------------------------------------------------------------

NP Bridge Fia                        Ports
-- ------ --- -------------------------------------------------
0  --     0   TenGigE0/0/0/0 - TenGigE0/0/0/3
1  --     1   TenGigE0/0/1/0 - TenGigE0/0/1/3
```

其次，请用**显示CEF <destination prefix>硬件入口详细资料位置<ingress lc>**检查入口LC**|我vqi**命令和出口LC与**显示CEF <dst prefix>硬件出口选派位置<egress lc>我vqi**命令。

此信息提供我们关于每位NP如何的信息被编程到达输出接口。在这种情况下，因为有八NPs在入口LC和两条等价多重通道的(ECMP)链路在出口LC，那里是16个条目。前八个条目是为第一条ECMP链路，并且下八个条目是为第二条ECMP链路。每套八应该配比，并且意味着每位NP被编程执行同样。每集应该是不同的，虽然有两个独立接口。如果他们是相同的，则您也许击中VQI CEF错误程序设计问题。

```
RP/0/RSP0/CPU0:ASR9006-H#show cef 123.29.62.1 hardware ingress loc 0/1/CPU0 | i vqi
Tue May  1 10:56:27.064 EDT
   sfp/vqi         : 0x58
   sfp/vqi         : 0x58
   sfp/vqi         : 0x58
   sfp/vqi         : 0x58
   sfp/vqi         : 0x58
   sfp/vqi         : 0x58
   sfp/vqi         : 0x58
   sfp/vqi         : 0x58
   sfp/vqi         : 0x59
   sfp/vqi         : 0x59
   sfp/vqi         : 0x59
   sfp/vqi         : 0x59
   sfp/vqi         : 0x59
   sfp/vqi         : 0x59
   sfp/vqi         : 0x59
   sfp/vqi         : 0x59
```

检查出口LC保证适当地被编程。在这种情况下，有两NPs，并且两条ECMP链路那么那里是需要被编程的两套两VQIs。

```
RP/0/RSP0/CPU0:ASR9006-H#show cef 123.29.62.1 hardware egress loc 0/0/CPU0 | i vqi
Tue May  1 10:57:29.221 EDT
        out_lbl_invalid: 0              match: 0          vqi/lag-id: 0x0
        out_lbl_invalid: 0              match: 0          vqi/lag-id: 0x0
   sfp/vqi         : 0x58
   sfp/vqi         : 0x58
        out_lbl_invalid: 0              match: 0          vqi/lag-id: 0x0
        out_lbl_invalid: 0              match: 0          vqi/lag-id: 0x0
```

```
   sfp/vqi         : 0x59
   sfp/vqi         : 0x59
```

检查的最后事是在接口的VQI分配。

这里，您能检查可变的switch_fabric_port和从十进制转换到十六进制。88是58和89是59，这些值与从意味着的这些命令的VQI分配配比CEF为VQI传输适当地被编程在ASR9K。

```
RP/0/RSP0/CPU0:ASR9006-H#show controller pm interface ten 0/0/0/2
Tue May  1 10:58:52.024 EDT

Ifname(1): TenGigE0_0_0_2, ifh: 0x4000140 :
iftype             0x1e
egress_uidb_index  0x7, 0x7
ingress_uidb_index 0x7, 0x7
port_num           0x2
subslot_num        0x0
ifsubinst          0x0
ifsubinst port     0x2
phy_port_num       0x2
channel_id         0x0
channel_map        0x0
lag_id             0x0
virtual_port_id    0x0
switch_fabric_port 88
in_tm_qid_fid0     0x20002
in_tm_qid_fid1     0xffffffff
in_qos_drop_base   0x690001
out_tm_qid_fid0    0x20022
out_tm_qid_fid1    0xffffffff
np_port            0x6

out_qos_drop_base  0x6900a1
bandwidth          10000000 kbps
ing_stats_ptrs     0x53016a, 0x0
egr_stats_ptrs     0x53017b, 0x0
l2_transport       0x0
ac_count           0x0
parent_ifh         0x0
parent_bundle_ifh  0x0
L2 protocols bmap  0x1000000
Cluster interface  0

RP/0/RSP0/CPU0:ASR9006-H#show controller pm interface ten 0/0/0/3
Tue May  1 10:59:08.886 EDT

Ifname(1): TenGigE0_0_0_3, ifh: 0x4000180 :
iftype             0x1e
egress_uidb_index  0x8, 0x8
ingress_uidb_index 0x8, 0x8
port_num           0x3
subslot_num        0x0
ifsubinst          0x0
ifsubinst port     0x3
phy_port_num       0x3
channel_id         0x0
channel_map        0x0
lag_id             0x0
virtual_port_id    0x0
switch_fabric_port 89
in_tm_qid_fid0     0x30002
in_tm_qid_fid1     0xffffffff
```

```
in_qos_drop_base   0x6e0001
out_tm_qid_fid0    0x30022
out_tm_qid_fid1    0xffffffff
np_port            0x7

out_qos_drop_base  0x6e00a1
bandwidth          10000000 kbps
ing_stats_ptrs     0x530183, 0x0
egr_stats_ptrs     0x530194, 0x0
l2_transport       0x0
ac_count           0x0
parent_ifh         0x0
parent_bundle_ifh  0x0
L2 protocols bmap  0x1000000
Cluster interface  0
```