BIOS Parameters by Server Model

This appendix contains the following sections:

C22 and C24 Servers

Main BIOS Parameters for C22 and C24 Servers

Name	Description
TPM Support **set TPMAdminCtrl**	TPM (Trusted Platform Module) is a microchip designed to provide basic security-related functions primarily involving encryption keys. This option allows you to control the TPM Security Device support for the system. It can be one of the following: • **Disabled—**The server does not use the TPM. • **Enabled—**The server uses the TPM. **Note** We recommend that you contact your operating system vendor to make sure the operating system supports this feature.

Advanced BIOS Parameters for C22 and C24 Servers

Processor Configuration Parameters

Name	Description
Intel Hyper-Threading Technology **set IntelHyperThread**	Whether the processor uses Intel Hyper-Threading Technology, which allows multithreaded software applications to execute threads in parallel within each processor. This can be one of the following: • **Disabled—**The processor does not permit hyperthreading. • **Enabled—**The processor allows for the parallel execution of multiple threads. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Number of Enabled Cores **set CoreMultiProcessing**	Allows you to disable one or more of the physical cores on the server. This can be one of the following: • **All—**Enables all physical cores. This also enables Hyper Threading on the associated logical processor cores. • **1** through ***n*—**Specifies the number of physical processor cores that can run on the server. Each physical core has an associated logical core. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Execute Disable **set ExecuteDisable**	Classifies memory areas on the server to specify where application code can execute. As a result of this classification, the processor disables code execution if a malicious worm attempts to insert code in the buffer. This setting helps to prevent damage, worm propagation, and certain classes of malicious buffer overflow attacks. This can be one of the following: • **Disabled—**The processor does not classify memory areas. • **Enabled—**The processor classifies memory areas. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.

Name	Description
Intel VT **set IntelVT**	Whether the processor uses Intel Virtualization Technology (VT), which allows a platform to run multiple operating systems and applications in independent partitions. This can be one of the following: • **Disabled—**The processor does not permit virtualization. • **Enabled—**The processor allows multiple operating systems in independent partitions. **Note** If you change this option, you must power cycle the server before the setting takes effect.
Intel VT-d **set IntelVTD**	Whether the processor uses Intel Virtualization Technology for Directed I/O (VT-d). This can be one of the following: • **Disabled—**The processor does not use virtualization technology. • **Enabled—**The processor uses virtualization technology.
Intel VT-d Coherency Support **set CoherencySupport**	Whether the processor supports Intel VT-d Coherency. This can be one of the following: • **Disabled—**The processor does not support coherency. • **Enabled—**The processor uses VT-d Coherency as required.
Intel VT-d ATS Support **set ATS**	Whether the processor supports Intel VT-d Address Translation Services (ATS). This can be one of the following: • **Disabled—**The processor does not support ATS. • **Enabled—**The processor uses VT-d ATS as required.

Name	Description
CPU Performance **set CPUPerformance**	Sets the CPU performance profile for the server. The performance profile consists of the following options: • DCU Streamer Prefetcher • DCU IP Prefetcher • Hardware Prefetcher • Adjacent Cache-Line Prefetch This can be one of the following: • **Enterprise—**All options are enabled. • **High_Throughput—**Only the DCU IP Prefetcher is enabled. The rest of the options are disabled. • **HPC—**All options are enabled. This setting is also known as high performance computing. • **Custom—**All performance profile options can be configured from the BIOS setup on the server. In addition, the Hardware Prefetcher and Adjacent Cache-Line Prefetch options can be configured in the fields below.
Hardware Prefetcher **set HardwarePrefetch**	Whether the processor allows the Intel hardware prefetcher to fetch streams of data and instruction from memory into the unified second-level cache when necessary. This can be one of the following: • **Disabled—**The hardware prefetcher is not used. • **Enabled—**The processor uses the hardware prefetcher when cache issues are detected.
Adjacent Cache Line Prefetcher **set AdjacentCacheLinePrefetch**	Whether the processor fetches cache lines in even/odd pairs instead of fetching just the required line. This can be one of the following: • **Disabled—**The processor only fetches the required line. • **Enabled—** The processor fetches both the required line and its paired line.

Name	Description
DCU Streamer Prefetch **set DcuStreamerPrefetch**	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache. This can be one of the following: • **Disabled—**The processor does not try to anticipate cache read requirements and only fetches explicitly requested lines. • **Enabled—**The DCU prefetcher analyzes the cache read pattern and prefetches the next line in the cache if it determines that it may be needed.
DCU IP Prefetcher **set DcuIpPrefetch**	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache. This can be one of the following: • **Disabled—**The processor does not preload any cache data. • **Enabled—**The DCU IP prefetcher preloads the L1 cache with the data it determines to be the most relevant.
Direct Cache Access Support **set DirectCacheAccess**	Allows processors to increase I/O performance by placing data from I/O devices directly into the processor cache. This setting helps to reduce cache misses. This can be one of the following: • **Disabled—**Data from I/O devices is not placed directly into the processor cache. • **Enabled—**Data from I/O devices is placed directly into the processor cache.

Name	Description
Power Technology **set CPUPowerManagement**	Enables you to configure the CPU power management settings for the following options: • Enhanced Intel Speedstep Technology • Intel Turbo Boost Technology • Processor Power State C6 Power Technology can be one of the following: • **Custom—**The server uses the individual settings for the BIOS parameters mentioned above. You must select this option if you want to change any of these BIOS parameters. • **Disabled—**The server does not perform any CPU power management and any settings for the BIOS parameters mentioned above are ignored. • **Energy_Efficient—**The server determines the best settings for the BIOS parameters mentioned above and ignores the individual settings for these parameters.
Enhanced Intel Speedstep Technology **set EnhancedIntelSpeedStep**	Whether the processor uses Enhanced Intel SpeedStep Technology, which allows the system to dynamically adjust processor voltage and core frequency. This technology can result in decreased average power consumption and decreased average heat production. This can be one of the following: • **Disabled—**The processor never dynamically adjusts its voltage or frequency. • **Enabled—**The processor utilizes Enhanced Intel SpeedStep Technology and enables all supported processor sleep states to further conserve power. We recommend that you contact your operating system vendor to make sure the operating system supports this feature. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.

Name	Description
Intel Turbo Boost Technology **set IntelTurboBoostTech**	Whether the processor uses Intel Turbo Boost Technology, which allows the processor to automatically increase its frequency if it is running below power, temperature, or voltage specifications. This can be one of the following: • **Disabled—**The processor does not increase its frequency automatically. • **Enabled—**The processor utilizes Turbo Boost Technology if required. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Processor Power State C6 **set ProcessorC6Report**	Whether the BIOS sends the C6 report to the operating system. When the OS receives the report, it can transition the processor into the lower C6 power state to decrease energy usage while maintaining optimal processor performance. This can be one of the following: • **Disabled—**The BIOS does not send the C6 report. • **Enabled—**The BIOS sends the C6 report, allowing the OS to transition the processor to the C6 low power state. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Processor Power State C1 Enhanced **set ProcessorC1EReport**	Whether the CPU transitions to its minimum frequency when entering the C1 state. This can be one of the following: • **Disabled—**The CPU continues to run at its maximum frequency in C1 state. • **Enabled—**The CPU transitions to its minimum frequency. This option saves the maximum amount of power in C1 state.
Frequency Floor Override **set CpuFreqFloor**	Whether the CPU is allowed to drop below the maximum non-turbo frequency when idle. This can be one of the following: • **Disabled—** The CPU can drop below the maximum non-turbo frequency when idle. This option decreases power consumption but may reduce system performance. • **Enabled—** The CPU cannot drop below the maximum non-turbo frequency when idle. This option improves system performance but may increase power consumption.

Name	Description
P-STATE Coordination **set PsdCoordType**	Allows you to define how BIOS communicates the P-state support model to the operating system. There are 3 models as defined by the Advanced Configuration and Power Interface (ACPI) specification. • **HW_ALL—**The processor hardware is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a package). • **SW_ALL—**The OS Power Manager (OSPM) is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a physical package), and must initiate the transition on all of the logical processors. • **SW_ANY—**The OS Power Manager (OSPM) is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a package), and may initiate the transition on any of the logical processors in the domain. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Energy Performance **set CpuEngPerfBias**	Allows you to determine whether system performance or energy efficiency is more important on this server. This can be one of the following: • **Balanced_Energy** • **Balanced_Performance** • **Energy_Efficient** • **Performance**

Memory Configuration Parameters

Name	Description
Select Memory RAS **set SelectMemoryRAS**	How the memory reliability, availability, and serviceability (RAS) is configured for the server. This can be one of the following: • **Maximum_Performance—**System performance is optimized. • **Mirroring—**System reliability is optimized by using half the system memory as backup. • **Lockstep—**If the DIMM pairs in the server have an identical type, size, and organization and are populated across the SMI channels, you can enable lockstep mode to minimize memory access latency and provide better performance. This option offers better system performance than Mirroring and better reliability than Maximum Performance but lower reliability than Mirroring and lower system performance than Maximum Performance.
DRAM Clock Throttling **set DRAMClockThrottling**	Allows you to tune the system settings between the memory bandwidth and power consumption. This can be one of the following: • **Balanced—** DRAM clock throttling is reduced, providing a balance between performance and power. • **Performance—**DRAM clock throttling is disabled, providing increased memory bandwidth at the cost of additional power. • **Energy_Efficient—**DRAM clock throttling is increased to improve energy efficiency.
NUMA **set NUMAOptimize**	Whether the BIOS supports NUMA. This can be one of the following: • **Disabled—**The BIOS does not support NUMA. • **Enabled—**The BIOS includes the ACPI tables that are required for NUMA-aware operating systems. If you enable this option, the system must disable Inter-Socket Memory interleaving on some platforms.

Name	Description
Low Voltage DDR Mode **set LvDDRMode**	Whether the system prioritizes low voltage or high frequency memory operations. This can be one of the following: • **Power_Saving_Mode—**The system prioritizes low voltage memory operations over high frequency memory operations. This mode may lower memory frequency in order to keep the voltage low. • **Performance_Mode—**The system prioritizes high frequency operations over low voltage operations.
DRAM Refresh rate **set DramRefreshRate**	Allows you to set the rate at which the DRAM cells are refreshed. This can be one of the following: • **1x—**DRAM cells are refreshed every 64ms. • **2x—**DRAM cells are refreshed every 32ms. • **3x—**DRAM cells are refreshed every 21ms. • **4x—**DRAM cells are refreshed every 16ms. • **Auto—**DRAM cells refresh rate is automatically chosen by the BIOS based on the system configuration. This is the recommended setting for this parameter.
Channel Interleaving **set ChannelInterLeave**	Whether the CPU divides memory blocks and spreads contiguous portions of data across interleaved channels to enable simultaneous read operations. This can be one of the following: • **Auto—**The CPU determines what interleaving is done. • **1_Way—**Some channel interleaving is used. • **2_Way** • **3_Way** • **4_Way—**The maximum amount of channel interleaving is used.

Name	Description
Rank Interleaving **set RankInterLeave**	Whether the CPU interleaves physical ranks of memory so that one rank can be accessed while another is being refreshed. This can be one of the following: • **Auto—**The CPU determines what interleaving is done. • **1_Way—**Some rank interleaving is used. • **2_Way** • **4_Way** • **8_Way—**The maximum amount of rank interleaving is used.
Patrol Scrub **set PatrolScrub**	Whether the system actively searches for, and corrects, single bit memory errors even in unused portions of the memory on the server. This can be one of the following: • **Disabled—**The system checks for memory ECC errors only when the CPU reads or writes a memory address. • **Enabled—**The system periodically reads and writes memory searching for ECC errors. If any errors are found, the system attempts to fix them. This option may correct single bit errors before they become multi-bit errors, but it may adversely affect performance when the patrol scrub is running.
Demand Scrub **set DemandScrub**	Whether the system corrects single bit memory errors encountered when the CPU or I/O makes a demand read. This can be one of the following: • **Disabled—** Single bit memory errors are not corrected. • **Enabled—** Single bit memory errors are corrected in memory and the corrected data is set in response to the demand read.

Name	Description
Altitude **set Altitude**	The approximate number of meters above sea level at which the physical server is installed. This can be one of the following: • **Auto—**The CPU determines the physical elevation. • **300_M—**The server is approximately 300 meters above sea level. • **900_M—**The server is approximately 900 meters above sea level. • **1500_M—**The server is approximately 1500 meters above sea level. • **3000_M—**The server is approximately 3000 meters above sea level.

QPI Configuration Parameters

Name	Description
QPI Link Frequency **set QPILinkFrequency**	The Intel QuickPath Interconnect (QPI) link frequency, in gigatransfers per second (GT/s). This can be one of the following: • **Auto—**The CPU determines the QPI link frequency. • **6.4_GT/s** • **7.2_GT/s** • **8.0_GT/s**

Onboard Storage Parameters

Name	Description
Onboard SCU Storage Support **set DisableSCU**	Whether the onboard software RAID controller is available to the server. This can be one of the following: • **Disabled—**The software RAID controller is not available. • **Enabled—**The software RAID controller is available.

USB Configuration Parameters

Name	Description
Legacy USB Support **set LegacyUSBSupport**	Whether the system supports legacy USB devices. This can be one of the following: • **Disabled—**USB devices are only available to EFI applications. • **Enabled—**Legacy USB support is always available. • **Auto—**Disables legacy USB support if no USB devices are connected.
Port 60/64 Emulation **set UsbEmul6064**	Whether the system supports 60h/64h emulation for complete USB keyboard legacy support. This can be one of the following: • **Disabled—**60h/64 emulation is not supported. • **Enabled—**60h/64 emulation is supported. You should select this option if you are using a non-USB aware operating system on the server.
All USB Devices **set AllUsbDevices**	Whether all physical and virtual USB devices are enabled or disabled. This can be one of the following: • **Disabled—**All USB devices are disabled. • **Enabled—**All USB devices are enabled.
USB Port: Rear **set UsbPortRear**	Whether the rear panel USB devices are enabled or disabled. This can be one of the following: • **Disabled—**Disables the rear panel USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled—**Enables the rear panel USB ports. Devices connected to these ports are detected by the BIOS and operating system.
USB Port: Front **set UsbPortFront**	Whether the front panel USB devices are enabled or disabled. This can be one of the following: • **Disabled—**Disables the front panel USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled—**Enables the front panel USB ports. Devices connected to these ports are detected by the BIOS and operating system.

Name	Description
USB Port: Internal **set UsbPortInt**	Whether the internal USB devices are enabled or disabled. This can be one of the following: • **Disabled—**Disables the internal USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled—**Enables the internal USB ports. Devices connected to these ports are detected by the BIOS and operating system.
USB Port: KVM **set UsbPortKVM**	Whether the KVM ports are enabled or disabled. This can be one of the following: • **Disabled—**Disables the KVM keyboard and/or mouse devices. Keyboard and/or mouse will not work in the KVM window. • **Enabled—**Enables the KVM keyboard and/or mouse devices.
USB Port: VMedia **set UsbPortVMedia**	Whether the virtual media devices are enabled or disabled. This can be one of the following: • **Disabled—**Disables the vMedia devices. • **Enabled—**Enables the vMedia devices.

PCI Configuration Parameters

Name	Description
MMIO Above 4GB **set MemoryMappedIOAbove4GB**	Whether to enable or disable memory mapped I/O of 64-bit PCI devices to 4GB or greater address space. Legacy option ROMs are not able to access addresses above 4GB. PCI devices that are 64-bit compliant but use a legacy option ROM may not function correctly with this setting enabled. This can be one of the following: • **Disabled—**The server does not map I/O of 64-bit PCI devices to 4GB or greater address space. • **Enabled—**The server maps I/O of 64-bit PCI devices to 4GB or greater address space.
ASPM Support **set ASPMSupport**	Allows you to set the level of ASPM (Active Power State Management) support in the BIOS. This can be one of the following: • **Disabled—**ASPM support is disabled in the BIOS. • **Force L0s—**Force all links to L0 standby (L0s) state. • **Auto—**The CPU determines the power state.

Name	Description
VGA Priority **set VgaPriority**	Allows you to set the priority for VGA graphics devices if multiple VGA devices are found in the system. This can be one of the following: • **Onboard—**Priority is given to the onboard VGA device. BIOS post screen and OS boot are driven through the onboard VGA port. • **Offboard—**Priority is given to the PCIE Graphics adapter. BIOS post screen and OS boot are driven through the external graphics adapter port. • **Onboard_VGA_Disabled—**Priority is given to the PCIE Graphics adapter, and the onboard VGA device is disabled. **Note** The vKVM does not function when the onboard VGA is disabled.

Serial Configuration Parameters

Name	Description
Console Redirection **set ConsoleRedir**	Allows a serial port to be used for console redirection during POST and BIOS booting. After the BIOS has booted and the operating system is responsible for the server, console redirection is irrelevant and has no effect. This can be one of the following: • **Disabled—**No console redirection occurs during POST. • **Enabled—**Enables console redirection on serial port A during POST.
Terminal Type **set TerminalType**	What type of character formatting is used for console redirection. This can be one of the following: • **PC-ANSI—**The PC-ANSI terminal font is used. • **VT100—**A supported vt100 video terminal and its character set are used. • **VT100+—**A supported vt100-plus video terminal and its character set are used. • **VT-UTF8—**A video terminal with the UTF-8 character set is used. **Note** This setting must match the setting on the remote terminal application.

Name	Description
Bits per second **set BaudRate**	What BAUD rate is used for the serial port transmission speed. If you disable Console Redirection, this option is not available. This can be one of the following: • **9600—**A 9,600 BAUD rate is used. • **19200—**A 19,200 BAUD rate is used. • **38400—**A 38,400 BAUD rate is used. • **57600—**A 57,600 BAUD rate is used. • **115200—**A 115,200 BAUD rate is used. **Note** This setting must match the setting on the remote terminal application.
Flow Control **set FlowCtrl**	Whether a handshake protocol is used for flow control. Request to Send / Clear to Send (RTS/CTS) helps to reduce frame collisions that can be introduced by a hidden terminal problem. This can be one of the following: • **None—**No flow control is used. • **Hardware_RTS/CTS—**RTS/CTS is used for flow control. **Note** This setting must match the setting on the remote terminal application.
Putty KeyPad **set PuttyFunctionKeyPad**	Allows you to change the action of the PuTTY function keys and the top row of the numeric keypad. This can be one of the following: • **VT100—**The function keys generate ESC OP through ESC O[. • **LINUX—**Mimics the Linux virtual console. Function keys F6 to F12 behave like the default mode, but F1 to F5 generate ESC [[A through ESC [[E. • **XTERMR6—**Function keys F5 to F12 behave like the default mode. Function keys F1 to F4 generate **ESC OP** through ESC OS, which are the sequences produced by the top row of the keypad on Digital terminals. • **SCO—**The function keys F1 to F12 generate ESC [M through ESC [X. The function and shift keys generate ESC [Y through ESC [j. The control and function keys generate ESC [k through ESC [v. The shift, control and function keys generate ESC [w through ESC [{. • **ESCN—**The default mode. The function keys match the general behavior of Digital terminals. The function keys generate sequences such as ESC [11~ and ESC [12~. • **VT400—**The function keys behave like the default mode. The top row of the numeric keypad generates ESC OP through ESC OS.

Name	Description
Redirection After BIOS POST **set RedirectionAfterPOST**	Whether BIOS console redirection should be active after BIOS POST is complete and control given to the OS bootloader. This can be one of the following: • **Always_Enable—**BIOS Legacy console redirection is active during the OS boot and run time. • **Bootloader—**BIOS Legacy console redirection is disabled before giving control to the OS boot loader.
Out-of-Band Mgmt Port **set comSpcrEnable**	Allows you to configure the COM port 0 that can be used for Windows Emergency Management services. ACPI SPCR table is reported based on this setup option. This can be one of the following: • **Disabled—**Configures the COM port 0 as a general purpose port for use with the Windows Operating System. • **Enabled—**Configures the COM port 0 as a remote management port for Windows Emergency Management services.

LOM and PCIe Slots Configuration Parameters

Name	Description
All Onboard LOM Ports **set AllLomPortControl**	Whether all LOM ports are enabled or disabled. This can be one of the following: • **Disabled—**All LOM ports are disabled. • **Enabled—**All LOM ports are enabled.
LOM Port *n* OptionROM **set LomOpromControlPort*n***	Whether Option ROM is available on the LOM port designated by ***n***. This can be one of the following: • **Disabled—**Option ROM is not available on LOM port ***n***. • **Enabled—**Option ROM is available on LOM port ***n***. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.

Name	Description
All PCIe Slots OptionROM **set PcieOptionROMs**	Whether the server can use the PCIe Option ROM expansion slots. This can be one of the following: • **Disabled—**PCIe Option ROMs are not available. • **Enabled—**PCIe Option ROMs are available. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.
PCIe Slot:*n* OptionROM **set Slot-*n*-ROM**	Whether PCIe expansion slot ***n*** is available to the server. This can be one of the following: • **Disabled—**The expansion slot ***n*** is not available. • **Enabled—**The expansion slot ***n*** is available. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.
PCIe Slot:*n* Link Speed **PCIe Slot:*n*LinkSpeed**	This option allows you to restrict the maximum speed of an adapter card installed in PCIe slot ***n***. This can be one of the following: • **GEN1—**2.5GT/s (gigatransfers per second) is the maximum speed allowed. • **GEN2—**5GT/s is the maximum speed allowed. • **GEN3—**8GT/s is the maximum speed allowed. • **Disabled—**The maximum speed is not restricted. For example, if you have a 3rd generation adapter card in PCIe slot 2 that you want to run at a maximum of 5GT/s instead of the 8GT/s that card supports, set the PCIe Slot 2 Link Speed to **GEN2**. The system then ignores the card's supported maximum speed of 8GT/s and forces it to run at a maximum of 5 GT/s.

Server Management BIOS Parameters for C22 and C24 Servers

Name	Description
FRB-2 Timer **set FRB-2**	Whether the FRB2 timer is used by CIMC to recover the system if it hangs during POST. This can be one of the following: • **Disabled—**The FRB2 timer is not used. • **Enabled—**The FRB2 timer is started during POST and used to recover the system if necessary.

Name	Description
OS Watchdog Timer **set OSBootWatchdogTimer**	Whether the BIOS programs the watchdog timer with a specified timeout value. This can be one of the following: • **Disabled—**The watchdog timer is not used to track how long the server takes to boot. • **Enabled—**The watchdog timer tracks how long the server takes to boot. If the server does not boot within the length of time specified by the **set OSBootWatchdogTimerTimeout** command, the CIMC logs an error and takes the action specified by the **set OSBootWatchdogTimerPolicy** command.
OS Watchdog Timer Timeout **set OSBootWatchdogTimerTimeOut**	What timeout value the BIOS uses to configure the watchdog timer. This can be one of the following: • **5_Minutes—**The watchdog timer expires 5 minutes after the OS begins to boot. • **10_Minutes—**The watchdog timer expires 10 minutes after the OS begins to boot. • **15_Minutes—**The watchdog timer expires 15 minutes after the OS begins to boot. • **20_Minutes—**The watchdog timer expires 20 minutes after the OS begins to boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.
OS Watchdog Timer Policy **set OSBootWatchdogTimerPolicy**	What action the system takes if the watchdog timer expires. This can be one of the following: • **Do_Nothing—**The server takes no action if the watchdog timer expires during OS boot. • **Power_Down—**The server is powered off if the watchdog timer expires during OS boot. • **Reset—**The server is reset if the watchdog timer expires during OS boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.

Name	Description
Boot Order Rules **set ManagedBootRule**	How the server changes the boot order list defined through the CIMC GUI or CLI when there are no devices of a particular device type available or when the user defines a different boot order using the server's BIOS Setup Utility. The supported device types are: • **HDD—**Hard disk drive • **FDD—**Floppy disk drive • **CDROM—**Bootable CD-ROM or DVD • **PXE—**PXE boot • **EFI—**Extensible Firmware Interface The Boot Order Rules option can be one of the following: • **Strict—**When no devices of a particular type are available, the system creates a placeholder for that device type in the boot order list. When a device of that type becomes available, it is added to the boot order in the previously defined position. If the user defines a boot order through the server's BIOS Setup Utility, that boot order is given priority over the boot order configured through the CIMC GUI or CLI. All device types defined through CIMC that are not present in the boot order defined through the BIOS Setup Utility are removed from the boot order list. • **Loose—**When no devices of a particular type are available, the system removes that device type from the boot order. When a device of that type becomes available, the system adds it to the end of the boot order list. If the boot order is configured through the server's BIOS Setup Utility, that boot order is given priority over the boot order configured through the CIMC GUI or CLI. All device types defined through CIMC that are not present in the boot order defined through the BIOS Setup Utility are moved to the end of the boot order list.

C220 and C240 Servers

Main BIOS Parameters for C220 and C240 Servers

Name	Description
TPM Support **set TPMAdminCtrl**	TPM (Trusted Platform Module) is a microchip designed to provide basic security-related functions primarily involving encryption keys. This option allows you to control the TPM Security Device support for the system. It can be one of the following: • **Disabled—**The server does not use the TPM. • **Enabled—**The server uses the TPM. **Note** We recommend that you contact your operating system vendor to make sure the operating system supports this feature.

Advanced BIOS Parameters for C220 and C240 Servers

Processor Configuration Parameters

Name	Description
Intel Hyper-Threading Technology **set IntelHyperThread**	Whether the processor uses Intel Hyper-Threading Technology, which allows multithreaded software applications to execute threads in parallel within each processor. This can be one of the following: • **Disabled—**The processor does not permit hyperthreading. • **Enabled—**The processor allows for the parallel execution of multiple threads. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.

Name	Description
Number of Enabled Cores **set CoreMultiProcessing**	Allows you to disable one or more of the physical cores on the server. This can be one of the following: • **All—**Enables all physical cores. This also enables Hyper Threading on the associated logical processor cores. • **1** through ***n*—**Specifies the number of physical processor cores that can run on the server. Each physical core has an associated logical core. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Execute Disable **set ExecuteDisable**	Classifies memory areas on the server to specify where application code can execute. As a result of this classification, the processor disables code execution if a malicious worm attempts to insert code in the buffer. This setting helps to prevent damage, worm propagation, and certain classes of malicious buffer overflow attacks. This can be one of the following: • **Disabled—**The processor does not classify memory areas. • **Enabled—**The processor classifies memory areas. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Intel VT **set IntelVT**	Whether the processor uses Intel Virtualization Technology (VT), which allows a platform to run multiple operating systems and applications in independent partitions. This can be one of the following: • **Disabled—**The processor does not permit virtualization. • **Enabled—**The processor allows multiple operating systems in independent partitions. **Note** If you change this option, you must power cycle the server before the setting takes effect.
Intel VT-d **set IntelVTD**	Whether the processor uses Intel Virtualization Technology for Directed I/O (VT-d). This can be one of the following: • **Disabled—**The processor does not use virtualization technology. • **Enabled—**The processor uses virtualization technology.

Name	Description
Intel VT-d Coherency Support **set CoherencySupport**	Whether the processor supports Intel VT-d Coherency. This can be one of the following: • **Disabled—**The processor does not support coherency. • **Enabled—**The processor uses VT-d Coherency as required.
Intel VT-d ATS Support **set ATS**	Whether the processor supports Intel VT-d Address Translation Services (ATS). This can be one of the following: • **Disabled—**The processor does not support ATS. • **Enabled—**The processor uses VT-d ATS as required.
CPU Performance **set CPUPerformance**	Sets the CPU performance profile for the server. The performance profile consists of the following options: • DCU Streamer Prefetcher • DCU IP Prefetcher • Hardware Prefetcher • Adjacent Cache-Line Prefetch This can be one of the following: • **Enterprise—**All options are enabled. • **High_Throughput—**Only the DCU IP Prefetcher is enabled. The rest of the options are disabled. • **HPC—**All options are enabled. This setting is also known as high performance computing. • **Custom—**All performance profile options can be configured from the BIOS setup on the server. In addition, the Hardware Prefetcher and Adjacent Cache-Line Prefetch options can be configured in the fields below.
Hardware Prefetcher **set HardwarePrefetch**	Whether the processor allows the Intel hardware prefetcher to fetch streams of data and instruction from memory into the unified second-level cache when necessary. This can be one of the following: • **Disabled—**The hardware prefetcher is not used. • **Enabled—**The processor uses the hardware prefetcher when cache issues are detected.

Name	Description
Adjacent Cache Line Prefetcher **set AdjacentCacheLinePrefetch**	Whether the processor fetches cache lines in even/odd pairs instead of fetching just the required line. This can be one of the following: • **Disabled—**The processor only fetches the required line. • **Enabled—** The processor fetches both the required line and its paired line.
DCU Streamer Prefetch **set DcuStreamerPrefetch**	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache. This can be one of the following: • **Disabled—**The processor does not try to anticipate cache read requirements and only fetches explicitly requested lines. • **Enabled—**The DCU prefetcher analyzes the cache read pattern and prefetches the next line in the cache if it determines that it may be needed.
DCU IP Prefetcher **set DcuIpPrefetch**	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache. This can be one of the following: • **Disabled—**The processor does not preload any cache data. • **Enabled—**The DCU IP prefetcher preloads the L1 cache with the data it determines to be the most relevant.
Direct Cache Access Support **set DirectCacheAccess**	Allows processors to increase I/O performance by placing data from I/O devices directly into the processor cache. This setting helps to reduce cache misses. This can be one of the following: • **Disabled—**Data from I/O devices is not placed directly into the processor cache. • **Enabled—**Data from I/O devices is placed directly into the processor cache.

Name	Description
Power Technology **set CPUPowerManagement**	Enables you to configure the CPU power management settings for the following options: • Enhanced Intel Speedstep Technology • Intel Turbo Boost Technology • Processor Power State C6 Power Technology can be one of the following: • **Custom—**The server uses the individual settings for the BIOS parameters mentioned above. You must select this option if you want to change any of these BIOS parameters. • **Disabled—**The server does not perform any CPU power management and any settings for the BIOS parameters mentioned above are ignored. • **Energy_Efficient—**The server determines the best settings for the BIOS parameters mentioned above and ignores the individual settings for these parameters.
Enhanced Intel Speedstep Technology **set EnhancedIntelSpeedStep**	Whether the processor uses Enhanced Intel SpeedStep Technology, which allows the system to dynamically adjust processor voltage and core frequency. This technology can result in decreased average power consumption and decreased average heat production. This can be one of the following: • **Disabled—**The processor never dynamically adjusts its voltage or frequency. • **Enabled—**The processor utilizes Enhanced Intel SpeedStep Technology and enables all supported processor sleep states to further conserve power. We recommend that you contact your operating system vendor to make sure the operating system supports this feature. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.

Name	Description
Intel Turbo Boost Technology **set IntelTurboBoostTech**	Whether the processor uses Intel Turbo Boost Technology, which allows the processor to automatically increase its frequency if it is running below power, temperature, or voltage specifications. This can be one of the following: • **Disabled—**The processor does not increase its frequency automatically. • **Enabled—**The processor utilizes Turbo Boost Technology if required. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Processor Power State C6 **set ProcessorC6Report**	Whether the BIOS sends the C6 report to the operating system. When the OS receives the report, it can transition the processor into the lower C6 power state to decrease energy usage while maintaining optimal processor performance. This can be one of the following: • **Disabled—**The BIOS does not send the C6 report. • **Enabled—**The BIOS sends the C6 report, allowing the OS to transition the processor to the C6 low power state. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Processor Power State C1 Enhanced **set ProcessorC1EReport**	Whether the CPU transitions to its minimum frequency when entering the C1 state. This can be one of the following: • **Disabled—**The CPU continues to run at its maximum frequency in C1 state. • **Enabled—**The CPU transitions to its minimum frequency. This option saves the maximum amount of power in C1 state.
Frequency Floor Override **set CpuFreqFloor**	Whether the CPU is allowed to drop below the maximum non-turbo frequency when idle. This can be one of the following: • **Disabled—** The CPU can drop below the maximum non-turbo frequency when idle. This option decreases power consumption but may reduce system performance. • **Enabled—** The CPU cannot drop below the maximum non-turbo frequency when idle. This option improves system performance but may increase power consumption.

Name	Description
P-STATE Coordination **set PsdCoordType**	Allows you to define how BIOS communicates the P-state support model to the operating system. There are 3 models as defined by the Advanced Configuration and Power Interface (ACPI) specification. • **HW_ALL—**The processor hardware is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a package). • **SW_ALL—**The OS Power Manager (OSPM) is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a physical package), and must initiate the transition on all of the logical processors. • **SW_ANY—**The OS Power Manager (OSPM) is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a package), and may initiate the transition on any of the logical processors in the domain. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Energy Performance **set CpuEngPerfBias**	Allows you to determine whether system performance or energy efficiency is more important on this server. This can be one of the following: • **Balanced_Energy** • **Balanced_Performance** • **Energy_Efficient** • **Performance**

Memory Configuration Parameters

Name	Description
Select Memory RAS **set SelectMemoryRAS**	How the memory reliability, availability, and serviceability (RAS) is configured for the server. This can be one of the following: • **Maximum_Performance—**System performance is optimized. • **Mirroring—**System reliability is optimized by using half the system memory as backup. • **Lockstep—**If the DIMM pairs in the server have an identical type, size, and organization and are populated across the SMI channels, you can enable lockstep mode to minimize memory access latency and provide better performance. This option offers better system performance than Mirroring and better reliability than Maximum Performance but lower reliability than Mirroring and lower system performance than Maximum Performance.
DRAM Clock Throttling **set DRAMClockThrottling**	Allows you to tune the system settings between the memory bandwidth and power consumption. This can be one of the following: • **Balanced—** DRAM clock throttling is reduced, providing a balance between performance and power. • **Performance—**DRAM clock throttling is disabled, providing increased memory bandwidth at the cost of additional power. • **Energy_Efficient—**DRAM clock throttling is increased to improve energy efficiency.
NUMA **set NUMAOptimize**	Whether the BIOS supports NUMA. This can be one of the following: • **Disabled—**The BIOS does not support NUMA. • **Enabled—**The BIOS includes the ACPI tables that are required for NUMA-aware operating systems. If you enable this option, the system must disable Inter-Socket Memory interleaving on some platforms.

Name	Description
Low Voltage DDR Mode **set LvDDRMode**	Whether the system prioritizes low voltage or high frequency memory operations. This can be one of the following: • **Power_Saving_Mode—**The system prioritizes low voltage memory operations over high frequency memory operations. This mode may lower memory frequency in order to keep the voltage low. • **Performance_Mode—**The system prioritizes high frequency operations over low voltage operations.
DRAM Refresh rate **set DramRefreshRate**	Allows you to set the rate at which the DRAM cells are refreshed. This can be one of the following: • **1x—**DRAM cells are refreshed every 64ms. • **2x—**DRAM cells are refreshed every 32ms. • **3x—**DRAM cells are refreshed every 21ms. • **4x—**DRAM cells are refreshed every 16ms. • **Auto—**DRAM cells refresh rate is automatically chosen by the BIOS based on the system configuration. This is the recommended setting for this parameter.
Channel Interleaving **set ChannelInterLeave**	Whether the CPU divides memory blocks and spreads contiguous portions of data across interleaved channels to enable simultaneous read operations. This can be one of the following: • **Auto—**The CPU determines what interleaving is done. • **1_Way—**Some channel interleaving is used. • **2_Way** • **3_Way** • **4_Way—**The maximum amount of channel interleaving is used.

Name	Description
Rank Interleaving **set RankInterLeave**	Whether the CPU interleaves physical ranks of memory so that one rank can be accessed while another is being refreshed. This can be one of the following: • **Auto—**The CPU determines what interleaving is done. • **1_Way—**Some rank interleaving is used. • **2_Way** • **4_Way** • **8_Way—**The maximum amount of rank interleaving is used.
Patrol Scrub **set PatrolScrub**	Whether the system actively searches for, and corrects, single bit memory errors even in unused portions of the memory on the server. This can be one of the following: • **Disabled—**The system checks for memory ECC errors only when the CPU reads or writes a memory address. • **Enabled—**The system periodically reads and writes memory searching for ECC errors. If any errors are found, the system attempts to fix them. This option may correct single bit errors before they become multi-bit errors, but it may adversely affect performance when the patrol scrub is running.
Demand Scrub **set DemandScrub**	Whether the system corrects single bit memory errors encountered when the CPU or I/O makes a demand read. This can be one of the following: • **Disabled—** Single bit memory errors are not corrected. • **Enabled—** Single bit memory errors are corrected in memory and the corrected data is set in response to the demand read.

Name	Description
Altitude **set Altitude**	The approximate number of meters above sea level at which the physical server is installed. This can be one of the following: • **Auto—**The CPU determines the physical elevation. • **300_M—**The server is approximately 300 meters above sea level. • **900_M—**The server is approximately 900 meters above sea level. • **1500_M—**The server is approximately 1500 meters above sea level. • **3000_M—**The server is approximately 3000 meters above sea level.

QPI Configuration Parameters

Name	Description
QPI Link Frequency **set QPILinkFrequency**	The Intel QuickPath Interconnect (QPI) link frequency, in gigatransfers per second (GT/s). This can be one of the following: • **Auto—**The CPU determines the QPI link frequency. • **6.4_GT/s** • **7.2_GT/s** • **8.0_GT/s**

Onboard Storage Parameters

Name	Description
Onboard SCU Storage Support **set DisableSCU**	Whether the onboard software RAID controller is available to the server. This can be one of the following: • **Disabled—**The software RAID controller is not available. • **Enabled—**The software RAID controller is available.

Name	Description
Onboard SCU Storage SW Stack **set PchScuOromSelect**	Allows you to choose a pre-boot software stack for an onboard SCU storage controller. This can be one of the following: • **Intel RSTe(1)** • **LSI SW RAID (0)** **Note** This configuration parameter is valid only for the C220 servers.

USB Configuration Parameters

Name	Description
Legacy USB Support **set LegacyUSBSupport**	Whether the system supports legacy USB devices. This can be one of the following: • **Disabled—**USB devices are only available to EFI applications. • **Enabled—**Legacy USB support is always available. • **Auto—**Disables legacy USB support if no USB devices are connected.
Port 60/64 Emulation **set UsbEmul6064**	Whether the system supports 60h/64h emulation for complete USB keyboard legacy support. This can be one of the following: • **Disabled—**60h/64 emulation is not supported. • **Enabled—**60h/64 emulation is supported. You should select this option if you are using a non-USB aware operating system on the server.
All USB Devices **set AllUsbDevices**	Whether all physical and virtual USB devices are enabled or disabled. This can be one of the following: • **Disabled—**All USB devices are disabled. • **Enabled—**All USB devices are enabled.
USB Port: Rear **set UsbPortRear**	Whether the rear panel USB devices are enabled or disabled. This can be one of the following: • **Disabled—**Disables the rear panel USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled—**Enables the rear panel USB ports. Devices connected to these ports are detected by the BIOS and operating system.

Name	Description
USB Port: Front **set UsbPortFront**	Whether the front panel USB devices are enabled or disabled. This can be one of the following: • **Disabled—**Disables the front panel USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled—**Enables the front panel USB ports. Devices connected to these ports are detected by the BIOS and operating system.
USB Port: Internal **set UsbPortInt**	Whether the internal USB devices are enabled or disabled. This can be one of the following: • **Disabled—**Disables the internal USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled—**Enables the internal USB ports. Devices connected to these ports are detected by the BIOS and operating system.
USB Port: KVM **set UsbPortKVM**	Whether the KVM ports are enabled or disabled. This can be one of the following: • **Disabled—**Disables the KVM keyboard and/or mouse devices. Keyboard and/or mouse will not work in the KVM window. • **Enabled—**Enables the KVM keyboard and/or mouse devices.
USB Port: VMedia **set UsbPortVMedia**	Whether the virtual media devices are enabled or disabled. This can be one of the following: • **Disabled—**Disables the vMedia devices. • **Enabled—**Enables the vMedia devices.
USB Port: SD Card **set UsbPortSdCard**	Whether the SD card drives are enabled or disabled. This can be one of the following: • **Disabled—**Disables the SD card drives. The SD card drives are not detected by the BIOS and operating system. • **Enabled—**Enables the SD card drives.

PCI Configuration Parameters

Name	Description
Memory Mapped I/O Above 4GB **set MemoryMappedIOAbove4GB**	Whether to enable or disable memory mapped I/O of 64-bit PCI devices to 4GB or greater address space. Legacy option ROMs are not able to access addresses above 4GB. PCI devices that are 64-bit compliant but use a legacy option ROM may not function correctly with this setting enabled. This can be one of the following: • **Disabled—**The server does not map I/O of 64-bit PCI devices to 4GB or greater address space. • **Enabled—**The server maps I/O of 64-bit PCI devices to 4GB or greater address space.
ASPM Support **set ASPMSupport**	Allows you to set the level of ASPM (Active Power State Management) support in the BIOS. This can be one of the following: • **Disabled—**ASPM support is disabled in the BIOS. • **Force L0s—**Force all links to L0 standby (L0s) state. • **Auto—**The CPU determines the power state.
VGA Priority **set VgaPriority**	Allows you to set the priority for VGA graphics devices if multiple VGA devices are found in the system. This can be one of the following: • **Onboard—**Priority is given to the onboard VGA device. BIOS post screen and OS boot are driven through the onboard VGA port. • **Offboard—**Priority is given to the PCIE Graphics adapter. BIOS post screen and OS boot are driven through the external graphics adapter port. • **Onboard_VGA_Disabled—**Priority is given to the PCIE Graphics adapter, and the onboard VGA device is disabled. **Note** The vKVM does not function when the onboard VGA is disabled.

Serial Configuration Parameters

Name	Description
Console Redirection **set ConsoleRedir**	Allows a serial port to be used for console redirection during POST and BIOS booting. After the BIOS has booted and the operating system is responsible for the server, console redirection is irrelevant and has no effect. This can be one of the following: • **Disabled—**No console redirection occurs during POST. • **COM_0—**Enables console redirection on COM port 0 during POST. • **COM_1—**Enables console redirection on COM port 1 during POST.
Terminal Type **set TerminalType**	What type of character formatting is used for console redirection. This can be one of the following: • **PC-ANSI—**The PC-ANSI terminal font is used. • **VT100—**A supported vt100 video terminal and its character set are used. • **VT100+—**A supported vt100-plus video terminal and its character set are used. • **VT-UTF8—**A video terminal with the UTF-8 character set is used. **Note** This setting must match the setting on the remote terminal application.
Bits per second **set BaudRate**	What BAUD rate is used for the serial port transmission speed. If you disable Console Redirection, this option is not available. This can be one of the following: • **9600—**A 9,600 BAUD rate is used. • **19200—**A 19,200 BAUD rate is used. • **38400—**A 38,400 BAUD rate is used. • **57600—**A 57,600 BAUD rate is used. • **115200—**A 115,200 BAUD rate is used. **Note** This setting must match the setting on the remote terminal application.

Name	Description
Flow Control **set FlowCtrl**	Whether a handshake protocol is used for flow control. Request to Send / Clear to Send (RTS/CTS) helps to reduce frame collisions that can be introduced by a hidden terminal problem. This can be one of the following: • **None—**No flow control is used. • **Hardware_RTS/CTS—**RTS/CTS is used for flow control. **Note** This setting must match the setting on the remote terminal application.
Putty KeyPad **set PuttyFunctionKeyPad**	Allows you to change the action of the PuTTY function keys and the top row of the numeric keypad. This can be one of the following: • **VT100—**The function keys generate ESC OP through ESC O[. • **LINUX—**Mimics the Linux virtual console. Function keys F6 to F12 behave like the default mode, but F1 to F5 generate ESC [[A through ESC [[E. • **XTERMR6—**Function keys F5 to F12 behave like the default mode. Function keys F1 to F4 generate **ESC OP** through ESC OS, which are the sequences produced by the top row of the keypad on Digital terminals. • **SCO—**The function keys F1 to F12 generate ESC [M through ESC [X. The function and shift keys generate ESC [Y through ESC [j. The control and function keys generate ESC [k through ESC [v. The shift, control and function keys generate ESC [w through ESC [{. • **ESCN—**The default mode. The function keys match the general behavior of Digital terminals. The function keys generate sequences such as ESC [11~ and ESC [12~. • **VT400—**The function keys behave like the default mode. The top row of the numeric keypad generates ESC OP through ESC OS.
Redirection After BIOS POST **set RedirectionAfterPOST**	Whether BIOS console redirection should be active after BIOS POST is complete and control given to the OS bootloader. This can be one of the following: • **Always_Enable—**BIOS Legacy console redirection is active during the OS boot and run time. • **Bootloader—**BIOS Legacy console redirection is disabled before giving control to the OS boot loader.

Name	Description
Out-of-Band Mgmt Port **set comSpcrEnable**	Allows you to configure the COM port 0 that can be used for Windows Emergency Management services. ACPI SPCR table is reported based on this setup option. This can be one of the following: • **Disabled—**Configures the COM port 0 as a general purpose port for use with the Windows Operating System. • **Enabled—**Configures the COM port 0 as a remote management port for Windows Emergency Management services.

LOM and PCIe Slots Configuration Parameters

Name	Description
All Onboard LOM Ports **set AllLomPortControl**	Whether all LOM ports are enabled or disabled. This can be one of the following: • **Disabled—**All LOM ports are disabled. • **Enabled—**All LOM ports are enabled.
LOM Port *n* OptionROM **set LomOpromControlPort*n***	Whether Option ROM is available on the LOM port designated by ***n***. This can be one of the following: • **Disabled—**The expansion slot ***n*** is not available. • **Enabled—**The expansion slot ***n*** is available. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.
All PCIe Slots OptionROM **set PcieOptionROMs**	Whether the server can use the PCIe Option ROM expansion slots. This can be one of the following: • **Disabled—**The expansion slot ***n*** is not available. • **Enabled—**The expansion slot ***n*** is available. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.

Name	Description
PCIe Slot:*n* OptionROM **set PcieSlot*n*OptionROM**	Whether PCIe expansion slot ***n*** is available to the server. This can be one of the following: • **Disabled—**The expansion slot ***n*** is not available. • **Enabled—**The expansion slot ***n*** is available. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.
PCIe Mezzanine OptionROM **set PcieMezzOptionROM**	Whether the PCIe mezzanine slot expansion ROM is available to the server. This can be one of the following: • **Disabled—**The expansion slot ***n*** is not available. • **Enabled—**The expansion slot ***n*** is available. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.
PCIe Slot:*n* Link Speed **PCIe Slot:*n*LinkSpeed**	This option allows you to restrict the maximum speed of an adapter card installed in PCIe slot ***n***. This can be one of the following: • **GEN1—**2.5GT/s (gigatransfers per second) is the maximum speed allowed. • **GEN2—**5GT/s is the maximum speed allowed. • **GEN3—**8GT/s is the maximum speed allowed. • **Disabled—**The maximum speed is not restricted. For example, if you have a 3rd generation adapter card in PCIe slot 2 that you want to run at a maximum of 5GT/s instead of the 8GT/s that card supports, set the PCIe Slot 2 Link Speed to **GEN2**. The system then ignores the card's supported maximum speed of 8GT/s and forces it to run at a maximum of 5 GT/s.

Server Management BIOS Parameters for C220 and C240 Servers

Name	Description
FRB-2 Timer **set FRB-2**	Whether the FRB2 timer is used by CIMC to recover the system if it hangs during POST. This can be one of the following: • **Disabled—**The FRB2 timer is not used. • **Enabled—**The FRB2 timer is started during POST and used to recover the system if necessary.

Name	Description
OS Watchdog Timer **set OSBootWatchdogTimer**	Whether the BIOS programs the watchdog timer with a specified timeout value. This can be one of the following: • **Disabled—**The watchdog timer is not used to track how long the server takes to boot. • **Enabled—**The watchdog timer tracks how long the server takes to boot. If the server does not boot within the length of time specified by the **set OSBootWatchdogTimerTimeout** command, the CIMC logs an error and takes the action specified by the **set OSBootWatchdogTimerPolicy** command.
OS Watchdog Timer Timeout **set OSBootWatchdogTimerTimeOut**	What timeout value the BIOS uses to configure the watchdog timer. This can be one of the following: • **5_Minutes—**The watchdog timer expires 5 minutes after the OS begins to boot. • **10_Minutes—**The watchdog timer expires 10 minutes after the OS begins to boot. • **15_Minutes—**The watchdog timer expires 15 minutes after the OS begins to boot. • **20_Minutes—**The watchdog timer expires 20 minutes after the OS begins to boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.
OS Watchdog Timer Policy **set OSBootWatchdogTimerPolicy**	What action the system takes if the watchdog timer expires. This can be one of the following: • **Do_Nothing—**The server takes no action if the watchdog timer expires during OS boot. • **Power_Down—**The server is powered off if the watchdog timer expires during OS boot. • **Reset—**The server is reset if the watchdog timer expires during OS boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.

Name	Description
Boot Order Rules **set ManagedBootRule**	How the server changes the boot order list defined through the CIMC GUI or CLI when there are no devices of a particular device type available or when the user defines a different boot order using the server's BIOS Setup Utility. The supported device types are: • **HDD—**Hard disk drive • **FDD—**Floppy disk drive • **CDROM—**Bootable CD-ROM or DVD • **PXE—**PXE boot • **EFI—**Extensible Firmware Interface The Boot Order Rules option can be one of the following: • **Strict—**When no devices of a particular type are available, the system creates a placeholder for that device type in the boot order list. When a device of that type becomes available, it is added to the boot order in the previously defined position. If the user defines a boot order through the server's BIOS Setup Utility, that boot order is given priority over the boot order configured through the CIMC GUI or CLI. All device types defined through CIMC that are not present in the boot order defined through the BIOS Setup Utility are removed from the boot order list. • **Loose—**When no devices of a particular type are available, the system removes that device type from the boot order. When a device of that type becomes available, the system adds it to the end of the boot order list. If the boot order is configured through the server's BIOS Setup Utility, that boot order is given priority over the boot order configured through the CIMC GUI or CLI. All device types defined through CIMC that are not present in the boot order defined through the BIOS Setup Utility are moved to the end of the boot order list.

C260 Servers

Main BIOS Parameters for C260 Servers

Name	Description
POST Error Pause **set POSTErrorPause**	What happens when the server encounters a critical error during POST. This can be one of the following: • **Enabled—**The BIOS pauses the attempt to boot the server and opens the Error Manager when a critical error occurs during POST. • **Disabled—**The BIOS continues to attempt to boot the server.
Boot Option Retry **set BootOptionRetry**	Whether the BIOS retries NON-EFI based boot options without waiting for user input. This can be one of the following: • **Enabled—**Continually retries NON-EFI based boot options without waiting for user input. • **Disabled—**Waits for user input before retrying NON-EFI based boot options.

Advanced BIOS Parameters for C260 Servers

Processor Configuration Parameters

Name	Description
Intel Turbo Boost Technology **set IntelTurboBoostTech**	Whether the processor uses Intel Turbo Boost Technology, which allows the processor to automatically increase its frequency if it is running below power, temperature, or voltage specifications. This can be one of the following: • **Disabled—**The processor does not increase its frequency automatically. • **Enabled—**The processor utilizes Turbo Boost Technology if required.

Name	Description
Enhanced Intel Speedstep Technology **set EnhancedIntelSpeedStep**	Whether the processor uses Enhanced Intel SpeedStep Technology, which allows the system to dynamically adjust processor voltage and core frequency. This technology can result in decreased average power consumption and decreased average heat production. This can be one of the following: • **Disabled—**The processor never dynamically adjusts its voltage or frequency. • **Enabled—**The processor utilizes Enhanced Intel SpeedStep Technology and enables all supported processor sleep states to further conserve power. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Intel Hyper-Threading Technology **set IntelHyperThread**	Whether the processor uses Intel Hyper-Threading Technology, which allows multithreaded software applications to execute threads in parallel within each processor. This can be one of the following: • **Disabled—**The processor does not permit hyperthreading. • **Enabled—**The processor allows for the parallel execution of multiple threads. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Number of Enabled Cores **set CoreMultiProcessing**	Allows you to disable one or more of the physical cores on the server. This can be one of the following: • **All—**Enables all physical cores. This also enables Hyper Threading on the associated logical processor cores. • **1** through ***n*—**Specifies the number of physical processor cores that can run on the server. Each physical core has an associated logical core. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.

Name	Description
Execute Disable **set ExecuteDisable**	Classifies memory areas on the server to specify where application code can execute. As a result of this classification, the processor disables code execution if a malicious worm attempts to insert code in the buffer. This setting helps to prevent damage, worm propagation, and certain classes of malicious buffer overflow attacks. This can be one of the following: • **Disabled—**The processor does not classify memory areas. • **Enabled—**The processor classifies memory areas. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Intel Virtualization Technology **set IntelVT**	Whether the processor uses Intel Virtualization Technology (VT), which allows a platform to run multiple operating systems and applications in independent partitions. This can be one of the following: • **Disabled—**The processor does not permit virtualization. • **Enabled—**The processor allows multiple operating systems in independent partitions. **Note** If you change this option, you must power cycle the server before the setting takes effect.
Intel VT for Directed IO **set IntelVTD**	Whether the processor uses Intel Virtualization Technology for Directed I/O (VT-d). This can be one of the following: • **Disabled—**The processor does not use virtualization technology. • **Enabled—**The processor uses virtualization technology.
Intel VT-d Interrupt Remapping **set InterruptRemap**	Whether the processor supports Intel VT-d Interrupt Remapping. This can be one of the following: • **Disabled—**The processor does not support remapping. • **Enabled—**The processor uses VT-d Interrupt Remapping as required.
Intel VT-d Coherency Support **set CoherencySupport**	Whether the processor supports Intel VT-d Coherency. This can be one of the following: • **Disabled—**The processor does not support coherency. • **Enabled—**The processor uses VT-d Coherency as required.

Name	Description
Intel VT-d Address Translation Services **set ATS**	Whether the processor supports Intel VT-d Address Translation Services (ATS). This can be one of the following: • **Disabled—**The processor does not support ATS. • **Enabled—**The processor uses VT-d ATS as required.
Intel VT-d PassThrough DMA **set PassThroughDMA**	Whether the processor supports Intel VT-d Pass-through DMA. This can be one of the following: • **Disabled—**The processor does not support pass-through DMA. • **Enabled—**The processor uses VT-d Pass-through DMA as required.
Direct Cache Access **set DirectCacheAccess**	Allows processors to increase I/O performance by placing data from I/O devices directly into the processor cache. This setting helps to reduce cache misses. This can be one of the following: • **Disabled—**Data from I/O devices is not placed directly into the processor cache. • **Enabled—**Data from I/O devices is placed directly into the processor cache.
Processor C3 Report **set ProcessorC3Report**	Whether the BIOS sends the C3 report to the operating system. When the OS receives the report, it can transition the processor into the lower C3 power state to decrease energy usage while maintaining optimal processor performance. This can be one of the following: • **Disabled—**The BIOS does not send the C3 report. • **ACPI_C2—**The BIOS sends the C3 report using the ACPI C2 format, allowing the OS to transition the processor to the C3 low power state. • **ACPI_C3—**The BIOS sends the C3 report using the ACPI C3 format, allowing the OS to transition the processor to the C3 low power state.

Name	Description
Processor C6 Report **set ProcessorC6Report**	Whether the BIOS sends the C6 report to the operating system. When the OS receives the report, it can transition the processor into the lower C6 power state to decrease energy usage while maintaining optimal processor performance. This can be one of the following: • **Disabled—**The BIOS does not send the C6 report. • **Enabled—**The BIOS sends the C6 report, allowing the OS to transition the processor to the C6 low power state.
Package C State Limit **set PackageCStateLimit**	The amount of power available to the server components when they are idle. This can be one of the following: • **C0_state—**The server provides all server components with full power at all times. This option maintains the highest level of performance and requires the greatest amount of power. • **C1_state—**When the CPU is idle, the system slightly reduces the power consumption. This option requires less power than C0 and allows the server to return quickly to high performance mode. • **C3_state—**When the CPU is idle, the system reduces the power consumption further than with the C1 option. This requires less power than C1 or C0, but it takes the server slightly longer to return to high performance mode. • **C6_state—**When the CPU is idle, the system reduces the power consumption further than with the C3 option. This option saves more power than C0, C1, or C3, but there may be performance issues until the server returns to full power. • **C7_state—**When the CPU is idle, the server makes a minimal amount of power available to the components. This option saves the maximum amount of power but it also requires the longest time for the server to return to high performance mode. • **No_Limit—**The server may enter any available C state. **Note** This option is used only if **CPU C State** is enabled.

Name	Description
CPU C State **set ProcessorCcxEnable**	Whether the system can enter a power savings mode during idle periods. This can be one of the following: • **Disabled—**The system remains in high performance state even when idle. • **Enabled—**The system can reduce power to system components such as the DIMMs and CPUs. The amount of power reduction is specified by the **set PackageCStateLimit** command.
C1E **set ProcessorC1eEnable**	Whether the CPU transitions to its minimum frequency when entering the C1 state. This can be one of the following: • **Disabled—**The CPU continues to run at its maximum frequency in C1 state. • **Enabled—**The CPU transitions to its minimum frequency. This option saves the maximum amount of power in C1 state. **Note** This option is used only if **ProcessorCcxEnable** is enabled.

Memory Configuration Parameters

Name	Description
Select Memory RAS **set SelectMemoryRAS**	How the memory reliability, availability, and serviceability (RAS) is configured for the server. This can be one of the following: • **Maximum_Performance—**System performance is optimized. • **Mirroring—**System reliability is optimized by using half the system memory as backup. • **Sparing—**The system reserves some memory for use in the event a DIMM fails. If that happens, the server takes the DIMM offline and replaces it with the reserved memory. This option provides less redundancy than mirroring, but it leaves more of the memory available for programs running on the server.

Name	Description
NUMA Optimized **set NUMAOptimize**	Whether the BIOS supports NUMA. This can be one of the following: • **Disabled—**The BIOS does not support NUMA. • **Enabled—**The BIOS includes the ACPI tables that are required for NUMA-aware operating systems. If you enable this option, the system must disable Inter-Socket Memory interleaving on some platforms.
Sparing Mode **set SparingMode**	The sparing mode used by the CIMC. This can be one of the following: • **Rank_Sparing—**The spared memory is allocated at the rank level. • **DIMM Sparing—**The spared memory is allocated at the DIMM level. **Note** This option is used only if **set SelectMemoryRAS** is set to **Sparing**.
Mirroring Mode **set MirroringMode**	Mirroring is supported across Integrated Memory Controllers (IMCs) where one memory riser is mirrored with another. This can be one of the following: • **Intersocket—**Each IMC is mirrored across two sockets. • **Intrasocket—**One IMC is mirrored with another IMC in the same socket. **Note** This option is used only if **SelectMemoryRAS** is set to **Mirroring**.
DRAM Refresh rate **set DramRefreshRate**	Allows you to set the rate at which the DRAM cells are refreshed. This can be one of the following: • **1x—**DRAM cells are refreshed every 64ms. • **2x—**DRAM cells are refreshed every 32ms. • **3x—**DRAM cells are refreshed every 21ms. • **4x—**DRAM cells are refreshed every 16ms. • **Auto—**DRAM cells refresh rate is automatically chosen by the BIOS based on the system configuration. This is the recommended setting for this parameter.

Name	Description
Patrol Scrub **set PatrolScrub**	Whether the system actively searches for, and corrects, single bit memory errors even in unused portions of the memory on the server. This can be one of the following: • **Disabled—**The system checks for memory ECC errors only when the CPU reads or writes a memory address. • **Enabled—**The system periodically reads and writes memory searching for ECC errors. If any errors are found, the system attempts to fix them. This option may correct single bit errors before they become multi-bit errors, but it may adversely affect performance when the patrol scrub is running.
Patrol Scrub Interval **set PatrolScrubDuration**	Controls the time interval between each patrol scrub memory access. A lower interval scrubs the memory more often but requires more memory bandwidth. Select a value between 5 and 23. The default value is 8. **Note** This option is used only if **Patrol Scrub** is enabled.
CKE Low Policy **set CkeLowPolicy**	Controls the DIMM power savings mode policy. This can be one of the following: • **Disabled—**DIMMs do not enter power saving mode. • **Slow—**DIMMs can enter power saving mode, but the requirements are higher. Therefore, DIMMs enter power saving mode less frequently. • **Fast—**DIMMs enter power saving mode as often as possible. • **Auto—**The BIOS controls when a DIMM enters power saving mode based on the DIMM configuration.

Serial Port Configuration Parameters

Name	Description
Serial A Enable **set Serial-PortA**	Whether serial port A is enabled or disabled. This can be one of the following: • **Disabled—**The serial port is disabled. • **Enabled—**The serial port is enabled.

USB Configuration Parameters

Name	Description
Make Device Non-Bootable **set MakeUSBDeviceNonBootable**	Whether the server can boot from a USB device. This can be one of the following: • **Disabled—**The server can boot from a USB device. • **Enabled—**The server cannot boot from a USB device.

PCI Configuration Parameters

Name	Description
Memory Mapped I/O Above 4GB **set MemoryMappedIOAbove4GB**	Whether to enable or disable memory mapped I/O of 64-bit PCI devices to 4GB or greater address space. Legacy option ROMs are not able to access addresses above 4GB. PCI devices that are 64-bit compliant but use a legacy option ROM may not function correctly with this setting enabled. This can be one of the following: • **Disabled—**The server does not map I/O of 64-bit PCI devices to 4GB or greater address space. • **Enabled—**The server maps I/O of 64-bit PCI devices to 4GB or greater address space.
Onboard NIC *n* ROM **set NIC-*n*-ROM**	Whether the system loads the embedded PXE option ROM for the onboard NIC designated by ***n***. This can be one of the following: • **Disabled—**PXE option ROM is not available for NIC ***n***. • **Enabled—**PXE option ROM is available for NIC ***n***.
PCIe OptionROMs **set PciOptionRomsDisable**	Whether the server can use the PCIe Option ROM expansion slots. This can be one of the following: • **Disabled—**PCIe Option ROMs are not available. • **Enabled—**PCIe Option ROMs are available. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.

Name	Description
PCIe Slot *n* ROM **set Slot-*n*-ROM**	Whether PCIe expansion slot ***n*** is available to the server. This can be one of the following: • **Disabled—**The expansion slot ***n*** is not available. • **Enabled—**The expansion slot ***n*** is available. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.
Onboard Gbit LOM **set OnboardNic1**	Whether Gbit LOM is enabled or disabled on the server. This can be one of the following: • **Disabled—**Gbit LOM is not available. • **Enabled—**10Git LOM is available.
Onboard 10Gbit LOM **set OnboardNic2**	Whether 10Gbit LOM is enabled or disabled on the server. This can be one of the following: • **Disabled—**10GBit LOM is not available. • **Enabled—**10GBit LOM is available.
Sriov **set SrIov**	Whether SR-IOV (Single Root I/O Virtualization) is enabled or disabled on the server. This can be one of the following: • **Disabled—**SR-IOV is disabled. • **Enabled—**SR-IOV is enabled.

Name	Description
IOH Resource Allocation **set IOHResource**	Enables you to distribute 64KB of 16-bit IO resources between IOH0 and IOH1 as per system requirement. This can be one of the following: • **IOH0 24k IOH1 40k—** Allocates 24KB of 16-bit IO resources to IOH0 and 40KB of 16-bit IO resources to IOH1. • **IOH0 32k IOH1 32k—** Allocates 32KB of 16-bit IO resources to IOH0 and 32KB of 16-bit IO resources to IOH1. • **IOH0 40k IOH1 24k—** Allocates 40KB of 16-bit IO resources to IOH0 and 24KB of 16-bit IO resources to IOH1. • **IOH0 48k IOH1 16k—** Allocates 48KB of 16-bit IO resources to IOH0 and 16KB of 16-bit IO resources to IOH1. • **IOH0 56k IOH1 8k—** Allocates 56KB of 16-bit IO resources to IOH0 and 8KB of 16-bit IO resources to IOH1.

Server Management BIOS Parameters for C260 Servers

Name	Description
Assert NMI on SERR **set AssertNMIOnSERR**	Whether the BIOS generates a non-maskable interrupt (NMI) and logs an error when a system error (SERR) occurs. This can be one of the following: • **Disabled—**The BIOS does not generate an NMI or log an error when a SERR occurs. • **Enabled—**The BIOS generates an NMI and logs an error when a SERR occurs. You must enable this setting if you want to enable **Assert_NMI_on_PERR**.
Assert NMI on PERR **set AssertNMIOnPERR**	Whether the BIOS generates a non-maskable interrupt (NMI) and logs an error when a processor bus parity error (PERR) occurs. This can be one of the following: • **Disabled—**The BIOS does not generate an NMI or log an error when a PERR occurs. • **Enabled—**The BIOS generates an NMI and logs an error when a PERR occurs. You must enable **Assert_NMI_on_SERR** to use this setting.

Name	Description
Console Redirection **set ConsoleRedir**	Allows a serial port to be used for console redirection during POST and BIOS booting. After the BIOS has booted and the operating system is responsible for the server, console redirection is irrelevant and has no effect. This can be one of the following: • **Disabled—**No console redirection occurs during POST. • **Serial_Port_A—**Enables console redirection on serial port A during POST. **Note** If you enable this option, you also disable the display of the Quiet Boot logo screen during POST.
Flow Control **set FlowCtrl**	Whether a handshake protocol is used for flow control. Request to Send / Clear to Send (RTS/CTS) helps to reduce frame collisions that can be introduced by a hidden terminal problem. This can be one of the following: • **None—**No flow control is used. • **RTS-CTS—**RTS/CTS is used for flow control. **Note** This setting must match the setting on the remote terminal application.
Baud Rate **set BaudRate**	What BAUD rate is used for the serial port transmission speed. If you disable Console Redirection, this option is not available. This can be one of the following: • **9.6k—**A 9600 BAUD rate is used. • **19.2k—**A 19200 BAUD rate is used. • **38.4k—**A 38400 BAUD rate is used. • **57.6k—**A 57600 BAUD rate is used. • **115.2k—**A 115200 BAUD rate is used. **Note** This setting must match the setting on the remote terminal application.

Name	Description
Terminal Type **set TerminalType**	What type of character formatting is used for console redirection. This can be one of the following: • **PC-ANSI—**The PC-ANSI terminal font is used. • **VT100—**A supported vt100 video terminal and its character set are used. • **VT100-PLUS—**A supported vt100-plus video terminal and its character set are used. • **VT-UTF8—**A video terminal with the UTF-8 character set is used. **Note** This setting must match the setting on the remote terminal application.
OS Boot Watchdog Timer Timeout **set OSBootWatchdogTimerTimeOut**	What timeout value the BIOS uses to configure the watchdog timer. This can be one of the following: • **5_Minutes—**The watchdog timer expires 5 minutes after the OS begins to boot. • **10_Minutes—**The watchdog timer expires 10 minutes after the OS begins to boot. • **15_Minutes—**The watchdog timer expires 15 minutes after the OS begins to boot. • **20_Minutes—**The watchdog timer expires 20 minutes after the OS begins to boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.
OS Boot Watchdog Policy **set OSBootWatchdogTimerPolicy**	What action the system takes if the watchdog timer expires. This can be one of the following: • **Power_Off—**The server is powered off if the watchdog timer expires during OS boot. • **Reset—**The server is reset if the watchdog timer expires during OS boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.

Name	Description
Legacy OS Redirection **set LegacyOSRedir**	Whether redirection from a legacy operating system, such as DOS, is enabled on the serial port. This can be one of the following: • **Disabled—**The serial port enabled for console redirection is hidden from the legacy operating system. • **Enabled—**The serial port enabled for console redirection is visible to the legacy operating system.
OS Boot Watchdog Timer **set OSBootWatchdogTimer**	Whether the BIOS programs the watchdog timer with a specified timeout value. This can be one of the following: • **Disabled—**The watchdog timer is not used to track how long the server takes to boot. • **Enabled—**The watchdog timer tracks how long the server takes to boot. If the server does not boot within the length of time specified by the **set OSBootWatchdogTimerTimeout** command, the CIMC logs an error and takes the action specified by the **set OSBootWatchdogTimerPolicy** command.

C420 Servers

Main BIOS Parameters for C420 Servers

Name	Description
TPM Support **set TPMAdminCtrl**	TPM (Trusted Platform Module) is a microchip designed to provide basic security-related functions primarily involving encryption keys. This option allows you to control the TPM Security Device support for the system. It can be one of the following: • **Disabled—**The server does not use the TPM. • **Enabled—**The server uses the TPM. **Note** We recommend that you contact your operating system vendor to make sure the operating system supports this feature.

Advanced BIOS Parameters for C420 Servers

Processor Configuration Parameters

Name	Description
Intel Hyper-Threading Technology **set IntelHyperThread**	Whether the processor uses Intel Hyper-Threading Technology, which allows multithreaded software applications to execute threads in parallel within each processor. This can be one of the following: • **Disabled—**The processor does not permit hyperthreading. • **Enabled—**The processor allows for the parallel execution of multiple threads. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Number of Enabled Cores **set CoreMultiProcessing**	Allows you to disable one or more of the physical cores on the server. This can be one of the following: • **All—**Enables all physical cores. This also enables Hyper Threading on the associated logical processor cores. • **1** through ***n*—**Specifies the number of physical processor cores that can run on the server. Each physical core has an associated logical core. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Execute Disable **set ExecuteDisable**	Classifies memory areas on the server to specify where application code can execute. As a result of this classification, the processor disables code execution if a malicious worm attempts to insert code in the buffer. This setting helps to prevent damage, worm propagation, and certain classes of malicious buffer overflow attacks. This can be one of the following: • **Disabled—**The processor does not classify memory areas. • **Enabled—**The processor classifies memory areas. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.

Name	Description
Intel VT **set IntelVT**	Whether the processor uses Intel Virtualization Technology (VT), which allows a platform to run multiple operating systems and applications in independent partitions. This can be one of the following: • **Disabled—**The processor does not permit virtualization. • **Enabled—**The processor allows multiple operating systems in independent partitions. **Note** If you change this option, you must power cycle the server before the setting takes effect.
Intel VT-d **set IntelVTD**	Whether the processor uses Intel Virtualization Technology for Directed I/O (VT-d). This can be one of the following: • **Disabled—**The processor does not use virtualization technology. • **Enabled—**The processor uses virtualization technology.
Intel VT-d Coherency Support **set CoherencySupport**	Whether the processor supports Intel VT-d Coherency. This can be one of the following: • **Disabled—**The processor does not support coherency. • **Enabled—**The processor uses VT-d Coherency as required.
Intel VT-d ATS Support **set ATS**	Whether the processor supports Intel VT-d Address Translation Services (ATS). This can be one of the following: • **Disabled—**The processor does not support ATS. • **Enabled—**The processor uses VT-d ATS as required.

Name	Description
CPU Performance **set CPUPerformance**	Sets the CPU performance profile for the server. The performance profile consists of the following options: • DCU Streamer Prefetcher • DCU IP Prefetcher • Hardware Prefetcher • Adjacent Cache-Line Prefetch This can be one of the following: • **Enterprise—**All options are enabled. • **High_Throughput—**Only the DCU IP Prefetcher is enabled. The rest of the options are disabled. • **HPC—**All options are enabled. This setting is also known as high performance computing. • **Custom—**All performance profile options can be configured from the BIOS setup on the server. In addition, the Hardware Prefetcher and Adjacent Cache-Line Prefetch options can be configured in the fields below.
Hardware Prefetcher **set HardwarePrefetch**	Whether the processor allows the Intel hardware prefetcher to fetch streams of data and instruction from memory into the unified second-level cache when necessary. This can be one of the following: • **Disabled—**The hardware prefetcher is not used. • **Enabled—**The processor uses the hardware prefetcher when cache issues are detected.
Adjacent Cache Line Prefetcher **set AdjacentCacheLinePrefetch**	Whether the processor fetches cache lines in even/odd pairs instead of fetching just the required line. This can be one of the following: • **Disabled—**The processor only fetches the required line. • **Enabled—** The processor fetches both the required line and its paired line.

Name	Description
DCU Streamer Prefetch **set DcuStreamerPrefetch**	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache. This can be one of the following: • **Disabled—**The processor does not try to anticipate cache read requirements and only fetches explicitly requested lines. • **Enabled—**The DCU prefetcher analyzes the cache read pattern and prefetches the next line in the cache if it determines that it may be needed.
DCU IP Prefetcher **set DcuIpPrefetch**	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache. This can be one of the following: • **Disabled—**The processor does not preload any cache data. • **Enabled—**The DCU IP prefetcher preloads the L1 cache with the data it determines to be the most relevant.
Direct Cache Access Support **set DirectCacheAccess**	Allows processors to increase I/O performance by placing data from I/O devices directly into the processor cache. This setting helps to reduce cache misses. This can be one of the following: • **Disabled—**Data from I/O devices is not placed directly into the processor cache. • **Enabled—**Data from I/O devices is placed directly into the processor cache.

Name	Description
Power Technology **set CPUPowerManagement**	Enables you to configure the CPU power management settings for the following options: • Enhanced Intel Speedstep Technology • Intel Turbo Boost Technology • Processor Power State C6 Power Technology can be one of the following: • **Custom—**The server uses the individual settings for the BIOS parameters mentioned above. You must select this option if you want to change any of these BIOS parameters. • **Disabled—**The server does not perform any CPU power management and any settings for the BIOS parameters mentioned above are ignored. • **Energy_Efficient—**The server determines the best settings for the BIOS parameters mentioned above and ignores the individual settings for these parameters.
Enhanced Intel Speedstep Technology **set EnhancedIntelSpeedStep**	Whether the processor uses Enhanced Intel SpeedStep Technology, which allows the system to dynamically adjust processor voltage and core frequency. This technology can result in decreased average power consumption and decreased average heat production. This can be one of the following: • **Disabled—**The processor never dynamically adjusts its voltage or frequency. • **Enabled—**The processor utilizes Enhanced Intel SpeedStep Technology and enables all supported processor sleep states to further conserve power. We recommend that you contact your operating system vendor to make sure the operating system supports this feature. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.

Name	Description
Intel Turbo Boost Technology **set IntelTurboBoostTech**	Whether the processor uses Intel Turbo Boost Technology, which allows the processor to automatically increase its frequency if it is running below power, temperature, or voltage specifications. This can be one of the following: • **Disabled—**The processor does not increase its frequency automatically. • **Enabled—**The processor utilizes Turbo Boost Technology if required. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Processor Power State C6 **set ProcessorC6Report**	Whether the BIOS sends the C6 report to the operating system. When the OS receives the report, it can transition the processor into the lower C6 power state to decrease energy usage while maintaining optimal processor performance. This can be one of the following: • **Disabled—**The BIOS does not send the C6 report. • **Enabled—**The BIOS sends the C6 report, allowing the OS to transition the processor to the C6 low power state. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Processor Power State C1 Enhanced **set ProcessorC1EReport**	Whether the CPU transitions to its minimum frequency when entering the C1 state. This can be one of the following: • **Disabled—**The CPU continues to run at its maximum frequency in C1 state. • **Enabled—**The CPU transitions to its minimum frequency. This option saves the maximum amount of power in C1 state.
Frequency Floor Override **set CpuFreqFloor**	Whether the CPU is allowed to drop below the maximum non-turbo frequency when idle. This can be one of the following: • **Disabled—** The CPU can drop below the maximum non-turbo frequency when idle. This option decreases power consumption but may reduce system performance. • **Enabled—** The CPU cannot drop below the maximum non-turbo frequency when idle. This option improves system performance but may increase power consumption.

Name	Description
P-STATE Coordination **set PsdCoordType**	Allows you to define how BIOS communicates the P-state support model to the operating system. There are 3 models as defined by the Advanced Configuration and Power Interface (ACPI) specification. • **HW_ALL—**The processor hardware is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a package). • **SW_ALL—**The OS Power Manager (OSPM) is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a physical package), and must initiate the transition on all of the logical processors. • **SW_ANY—**The OS Power Manager (OSPM) is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a package), and may initiate the transition on any of the logical processors in the domain. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Energy Performance **set CpuEngPerfBias**	Allows you to determine whether system performance or energy efficiency is more important on this server. This can be one of the following: • **Balanced_Energy** • **Balanced_Performance** • **Energy_Efficient** • **Performance**

Memory Configuration Parameters

Name	Description
Select Memory RAS **set SelectMemoryRAS**	How the memory reliability, availability, and serviceability (RAS) is configured for the server. This can be one of the following: • **Maximum_Performance—**System performance is optimized. • **Mirroring—**System reliability is optimized by using half the system memory as backup. • **Lockstep—**If the DIMM pairs in the server have an identical type, size, and organization and are populated across the SMI channels, you can enable lockstep mode to minimize memory access latency and provide better performance. This option offers better system performance than Mirroring and better reliability than Maximum Performance but lower reliability than Mirroring and lower system performance than Maximum Performance.
DRAM Clock Throttling **set DRAMClockThrottling**	Allows you to tune the system settings between the memory bandwidth and power consumption. This can be one of the following: • **Balanced—** DRAM clock throttling is reduced, providing a balance between performance and power. • **Performance—**DRAM clock throttling is disabled, providing increased memory bandwidth at the cost of additional power. • **Energy_Efficient—**DRAM clock throttling is increased to improve energy efficiency.
NUMA **set NUMAOptimize**	Whether the BIOS supports NUMA. This can be one of the following: • **Disabled—**The BIOS does not support NUMA. • **Enabled—**The BIOS includes the ACPI tables that are required for NUMA-aware operating systems. If you enable this option, the system must disable Inter-Socket Memory interleaving on some platforms.

Name	Description
Low Voltage DDR Mode **set LvDDRMode**	Whether the system prioritizes low voltage or high frequency memory operations. This can be one of the following: • **Power_Saving_Mode—**The system prioritizes low voltage memory operations over high frequency memory operations. This mode may lower memory frequency in order to keep the voltage low. • **Performance_Mode—**The system prioritizes high frequency operations over low voltage operations.
DRAM Refresh rate **set DramRefreshRate**	Allows you to set the rate at which the DRAM cells are refreshed. This can be one of the following: • **1x—**DRAM cells are refreshed every 64ms. • **2x—**DRAM cells are refreshed every 32ms. • **3x—**DRAM cells are refreshed every 21ms. • **4x—**DRAM cells are refreshed every 16ms. • **Auto—**DRAM cells refresh rate is automatically chosen by the BIOS based on the system configuration. This is the recommended setting for this parameter.
Channel Interleaving **set ChannelInterLeave**	Whether the CPU divides memory blocks and spreads contiguous portions of data across interleaved channels to enable simultaneous read operations. This can be one of the following: • **Auto—**The CPU determines what interleaving is done. • **1_Way—**Some channel interleaving is used. • **2_Way** • **3_Way** • **4_Way—**The maximum amount of channel interleaving is used.

Name	Description
Rank Interleaving **set RankInterLeave**	Whether the CPU interleaves physical ranks of memory so that one rank can be accessed while another is being refreshed. This can be one of the following: • **Auto—**The CPU determines what interleaving is done. • **1_Way—**Some rank interleaving is used. • **2_Way** • **4_Way** • **8_Way—**The maximum amount of rank interleaving is used.
Patrol Scrub **set PatrolScrub**	Whether the system actively searches for, and corrects, single bit memory errors even in unused portions of the memory on the server. This can be one of the following: • **Disabled—**The system checks for memory ECC errors only when the CPU reads or writes a memory address. • **Enabled—**The system periodically reads and writes memory searching for ECC errors. If any errors are found, the system attempts to fix them. This option may correct single bit errors before they become multi-bit errors, but it may adversely affect performance when the patrol scrub is running.
Demand Scrub **set DemandScrub**	Whether the system corrects single bit memory errors encountered when the CPU or I/O makes a demand read. This can be one of the following: • **Disabled—** Single bit memory errors are not corrected. • **Enabled—** Single bit memory errors are corrected in memory and the corrected data is set in response to the demand read.

Name	Description
Altitude **set Altitude**	The approximate number of meters above sea level at which the physical server is installed. This can be one of the following: • **Auto—**The CPU determines the physical elevation. • **300_M—**The server is approximately 300 meters above sea level. • **900_M—**The server is approximately 900 meters above sea level. • **1500_M—**The server is approximately 1500 meters above sea level. • **3000_M—**The server is approximately 3000 meters above sea level.

QPI Configuration Parameters

Name	Description
QPI Link Frequency **set QPILinkFrequency**	The Intel QuickPath Interconnect (QPI) link frequency, in gigatransfers per second (GT/s). This can be one of the following: • **Auto—**The CPU determines the QPI link frequency. • **6.4_GT/s** • **7.2_GT/s** • **8.0_GT/s**

USB Configuration Parameters

Name	Description
Legacy USB Support **set LegacyUSBSupport**	Whether the system supports legacy USB devices. This can be one of the following: • **Disabled—**USB devices are only available to EFI applications. • **Enabled—**Legacy USB support is always available. • **Auto—**Disables legacy USB support if no USB devices are connected.

Name	Description
All USB Devices **set AllUsbDevices**	Whether all physical and virtual USB devices are enabled or disabled. This can be one of the following: • **Disabled—**All USB devices are disabled. • **Enabled—**All USB devices are enabled.
USB Port: Rear **set UsbPortRear**	Whether the rear panel USB devices are enabled or disabled. This can be one of the following: • **Disabled—**Disables the rear panel USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled—**Enables the rear panel USB ports. Devices connected to these ports are detected by the BIOS and operating system.
USB Port: Front **set UsbPortFront**	Whether the front panel USB devices are enabled or disabled. This can be one of the following: • **Disabled—**Disables the front panel USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled—**Enables the front panel USB ports. Devices connected to these ports are detected by the BIOS and operating system.
USB Port: Internal **set UsbPortInt**	Whether the internal USB devices are enabled or disabled. This can be one of the following: • **Disabled—**Disables the internal USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled—**Enables the internal USB ports. Devices connected to these ports are detected by the BIOS and operating system.
USB Port: KVM **set UsbPortKVM**	Whether the KVM ports are enabled or disabled. This can be one of the following: • **Disabled—**Disables the KVM keyboard and/or mouse devices. Keyboard and/or mouse will not work in the KVM window. • **Enabled—**Enables the KVM keyboard and/or mouse devices.
USB Port: VMedia **set UsbPortVMedia**	Whether the virtual media devices are enabled or disabled. This can be one of the following: • **Disabled—**Disables the vMedia devices. • **Enabled—**Enables the vMedia devices.

Name	Description
USB Port: SD Card **set UsbPortSdCard**	Whether the SD card drives are enabled or disabled. This can be one of the following: • **Disabled—**Disables the SD card drives. The SD card drives are not detected by the BIOS and operating system. • **Enabled—**Enables the SD card drives.

PCI Configuration Parameters

Name	Description
MMIO Above 4GB **set MemoryMappedIOAbove4GB**	Whether to enable or disable memory mapped I/O of 64-bit PCI devices to 4GB or greater address space. Legacy option ROMs are not able to access addresses above 4GB. PCI devices that are 64-bit compliant but use a legacy option ROM may not function correctly with this setting enabled. This can be one of the following: • **Disabled—**The server does not map I/O of 64-bit PCI devices to 4GB or greater address space. • **Enabled—**The server maps I/O of 64-bit PCI devices to 4GB or greater address space.
ASPM Support **set ASPMSupport**	Allows you to set the level of ASPM (Active Power State Management) support in the BIOS. This can be one of the following: • **Disabled—**ASPM support is disabled in the BIOS. • **Force L0s—**Force all links to L0 standby (L0s) state. • **Auto—**The CPU determines the power state.

Name	Description
VGA Priority **set VgaPriority**	Allows you to set the priority for VGA graphics devices if multiple VGA devices are found in the system. This can be one of the following: • **Onboard—**Priority is given to the onboard VGA device. BIOS post screen and OS boot are driven through the onboard VGA port. • **Offboard—**Priority is given to the PCIE Graphics adapter. BIOS post screen and OS boot are driven through the external graphics adapter port. • **Onboard_VGA_Disabled—**Priority is given to the PCIE Graphics adapter, and the onboard VGA device is disabled. **Note** The vKVM does not function when the onboard VGA is disabled.

Serial Configuration Parameters

Name	Description
Console Redirection **set ConsoleRedir**	Allows a serial port to be used for console redirection during POST and BIOS booting. After the BIOS has booted and the operating system is responsible for the server, console redirection is irrelevant and has no effect. This can be one of the following: • **Disabled—**No console redirection occurs during POST. • **Enabled—**Enables console redirection on serial port A during POST.
Terminal Type **set TerminalType**	What type of character formatting is used for console redirection. This can be one of the following: • **PC-ANSI—**The PC-ANSI terminal font is used. • **VT100—**A supported vt100 video terminal and its character set are used. • **VT100+—**A supported vt100-plus video terminal and its character set are used. • **VT-UTF8—**A video terminal with the UTF-8 character set is used. **Note** This setting must match the setting on the remote terminal application.

Name	Description
Bits per second **set BaudRate**	What BAUD rate is used for the serial port transmission speed. If you disable Console Redirection, this option is not available. This can be one of the following: • **9600—**A 9,600 BAUD rate is used. • **19200—**A 19,200 BAUD rate is used. • **38400—**A 38,400 BAUD rate is used. • **57600—**A 57,600 BAUD rate is used. • **115200—**A 115,200 BAUD rate is used. **Note** This setting must match the setting on the remote terminal application.
Flow Control **set FlowCtrl**	Whether a handshake protocol is used for flow control. Request to Send / Clear to Send (RTS/CTS) helps to reduce frame collisions that can be introduced by a hidden terminal problem. This can be one of the following: • **None—**No flow control is used. • **Hardware_RTS/CTS—**RTS/CTS is used for flow control. **Note** This setting must match the setting on the remote terminal application.
Putty KeyPad **set PuttyFunctionKeyPad**	Allows you to change the action of the PuTTY function keys and the top row of the numeric keypad. This can be one of the following: • **VT100—**The function keys generate ESC OP through ESC O[. • **LINUX—**Mimics the Linux virtual console. Function keys F6 to F12 behave like the default mode, but F1 to F5 generate ESC [[A through ESC [[E. • **XTERMR6—**Function keys F5 to F12 behave like the default mode. Function keys F1 to F4 generate **ESC OP** through ESC OS, which are the sequences produced by the top row of the keypad on Digital terminals. • **SCO—**The function keys F1 to F12 generate ESC [M through ESC [X. The function and shift keys generate ESC [Y through ESC [j. The control and function keys generate ESC [k through ESC [v. The shift, control and function keys generate ESC [w through ESC [{. • **ESCN—**The default mode. The function keys match the general behavior of Digital terminals. The function keys generate sequences such as ESC [11~ and ESC [12~. • **VT400—**The function keys behave like the default mode. The top row of the numeric keypad generates ESC OP through ESC OS.

Name	Description
Redirection After BIOS POST **set RedirectionAfterPOST**	Whether BIOS console redirection should be active after BIOS POST is complete and control given to the OS bootloader. This can be one of the following: • **Always_Enable—**BIOS Legacy console redirection is active during the OS boot and run time. • **Bootloader—**BIOS Legacy console redirection is disabled before giving control to the OS boot loader.

LOM and PCIe Slots Configuration Parameters

Name	Description
All Onboard LOM Ports **set AllLomPortControl**	Whether all LOM ports are enabled or disabled. This can be one of the following: • **Disabled—**All LOM ports are disabled. • **Enabled—**All LOM ports are enabled.
LOM Port *n* OptionROM **set LomOpromControlPort*n***	Whether Option ROM is available on the LOM port designated by ***n***. This can be one of the following: • **Disabled—**Option ROM is not available on LOM port ***n***. • **Enabled—**Option ROM is available on LOM port ***n***. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.
All PCIe Slots OptionROM **set PcieOptionROMs**	Whether the server can use the PCIe Option ROM expansion slots. This can be one of the following: • **Disabled—**PCIe Option ROMs are not available. • **Enabled—**PCIe Option ROMs are available. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.

Name	Description
PCIe Slot:*n* OptionROM **set PcieSlot*n*OptionROM**	Whether PCIe expansion slot ***n*** is available to the server. This can be one of the following: • **Disabled—**The expansion slot ***n*** is not available. • **Enabled—**The expansion slot ***n*** is available. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.
PCIe Slot:*n* Link Speed **PCIe Slot:*n*LinkSpeed**	This option allows you to restrict the maximum speed of an adapter card installed in PCIe slot ***n***. This can be one of the following: • **GEN1—**2.5GT/s (gigatransfers per second) is the maximum speed allowed. • **GEN2—**5GT/s is the maximum speed allowed. • **GEN3—**8GT/s is the maximum speed allowed. • **Disabled—**The maximum speed is not restricted. For example, if you have a 3rd generation adapter card in PCIe slot 2 that you want to run at a maximum of 5GT/s instead of the 8GT/s that card supports, set the PCIe Slot 2 Link Speed to **GEN2**. The system then ignores the card's supported maximum speed of 8GT/s and forces it to run at a maximum of 5 GT/s.

Server Management BIOS Parameters for C420 Servers

Name	Description
FRB-2 Timer **set FRB-2**	Whether the FRB2 timer is used by CIMC to recover the system if it hangs during POST. This can be one of the following: • **Disabled—**The FRB2 timer is not used. • **Enabled—**The FRB2 timer is started during POST and used to recover the system if necessary.

Name	Description
OS Watchdog Timer **set OSBootWatchdogTimer**	Whether the BIOS programs the watchdog timer with a specified timeout value. This can be one of the following: • **Disabled—**The watchdog timer is not used to track how long the server takes to boot. • **Enabled—**The watchdog timer tracks how long the server takes to boot. If the server does not boot within the length of time specified by the **set OSBootWatchdogTimerTimeout** command, the CIMC logs an error and takes the action specified by the **set OSBootWatchdogTimerPolicy** command.
OS Watchdog Timer Timeout **set OSBootWatchdogTimerTimeOut**	What timeout value the BIOS uses to configure the watchdog timer. This can be one of the following: • **5_Minutes—**The watchdog timer expires 5 minutes after the OS begins to boot. • **10_Minutes—**The watchdog timer expires 10 minutes after the OS begins to boot. • **15_Minutes—**The watchdog timer expires 15 minutes after the OS begins to boot. • **20_Minutes—**The watchdog timer expires 20 minutes after the OS begins to boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.
OS Watchdog Timer Policy **set OSBootWatchdogTimerPolicy**	What action the system takes if the watchdog timer expires. This can be one of the following: • **Do_Nothing—**The server takes no action if the watchdog timer expires during OS boot. • **Power_Down—**The server is powered off if the watchdog timer expires during OS boot. • **Reset—**The server is reset if the watchdog timer expires during OS boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.

Name	Description
Boot Order Rules **set ManagedBootRule**	How the server changes the boot order list defined through the CIMC GUI or CLI when there are no devices of a particular device type available or when the user defines a different boot order using the server's BIOS Setup Utility. The supported device types are: • **HDD—**Hard disk drive • **FDD—**Floppy disk drive • **CDROM—**Bootable CD-ROM or DVD • **PXE—**PXE boot • **EFI—**Extensible Firmware Interface The Boot Order Rules option can be one of the following: • **Strict—**When no devices of a particular type are available, the system creates a placeholder for that device type in the boot order list. When a device of that type becomes available, it is added to the boot order in the previously defined position. If the user defines a boot order through the server's BIOS Setup Utility, that boot order is given priority over the boot order configured through the CIMC GUI or CLI. All device types defined through CIMC that are not present in the boot order defined through the BIOS Setup Utility are removed from the boot order list. • **Loose—**When no devices of a particular type are available, the system removes that device type from the boot order. When a device of that type becomes available, the system adds it to the end of the boot order list. If the boot order is configured through the server's BIOS Setup Utility, that boot order is given priority over the boot order configured through the CIMC GUI or CLI. All device types defined through CIMC that are not present in the boot order defined through the BIOS Setup Utility are moved to the end of the boot order list.

C460 Servers

Main BIOS Parameters for C460 Servers

Name	Description
POST Error Pause **set POSTErrorPause**	What happens when the server encounters a critical error during POST. This can be one of the following: • **Enabled—**The BIOS pauses the attempt to boot the server and opens the Error Manager when a critical error occurs during POST. • **Disabled—**The BIOS continues to attempt to boot the server.
Boot Option Retry **set BootOptionRetry**	Whether the BIOS retries NON-EFI based boot options without waiting for user input. This can be one of the following: • **Enabled—**Continually retries NON-EFI based boot options without waiting for user input. • **Disabled—**Waits for user input before retrying NON-EFI based boot options.

Advanced BIOS Parameters for C460 Servers

Processor Configuration Parameters

Name	Description
Intel Turbo Boost Technology **set IntelTurboBoostTech**	Whether the processor uses Intel Turbo Boost Technology, which allows the processor to automatically increase its frequency if it is running below power, temperature, or voltage specifications. This can be one of the following: • **Disabled—**The processor does not increase its frequency automatically. • **Enabled—**The processor utilizes Turbo Boost Technology if required.

Name	Description
Enhanced Intel Speedstep Technology **set EnhancedIntelSpeedStep**	Whether the processor uses Enhanced Intel SpeedStep Technology, which allows the system to dynamically adjust processor voltage and core frequency. This technology can result in decreased average power consumption and decreased average heat production. This can be one of the following: • **Disabled—**The processor never dynamically adjusts its voltage or frequency. • **Enabled—**The processor utilizes Enhanced Intel SpeedStep Technology and enables all supported processor sleep states to further conserve power. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Intel Hyper-Threading Technology **set IntelHyperThread**	Whether the processor uses Intel Hyper-Threading Technology, which allows multithreaded software applications to execute threads in parallel within each processor. This can be one of the following: • **Disabled—**The processor does not permit hyperthreading. • **Enabled—**The processor allows for the parallel execution of multiple threads. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Number of Enabled Cores **set CoreMultiProcessing**	Allows you to disable one or more of the physical cores on the server. This can be one of the following: • **All—**Enables all physical cores. This also enables Hyper Threading on the associated logical processor cores. • **1** through ***n*—**Specifies the number of physical processor cores that can run on the server. Each physical core has an associated logical core. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.

Name	Description
Execute Disable **set ExecuteDisable**	Classifies memory areas on the server to specify where application code can execute. As a result of this classification, the processor disables code execution if a malicious worm attempts to insert code in the buffer. This setting helps to prevent damage, worm propagation, and certain classes of malicious buffer overflow attacks. This can be one of the following: • **Disabled—**The processor does not classify memory areas. • **Enabled—**The processor classifies memory areas. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Intel Virtualization Technology **set IntelVT**	Whether the processor uses Intel Virtualization Technology (VT), which allows a platform to run multiple operating systems and applications in independent partitions. This can be one of the following: • **Disabled—**The processor does not permit virtualization. • **Enabled—**The processor allows multiple operating systems in independent partitions. **Note** If you change this option, you must power cycle the server before the setting takes effect.
Intel VT for Directed IO **set IntelVTD**	Whether the processor uses Intel Virtualization Technology for Directed I/O (VT-d). This can be one of the following: • **Disabled—**The processor does not use virtualization technology. • **Enabled—**The processor uses virtualization technology.
Intel VT-d Interrupt Remapping **set InterruptRemap**	Whether the processor supports Intel VT-d Interrupt Remapping. This can be one of the following: • **Disabled—**The processor does not support remapping. • **Enabled—**The processor uses VT-d Interrupt Remapping as required.
Intel VT-d Coherency Support **set CoherencySupport**	Whether the processor supports Intel VT-d Coherency. This can be one of the following: • **Disabled—**The processor does not support coherency. • **Enabled—**The processor uses VT-d Coherency as required.

Name	Description
Intel VT-d Address Translation Services **set ATS**	Whether the processor supports Intel VT-d Address Translation Services (ATS). This can be one of the following: • **Disabled—**The processor does not support ATS. • **Enabled—**The processor uses VT-d ATS as required.
Intel VT-d PassThrough DMA **set PassThroughDMA**	Whether the processor supports Intel VT-d Pass-through DMA. This can be one of the following: • **Disabled—**The processor does not support pass-through DMA. • **Enabled—**The processor uses VT-d Pass-through DMA as required.
Direct Cache Access **set DirectCacheAccess**	Allows processors to increase I/O performance by placing data from I/O devices directly into the processor cache. This setting helps to reduce cache misses. This can be one of the following: • **Disabled—**Data from I/O devices is not placed directly into the processor cache. • **Enabled—**Data from I/O devices is placed directly into the processor cache.
Processor C3 Report **set ProcessorC3Report**	Whether the BIOS sends the C3 report to the operating system. When the OS receives the report, it can transition the processor into the lower C3 power state to decrease energy usage while maintaining optimal processor performance. This can be one of the following: • **Disabled—**The BIOS does not send the C3 report. • **ACPI_C2—**The BIOS sends the C3 report using the ACPI C2 format, allowing the OS to transition the processor to the C3 low power state. • **ACPI_C3—**The BIOS sends the C3 report using the ACPI C3 format, allowing the OS to transition the processor to the C3 low power state.

Name	Description
Processor C6 Report **set ProcessorC6Report**	Whether the BIOS sends the C6 report to the operating system. When the OS receives the report, it can transition the processor into the lower C6 power state to decrease energy usage while maintaining optimal processor performance. This can be one of the following: • **Disabled—**The BIOS does not send the C6 report. • **Enabled—**The BIOS sends the C6 report, allowing the OS to transition the processor to the C6 low power state.
Package C State Limit **set PackageCStateLimit**	The amount of power available to the server components when they are idle. This can be one of the following: • **C0_state—**The server provides all server components with full power at all times. This option maintains the highest level of performance and requires the greatest amount of power. • **C1_state—**When the CPU is idle, the system slightly reduces the power consumption. This option requires less power than C0 and allows the server to return quickly to high performance mode. • **C3_state—**When the CPU is idle, the system reduces the power consumption further than with the C1 option. This requires less power than C1 or C0, but it takes the server slightly longer to return to high performance mode. • **C6_state—**When the CPU is idle, the system reduces the power consumption further than with the C3 option. This option saves more power than C0, C1, or C3, but there may be performance issues until the server returns to full power. • **C7_state—**When the CPU is idle, the server makes a minimal amount of power available to the components. This option saves the maximum amount of power but it also requires the longest time for the server to return to high performance mode. • **No_Limit—**The server may enter any available C state. **Note** This option is used only if **CPU C State** is enabled.

Name	Description
CPU C State **set ProcessorCcxEnable**	Whether the system can enter a power savings mode during idle periods. This can be one of the following: • **Disabled—**The system remains in high performance state even when idle. • **Enabled—**The system can reduce power to system components such as the DIMMs and CPUs. The amount of power reduction is specified by the **set PackageCStateLimit** command.
C1E **set ProcessorC1eEnable**	Whether the CPU transitions to its minimum frequency when entering the C1 state. This can be one of the following: • **Disabled—**The CPU continues to run at its maximum frequency in C1 state. • **Enabled—**The CPU transitions to its minimum frequency. This option saves the maximum amount of power in C1 state. **Note** This option is used only if **ProcessorCcxEnable** is enabled.

Memory Configuration Parameters

Name	Description
Select Memory RAS **set SelectMemoryRAS**	How the memory reliability, availability, and serviceability (RAS) is configured for the server. This can be one of the following: • **Maximum_Performance—**System performance is optimized. • **Mirroring—**System reliability is optimized by using half the system memory as backup. • **Sparing—**The system reserves some memory for use in the event a DIMM fails. If that happens, the server takes the DIMM offline and replaces it with the reserved memory. This option provides less redundancy than mirroring, but it leaves more of the memory available for programs running on the server.

Name	Description
NUMA Optimized **set NUMAOptimize**	Whether the BIOS supports NUMA. This can be one of the following: • **Disabled—**The BIOS does not support NUMA. • **Enabled—**The BIOS includes the ACPI tables that are required for NUMA-aware operating systems. If you enable this option, the system must disable Inter-Socket Memory interleaving on some platforms.
Sparing Mode **set SparingMode**	The sparing mode used by the CIMC. This can be one of the following: • **Rank_Sparing—**The spared memory is allocated at the rank level. • **DIMM Sparing—**The spared memory is allocated at the DIMM level. **Note** This option is used only if **set SelectMemoryRAS** is set to **Sparing**.
Mirroring Mode **set MirroringMode**	Mirroring is supported across Integrated Memory Controllers (IMCs) where one memory riser is mirrored with another. This can be one of the following: • **Intersocket—**Each IMC is mirrored across two sockets. • **Intrasocket—**One IMC is mirrored with another IMC in the same socket. **Note** This option is used only if **SelectMemoryRAS** is set to **Mirroring**.
Patrol Scrub **set PatrolScrub**	Whether the system actively searches for, and corrects, single bit memory errors even in unused portions of the memory on the server. This can be one of the following: • **Disabled—**The system checks for memory ECC errors only when the CPU reads or writes a memory address. • **Enabled—**The system periodically reads and writes memory searching for ECC errors. If any errors are found, the system attempts to fix them. This option may correct single bit errors before they become multi-bit errors, but it may adversely affect performance when the patrol scrub is running.

Name	Description
Patrol Scrub Interval **set PatrolScrubDuration**	Controls the time interval between each patrol scrub memory access. A lower interval scrubs the memory more often but requires more memory bandwidth. Select a value between 5 and 23. The default value is 8. **Note** This option is used only if **Patrol Scrub** is enabled.
CKE Low Policy **set CkeLowPolicy**	Controls the DIMM power savings mode policy. This can be one of the following: • **Disabled—**DIMMs do not enter power saving mode. • **Slow—**DIMMs can enter power saving mode, but the requirements are higher. Therefore, DIMMs enter power saving mode less frequently. • **Fast—**DIMMs enter power saving mode as often as possible. • **Auto—**The BIOS controls when a DIMM enters power saving mode based on the DIMM configuration.

Serial Port Configuration Parameters

Name	Description
Serial A Enable **set Serial-PortA**	Whether serial port A is enabled or disabled. This can be one of the following: • **Disabled—**The serial port is disabled. • **Enabled—**The serial port is enabled.

USB Configuration Parameters

Name	Description
Make Device Non-Bootable **set MakeUSBDeviceNonBootable**	Whether the server can boot from a USB device. This can be one of the following: • **Disabled—**The server can boot from a USB device. • **Enabled—**The server cannot boot from a USB device.

PCI Configuration Parameters

Name	Description
Memory Mapped I/O Above 4GB **set MemoryMappedIOAbove4GB**	Whether to enable or disable memory mapped I/O of 64-bit PCI devices to 4GB or greater address space. Legacy option ROMs are not able to access addresses above 4GB. PCI devices that are 64-bit compliant but use a legacy option ROM may not function correctly with this setting enabled. This can be one of the following: • **Disabled—**The server does not map I/O of 64-bit PCI devices to 4GB or greater address space. • **Enabled—**The server maps I/O of 64-bit PCI devices to 4GB or greater address space.
Onboard NIC *n* ROM **set NIC-*n*-ROM**	Whether the system loads the embedded PXE option ROM for the onboard NIC designated by ***n***. This can be one of the following: • **Disabled—**PXE option ROM is not available for NIC ***n***. • **Enabled—**PXE option ROM is available for NIC ***n***.
PCIe OptionROMs **set PciOptRomsDisable**	Whether the server can use the PCIe Option ROM expansion slots. This can be one of the following: • **Disabled—**PCIe Option ROMs are not available. • **Enabled—**PCIe Option ROMs are available. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.
PCIe Slot *n* ROM **set Slot-*n*-ROM**	Whether PCIe expansion slot ***n*** is available to the server. This can be one of the following: • **Disabled—**The expansion slot ***n*** is not available. • **Enabled—**The expansion slot ***n*** is available. • **UEFI_Only—**The expansion slot ***n*** is available for UEFI only. • **Legacy_Only—**The expansion slot ***n*** is available for legacy only.

Name	Description
Onboard Gbit LOM **set OnboardNic1**	Whether Gbit LOM is enabled or disabled on the server. This can be one of the following: • **Disabled—**Gbit LOM is not available. • **Enabled—**10Git LOM is available.
Onboard 10Gbit LOM **set OnboardNic2**	Whether 10Gbit LOM is enabled or disabled on the server. This can be one of the following: • **Disabled—**10GBit LOM is not available. • **Enabled—**10GBit LOM is available.
Sriov **set SrIov**	Whether SR-IOV (Single Root I/O Virtualization) is enabled or disabled on the server. This can be one of the following: • **Disabled—**SR-IOV is disabled. • **Enabled—**SR-IOV is enabled.
IOH Resource Allocation **set IOHResource**	Enables you to distribute 64KB of 16-bit IO resources between IOH0 and IOH1 as per system requirement. This can be one of the following: • **IOH0 24k IOH1 40k—** Allocates 24KB of 16-bit IO resources to IOH0 and 40KB of 16-bit IO resources to IOH1. • **IOH0 32k IOH1 32k—** Allocates 32KB of 16-bit IO resources to IOH0 and 32KB of 16-bit IO resources to IOH1. • **IOH0 40k IOH1 24k—** Allocates 40KB of 16-bit IO resources to IOH0 and 24KB of 16-bit IO resources to IOH1. • **IOH0 48k IOH1 16k—** Allocates 48KB of 16-bit IO resources to IOH0 and 16KB of 16-bit IO resources to IOH1. • **IOH0 56k IOH1 8k—** Allocates 56KB of 16-bit IO resources to IOH0 and 8KB of 16-bit IO resources to IOH1.

Server Management BIOS Parameters for C460 Servers

Name	Description
Assert NMI on SERR **set AssertNMIOnSERR**	Whether the BIOS generates a non-maskable interrupt (NMI) and logs an error when a system error (SERR) occurs. This can be one of the following: • **Disabled—**The BIOS does not generate an NMI or log an error when a SERR occurs. • **Enabled—**The BIOS generates an NMI and logs an error when a SERR occurs. You must enable this setting if you want to enable **Assert_NMI_on_PERR**.
Assert NMI on PERR **set AssertNMIOnPERR**	Whether the BIOS generates a non-maskable interrupt (NMI) and logs an error when a processor bus parity error (PERR) occurs. This can be one of the following: • **Disabled—**The BIOS does not generate an NMI or log an error when a PERR occurs. • **Enabled—**The BIOS generates an NMI and logs an error when a PERR occurs. You must enable **Assert_NMI_on_SERR** to use this setting.
Console Redirection **set ConsoleRedir**	Allows a serial port to be used for console redirection during POST and BIOS booting. After the BIOS has booted and the operating system is responsible for the server, console redirection is irrelevant and has no effect. This can be one of the following: • **Disabled—**No console redirection occurs during POST. • **Serial_Port_A—**Enables console redirection on serial port A during POST. **Note** If you enable this option, you also disable the display of the Quiet Boot logo screen during POST.
Flow Control **set FlowCtrl**	Whether a handshake protocol is used for flow control. Request to Send / Clear to Send (RTS/CTS) helps to reduce frame collisions that can be introduced by a hidden terminal problem. This can be one of the following: • **None—**No flow control is used. • **RTS-CTS—**RTS/CTS is used for flow control. **Note** This setting must match the setting on the remote terminal application.

Name	Description
Baud Rate **set BaudRate**	What BAUD rate is used for the serial port transmission speed. If you disable Console Redirection, this option is not available. This can be one of the following: • **9.6k—**A 9600 BAUD rate is used. • **19.2k—**A 19200 BAUD rate is used. • **38.4k—**A 38400 BAUD rate is used. • **57.6k—**A 57600 BAUD rate is used. • **115.2k—**A 115200 BAUD rate is used. **Note** This setting must match the setting on the remote terminal application.
Terminal Type **set TerminalType**	What type of character formatting is used for console redirection. This can be one of the following: • **PC-ANSI—**The PC-ANSI terminal font is used. • **VT100—**A supported vt100 video terminal and its character set are used. • **VT100-PLUS—**A supported vt100-plus video terminal and its character set are used. • **VT-UTF8—**A video terminal with the UTF-8 character set is used. **Note** This setting must match the setting on the remote terminal application.
OS Boot Watchdog Timer Timeout **set OSBootWatchdogTimerTimeOut**	What timeout value the BIOS uses to configure the watchdog timer. This can be one of the following: • **5_Minutes—**The watchdog timer expires 5 minutes after the OS begins to boot. • **10_Minutes—**The watchdog timer expires 10 minutes after the OS begins to boot. • **15_Minutes—**The watchdog timer expires 15 minutes after the OS begins to boot. • **20_Minutes—**The watchdog timer expires 20 minutes after the OS begins to boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.

Name	Description
OS Boot Watchdog Policy **set OSBootWatchdogTimerPolicy**	What action the system takes if the watchdog timer expires. This can be one of the following: • **Power_Off—**The server is powered off if the watchdog timer expires during OS boot. • **Reset—**The server is reset if the watchdog timer expires during OS boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.
Legacy OS Redirection **set LegacyOSRedir**	Whether redirection from a legacy operating system, such as DOS, is enabled on the serial port. This can be one of the following: • **Disabled—**The serial port enabled for console redirection is hidden from the legacy operating system. • **Enabled—**The serial port enabled for console redirection is visible to the legacy operating system.
OS Boot Watchdog Timer **set OSBootWatchdogTimer**	Whether the BIOS programs the watchdog timer with a specified timeout value. This can be one of the following: • **Disabled—**The watchdog timer is not used to track how long the server takes to boot. • **Enabled—**The watchdog timer tracks how long the server takes to boot. If the server does not boot within the length of time specified by the **set OSBootWatchdogTimerTimeout** command, the CIMC logs an error and takes the action specified by the **set OSBootWatchdogTimerPolicy** command.