Processor

Processor

The following table lists the Processor BIOS settings that you can configure through a BIOS policy or the default BIOS settings:

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
PRMRR Size	Processor Reserved Memory Range Registers (PRMRR) is the size of the protected region in the systems DRAM.	4.3(2)	X210c M7, X410c M7, C220M7, C240M7, C220M6, C240M6, C220 M7, C240 M7, X210c M7, X410c M7	Invalid Config, 128M, **256M**, 512M,1G, 2G, 4G, 8G, 16G, 32G, 64G, 128G, 256G, 512G	
Adjacent Cache Line Prefetcher	Whether the processor fetches cache lines in even/odd pairs instead of fetching just the required line.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, B200 M6, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled • Disabled—This option is Disabled. • Enable—This options is enabled.	**CPU Performance** must be set to **Custom** in order to specify this value. For any value other than **Custom**, this option is overridden by the setting in the selected CPU performance profile.

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
Altitude	The approximate number of meters above sea level at which the physical server is installed.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6	**Auto**, 300, 900, 1500, 3000 • Auto—The CPU determines the physical elevation. • *.n* M, where *n* is 300, 900, 1500, 3000—The server is approximately *n* meters above sea level.	
Autonomous Core C State	Enables CPU Autonomous C-State, which converts the HALT instructions to the MWAIT instructions.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	
CPU Autonomous C State	This enables or disables CPU Autonomous state.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6	**Disabled**, Enabled	
Boot Performance Mode	Allows the user to select the BIOS performance state that is set before the operating system handoff.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
Burst and Postponed Refresh	Allows the memory controller to defer the refresh cycles when the memory is active and accomplishes the refresh within a specified window. The deferred refresh cycles may run in a burst of several refresh cycles.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	C225 M6, C245 M6	**Disabled**, Enabled	It is recommended to leave this setting in the default state of **Disabled** to mitigate Rowhammer-style attacks.
APBDIS	Allows you to select the Algorithm Performance Boost (APB) Disable value for the SMU.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	C225 M6, C245 M6	**Auto**, 0, 1 • **Auto**—Sets an auto ApbDis for the SMU. This is the default option. • **0**—Clear ApbDis to SMU • **1**—Set ApbDis to SMU	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
Downcore Control	Provides the ability to remove one or more cores from operation is supported in the silicon. It may be desirable to reduce the number of cores due to OS restrictions, or power reduction requirements of the system. This item allows the control on the number of cores that are running. This setting can only reduce the number of cores from only those available in the processor.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6	**Auto**, Two (2+0), Two (1+1), Three (3+0), Six (3+3), Four (2+2), Four (2+0) • **Auto**—The CPU determines how many cores need to be enabled. This is the default option. • **Two (2+0)(1+1)**—Two cores enabled on one CPU complex. • **Three (3+0)**—Three cores enabled on one CPU complex. • **Four (4+0)(2+2)**—Four cores enabled on one CPU complex. • **Six (3+3)**—Six cores enabled on one CPU complex.	This token is applicable only for the servers with 7xx2 and 7xx3 Model processors.

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
Streaming Stores Control	Enables the streaming stores functionality.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6	**Auto**, Disabled, Enabled	
Fixed SOC P-State	This option defines the target P-state when APBDIS (to disable Algorithm Performance Boost (APB)) is set. The **P-x** specify a valid P-state for the processor installed.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6	**Auto**, P0, P1, P2, P3 • **Auto**—Sets a valid P-state suitable for the processor. This is the default option. • **P0 to P3**—Hard sets SOC P-state to highest performing to lowest performing SOC P-state.	
DF C-States	When long duration idleness is expected in a system, this control allows the system to transition into a DF Cstate which can set the system into an even lower power state.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6	**Auto**, Disabled, Enabled	
CCD Control	Allows you to specify the number of charge-coupled device CCDs that are desired to be enable in the system.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	C225 M6, C245 M6	**Auto**, Disabled, Enabled	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
CPU Downcore control	Provides the ability to remove one or more cores from operation is supported in the silicon. It may be desirable to reduce the number of cores due to OS restrictions, or power reduction requirements of the system. This item allows the control on the number of cores that are running. This setting can only reduce the number of cores from only those available in the processor.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6	**Auto**, Disabled, Enabled	
CPU SMT Mode	Simultaneous multithreading (SMT) is a processor technology that allows multiple instruction streams (threads) to run concurrently on the same physical processor, improving overall throughput.	4.2(1)	C225 M6, C245 M6	Disabled, **Enabled**	
ACPI SRAT L3 Cache As NUMA Domain	Creates a layer of virtual domains on top of the physical domains in which each CCX is declared to be in its on domain.	4.2(1)	C225 M6, C245 M6	**Auto**, Disabled, Enabled	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
Channel Interleaving	Whether the CPU divides memory blocks and spreads contiguous portions of data across interleaved channels to enable simultaneous read operations.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6	**Auto**, 1-way to 4-way	
Cisco xGMI Max Speed	This option enables 18 Gbps XGMI link speed.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	C225 M6, C245 M6	**Disabled**, Enabled	
Closed Loop Thermal Throttling	To configure Closed Loop Thermal Throttling	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6	**Disabled**, Enabled	
Processor CMCI	Enables CMCI generation.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	
Config TDP	To configure TDP.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6	**Disabled**, Enabled	
Configurable TDP Level	Allows you to set customized value for Thermal Design Power (TDP).	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Normal**, Level 1, Level 2	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
Core Multi Processing	Sets the state of logical processor cores per CPU in a package. If you choose All as the value, Intel Hyper Threading technology is also enabled.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1), 5.0(1), 5.0(2)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6, B200 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7	**All**, 1 through 64 • All—Enables multiprocessing on all logical processor cores. • 1 through 64—Specifies the number of logical processor cores per CPU that can run on the server. To disable multiprocessing and have only one logical processor core per CPU running on the server, choose 1	We recommend that you contact your operating system vendor to make sure your operating system supports this feature.
Energy Performance	Allows you to determine whether system performance or energy efficiency is more important on this server.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Performance** , Balanced Performance, Balanced Energy, Energy Efficient	**Power Technology** must be set to **Custom** or the server ignores the setting for this parameter.
Frequency Floor Override	Whether the CPU is allowed to drop below the maximum non-turbo frequency when idle.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6	**Disabled**, Enabled	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
CPU Performance	CPU performance by adjusting server settings automatically.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, B200 M6, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	
Power Technology	Enables you to configure the CPU power management settings for Enhanced Intel Speedstep Technology, Intel Turbo Boost Technology and Processor Power State C6.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, B200 M6, C220 M6, C240 M6	**Disabled**, Energy efficient, Custom, Performance	
Demand Scrub	Whether the system corrects single bit memory errors encountered when the CPU or I/O makes a demand read.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6	**Disabled**, Enabled	
Direct Cache Access Support	Allows processors to increase I/O performance by placing data from I/O devices directly into the processor cache. This setting helps to reduce cache misses.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6	**Auto**, Disabled, Enabled	
DRAM Clock Throttling	Allows you to tune the system settings between the memory bandwidth and power consumption.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6	**Auto**, Balanced, Performance, Energy Efficient	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
Energy Efficient Turbo	When energy efficient turbo is enabled, the optimal turbo frequency of the CPU turns dynamic based on CPU utilization. The power/performance bias setting also influences energy efficient turbo.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, B200 M6, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	
Energy Performance Tuning	Determines if the BIOS or Operating System can turn on the energy performance bias tuning. The options are BIOS and OS.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6	**Disabled**, Enabled	
Enhanced Intel Speedstep(R) Technology	Whether the processor uses Enhanced Intel SpeedStep Technology, which allows the system to dynamically adjust processor voltage and core frequency. This technology can result in decreased average power consumption and decreased average heat production.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	
Processor EPP Enable	Allows you to determine whether system performance or energy efficiency is more important on this server.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6	**Disabled**, Enabled	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
EPP Profile	Allows you to determine whether system performance or energy efficiency is more important on this server.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	
Execute Disable Bit	Classifies memory areas on the server to specify where the application code can execute. As a result of this classification, the processor disables code execution if a malicious worm attempts to insert code in the buffer. This setting helps to prevent damage, worm propagation, and certain classes of malicious buffer overflow attacks.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6, X210c M6	**Disabled**, Enabled	
Local X2 Apic	Allows you to set the type of Advanced Processor Interrupt controller (APIC) architecture.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled, X2APIC, XAPIC	
Hardware Prefetcher	Whether the processor allows the Intel hardware prefetcher to fetch streams of data and instruction from memory into the unified second-level cache when necessary.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
CPU Hardware Power Management	nables processor Hardware Power Management (HWPM).	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, HWPM Native Mode, HWPM OOB Mode	
IMC Interleaving	This BIOS option controls the interleaving between the Integrated Memory Controllers (IMCs).	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6	**Auto**, 1-way Interleave, 2-way Interleave	
Intel Dynamic Speed Select	Intel Dynamic Speed Select modes allow you to run the CPU with different speed and cores in auto mode.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 5.0(1), 5.0(2)	All M5 servers, B200 M6, C220 M6, C240 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	
Intel HyperThreading Tech	Whether the processor uses Intel Hyper-Threading Technology, which allows multithreaded software applications to execute threads in parallel within each processor.	4.0(2), 4.0(4), 4.1(1), 4.1(3)	All M5 servers, B200 M6, C220 M6, C240 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 servers	**Disabled**, Enabled	
Intel Turbo Boost Tech	Whether the processor uses Intel Turbo Boost Technology, which allows the processor to automatically increase its frequency if it is running below power, temperature, or voltage specifications.	4.0(2), 4.0(4), 4.1(1), 4.1(3),	All M5 servers, B200 M6, C220 M6, C240 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 servers	**Disabled**, Enabled	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
Intel(R) VT	Whether the processor uses Intel Virtualization Technology for Directed I/O (VT-R)	4.0(2), 4.0(4), 4.1(1), 4.1(3)	All M5 servers, B200 M6, C220 M6, C240 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 servers	**Disabled**, Enabled	
DCU IP Prefetcher	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache.	4.0(2), 4.0(4), 4.1(1), 4.1(3)	All M5 servers, B200 M6, C220 M6, C240 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 servers	**Disabled**, Enabled	
KTI Prefetch	KTI prefetch is a mechanism to get the memory read started early on a DDR bus.	4.0(2), 4.0(4), 4.1(1), 4.1(3)	All M5 servers, B200 M6, C220 M6, C240 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 servers	**Disabled**, Enabled	
LLC Prefetch	Whether the processor uses the LLC Prefetch mechanism to fetch the date into the LLC.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, B200 M6, C220 M6, C240 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 servers.	**Disabled**, Enabled	
Intel Memory Interleaving	Whether the CPU interleaves the physical memory so that the memory can be accessed while another is being refreshed.	4.0(2), 4.0(4), 4.1(1), 4.1(3)	All M5 servers	**Disabled**, Enabled	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
Package C State Limit	The amount of power available to the server components when they are idle.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, B200 M6, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	No Limit, Auto, **C0 C1 State**, C2, C6 Non Retention, C6 Retention	If you are changing the **Package C State Limit** token then ensure that the **Power Technology** is set to **Custom**.

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
Patrol Scrub	It sets the interval for a full memory scan.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, B200 M6, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled • Enable—The system periodically reads and writes memory searching for ECC errors. If any errors are found, the system attempts to fix them. This option may correct single bit errors before they become multi-bit errors, but it may adversely affect performance when the patrol scrub is running. • Disable—The system checks for memory ECC errors only when the CPU reads or writes a memory address.	The lower the interval, the more memory bandwidth is used for scrubbing.

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
Patrol Scrub Interval	Whether the system actively searches for, and corrects, single bit memory errors even in unused portions of the memory on the server at an interval of 5 to 23 hours.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6	Platform default	
Processor C1E	Allows the processor to transition to its minimum frequency upon entering C1. This setting does not take effect until after you have rebooted the server.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	
Processor C3 Report	Whether the processor sends the C3 report to the operating system.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6	**Disabled**, Enabled, ACPI C2, ACPI C3	
Processor C6 Report	Whether the processor sends the C6 report to the operating system.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	
CPU C State	Whether the AMD processors control IO-based C-state generation and DF C-states.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	C225 M5, C245 M5	**Auto**, Disabled, Enabled	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
P-STATE Coordination **Note** It is also called EIST PSD Function in UCSM.	Allows you to define how BIOS communicates the P-state support model to the operating system. There are 3 models as defined by the Advanced Configuration and Power Interface (ACPI) specification.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C225 M6, C245 M6, C220 M7, C240 M7, X210c M7, X410c M7	**SW All**, HW All, SW Any	**Power Technology** must be set to **Custom** or the server ignores the setting for this parameter.
Power Performance Tuning	Determines if the BIOS or Operating System can turn on the energy performance bias tuning. The options are BIOS and OS.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1), C220 M7, C240 M7	All M5 servers, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	BIOS, **OS**, PECI	
UPI Link Frequency Select	Allows you to select different UPI link frequency running.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1), 5.0(1), 5.0(2)	All M5 servers, C220 M6, C240 M6, B200 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7	**Auto**, 9.6GT/S, 10.4GT/S, 11.2GT/S, 12.8GT/s, 14.4GT/s, 16.0GT/s, 20.0GT/s	
Rank Interleaving	Whether the CPU interleaves physical ranks of memory so that one rank can be accessed while another is being refreshed	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6	**Auto**, 1-way, 2-way, 4-way, 8-way	
SMT Mode	Whether the processor uses AMD Simultaneous MultiThreading Technology, which allows multithreaded software applications to execute threads in parallel within each processor.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	C225 M6, C245 M6	**Disabled**, Enabled	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
Sub Numa Clustering	Whether the CPU supports sub NUMA clustering, in which the tag directory and the memory channel are always in the same region.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled, SNC2, SNC4	
DCU Streamer Prefetch	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	
SVM Mode	Whether the processor uses AMD Secure Virtual Machine Technology.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	C225 M6, C245 M6	**Disabled**, Enabled	
Uncore Frequency Scaling	Allows you configure the scaling of the uncore frequency of the processor.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1), 5.0(1), 5.0(2)	All M5 servers, C220 M6, C240 M6, B200 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7	Disabled, **Enabled**	
Workload Configuration	This feature allows for workload optimization.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	Balanced, **IO Sensitive**, NUMA, UMA	
XPT Prefetch	Whether XPT prefetch is used to enable a read request sent to the last level cache to issue a copy of that request to the memory controller prefetcher.	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1)	All M5 servers, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	

Name	Description	Supported Attributes			
		Versions	Platforms	Values	Dependencies
X2APIC Opt-Out Flag	Prevents the OS from enabling extended xAPIC (x2APIC) mode when the OS is not working with x2APIC.	4.2(3)	C220M6, C240M6, B200M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7	**Disabled**, Enabled	
Intel Speed Select	Allows you to adjust different core to operate in different frequency to have a better power efficiency. The values **Config 1** and **Config 2** are not supported on Cisco UCS M6 and M7 servers. For Cisco UCS M6 and Cisco UCS M7 servers, the values **Config 3** and **Config 4** (4th Gen Intel Xeon Scalable processors and 5th Gen Intel Xeon Scalable processors) are equivalent to the values **Config 1** and **Config 2** (3rd Gen Intel Xeon Scalable processors).	4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1), 5.0(1), 5.0(2), 4.2(3)	C220M6, C240M6, B200M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7	**Auto**, Base, Config 1, Config 2, Config 3, Config 4	

Processor