# Memory



## Memory

The following table lists the memory BIOS settings that you can configure through a BIOS policy or the default BIOS settings:

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Enhanced Memory Test** | Enables enhanced memory tests during the system boot and increases the boot time based on the memory. | 4.0 (1), 4.0(2), 4.0(4), 4.1(1), 4.2(1), 5.0(1), 5.0(2) | C220 M5, C240 M5, B200 M6, C220 M6,C240 M6, C225 M6, C245 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | Disabled, Enabled, **Auto**<br>• **Disabled**—Options are Disabled.<br>• **Enabled**—Options are enabled.<br>• **Auto**—Option is in auto mode. | It is recommended to leave this setting in the default state of Auto. |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **BME DMA Mitigation** | Allows you to disable the PCI BME bit to mitigate the threat from an unauthorized external DMA | 4.0 (1), 4.0(2), 4.0(4), 4.1(1), 4.2(1) | C220 M5, C240 M5, B200 M6, C240 M6, C225 M6, C245 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | Enabled, **Disabled**<br>• Disabled—Option is not restricted.<br>• Enabled—Option is restricted. | |
| **Burst and Postponed Refresh** | Allows the memory controller to defer the refresh cycles when the memory is active and accomplishes the refresh within a specified window. The deferred refresh cycles may run in a burst of several refresh cycles. | 4.0 (1), 4.0(2), 4.0(4), 4.1(1), 4.2(1) | C225 M6 and C245 M6 | Enabled, **Disabled**<br>• Disabled—Option is not restricted.<br>• Enabled—Option is restricted. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **CPU SMEE** | Whether the processor uses the Secure Memory Encryption Enable (SMEE) function, which provides memory encryption support. | 4.0(2), 4.0(4), 4.1(1), 4.2(1) | C125 M6, C225 M6, C245 M6 | Disabled, **Enabled**, Auto<br>• Disabled—Options are Disabled.<br>• Enabled—Options are enabled.<br>• **Auto**—Option is in auto mode. | |
| **IOMMU** | Input Output Memory Management Unit(IOMMU) allows AMD processors to map virtual addresses to physical addresses. | 4.0(2), 4.0(4), 4.1(1), 4.2(1) | C125 M6, C225 M6, C245 M6 | Disabled, Enabled, **Auto**<br>• Disabled—Options are Disabled.<br>• Enabled—Options are enabled.<br>• Auto—Option is in auto mode. | |
| **Bank Group Swap** | Determines how physical addresses are assigned to applications. | 4.0 (1), 4.0(4), 4.1(1)4.2(10 | C125 M5, C225 M6, C245 M6 | Disabled, Enabled, **Auto**<br>• Disabled—Options are Disabled.<br>• Enabled—Options are enabled.<br>• Auto—Option is in auto mode. | |
| **Chipset Interleave** | Whether memory blocks across the DRAM chip selects for node 0 are interleaved. | 4.2(1) | C225 M6, C245 M6 | Disabled, Enabled, **Auto**<br>• Disabled—Options are Disabled.<br>• Enabled—Options are enabled.<br>• Auto—Option is in auto mode. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **SNP Memory Coverage** | This option selects the operating mode of the Secured Nested Paging (SNP) Memory and the reverse Map Table (RMP). The RMP is used to ensure a one-to-one mapping between system physical addresses and guest physical addresses. | 4.2(1) | C225 M6, C245 M6 | Disabled, Enabled, **Auto**<br>• Disabled—Options are Disabled.<br>• Enabled—Options are enabled.<br>• Auto—Option is in auto mode. | |
| **SNP Memory Size to Cover in MiB** | Allows you to configure SNP memory size. | 4.2(1) | C225 M6, C245 M6 | Disabled, Enabled, **Auto**<br>• Disabled—Options are Disabled.<br>• Enabled—Options are enabled.<br>• Auto—Option is in auto mode. | |
| **NUMA Nodes per Socket** | Enables or disables MMIO above 4GB or not. | 4.2(1) | C225 M6, C245 M6 | **Auto**, NPS0, NPS1, NPS2, NPS4<br>• NPS0—Zero NUMA node per socket.<br>• NPS1—One NUMA node per socket.<br>• NPS2—Two NUMA node per socket.<br>• NPS4—Four NUMA node per socket.<br>• Auto—Number of channels are set to auto. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **AMD Memory Interleaving** | Determines the memory blocks to be interleaved. It also determines the starting address of the interleave (bit 8,9,10 or 11). | 4.0(2), 4.0(4), 4.1(1) | C125 M5 | **Auto**, Channel, Die, none, Socket | |
| **AMD Memory Interleaving Size** | Determines the size of the memory blocks to be interleaved. It also determines the starting address of the interleave (bit 8,9,10 or 11). | 4.0(2), 4.0(4), 4.1(1) | C125 M5 | 1 KB, 2 KB, 256 Bytes, 512 Bytes, **Auto** | |
| **SEV-SNP Support** | Allows you to enable Secure Nested Paging feature. | 4.2(1) | C225 M6, C245 M6 | **Disabled**, Enabled<br>• Disabled—Options are Disabled.<br>• Enabled—Options are enabled. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **CR QoS** | Prevents DRAM and overall system BW drop in the presence of concurrent DCPMM BW saturating threads, with minimal impact to homogenous DDRT-only usages, Good for multi-tenant use cases, VMs, etc. Targeted for App Direct, but also improves memory mode. Targets the "worst-case" degradations. | 4.1(2), 4.2(1), 5.0(1), 5.0(2) | C220 M5, C240 M5, C220 M6, C240 M6 servers, B200 M6, and X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | **Disabled**, Recipe 1, Recipe 2, Recipe 3, Mode 0, Mode 1, Mode 2<br>• Disabled—Feature disabled.<br>• Recipe 1—6 modules, 4 modules per socket optimized<br>• Recipe 2—2 modules per socket optimized<br>• Recipe 3—1 module per socket optimized<br>• Mode 0 - Disable the PMem QoS Feature<br>• Mode 1 - M2M QoS Enable;CHA QoS Disable<br>• Mode 2 - M2M QoS Enable;CHA QoS Enable | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **CR FastGo Config** | CR FastGo Config improves DDRT non-temporal write bandwidth when FastGO is disabled. When FastGO is enabled, it gives faster flow of NT writes into the uncore, When FastGO is disabled, it lessens NT writes queueing up in the CPU uncore, thereby improving sequentially at DCPMM, resulting in improved bandwidth. | 4.1(2), 4.2(1), 5.0(1), 5.0(2) | C220 M5, C240 M5, C220 M6, C240 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | **Auto**, Option 1—5, Enable Optimization, Disable Optimization | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **DCPMM Firmware Downgrade** | To configure DCPMM Firmware Downgrade. | 4.0 (1), 4.0(2), 4.0(4), 4.1(1), 4.2(1) | B480 M5, C220 M5, C240 M5, C480 M5, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7 servers | **Disabled**, Enabled<br>• Disabled—Options are Disabled.<br>• Enabled—Options are enabled. | |
| **DRAM Refresh Rate** | To configure the refresh interval rate for internal memory. | 4.0 (1), 4.0(2), 4.0(4), 4.1(1), 4.2(1) | C125 M5 | Auto, 1x, **2x**, 3x, 4x | |
| **DRAM SW Thermal Throttling** | To configure DRAM SW thermal throttling. | 4.0 (1), 4.0(2), 4.0(4), 4.1(1) | C125 M5 | Disabled, Enabled<br>• Disabled—Options are Disabled.<br>• Enabled—Options are enabled. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **eADR Support** | Extended asynchronous DRAM refresh (eADR) ensures that CPU caches lines with data are flushed at the right time and in the desired order and are also included in the power fail protected domain. | 4.2(1), 5.0(1), 5.0(2) | B200 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | **Disabled**, Enabled, Auto<br>• Disabled—Options are Disabled.<br>• Enabled—Options are enabled.<br>• Auto—Option is in auto mode. | |
| **Low Voltage DDR Mode** | Whether the system prioritizes low voltage or high frequency memory operations. | 4.0 (1), 4.0(2), 4.0(4), 4.1(1) | All M5 servers | **Auto**, Power Saving Mode, Performance Mode<br>• Auto—The CPU determines whether to prioritize low voltage or high frequency memory operations.<br>• Power Saving Mode—The system prioritizes low voltage memory operations over high frequency memory operations. This mode may lower memory frequency in order to keep the voltage low<br>• Performance Mode—The system prioritizes high frequency operations over low voltage operations<br>• Auto—Option is in auto mode. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Memory Bandwidth Boost** | Allows to boost the memory bandwidth. | 4.2(1), 5.0(1), 5.0(2) | C220 M6, C240 M6, B200 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | Disabled, Enabled<br>• Disabled—Options are Disabled.<br>• Enabled—Options are enabled. | |
| **Memory Refresh Rate** | Controls the refresh rate of the memory controller and might affect the memory performance and power depending on memory configuration and workload. | 4.0(2), 4.0(4), 4.1(1), 4.2(1), 5.0(1), 5.0(2) | C220 M5, C240 M5, B200 M6, C220 M6, C240 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | 1x Refresh, **2x Refresh**<br>**Note** Default value for M7 servers is 1x Refresh | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Memory Size Limit in GiB** | Limits the capacity in Partial Memory Mirror Mode up to 50 percent of the total memory capacity. The memory size can range from 0 GB to 65535 GB in increments of 1 GB. | 4.0(2), 4.0(4), 4.1(1), 4.2(1) | C220 M5, C240 M5, B200 M6, C240 M6, C225 M6, C245 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | **0** - 65535 with a step size of 1 | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Memory Thermal Throttling Mode** | Provides a protective mechanism to ensure the memory temperature is within the limits. When the temperature exceeds the maximum threshold value, the memory accessrate isreduced and Baseboard Management Controller (BMC) adjusts the fan to cool down the memory to avoid DIMM damage due to overheat | 4.0 (1), 4.0(2), 4.0(4), 4.1(1) | All M5 servers and , C220 M7, C240 M7 , X210c M7, X410c M7 servers | **CLTT with PECI**, Disabled<br>• Disabled—Options are Disabled.<br>• CLTT with PECI—Closed Loop Thermal Throttling (CLTT) with Platform Environment Control Interface (PECI). | This token is not supported on C125 M5 servers. |
| **Mirroring Mode** | Memory mirroring enhances system reliability by keeping two identical data images in memory. | 4.0 (1), 4.0(2), 4.0(4), 4.1(1) | All M5 servers | **Inter-socket**, Intra-socket<br>• Inter-Socket—Memory is mirrored between two Integrated Memory Controllers (IMCs) across CPU sockets.<br>• Intra-Socket—One IMC is mirrored with another IMC in the same socket. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **NUMA Optimized** | Whether the BIOS supports NUMA. | 4.0 (1), 4.0(2), 4.0(4), 4.1(1) | C220 M5, C240 M5, B200 M6, C220 M6, C240 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | **Enabled**, Disabled<br>• Disabled—The BIOS does not support NUMA.<br>• Enabled—The BIOS includes the ACPI tables that are required for NUMA-aware operating systems. If you enable this option, the system must disable Inter-Socket Memory interleaving on some platforms. | |
| **NVM Performance Setting** | enables efficient major mode arbitration between DDR and DDRT transactions on the DDR channel to optimize channel BW and DRAM latency. | 4.0(2), 4.0(4), 4.1(1) | C220 M5, C240 M5, B200 M6, C220 M6, C240 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | **BW Optimized**, Latency Optimized, Balanced Profile<br>• BW Optimized—Optimized for DDR and DDRT BW. This is the default option.<br>• Latency Optimized—Better DDR latency in the presence of DDRT BW.<br>• Balanced Profile—Optimized for Memory mode. | |
| **Operation Mode** | This option allows you to configure Operation Mode. | 4.2(1), 4.2(2) | C225 M5, C245 M5 | **Test-Only**, Test and Repair | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Panic and High Watermark** | Controls the delayed refresh capability of the memory controller. | 4.2(1) | B200 M6, C220 M6, C240 M6, C220 M7, C240 M7, X210c M7, X410c M7 | High, **Low**<br>• High—The memory controller is allowed to postpone up to a maximum of eight refresh commands. The memory controller executes all the postponed refreshes within the refresh interval.For the ninth refresh command, the refresh priority becomes Panic and the memory controller pauses the normal memory transactions until all the postponed refresh commands are executed.<br>• Low—The memory controller is not allowed to postpone refresh commands.<br>**Note** It is recommended to leave this setting in the default state (Low) which will help to reduce susceptibility to Rowhammer-style attacks. | It is recommended to leave this setting in the default state (**Low**) which will help to reduce susceptibility to Rowhammer-style attacks. |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Partial Cache Line Sparing** | Partial cache line sparing (PCLS) is an error-prevention mechanism in memory controllers. PCLS statically encodes the locations of the faulty nibbles of bits into a sparing directory along with the corresponding data content for replacement during memory accesses. | 4.2(1), 5.0(1), 5.0(2) | B200 M6, C240 M6, C220 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | Disabled, **Enabled**<br>**Note** For M7 servers, **Disabled** is the default value.<br>• Disabled—Options are Disabled.<br>• Enabled—Options are enabled. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Partial Memory Mirror Mode** | enables you to partially mirror by GB or by a percentage of the memory capacity. Depending on the option selected here, you can define either a partial mirror percentage or a partial mirror capacity in GB in available fields. You can partially mirror up to 50 percent of the memory capacity. | 4.1(1), | B200 M5, B480 M5, C220 M5, C240 M5, C480 M5, B200 M6, C220 M6, C240 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | **Disabled**, Percentage, Value in GB<br>• Disabled—Options are Disabled.<br>• Percentage—The amount of memory to be mirrored in the Partial Memory Mode is defined as a percentage of the total memory.<br>• Value in GB—The amount of memory to be mirrored in the Partial Memory Mode is defined in GB.<br>**Note** Partial Memory Mirror Mode is mutually exclusive to standard Mirroring Mode.<br>Partial Mirrors 1-4 can be used in any number or configuration, provided they do not exceed the capacity limit set in GB or Percentage in the related options. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Partial Mirror Percentage** | Limits the amount of available memory to be mirrored as a percentage of the total memory. This can range from 0.000.01 % to 50.00 % in increments of 0.01 %. | 4.1(1) | B200 M5, B480 M5, C220 M5, C240 M5, C480 M5, B200 M6, C220 M6, C240 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | **0.00** - 50.00 with a step size of 0.01 | **Note** Applicable only when partial mirror mode is set to a value in GB.<br>• In Memory RAS Configuration, select **Partial Mirror Mode 1LM**<br>• Partial Memory Mirror Mode configuration should be set to **Percentage**. |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Partial Mirror*n* Size in GB,** where *n* ranges from 1 to 4. | Limits the amount of memory in Partial Mirror*n* in GB. This can range from 0 GB to 65535 GB in increments of 1 GB. | 4.1(1) | B200 M5, B480 M5, C220 M5, C240 M5, C480 M5, C125 M5, C220 M7, C240 M7, X210c M7, X410c M7 | **0** - 65535 with a step size of 1 | **Note** Applicable only when partial mirror mode is set to a value in GB.<br>When *n=2:*<br>• In Memory RAS Configuration, select **Partial Mirror Mode 1LM**<br>• Partial Memory Mirror Mode configuration should be set to **Percentage**. |
| **PCIe RAS Support** | Whether the PCIe RAS port is enabled or disabled. | 4.0 (1), 4.0(2), 4.0(4), 4.1(1), 4.1(3) | All M5 servers and , C220 M7, C240 M7 , X210c M7, X410c M7 servers | Disabled, **Enabled**, Auto<br>• Disabled—This option is Disabled.<br>• Enabled—This options is enabled.<br>• Auto—PCIe RAS Support is in auto mode. | |
| **Post Package Repair** | Post Package Repair (PPR) provides the ability to repair faulty memory cells by replacing them with spare cells. | 4.2(1) | B200 M6, C240 M6, C220 M6, C225 M6, C245 M6, X210c M6 | Disabled, **Hard PPR**<br>• Disabled—This option is Disabled.<br>• Hard PPR—This results in a permanent remapping of damaged storage cells. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Memory RAS Configuration** | How the memory reliability, availability, and serviceability (RAS) is configured for the server. | 4.0 (1), 4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1), 5.0(1), 5.0(2) | C220 M5, C240 M5, B200 M6, C240 M6, C220 M6, C220 M7, C240 M7, X210c M7, X410c M7 | | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| | | | | Maximum Performance, Mirroring, Lockstep, Mirror Mode 1LM, Partial Mirror Mode 1LM, Sparing, **ADDDC Sparing**<br>• Maximum Performance—Optimizes the system performance and disables all the advanced RAS features.<br>• Mirroring—System reliability is optimized by using half the system memory as backup. This mode is used for UCS M4 and lower blade servers<br>• Lockstep—If the DIMM pairs in the server have an identical type, size, and organization and are populated across the SMI channels, you can enable lockstep mode to minimize memory access latency and provide better performance. Lockstep is enabled by default for B440 servers.<br>• Mirror Mode 1LM—Mirror Mode 1LM willset the entire 1LM memory in the system to be mirrored, consequently reducing the memory capacity by half. This mode is used for UCS M5 and M6 blade servers.<br>• Partial Mirror Mode 1LM—Partial Mirror Mode 1LM will set a part of the 1LM memory in the system to be mirrored, consequently reducing the memory capacity by half. This mode is used for UCS M5 and M6 blade servers.<br>• Sparing—System reliability | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| | | | | is optimized by holding memory in reserve so that it can be used in case other DIMMs fail. This mode provides some memory redundancy, but does not provide as much redundancy as mirroring.<br>• ADDDC Sparing—System reliability is optimized by holding memory in reserve so that it can be used in case other DIMMs fail. This mode provides some memory redundancy, but does not provide as much redundancy as mirroring. | |
| **PPR Type** | Post Package Repair (PPR) provides the ability to repair faulty memory cells by replacing them with spare cells. | 4.1(1), 4.2(1) | C220 M5, C240 M5, B200 M5, B200 M6, C240 M6, C220 M6, C225 M6, C245 M6, C220 M7, C240 M7, X210c M7, X410c M7 | Disabled, **Hard PPR**<br>• Disabled—Options are Disabled.<br>• Hard PPR—This results in a permanent remapping of damaged storage cells. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Secured Encrypted Virtualization** | Enables running encrypted virtual machines(VMs) in which the code and data of the VM are isolated. | 4.2(1) | C125 M5, C225 M6, C245 M6 | 253 ASIDs, 509 ASIDs, Auto<br>• 253 ASIDs<br>• 509 ASIDs<br>• Auto<br>**Note** It is recommended to leave this setting in the default state of Auto to mitigate Rowhammer-style attacks. | |
| **SMEE** | Whether the processor uses the Secure Memory Encryption Enable (SMEE) function, which provides memory encryption support. | 4.0(4), 4.1(1), 4.1(3), 4.2(1) | C125 M5, C225 M6, C245 M6 | Disabled, **Enabled**<br>• Disabled—This option is Disabled.<br>• Enabled—This options is enabled. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Snoopy Mode for 2LM** | | 4.0 (1), 4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1) | All M5 servers and , C220 M7, C240 M7 , X210c M7, X410c M7 servers | **Disabled**, Enabled<br>• Disabled—This option is Disabled.<br>• Enabled—This options is enabled. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| | Enables snoop-mode for DCPMM accesses while maintaining directory on all DRAM accesses. Snoops maintain cache coherence between sockets. Directory reducessnoops by keeping the remote node information locally (in memory). Directory lookups and updates add memory traffic<br>Directory is a good tradeoff for DRAM, but not necessarily for DCPMM. For non-NUMA workload, when the feature is enabled, directory updates to DCPMM are eliminated, thereby helping DDRT bandwidth bound workloads. Directory is disabled for far memory | | | | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| | accesses and instead snoops remote sockets to check for ownership. Directory is used only for DRAM (near memory). | | | | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Snoopy Mode for AD** | | 4.0 (1), 4.0(2), 4.0(4), 4.1(1), 4.1(3), 4.2(1) | All M5 servers and , C220 M7, C240 M7 , X210c M7, X410c M7 servers | **Disabled**, Enabled<br>• Disabled—This option is Disabled.<br>• Enabled—This options is enabled. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| | Enables snoop-mode for DCPMM accesses while maintaining directory on all DRAM accesses. Snoops maintain cache coherence between sockets. Directory reducessnoops by keeping the remote node information locally (in memory). Directory lookups and updates add memory traffic.<br>Directory is a good tradeoff for DRAM, but not necessarily for DCPMM. For non-NUMA workload, when the feature is enabled, directory updates to DCPMM are eliminated, thereby helping DDRT bandwidth bound workloads. Directory is disabled for | | | | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| | accesses to AD and instead snoops remote sockets to check for ownership. Directory is used only for DRAM accesses. | | | | |
| **Transparent Secure Memory Encryption** | Provides transparent hardware memory encryption of all data stored on system memory. | 4.1(3) | C125 M5 servers | Disabled, Enabled, **Auto**<br>• Disabled—This option is Disabled.<br>• Auto—This options is set to auto mode. | |
| **UMA Based Clustering** | As the name implies, UMA based clustering is the suggested clustering mode when the processor is configured as Uniform Memory Access (UMA) node, i.e. SNC is disabled. | 4.2(1) | C220 M6, C240 M6, B200 M6, X210 M6, C220 M7, C240 M7, X210c M7, X410c M7 | Disable-All-2All, **Hemisphere-2-clusters**, Quadrant-4-clusters<br>**Note** For M7 servers, the default value is **Quadrant-4-clusters**. | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Volatile Memory Mode** | Allows the memory mode configuration. | 4.0(2), 4.0(4), 4.1(1), 4.2(1), 5.0(1), 5.0(2) | C220 M6, C240 M6, B200 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | 1LM, **2LM**<br>• 1LM—Configures 1 Layer Memory(1LM).This is the default value for M7 servers.<br>• 2LM—Configures 2 Layer Memory(1LM). | |
| **Error Check Scrub** | Allows you to enable a memory device to perform memory checking, correction and count errors. | 4.0(2), 4.0(4), 4.1(1), 4.2(1), 5.0(1), 5.0(2) | C220 M6, C240 M6, B200 M6, X210c M6, C220 M7, C240 M7, X210c M7, X410c M7 | Disabled, **Enabled with result collection**, Enabled without result collection | |
| **Rank Margin Tool** | Allows automated memory margin testing and is used to identify DDR margins at the rank level. | 4.0(2), 4.0(4), 4.1(1), 4.2(1), 5.0(1), 5.0(2) | C220 M6, C240 M6, B200 M6, X210c M6, C220 M7, C240 M7, X210c M6 | Enable, **Disable** | |

| Name | Description | Supported Attributes | | | |
|---|---|---|---|---|---|
| | | Versions | Platforms | Values | Dependencies |
| **Adaptive Refresh Management Level** | Selects Adaptive Refresh Management (ARFM) Level when refresh management (RFM) is required. | 4.0(2), 4.0(4), 4.1(1), 4.2(1), 5.0(1), 5.0(2) | C220 M6, C240 M6, X210c M6 , C220 M7, C240 M7, X210c M7, X410c M7 | Enable, **Disable** | |