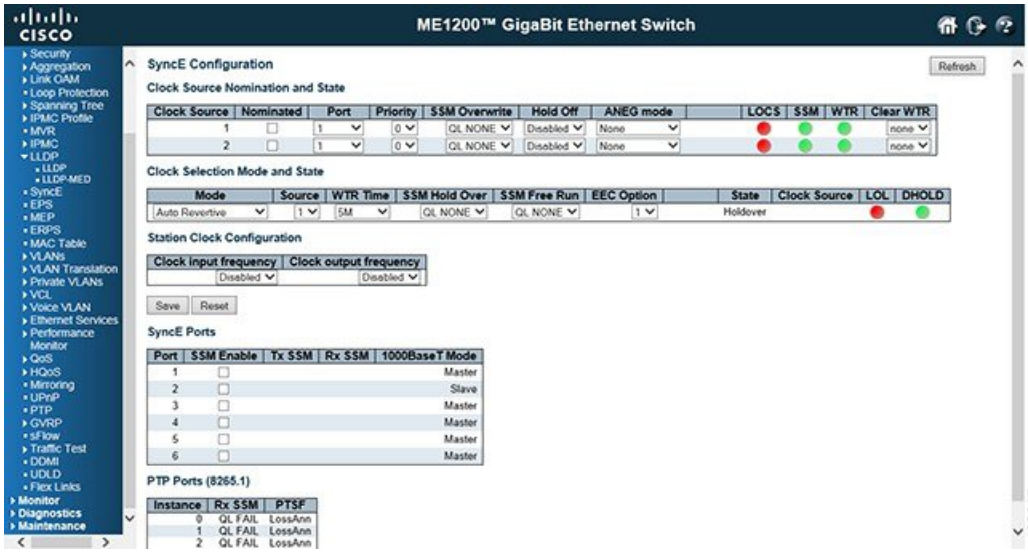
Configuring SyncE

Synchronous Ethernet Configuration

This feature allows you to inspect and configure the current SyncE port settings.



Clock Source Nomination and State

For each possible clock source, you can configure the following:

- **Clock Source**: This is the instance number of the clock source. This has to be referenced when selecting Manual' mode.
- **Nominated**: When a clock source is nominated, the clock output from the related PHY (Port) is enabled against the clock controller. This makes it available as a possible source in the clock selection process.

If it is supported by the actual HW configuration, The Station clock input can be nominated as a Clock Source.

- **Port**: In this drop down box, the ports that are possible to select for this clock source, is presented. The PCB104 Synce module supports 10MHz station clock input. The station clock input is indicated by a port number = 'Number of ethernet ports' + 1. The serval has a limitation that chip port 1 cannot be nominated as source 1. On the ME1200 board, it is port 3 (interface gi 1/3) .
- **Priority**: The priority for this clock source. Lowest number (0) is the highest priority. If two clock sources has the same priority, the lowest clock source number gets the highest priority in the clock selection process
- **SSM Overwrite**: A selectable clock source Quality Level (QL) to overwrite any QL received in a SSM. If QL is not Received in a SSM (SSM is not enabled on this port), the SSM Overwrite QL is used as if received. The SSM Overwrite can be set to QL_NONE, indicating that the clock source is without any know quality (Lowest compared to clock source with known quality).
- **Hold Off**: The Hold Off timer value. Active loss of clock Source will be delayed the selected amount of time. The clock selector will not change clock source if the loss of clock condition is cleared within this time.
- **ANEG mode**: This is relevant for 1000BaseT ports only. In order to recover clock from port it must be negotiated to 'Slave' mode. In order to distribute clock the port must be negotiated to 'Master' mode. This different ANEG modes can be activated on a Clock Source port:
  - *Prefer Slave*: The Port will be negotiated to 'Slave' mode if possible.
  - *Prefer Master*: The Port will be negotiated to 'Master' mode if possible.

    The selected port in 'Locked' state will always be negotiated to 'Slave' if possible.
- **LOCS**: Signal is lost on this clock source.
- **SSM**: If SSM is enabled and not received properly. Type of SSM fail will be indicated in the 'Rx SSM' field.
- **WTR**: Wait To Restore timer is active.
- **Clear WTR**: Clears the WTR timer and makes this clock source available to the clock selection process.

Synchronous Ethernet Configuration contd

Clock Selection Mode and State

The Clock Selector is only in one instance - the one who selects between the nominated clock sources.

- **Mode**: The definition of the 'best' clock source is firstly the one with the highest (QL) and secondly (the ones with equal QL) the highest priority. Clock Selector can be in different modes:
  - *Manual* : Clock selector will select the clock source stated in Source (see below). If this manually selected clock source is failing, the clock selector will go into holdover state.
  - *Manual To Selected*: Same as Manual mode where the pt. selected clock source will become Source.
  - **Auto NonRevertive**: Clock Selection of the best clock source is only done when the selected clock fails.

- *Auto Revertive*: Clock Selection of the best clock source is constantly done.
- *Force Hold Over*: Clock Selector is forced to Hold Over State.
- *Force Free Run*: Clock Selector is forced to Free Run State.

- **Source**: Only relevant if Manual mode is selected (see above).
- **WTR Time**: WTR is the Wait To Restore timer value in minutes. The WTR time is activated on the falling edge of a clock source failure (in Revertive mode). This means that the clock source is first available for clock selection after WTR Time (can be cleared).
- **SSM Hold Over**: This is the transmitted SSM QL value when clock selector is in Hold Over State.
- **SSM Free Run**: This is the transmitted SSM QL value when clock selector is in Free Run State.
- **EEC Option**: The ZL30xxx based Synce modules support both EEC1 and EEC2 option. The difference is: EEC1 => DPLL bandwidth = 3,5 Hz, EEC2 => DPLL bandwidth = 0,1 Hz.
- **State**: This is indicating the state of the clock selector. Possible states are:
  - *Free Run*: There is no external clock sources to lock to (unlocked state). The Clock Selector has never been locked to a clock source long enough to calculate the hold over frequency offset to local oscillator. The frequency of this node is the frequency of the local oscillator.
  - *Hold Over*: There is no external clock sources to lock to (unlocked state). The Clock Selector has calculate the holdover frequency offset to local oscillator. The frequency of this node is hold to the frequency of the clock source previous locked to.
  - *Locked*: Clock selector is locked to the clock source indicated (See next).
  - *Top*: Clock selector is locked to Time over packets, for example, PTP (See next).
- **Clock Source**: The clock source locked to when clock selector is in locked state.
- **LOL**: Clock selector has raised the Los Of Lock alarm.
- **DHOLD**: Clock selector has not yet calculated the holdover frequency offset to local oscillator. This becomes active for about 10 s, when a new clock source is selected.

Station Clock Configuration

The SyncE module may have a Station clock input and/or a Station clock output.

- **Clock input frequency**: If supported by the Synce HW, the station clock input frequency can be configured, the possible frequencies are:1,544 MHz, 2,048 MHz or 10 MHz.
- **Clock output frequency**: If supported by the Synce HW, the station clock output frequency can be configured, the possible frequencies are:1, 544 MHz, 2, 048 MHz or 10 MHz.

SyncE Ports

For each possible port on switch.

- **Port**: The port number to configure.
- **SSM Enable**: Enable and disable of SSM functionality on this port.
- **Tx SSM**: Monitoring of the transmitted SSM QL on this port. Transmitted QL should be the Quality Level of the clock generated by this node. This means the QL of the clock source this node is locked.

- **Rx SSM**: Monitoring of the received SSM QL on this port. If link is down on port, QL_LINK is indicated. If no SSM is received, QL_FAIL is indicated.
- **1000BaseT Mode**: If PHY is in 1000BaseT Mode then this is monitoring the master/slave mode. In order to receive clock on a port, it has to be in slave mode. To transmit clock on a port, it has to be in master mode.