Single-Chassis System Summary

This chapter provides a summary of the single-chassis system and an overview of the cabling and system interconnection for the Cisco CRS Series Enhanced 16-Slot Line Card Chassis (LCC). It includes the following sections:

For instructions on cabling a Cisco CRS Series single-shelf system, see *Cisco CRS Carrier Routing System 16-Slot Line Card Chassis Installation Guide*.

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The single-shelf system comprises one LCC that contains a set of switch fabric cards (SFCs) that make up the complete three-stage Benes switch fabric. Because the single-shelf system is a standalone system, it is not interconnected with any other chassis, and does not require interconnection cabling.

In a single-shelf system, the following components or functions have external connectivity:

- CONSOLE or AUX RJ-45 RS-232 serial ports on the route processor cards for terminal connections
- Ethernet ports on the route processor for connecting network management equipment
- Physical layer interface modules (PLIMs) for data connections
- RJ-45 external clock (EXT CLK 1 and EXT CLK 2) connectors for the Building Integrated Timing Source (BITS) signal
- Alarm module alarm-out connector

Building Integrated Timing Source

Note Support for BITS is not currently available on the Cisco CRS. This information is provided as future reference only.

The LCC fan controller card contains the circuitry for the building integrated timing source (BITS) clocking. BITS is centralized clocking architecture that provides a single common network clock for all SONET/SDH equipment in a point-of-presence (POP) or central office.

The main component of the BITS architecture is a Stratum 1 clock signal that comes from a dedicated transport facility or a GPS receiver. A BITS “box” in the central office or POP receives this reference clock signal and distributes it through dedicated T1 (1.544 MHz) or E1 (2.048 MHz) facilities to all of the SONET/SDH equipment that requires network timing (digital switches, DCSs, ADMs, routers, and so on). In this way, all of the equipment is synchronized to the same master clock. The BITS box also contains a Stratum 2 (or Stratum 3E) local clock to provide a holdover clock signal in case the primary network clock signal is lost. If the input Stratum 1 clock fails, the holdover clock signal is used.

Note The BITS clock signals are analog alternate mark inversion (AMI) signals.

The fan controller card receives the BITS clock signal through an RJ-45 connector on its front panel. The BITS clock signal is routed to synchronous equipment timing source (SETS) circuitry on the fan controller card. The SETS circuitry locks onto the BITS reference timing signal and generates a 19-MHz clock signal, which it then distributes to each PLIM slot in the LCC. This ensures that all PLIMs are synchronized to the same master clock.

For redundant operation, each fan controller card receives two independent input BITS clock signals (EXT CLK 1 and EXT CLK 2). If one of the primary clock sources fails, the SETS circuitry reverts to the redundant input BITS reference timing signal. If both input timing signals fail, the SETS circuitry enters a holdover mode and uses an internal Stratum 3 (12.8-MHz) clock as the reference timing signal. This way, all of the PLIMs in the LCC receive an accurate timing signal.

Each BITS RJ-45 connector supports one input signal:

- Pins 1 and 2 support one pair of RTIP and RRING signals.
- Pins 4 and 5 are not used.

Each fan controller card has two RJ-45 BITS connectors. This means that the LCC can receive four BITS input clock references (2 per fan controller card).