Clock Recovery System for CESoPSN

The Clock Recovery System recovers the service clock using Adaptive Clock Recovery (ACR) and Differential Clock Recovery (DCR).

Finding Feature Information

Your software release may not support all the features documented in this module. For the latest caveats and feature information, see Bug Search Tool and the release notes for your platform and software release. To find information about the features documented in this module, and to see a list of the releases in which each feature is supported, see the feature information table.

Use Cisco Feature Navigator to find information about platform support and Cisco software image support. To access Cisco Feature Navigator, go to www.cisco.com/go/cfn. An account on Cisco.com is not required.

Information About Clock Recovery

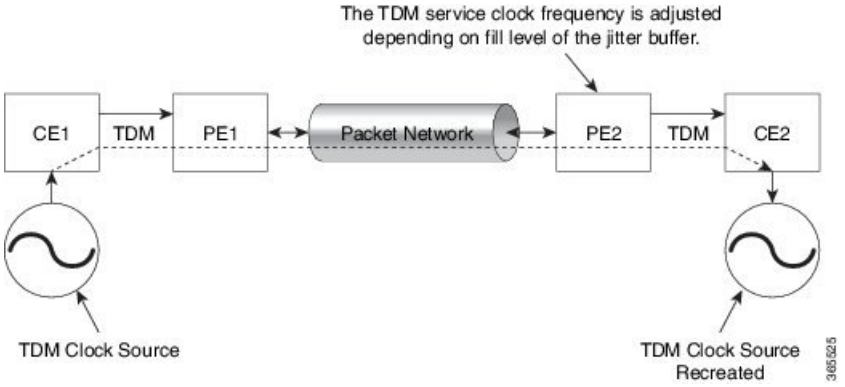
Clock Recovery System in CESoPSN

The Clock Recovery System is able to recover the service clock using two methods, the Adaptive Clock Recovery and Differential Clock Recovery.

Adaptive Clock Recovery in CESoPSN

When emulating TDM over PSNs, the physical layer clock is sometimes not available to both ends. Adaptive Clock Recovery (ACR) is a technique where the clock from the TDM domain is mapped through the packet domain. The sending Inter Working Function (IWF) processes outgoing packets with an internal free-running clock, and the receiving IWF creates a clock based on packet arrival. The service clock frequency is adjusted depending on fill level of the jitter buffer.

- When sending TDM digital signal over PSN, the TDM data is inserted into packets in the master IWF and sent to the desired destination (slave IWF).
- The rate at which the packets are transmitted to the PSN is constant. Due to the nature of the PSN, the packets might arrive to the destination in bursts and with varying rate.
- The long-term average of this rate is equal to the insertion rate at the master IWF. Moreover, the packets in the PSN might switch their order and even be lost.
- The IWF at the far end of the PSN (slave IWF) recovers the service clock (E1/T1) used by the master IWF.
- The recovered clock is used by the slave IWF for the transmission of the data back into the TDM lines.
- The master IWF aggregates the TDM data and creates the PWE packets; these packets are transmitted to the PSN.
- The packets are received by the slave IWF and stored in a jitter buffer designed to absorb the packet delay variation (PDV).
- The packets are extracted from the jitter buffer and the clock recovery algorithm updates the service clock based on the timing information available.

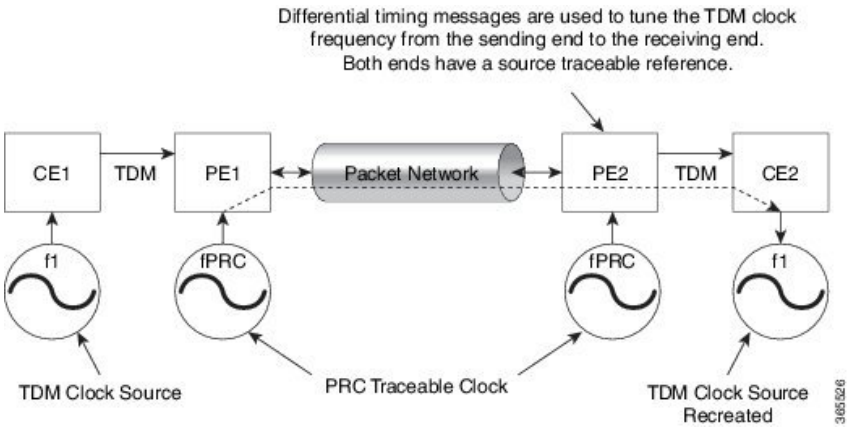


Differential Clock Recovery in CESoPSN

DCR (Differential Clock Recovery) is another technique used for Circuit Emulation (CEM) to recover clocks based on the difference between PE clocks. The clock from the TDM domain is mapped through the packet domain. It differs from ACR in that a PRC traceable clock is used at each end. Differential timing messages are used to tune the TDM clock frequency from the sending end to the receiving end. Both ends have a source traceable reference. Because of this, the recovered clock is not affected by PDV when using DCR.

In contrast with DCR, a PRC traceable clock source is available at each end. ACR is used when a traceable source is not available at both ends of the PSN link.

The recreated service clock accuracy is dependent on the accuracy between the sending and receiving PRC frequencies.



Benefits of Clock Recovery

- Customer-edge devices (CEs) can have different clock from that of the Provide-edge devices (PEs).
- In CESoPSN, a slave clock is supported for clock redundancy.

Scaling Information

IM Card	Pseudowires Supported (Number of Clocks Derived)
48-Port T1/E1 CEM Interface Module	48

Prerequisites for Clock Recovery

- The clock of interface modules must be used as service clock.
- CEM must be configured before configuring the global clock recovery.
- RTP must be enabled for DCR in CEM, as the differential clock information is transferred in the RTP header.

Restrictions for Clock Recovery

- The reference clock source is used and locked to a single clock.
- The clock ID should be unique for a particular interface module for ACR or DCR configuration.
- ACR clock configuration under each controller should be performed before configuring CEM group.

How to Configure ACR and DCR

Configuring ACR for T3/E3

Configuring Adaptive Clock Recovery of T3/E3 Interfaces for CESoPSN

Before You Begin

Before configuring Adaptive Clock Recovery, CEM must be configured. Below are the guidelines to configure clock recovery:

- The node (chassis) on which the DS1 is configured for ACR, must have its own clock derived from BITS/GPS/Stratum clock.
- The minimum packet size of CEM pseudowires on the network that delivers robust clock recovery is 64 bytes.

To configure the clock on T3/E3 interfaces for CESoPSN in controller mode, use the following commands:

```
enable
configure terminal
controller t3 <slot>/<bay>/<port>
t1 <t1_num>  clock source recovered <clock-id>
t1 <t1_num> cem-group < cem-group-no > timeslots <1-24>
exit
```

To configure the clock recovery on T3/E3 interfaces in global configuration mode, use the following commands:

```
recovered-clock <slot> <bay>
clock recovered <clock-id> adaptive cem <port-no> <cem-group-no>
exit
```

To remove the clock configuration in ACR and DCR, you must remove the recovery clock configuration in global configuration mode and then remove the controller configuration.

Configuring DCR for T3/E3

Configuring Differential Clock Recovery of T3/E3 Interfaces for CESoPSN

Before You Begin

Before configuring Differential Clock Recovery, CEM must be configured. Below are the guidelines to configure clock recovery:

- The node (chassis) on which the DS1 is configured for DCR, must have its own clock derived from BITS/GPS/Stratum clock.
- The minimum packet size of CEM pseudowires on the network that delivers robust clock recovery is 64 bytes.

To configure the clock on T3/E3 interfaces for CESoPSN in controller mode, use the following commands:

```
enable
configure terminal
controller t3 <slot>/<bay>/<port>
t1 <t1_num> clock source Recovered <clock-id>
t1 <t1_num> cem-group < cem-group-no> timeslots <1-24>

interface cem <slot>/<bay>/<port>
cem < cem-group-no>
rtp-present

recovered-clock  <bay> <slot>
clock recovered <clock-id> differential cem <port-no> <cem-group-no> priority <1|2>
exit
```

Note To remove the clock configuration in ACR and DCR, perform the following steps:

- Use the **no clock source recovered** command.
- Remove the global clock.
- Remove CEM configuration, if required.