



## SR-TE Optimization

The Segment Routing (SR) TE Optimization tool creates or updates segment lists<sup>1</sup> to minimize the sum total of user-specified metrics for selected SR LSPs using the fewest number of segment list hops as possible. The tool sets the routes based on traffic engineering criteria and optimizes a sequence of node or adjacency hops for the SR LSP paths to follow.

You can use the SR-TE Optimization tool to design, capacity plan, and manually configure networks to meet the following two objectives. Additionally, you can embed the results into a WAE workflow so as to re-optimize and re-configure SR LSPs reactively after events such as network failures and subsequent route reconvergence.

- **TE Metric or Delay Minimization**—Minimize distance between hops with respect to metrics other than IGP metrics. These can be either TE metrics configured on interfaces (which can be set proportional to circuit latency) or latencies (delays) for each circuit. An example application is a differentiated service in which latency-sensitive network traffic is routed on shortest latency paths, while the bulk of the traffic routes over cost-optimized paths.
- **Node Avoidance**—Create or optimize segment lists so they avoid routing through specified nodes. An example application is routing pairs of LSPs, each over a different plane in a dual-plane network. The same traffic is routed over both LSPs simultaneously, thus improving availability.

While there is an option to specify a maximum number of hops, doing so might not achieve the lowest possible latency. In this case, the best achievable solution is provided.

You can additionally avoid unnecessary LSP churn by specifying boundaries (bounds) on the path length and margins within which the shortest path must be optimized.



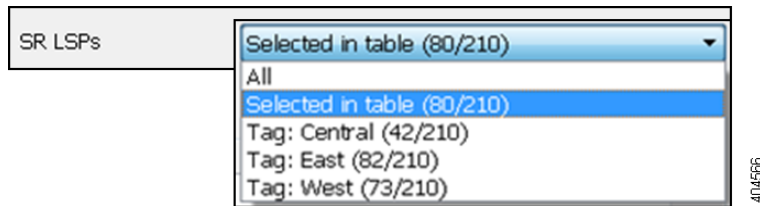
### Note

Unless qualified with “TE” or “IGP,” the term *metric* in this chapter applies to IGP metric, TE metric, or delay.

## Optimize SR-TE LSPs

Select the Tools->SR-TE Optimization menu. Then identify which SR LSPs to optimize: all SR LSPs, those selected prior to opening the dialog box, or those with specific tags. The default is to optimize all selected SR LSPs, and by default, all SR LSPs are considered selected.

<sup>1</sup>WAE Design uses the terms *SR LSP* that uses *segment lists* which contain *segment list hops*. In Cisco routing terminology, these terms are *SR tunnel* that uses *segment ID (SID) lists*, which contain *SIDs*.



Upon completion, WAE Design tags the LSPs with *SROpt* and generates a new plan file named with an *-SROpt* suffix. WAE Design also writes a report containing the results of the optimization, as well as verifications that the results met the criteria for avoiding nodes and meeting the specified bounds. To access this information later, select the Window->Reports menu.

- Parameters for optimizing explicit LSP paths are specified in the Bound, Margin, and Constraints sections of the dialog box. If you do not specify a bound, margin, or constraint, WAE Design generates the best possible SR LSP routes for the given path metric.
- A segment list is created or updated for all SR LSP paths that can be optimized using the minimum number of segment list hops possible.
  - If an LSP has a directly associated segment list, then the segment list is deleted.
  - If an LSP has no LSP paths, an LSP path with a path option of 1 is created.
  - If an LSP has no segment list, but it has LSP paths, then a segment list is created for the active path if it exists and if not, for the lowest path option (where lowest means the smallest value).
  - If an LSP has associated LSP paths and a segment list associated with either the active path or lowest path option, then the segment list hops in the segment list are updated.

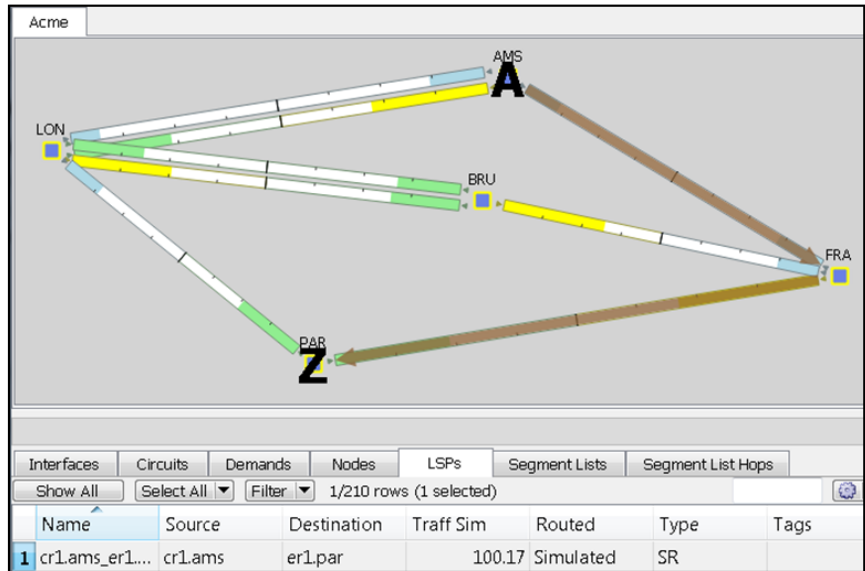
**Example:** Figure 21-1 shows an SR LSP that normally routes from AMS-FRA-PAR based on IGP metrics. It has no LSP paths. All circuits have a Delay Sim value of 50 except for the AMS-FRA circuit, which has a Delay Sim value of 60. Optimizing this SR LSP based on delay results in rerouting the SR LSP over the shortest achievable delay path, creating an LSP path with a path option of 1, and creating a segment list node hop on the cr.lon node.

- If it is not possible to achieve the lowest possible path without exceeding the specified maximum number of segment list hops, WAE Design provides the best achievable solution within this restriction of maximum permissible hops.
- If it is not possible to avoid all specified nodes for an SR LSP, then that SR LSP is not updated.
- If an existing segment list would be better optimized by removing all segment list hops, then those hops are removed, though the segment list remains.
- If a previously optimized SR LSP does not need further optimization, it is not changed and its previously set SROpt tag is removed.
- If the source and destination nodes are in different IGP areas, WAE Design creates an explicit hop on the most optimal ABR<sup>2</sup> for each IGP area that the SR LSP traverses. For information on routing inter-area LSPs, see the [MPLS Simulation](#) chapter.

<sup>2</sup>An OSPF Area Border Router (ABR) is a node belonging to both the area and the OSPF area. An IS-IS ABR is a node belonging to both the Level 2 area and another IS-IS level.

Figure 21-1 Example SR LSP Optimization

SR LSP Routed Based on IGP Metrics Before Optimization



SR LSP Route Optimized for Best Path Based on Delay

Minimize Path Metric  Delay

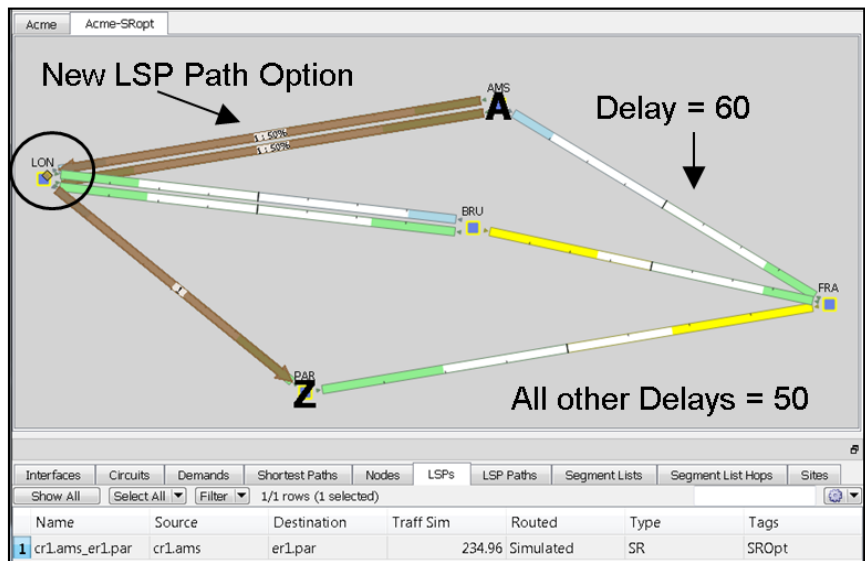
Bound on path length

Fixed

Margin above shortest path

Fixed

Percentage



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## Optimize Path Metric

The Minimize Path Metric selection defines whether to optimize SR LSPs based on interface IGP metrics, interface TE metrics, or circuit delays. All of these properties are configurable from an interface Properties dialog box, and delays can also be set in a circuit Properties dialog box.

Minimize Path Metric

- TE Metric
- IGP Metric
- TE Metric**
- Delay

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## Bound and Margins

Bounds and margins identify which paths to optimize, as well as when to stop optimizing a given path. If you enter a value for more than one restriction, WAE Design uses the strictest limitation as the optimization target. If there is no bound or margin specified, WAE Design optimizes LSP paths to the best possible solution (lowest total metrics for the LSP path).

### Bound: Maximum Acceptable Path Length

The Fixed Bound entry enables you to set the maximum path metric that is acceptable. WAE Design attempts to optimize LSP paths with metrics that exceed this bound. If a solution adhering to this bound cannot be found, the best possible solution is provided and bound violations are listed in the report. LSP paths that are less than or equal to this bound are not optimized.

**Example:** If you select to optimize LSP paths based on TE metrics, the value entered is 50, and the sum of TE metrics on the LSP path is 51, that LSP path is optimized.

Enter a number based on the selected path metric. A TE metric is a property values whose total sum for the LSP path cannot be exceeded. The delay is also a property value, but it is in milliseconds (ms). Meaning, if you enter “50” and you have selected delay as the metric to optimize, this represents 50 ms as the maximum acceptable delay for the LSP path.

### Margins: Maximum Acceptable Metric above Shortest Path

The Margin entries enable you to identify the acceptable deviation above the shortest achievable path metric. Any existing LSP path having a metric that is less than or equal to the shortest path metric plus the margin is not optimized.

- Fixed—The amount by which a metric must be surpassed before it is optimized.

**Example:** If an SR LSP route has a delay of 110 (as in [Figure 21-1](#)), a fixed margin set to 10, and the shortest achievable delay path is 100, then the current SR LSP is within the margin and will not be updated ([Figure 21-2](#)). If the fixed margin is set to 9, then the SR LSP would be optimized.

$100$  (shortest path) +  $10$  (fixed margin) =  $110$ , so all paths greater than  $110$  are optimized

- Percentage—The amount by which a metric must be surpassed, expressed as a percentage of the shortest path, before it is optimized.

**Example:** If an existing SR LSP route has a TE metric of 210, a percentage margin set to 10%, and the shortest achievable TE metric path is 200, then the current SR LSP is within the margin and will not be updated. If the current SR LSP had a metric of 225, then it would be optimized.

$200$  (shortest path) x  $.10$  (percentage margin) =  $20$ , so all paths greater than  $220$  must be optimized

**Example:** If an SR LSP route has a delay of 110 (as in [Figure 21-1](#)), a fixed bound is set to 120, a fixed margin is set to 15, a percentage margin is set to 5%, and the shortest achievable delay path is 100, then the strictest of these restrictions takes precedence, and the SR LSP is optimized ([Figure 21-2](#)).

Fixed Bound = 120

$100$  (shortest path) +  $15$  (fixed margin) =  $115$

$100$  (shortest path) x  $.05$  (percentage margin) =  $5$ , so all paths greater than  $105$  are optimized since it is the strictest margin

Figure 21-2 Example SR LSPs Optimized with Margins

Shortest Delay = 100  
 SR LSP Delay = 110

SR LSP Is Not Optimized

Minimize Path Metric Delay

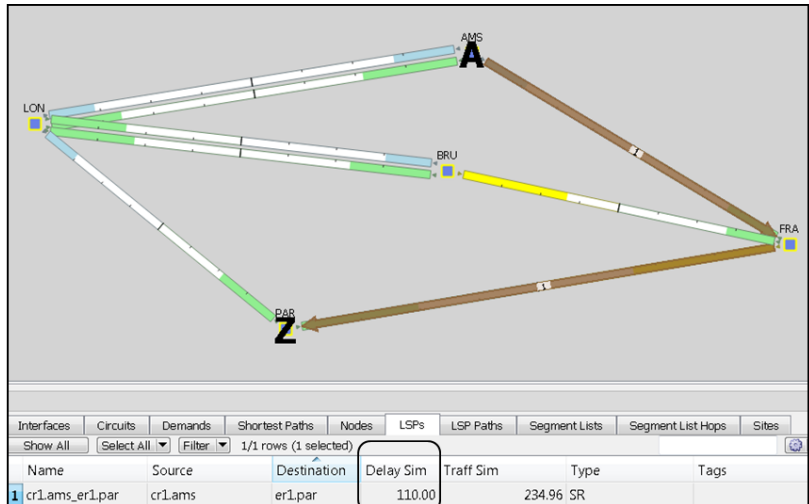
Bound on path length

Fixed

Margin above shortest path

Fixed

Percentage



SR LSP Is Optimized

Minimize Path Metric Delay

Bound on path length

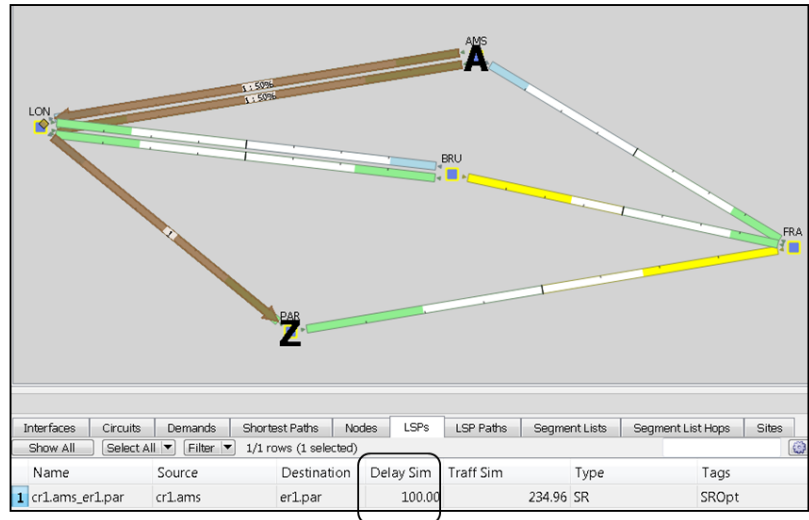
Fixed

Margin above shortest path

Fixed

Percentage

Strictest →



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## Constraints

The Constraints enable you to specify restrictions for the optimizations.

Constraints

Maximum Segment List Hops per SR LSP

Avoid nodes containing tag

Restrict segment nodes to core nodes

**Note**

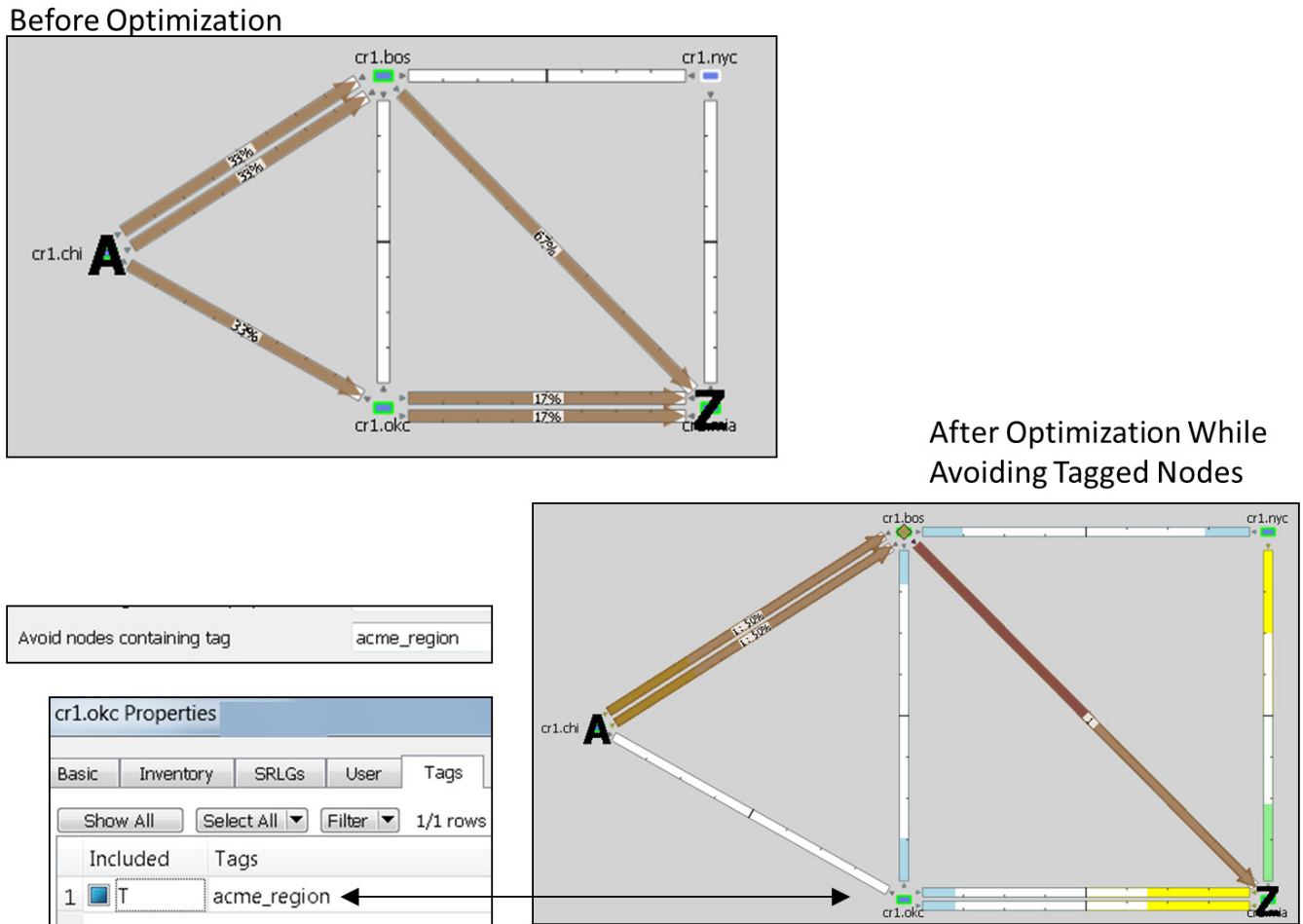
If it is not possible to achieve the lowest possible path without exceeding the specified maximum number of segment list hops, WAE Design provides the best achievable solution within this restriction of maximum permissible hops. If it is not possible to avoid all specified nodes, the SR LSP is not updated.

- **Maximum Segment List Hop**—The maximum number of segment list hops that any given segment list can contain after optimization. If no value is specified, WAE Design creates as many hops as needed to best optimize the SR LSP.
- **Avoid nodes containing tag**—Exclude all nodes containing the specified tag in the optimization. This is useful when modeling dual-plane topologies that route disjoint LSPs. For information on how to create tags, see the [Plan Objects](#) chapter.

**Example:** [Figure 21-3](#) shows an example of an SR LSP from cr1.chi to cr1.mia that is routed based on its shortest IGP route. It also shows the optimized SR LSP path if it were to avoid cr1.okc based on its tag.

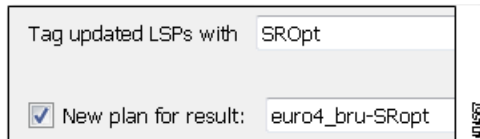
- **Restrict segment nodes to core nodes**—Segment list node hops must be core nodes (nodes that have their Function property set to “core”), and the local node of segment list interface hops must be a core node. Note that an SR LSP could still route using edge nodes provided they are not used as hops.

Figure 21-3 Example of Avoiding Tagged Nodes During SR-TE Optimization



## Use SR Tags and Create New Plan Files

These options identify whether and how optimized SR LSPs are tagged, and whether to create new plan files containing the results.



- Tag updated LSPs with —Create and add tags to all SR LSPs rerouted during optimization. Using tags makes it easier to find the changed SR LSPs that are deployed to the network or to find those SR LSPs that need to be reconfigured in the actual network according to the optimization results. By default, newly optimized LSPs are tagged as *SROpt*.
- New plan for result—This default option creates a new plan with the results of the optimization. Unless a name is specified, WAE Design attaches an *-SROpt* suffix to the current plan file name. If not selected, WAE Design changes the current plan file with the updated information. Saving this plan file then simplifies the process of identifying which LSPs to reconfigure in the network.

## Related Topics

- [MPLS Simulation](#) chapter
- [Segment Routing Simulation](#) chapter
- [LSP Loadshare Optimization](#) chapter