Overview of the Serial SPAs

This chapter provides an overview of the release history, supported features, restrictions, and Management Information Base (MIB) support for the serial SPAs on the Cisco ASR 1000 Series Aggregation Services Routers.

This chapter includes the following sections:

Release History

Release	Modification
Cisco IOS XE Release 3.12	The following serial SPAs were supported on the SIP-400 linecard. • Channelized TE1 SPA (Maverick) • Channelized T3 SPA (Patriot) • Channelized OC3 STM SPA (Prowler) • Clear Channel T3E3 SPA (Javelin) All serial SPAs supported SIP-200 on Cascades release will be supported on SIP-400
Cisco IOS XE Release 3.10	Support for the 8-Port Channelized T1/E1 Serial SPA (SPA-8XCHT1/E1-V2) was introduced on the Cisco ASR 1000 Series SIPs.

Release	Modification
Cisco IOS XE Release 3.8	Support for the 8-Port Clear-Channel T3/E3 Serial SPA (SPA-8XT3/E3) was introduced on the Cisco ASR 1000 Series SIPs.
Cisco IOS XE Release 2.6	Support for the 1-Port Channelized OC-12/STM-4 SPA was introduced on the Cisco ASR 1000 Series SIPs.
Cisco IOS XE Release 2.2	Support for the 1-Port Channelized OC-3/STM-1 SPA was introduced on the Cisco ASR 1000 Series SIPs.
Cisco IOS XE Release 2.1	Support for the following SPAs was introduced on the Cisco ASR 1000 Series SIPs: • 2-Port T3/E3 Serial SPA (SPA-2XT3/E3) • 4-Port T3/E3 Serial SPA (SPA-4XT3/E3) • 8-Port Channelized T1/E1 Serial SPA (SPA-8XCHT1/E1) • 2-Port Channelized T3 SPA(SPA-2XCT3/DS0) • 4-Port Channelized T3 SPA (SPA-4XCT3/DS0) • 4-Port Serial SPA (SPA-4TX-Serial)

Supported Features

Note There are some variations in the support provided by SPA models and software releases. These differences are described in the Restrictions, on page 5, and in the corresponding configuration chapter pertaining to that SPA.

The following is a list of some of the significant software features supported by the serial SPAs on the Cisco ASR 1000 Series Aggregation Services Routers:

- Software selectable between T1, E1, T3, or E3 framing on each card (all the ports can be simultaneously configured as T1, E1, T3, or E3). Applies to the 2-Port and 4-Port Clear-Channel T3/E3 SPAs and the 8-Port Channelized T1/E1 SPA.
- Layer 2 encapsulation support:
  - Point-to-Point Protocol (PPP)
  - High-level Data Link Control (HDLC)
  - Frame Relay
- Internal or network clock (selectable per port).

- Online insertion and removal (OIR).
- Hot Standby Router Protocol (HSRP).
- Alarm reporting: 24-hour history maintained, 15-minute intervals on all errors.
- 16-bit and 32-bit cyclic redundancy checks (CRC) supported (16-bit is the default).
- Local and remote loopback.
- Bit error rate testing (BERT) pattern generation and detection per port.
- Programmable BERT pattern enhancements.

Note The programmable BERT pattern enhancements are not supported on the 2-Port, 4-Port, and 8-Port Clear-Channel T3/E3 Serial SPAs and the 8-Port Channelized T1/E1 SPA.

- Dynamic provisioning—Allows for the addition of new customer circuits within a channelized interface without affecting other customers.
- Field-programmable device (FPD) upgrades.
- End-to-end FRF.12 fragmentation support (Quantum Flow Processor [QFP] based).
- QFP-based Multilink PPP (MLPPP) and Link Fragmentation and Interleaving (LFI).
- Support for MLPPP across all SPAs.
- Support for MLPPP using any combination of E1, T1, and NxDS0 member links.
- Compressed Real-Time Protocol (cRTP)—8-Port Channelized T1/E1 Serial SPA and 2-Port and 4-Port Channelized T3 SPAs only.
- Effective from Cisco IOS XE Release 3.9, the 8-Port Clear-Channel T3/E3 Serial SPA is supported on the Cisco ASR1000-SIP10, the Cisco ASR 1001 Router, the Cisco ASR 1002 Router, and the Cisco ASR 1002-F Router.
- T1 features
  - All ports can be fully channelized down to DS0.
  - Data rates in multiples of 56 Kbps or 64 Kbps per channel.
  - Maximum 1.536 Mbps for each T1 port.
  - D4 Superframe (SF) and Extended Superframe (ESF) support for each T1 port.
  - ANSI T1.403 and AT&T TR54016 CI FDL support.
  - Internal and receiver recovered clocking modes.
  - Short haul and long haul channel service unit (CSU) support.
  - Bipolar eight zero substitution (B8ZS) and alternate mark inversion (AMI) line encoding.

Note B8ZS and AMI line encoding are not configurable for TW on the 2-Port and 4-Port Channelized T3 SPA.

- E1 features

Note E1 is not supported on the 1-Port Channelized OC-12/STM-4 SPA in Cisco IOS XE Release 2.6.

- ◦ Maximum 1.984 Mbps for each E1 port in framed mode and a 2.048 Mbps in unframed E1 mode.
  ◦ All ports can be fully channelized down to DS0.
  ◦ Compliant with ITU G7.03, G.704, ETSI and ETS300156.
  ◦ Internal and receiver recovered clocking modes.
  ◦ Hi-density bipolar with three zones (HDB3) and AMI line encoding.

- E3 features

Note E3 is not supported on the 1-Port Channelized OC-12/STM-4 SPA in Cisco IOS XE Release 2.6.

- ◦ Full duplex connectivity at E3 rate (34.368 MHz).
  ◦ Supports ITU-T G.751 or G.832 framing (software selectable).
  ◦ HD3B line coding.
  ◦ Compliant with E3 pulse mask.
  ◦ Line build-out: configured for up to 450 feet (135 m) of type 728A or equivalent coaxial cable.
  ◦ Loopback modes: data terminal equipment (DTE), local, dual, and network.
  ◦ E3 alarm/event detection (once per second polling):

- Alarm indication signal (AIS)
- Loss of frame (LOF)
- Remote alarm indication (RAI)

- ◦ Subrate and scrambling features for these data service unit (DSU) vendors:

- Digital Link
- ADC Kentrox

- T3 features
  ◦ Binary 3-zero substitution (B3ZS) line coding.
  ◦ Compliant with DS3 pulse mask per ANSI T1.102-1993.
  ◦ DS3 far-end alarm and control (FEAC) channel support.
  ◦ Full duplex connectivity at DS3 rate (44.736 MHz).
  ◦ 672 DS0s per T3.

- Loopback modes: DTE, local, remote, dual, and network.
- C-bit or M23 framing (software selectable).
- Line build-out: configured for up to 450 feet (135 m) of type 734A or equivalent coaxial cable.
- DS3 alarm/event detection (once per second polling):

- AIS
- Out of frame (OOF)
- Far-end receive failure (FERF)

- Generation and termination of DS3 Maintenance Data Link (MDL) in C-bit framing.
- Full FDL support and FDL performance monitoring.

Note FDL is not supported on the 2-Port, 4-Port, and 8-Port Clear-Channel T3/E3 SPAs. Whereas, FDL is supported on the 2-Port and 4-Port Channelized T3 SPAs, the 1-Port Channelized OC-3/STM-1 SPA, and the 1-Port Channelized OC-12/STM-4 SPA.

- Subrate and scrambling features for these DSU vendors:

– Cisco
– Digital Link
– ADC Kentrox
– Adtran
– Verilink
– Larscom

Note Mixed Port type (T3/E3) is supported on the 8-Port Clear-Channel T3/E3 SPA.

Restrictions

Consider the following restrictions when configuring the serial SPAs on the Cisco ASR 1000 Series Aggregation Services Routers:

Note For additional information, see also the configuration chapters for the corresponding SPA model. For other SIP-specific features and restrictions see also Overview of the Serial SPAs, on page 1.

- FRF.16—Multilink Frame Relay (MLFR) is not supported.

- MLPPP is only supported on serial PPP interfaces. MLPPP is not supported over Frame Relay, ATM, or PPPoE interfaces.
- On a 2-Port and 4-Port Channelized T3 SPA, when one of the T3 ports is configured as a DS3 Clear-Channel interface and the other T3 ports are configured with a large number (greater than or equal to 400) of low bandwidth channels (NxDS0, N=1, 2, 3, or 4), the DS3 Clear-Channel interface is not able to run at 100 percent DS3 line rate when the low bandwidth channels are idle (when not transmitting or receiving packets). This issue does not occur if the low bandwidth channels are not idle.
- The maximum number of channels supported on the channelized SPAs are:
  - 1023 channels per SPA—On a 2-Port and 4-Port Channelized T3 SPA or 1-Port Channelized OC-3/STM-1 SPA.
  - 2000 NxDS0 per SPA—On a 1-Port Channelized OC-12/STM-4 SPA.
- On a 2-Port and 4-Port Channelized T3 SPA or 1-Port Channelized OC-3/STM-1 SPA, the maximum number of FIFO buffers is 4096. The FIFO buffers are shared among the interfaces; how they are shared is determined by speed. If all the FIFO buffers have been assigned to existing interfaces, a new interface cannot be created, and the "%Insufficient FIFOs to create channel group" error message is seen.

To find the number of available FIFO buffers, use the **show controller t3** command:

```
Router# show controller t3 1/0/0

T3 1/0/0 is up.
  Hardware is SPA-4XCT3/DS0
  IO FPGA version: 2.6, HDLC Framer version: 0
  T3/T1 Framer(1) version: 2, T3/T1 Framer(2) version: 2
  SUBRATE FPGA version: 1.4
  HDLC controller available FIFO buffers 3112
```

The following table provides information about FIFO allocation.

Table 1: FIFO Allocation

Number of Time Slots	Number of FIFO Buffers
1–6 DS0	4
7–8 DS0	6
9 DS0	6
10–12 DS0	8
13–23 DS0	12
1–6 E1 TS	4
7–9 E1 TS	6
11–16 E1 TS	8
17–31 E1 TS	16

Number of Time Slots	Number of FIFO Buffers
T1	12
E1	16
DS3	336

Supported MIBs

The following MIBs are supported for the serial SPAs on the Cisco ASR 1000 Series Routers:

Serial SPAs

- CISCO-ENTITY-ALARM-MIB
- CISCO-CLASS-BASED-QOS-MIB
- CISCO-ENTITY-ASSET-MIB
- CISCO-ENTITY-FRU-CONTROL-MIB
- CISCO-ENTITY-SENSOR-MIB
- ENTITY-MIB
- IF-MIB
- RMON-MIB
- MPLS-LDP-STD-MIB
- MPLS-LSR-STD-MIB
- MPLS-TE-MIB
- MPLS-VPN-MIB

2-Port, 4-Port, and 8-Port Clear-Channel T3/E3 SPAs

- DS3-MIB

8-Port Channelized T1/E1 SPA

- DS1-MIB

2-Port and 4-Port Channelized T3 SPA

- DS1-MIB
- DS3-MIB
- CISCO-FRAME-RELAY-MIB

- IANAifType-MIB -- not in MIB doc
- RFC1381-MIB -- not in MIB doc

1-Port Channelized STM-1/OC-3 SPA

- DS1-MIB
- DS3-MIB
- SONET-MIB

1-Port Channelized OC-12/STM-4 SPA

- CISCO-ENTITY-ALARM-MIB
- CISCO-ENTITY-FRU-CONTROL-MIB
- CISCO-ENTITY-SENSOR-MIB
- CISCO-ENTITY-VENDORTYPE-OID-MIB
- CISCO-SONET-MIB
- DS1-MIB
- DS-3-MIB
- ENTITY-MIB
- ENTITY-SENSOR-MIB
- IF-MIB
- SONET-MIB

To locate and download MIBs for selected platforms, Cisco IOS XE releases, and feature sets, use Cisco MIB Locator found at the following URL:

http://tools.cisco.com/ITDIT/MIBS/servlet/index

If Cisco MIB Locator does not support the MIB information that you need, you can also obtain a list of supported MIBs and download MIBs from the Cisco MIBs page at the following URL:

http://www.cisco.com/public/sw-center/netmgmt/cmtk/mibs.shtml

To access Cisco MIB Locator, you must have an account on Cisco.com. If you have forgotten or lost your account information, send a blank e-mail to cco-locksmith@cisco.com. An automatic check will verify that your e-mail address is registered with Cisco.com. If the check is successful, account details with a new random password will be e-mailed to you. Qualified users can establish an account on Cisco.com by following the directions found at this URL:

https://tools.cisco.com/RPF/register/register.do

Displaying the SPA Hardware Type

To verify the SPA hardware type that is installed in your Cisco ASR 1000 Series Routers, you can use the **show platform** command or the **show interface** command (once the interface has been configured). There are several other commands on the Cisco ASR 1000 Series Routers that also provide SPA hardware information.

The following table shows the hardware description that appears in the **show** command output for each type of SPA that is supported on the Cisco ASR 1000 Series Routers.

Table 2: SPA Hardware Descriptions in show Commands

SPA	Description in show interfaces and show controllers Commands
2-Port Clear-Channel T3/E3 SPA	"Hardware is SPA-2XT3/E3"
4-Port Clear-Channel T3/E3 SPA	"Hardware is SPA-4XT3/E3"
8-Port Clear-Channel T3/E3 SPA	"Hardware is SPA-8XT3/E3"
8-Port Channelized T1/E1 SPA	"Hardware is SPA-8XCHT1/E1-V2"
4-Port Serial Interface SPA	"Hardware is SPA-4XT-SERIAL"
1-Port Channelized OC-3/STM-1 SPA	"Hardware is SPA-1XCHSTM1/OC3"
1-Port Channelized OC-12/STM-4 SPA	"Hardware is SPA-1XCHOC12/DS0"

Examples of the show interfaces Command

The following example shows an output of the **show interfaces serial** command on a Cisco ASR 1000 Series Router with a 4-Port Clear-Channel T3/E3 SPA installed in slot 2:

```
router#: show interfaces serial 2/0/0
Serial2/0/0 is up, line protocol is up
Hardware is SPA-4XT3/E3[3/0]
MTU 4470 bytes, BW 44210 Kbit, DLY 200 usec,
reliability 248/255, txload 1/255, rxload 1/255
Encapsulation HDLC, crc 16, loopback not set
Keepalive set (10 sec)
Last input 00:00:06, output 00:00:07, output hang never
Last clearing of ''show interface'' counters 00:00:01
Input queue: 0/75/0/0 (size/max/drops/flushes); Total output drops: 0
Queueing strategy: fifo
Output queue: 0/40 (size/max)
5 minute input rate 0 bits/sec, 0 packets/sec
5 minute output rate 0 bits/sec, 0 packets/sec
0 packets input, 0 bytes, 0 no buffer
Received 0 broadcasts (0 IP multicast)
0 runts, 0 giants, 0 throttles
0 parity
0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored, 0 abort
0 packets output, 0 bytes, 0 underruns
0 output errors, 0 applique, 0 interface resets
```

```
0 output buffer failures, 0 output buffers swapped out
0 carrier transitions
```

The following example shows an output of the **show interfaces serial** command on a Cisco ASR 1000 Series Router with a 8-Port Clear-Channel T3/E3 SPA installed in slot 1:

```
router# show interfaces serial 1/0/0 controller
Serial1/0/0 is up, line protocol is up
  Hardware is SPA-8XT3/E3
  MTU 4470 bytes, BW 44210 Kbit/sec, DLY 200 usec,
     reliability 255/255, txload 1/255, rxload 1/255
  Encapsulation HDLC, crc 16, loopback not set
  Keepalive set (10 sec)
  Last input 00:00:01, output 00:00:04, output hang never
  Last clearing of "show interface" counters never
  Input queue: 0/375/0/0 (size/max/drops/flushes); Total output drops: 0
  Queueing strategy: fifo
  Output queue: 0/40 (size/max)
  5 minute input rate 0 bits/sec, 0 packets/sec
  5 minute output rate 0 bits/sec, 0 packets/sec
     22 packets input, 528 bytes, 0 no buffer
     Received 0 broadcasts (0 IP multicasts)
     0 runts, 0 giants, 0 throttles
              0 parity
     0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored, 0 abort
     22 packets output, 528 bytes, 0 underruns
     0 output errors, 0 applique, 4 interface resets
     0 unknown protocol drops
     0 output buffer failures, 0 output buffers swapped out
     3 carrier transitions
```

The following example shows an output of the **show interfaces serial** command on a Cisco ASR 1000 Series Router with an 8-Port Channelized T1/E1 SPA installed in slot 0:

```
router# show interfaces serial 0/3/0:0
Serial0/3/0:0 is up, line protocol is up
  Hardware is SPA-8XCHT1/E1
  Internet address is 79.1.1.2/16
  MTU 1500 bytes, BW 1984 Kbit, DLY 20000 usec,
     reliability 255/255, txload 240/255, rxload 224/255
  Encapsulation HDLC, crc 16, loopback not set
  Keepalive not set
  Last input 3d21h, output 3d21h, output hang never
  Last clearing of ''show interface'' counters never
  Input queue: 0/375/0/0 (size/max/drops/flushes); Total output drops: 2998712
  Queueing strategy: fifo
  Output queue: 0/40 (size/max)
  5 minute input rate 1744000 bits/sec, 644 packets/sec
  5 minute output rate 1874000 bits/sec, 690 packets/sec
     180817311 packets input, 61438815508 bytes, 0 no buffer
     Received 0 broadcasts (0 IP multicasts)
     0 runts, 0 giants, 0 throttles
     2 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored, 2 abort
     180845200 packets output, 61438125092 bytes, 0 underruns
     0 output errors, 0 collisions, 2 interface resets
     0 output buffer failures, 0 output buffers swapped out
     1 carrier transitions no alarm present
  Timeslot(s) Used:1-31, subrate: 64Kb/s, transmit delay is 0 flags 2
```

Examples of the show controllers Command

The following example shows an output of the **show controllers serial** command on a Cisco ASR 1000 Series Router with a 2-Port Clear-Channel T3/E3 SPA installed in slot 2:

```
Router# show controllers serial 2/2/0
Serial2/2/0 - (SPA-2XT3/E3) is up
   Current mode is T3
   Framing is c-bit, Clock Source is Line
```

```
   Bandwidth limit is 44210, DSU mode 0, Cable length is 10 feet
   rx FEBE since last clear counter 0, since reset 0
   Data in current interval (820 seconds elapsed):
     0 Line Code Violations, 0 P-bit Coding Violation
     0 C-bit Coding Violation
     0 P-bit Err Secs, 0 P-bit Sev Err Secs
     0 Sev Err Framing Secs, 0 Unavailable Secs
     0 Line Errored Secs, 0 C-bit Errored Secs, 0 C-bit Sev Err Secs
     0 Severely Errored Line Secs
     0 Far-End Errored Secs, 0 Far-End Severely Errored Secs
     0 CP-bit Far-end Unavailable Secs
     0 Near-end path failures, 0 Far-end path failures
     0 Far-end code violations, 0 FERF Defect Secs
     0 AIS Defect Secs, 0 LOS Defect Secs
  Data in Interval 1:
     0 Line Code Violations, 0 P-bit Coding Violation
     0 C-bit Coding Violation
     0 P-bit Err Secs, 0 P-bit Sev Err Secs
     0 Sev Err Framing Secs, 0 Unavailable Secs
```

The following example shows an output of the **show controllers serial** command on a Cisco ASR 1000 Series Router with a 2-Port Clear-Channel T3/E3 SPA installed in slot 2:

```
Router# show controllers serial 2/2/0
Serial1/0/1 - (SPA-8XT3/E3) is up
Current mode is T3
Framing is c-bit, Clock Source is Line
Bandwidth limit is 44210, DSU mode 0, Cable length is 10 feet
rx FEBE since last clear counter 0, since reset 0
Tabular MIB:
INTERVAL      LCV   PCV   CCV   PES  PSES  SEFS   UAS   LES   CES  CSES
01:30-01:36     0     0     0     0     0     0     0     0    14    14
01:15-01:30     1     0     0     0     0     0     1     1     0     0
Total           1     0     0     0     0     0     1     1     0     0
No alarms detected.
No FEAC code is being received
MDL transmission is disabled
```

The following example shows an output of the **show controllers** command on a Cisco ASR 1000 Series Router with an 8-Port Channelized T1/E1 SPA installed in slot 0:

```
Router# show controllers e1 0/3/0 brief
E1 0/3/0 is up.
  Applique type is SPA-8XCHT1/E1
  No alarms detected.
  alarm-trigger is not set
  Framing is crc4, Line Code is HDB3, Clock Source is Line.
  Data in current interval (571 seconds elapsed):
     0 Line Code Violations, 0 Path Code Violations
     0 Slip Secs, 0 Fr Loss Secs, 0 Line Err Secs, 0 Degraded Mins
     0 Errored Secs, 0 Bursty Err Secs, 0 Severely Err Secs, 0 Unavail Secs
  Total Data (last 24 hours)
     0 Line Code Violations, 0 Path Code Violations,
     0 Slip Secs, 0 Fr Loss Secs, 0 Line Err Secs, 0 Degraded Mins,
     0 Errored Secs, 0 Bursty Err Secs, 0 Severely Err Secs, 0 Unavail Secs
```

The following example shows an output of the **show controllers** command on a Cisco ASR 1000 Series Router with a 4-Port Channelized T3 SPA installed in slot 2:

```
Router# show controllers t3
T3 2/0/0 is up.
  Hardware is SPA-2XCT3/DS0
  IO FPGA version: 2.7, HDLC Framer version: 0
  T3/T1 Framer(1) version: 2
  SUBRATE FPGA version: 1.4
  HDLC controller available FIFO buffers 4084
  Applique type is Channelized T3/T1
  No alarms detected.
  MDL transmission is disabled

  FEAC code received: No code is being received
  Framing is C-BIT Parity, Line Code is B3ZS, Cablelength is 224
```

```
  Clock Source is Internal
  Equipment customer loopback
  Data in current interval (204 seconds elapsed):
     2 Line Code Violations, 6 P-bit Coding Violation
     0 C-bit Coding Violation, 1 P-bit Err Secs
     1 P-bit Severely Err Secs, 1 Severely Err Framing Secs
     0 Unavailable Secs, 1 Line Errored Secs
     1 C-bit Errored Secs, 1 C-bit Severely Errored Secs
     0 Severely Errored Line Secs
     0 Far-End Errored Secs, 0 Far-End Severely Errored Secs
     11 CP-bit Far-end Unavailable Secs
     0 Near-end path failures, 1 Far-end path failures
     0 Far-end code violations, 10 FERF Defect Secs
     0 AIS Defect Secs, 0 LOS Defect Secs
  T1 1 is down
  timeslots: 1-24
  FDL per AT&T 54016 spec.
  Transmitter is sending LOF Indication.
  Receiver is getting AIS.
  Framing is ESF, Clock Source is Internal
  Data in current interval (202 seconds elapsed):
     0 Line Code Violations, 0 Path Code Violations
     0 Slip Secs, 0 Fr Loss Secs, 0 Line Err Secs, 0 Degraded Mins
     0 Errored Secs, 0 Bursty Err Secs, 0 Severely Err Secs
     9 Unavail Secs, 0 Stuffed Secs
     5 Near-end path failures, 0 Far-end path failures, 0 SEF/AIS Secs
  T1 2
    Not configured.
  T1 3
    Not configured.
```

The following example shows an output of the **show controllers sonet** command on a Cisco ASR 1000 Series Aggregation Services Router with a 1-Port Channelized STM-1/OC-3 SPA installed in slot 1:

```
Router# show controllers sonet 1/0/0

SONET 1/0/0 is up.
  Hardware is SPA-1XCHSTM1/OC3
  IO FPGA version: 1.7, HDLC Framer version: 0
  T3/T1 Framer(1) version: 1
  Sonet/SDH Framer version: 0
  SUBRATE FPGA version: 1.4
  HDLC controller available FIFO buffers 3760
 Applique type is Channelized Sonet/SDH

 Clock Source is Line
Medium info:
  Type: Sonet, Line Coding: NRZ,
 SECTION:
  LOS = 0          LOF = 0                           BIP(B1) = 85

SONET/SDH Section Tables
  INTERVAL       CV    ES   SES  SEFS
  23:15-23:20     0     0     0     0
  23:00-23:15     0     0     0     0
  22:45-23:00    85     1     1     0
Total of Data in Current and Previous Intervals
  22:45-23:20    85     1     1     0
(remaining text not shown)
```