CHAPTER 6

Overview of the ATM SPAs

This chapter provides an overview of the release history, features, and MIB support for the 1-Port OC-48c/STM-16 ATM SPA, 1-Port OC-12c/STM-4 ATM SPA, and the 2-Port and 4-Port OC-3c/STM-1 ATM SPA. This chapter includes the following sections:

Release History

Release	Modification
12.2(33)SXI	Support was restored for the ATM SPAs.
12.2(33)SXH	Support was temporarily removed for the ATM SPAs.
12.2(18)SXF2	• Support for the "Enhancements to RFC 1483 Spanning Tree Interoperability" feature was added for ATM SPAs on the Cisco 7600 series router and Catalyst 6500 series switch. • Documentation of a workaround for ATM SPA configuration on the Cisco 7600 SIP-200 has been added in Chapter 7, "Configuring the ATM SPAs" to address a Routed Bridge Encapsulation (RBE) limitation where only one remote MAC address is supported.
12.2(18)SXF	Support was introduced for the 1-Port OC-48c/STM-16 ATM SPA on the Cisco 7600 SIP-400 on the Cisco 7600 series router and Catalyst 6500 series switch.
12.2(18)SXE	• Support was introduced for the 2-Port and 4-Port OC-3c/STM-1 ATM SPAs on the Cisco 7600 SIP-200 and Cisco 7600 SIP-400 SPA interface processors (SIPs) on the Cisco 7600 series router and Catalyst 6500 series switch. • Support was introduced for the 1-Port OC-12c/STM-4 ATM SPA on the Cisco 7600 SIP-400 carrier card on the Cisco 7600 series router and Catalyst 6500 series switch.

Overview

The ATM SPAs are single-width, double-height, cross-platform Optical Carrier (OC) ATM adapter cards that provide OC-3c/STM-1c (155.52 Mbps), OC-12c/STM-4c (622.080 Mbps), or OC-48/STM-16 (2488 Mbps) connectivity and can be used in a Catalyst 6500 Series switch. The ATM SPAs come in the following models:

- 2-Port and 4-Port OC-3c/STM-1 ATM SPA (SPA-2XOC3-ATM=, SPA-4XOC3-ATM=)
- 1-Port OC-12c/STM-4 ATM SPA (SPA-1XOC12-ATM=)
- 1-Port OC-48c/STM-16 ATM SPA (SPA-1XOC48-ATM=)

The OC-3c ATM SPAs must be installed in a Cisco 7600 SIP-200 or Cisco 7600 SIP-400 SPA interface processor (SIP) before they can be used in the Catalyst 6500 Series switch. The 1-Port OC-12c/STM-4 ATM SPA and 1-Port OC-48c/STM-16 ATM SPA card must be installed in a Cisco 7600 SIP-400 before it can be used in the Catalyst 6500 Series switch.

You can install the SPA in the SIP carrier before or after you insert the SIP into the switch chassis. This allows you to perform online insertion and removal (OIR) operations either by removing individual SPAs from the SIP, or by removing the entire SIP (and its contained SPAs) from the switch chassis.

The ATM SPAs provide cost-effective wide area networking (WAN) connectivity for service providers across their existing ATM networks. Using a highly modular approach, the SPA and SIP form factors maximize the flexibility of an existing Catalyst 6500 Series switch, allowing service providers to mix and match SPAs to more easily meet evolving port-density and networking media needs.

The ATM SPAs also use small form-factor pluggable (SFP) optical transceivers, giving service providers port-level flexibility for different types of optical media (such as single mode and multimode). Changing the type of optical network involves simply replacing the transceiver, not the SPAs or SIP.

Note A maximum of two ATM SPAs can be installed in each SIP, and these SPAs can be different models (such as 2-Port OC-3c/STM-1 ATM SPA and 1-Port OC-12c/STM-4 ATM SPA). You can also mix SPAs of different types, such as ATM and POS, in a SIP, depending on the space requirements of the SIPs. An exception is that only one 1-Port OC-48c/STM-16 ATM SPA can be installed in a SIP; the other bay should be left empty.

See the following sections for more information about the ATM SPAs:

- ATM Overview, page 6-3
- PVC and SVC Encapsulations, page 6-3
- PVC and SVC Service Classes, page 6-4
- Advanced Quality of Service, page 6-5

ATM Overview

Asynchronous Transfer Mode (ATM) uses cell-switching and multiplexing technology that combines the benefits of circuit switching (constant transmission delay and guaranteed capacity) with those of packet switching (flexibility and efficiency for intermittent traffic). ATM transmits small cells (53 bytes) with minimal overhead (5 bytes of header and checksum, with 48 bytes for data payload), allowing for very quick switching times between the input and output interfaces on a switch.

ATM is a connection-oriented environment, in which each ATM endpoint (or node) must establish a separate connection to the specific endpoints in the ATM network with which it wants to exchange traffic. This connection (or channel) between the two endpoints is called a virtual circuit (VC).

Each VC is uniquely identified by the combination of a virtual path identifier (VPI) and virtual channel identifier (VCI). The VC is treated as a point-to-point mechanism to another switch or host and is capable of supporting bidirectional traffic.

In an ATM network, a VC can be either a permanent virtual circuit (PVC) or a switched virtual circuit (SVC). A network operator must manually configure a PVC, which remains active until it is manually torn down. An SVC is set up and torn down using an ATM signaling mechanism. On the ATM SPAs, this signaling is based on the ATM Forum User-Network Interface (UNI) specification V3.x and V4.0.

PVC and SVC Encapsulations

PVCs and SVCs are configured with an ATM encapsulation type that is based upon the ATM Adaptation Layer (AAL). The following types are supported:

- AAL5CISCOPPP—AAL5 Cisco PPP encapsulation, which is Cisco's proprietary PPP over ATM encapsulation.
- AAL5MUX—ATM Adaptation Layer 5 MUX encapsulation, also known as null encapsulation, that supports a single protocol (IP or IPX).

- AAL5NLPID—(Supported on ATM SPAs in a Cisco 7600 SIP-200 only) AAL5 Network Layer Protocol Identification (NLPID) encapsulation, which allows ATM interfaces to interoperate with High-Speed Serial Interfaces (HSSIs) that are using an ATM data service unit (ADSU) and running ATM-Data Exchange Interface (DXI).
- AAL5SNAP—AAL5 Logical Link Control/Subnetwork Access Protocol (LLC/SNAP) encapsulation, which supports Inverse ARP and incorporates the LLC/SNAP that precedes the protocol datagram. This allows the use of multiple protocols over the same VC, and is particularly well–suited for encapsulating IP packets.

Note The 1-Port OC-48c/STM-16 ATM SPA supports only AAL5MUX and AAL5SNAP encapsulations.

PVC and SVC Service Classes

ATM was designed with built-in quality of service capabilities to allow it to efficiently multiplex different types of traffic over the same links. To accomplish this, each PVC or SVC is configured with a service class that defines the traffic parameters, such as maximum cell rate or burst rate, for the circuit. The following service classes are available in ATM networks:

- Constant Bit Rate (CBR)—The ATM switch transmits ATM cells in a continuous bit-stream that is suitable for real-time traffic, such as voice and video. CBR is typically used for VCs that need a static amount of bandwidth (constant bit rate or average cell rate) that is continuously available for the duration of the active connection. The ATM switch guarantees that a VC with a CBR service class can send cells at the PCR at any time, but the VC is also free to use only part of the allocated bandwidth, or none of the bandwidth, as well.
- Unspecified Bit Rate (UBR)—The ATM switch does not make any quality of service (QoS) commitment at all to the PVC or SVC, but instead uses a best-effort attempt to send the traffic transmitted by the PVC or SVC. UBR typically is the default configuration and is used for non-critical Internet connectivity, including e–mail, file transfers, web browsing, and so forth. The ATM switch enforces a maximum peak cell rate (PCR) for the VC, to prevent the VC from using all bandwidth that is available on the line.
- Unspecified Bit Rate Plus (UBR+)—UBR+ is a special ATM service class developed by Cisco Systems. UBR+ uses MCR (minimum cell rate) along with PCR (peak cell rate). In UBR+, the MCR is a “soft guarantee” of minimum bandwidth. A switch signals the MCR value at call setup time when a switched VC is created. The ATM switch is then responsible for the guarantee of the bandwidth specified in the MCR parameter. A UBR+ VC is a UBR VC for which the MCR is signaled by the switch and guaranteed by the ATM switch. Therefore, UBR+ affects connection admission control and resource allocation on ATM switches. The UBR+ service class is supported only on SVCs for an ATM SPA. It is not supported on PVCs for an ATM SPA.

Note UBR+ is not supported on the 1-Port OC-48c/STM-16 ATM SPA.

- Variable Bit Rate–Non-Real Time (VBR–nrt)—The ATM switch attempts to guarantee a minimum burst size (MBS) and sustained cell rate (SCR) for non-real-time traffic that is bursty in nature, such as database queries or aggregating large volumes of traffic from many different sources. The ATM switch also enforces a maximum peak cell rate (PCR) for the VC, to prevent the VC from using all bandwidth that is available on the line.

- Variable Bit Rate–Real Time (VBR–rt)—The ATM switch guarantees a minimum burst size (MBS) and sustainable cell rate (SCR) for real-time traffic that is bursty in nature, such as voice, video conferencing, and multiplayer gaming. VBR-rt traffic has a higher priority than VBR-nrt traffic, allowing the real-time traffic to preempt the non-real-time traffic, if necessary. The ATM switch also enforces a maximum peak cell rate (PCR) for the VC, to prevent the VC from using all the bandwidth that is available on the line.

Note The ATM SPAs do not support the available bit rate (ABR) service class, which uses a minimum cell rate (MCR).

Advanced Quality of Service

In addition to the integrated QoS capabilities that are provided by the standard ATM service classes, the ATM SPA cards support a number of advanced QoS features. These features include the following:

- Per-VC and Per-VP Traffic Shaping—Enables service providers to control the bandwidth provided at the VC or VP level. (You cannot shape a VC that is part of a shaped VP. We can however enable both VC and VP shaping simultaneously (as long as shaped VCs use a different VPI value than the shaped VP.)
- Layer 3 (IP) QoS at the Per-VC Level—Allows marking and classifying traffic at the IP layer, for each VC, enabling service providers to control the individual traffic flows for a customer, so as to meet the customer's particular QoS needs. The IP QoS can use the IP type of service (ToS) bits, the RFC 2475 Differentiated Services Code Point (DSCP) bits, and the MPLS EXP bits. WRED, LLQ, CBWFQ, policing, classification, and marking are supported.
- Multiprotocol Label Switching (MPLS)—Allows service providers to provide cost-effective virtual private networks (VPNs) to their customers, while simplifying load balancing and QoS management, without incurring the overhead of extensive Layer 3 routing.
- IP to ATM Mapping—Creates a mapping between the Cell Loss Priority (CLP) bit in ATM cell headers and the IP precedence or IP Differentiated Services Code Point (DSCP) bits.
- VC Bundling—Selects the output VC on the basis of the IP class of service (CoS) bits. (Supported only when using the Cisco 7600 SIP-200 and not the Cisco 7600 SIP-400.)

Note Additional QoS features are expected to be added with each Cisco IOS software release. See the release notes for each release for additional features that might be supported and for the restrictions that might affect existing features.

Supported Features

This section provides a list of some of the primary features supported by the ATM hardware and software:

SIP-Dependent Features

Most features for the ATM SPAs are supported on both the Cisco 7600 SIP-200 and Cisco 7600 SIP-400, but some features are supported only on a particular model of SIP. Table 6-1 lists the features that are supported on only one model of SIP. Any supported features for the ATM SPAs that are not listed in this table are supported on both SIPs.

Table 6-1 SIP-Dependent Feature Support

Feature	Supported on Cisco 7600 SIP-200	Supported on Cisco 7600 SIP-400
AAL5NLPID encapsulation and Routed-NLPID-PDUs	Yes	No
ATM VC Access Trunk Emulation (multi-VLAN to VC)	Yes	No
Bridging of Routed Encapsulations (BRE)	Yes	No
Frame Relay to ATM (FR-ATM) internetworking	No	No
Network-Based Application Recognition (NBAR)	Yes	No
RFC-1483 ATM Half-Bridging and Routed Bridged Encapsulation (RBE)	Yes	No
VC Bundling (Selects the output VC on the basis of the IP CoS bits)	Yes	No
RFC 1483, *Multiprotocol Encapsulation over ATM Adaptation Layer 5*, Multipoint Bridging (MPB) (also known as multi-VC to VLAN)on the 2-Port and 4-Port OC-3c/STM-1c ATM SPA	Yes	No
Aggregate WRED	Yes	Yes

Basic Features

- Bellcore GR-253-CORE SONET/SDH compliance (ITU-T G.707, G.783, G.957, G.958)
- Interface-compatible with other Cisco ATM adapters

Note The ATM SPA is functionally similar to other ATM port adapters on the Catalyst 6500 Series switch, but because it is a different card type, the configuration for the slot is lost when you replace an existing ATM port adapter with an ATM SPA in a SIP.

- Supports both permanent virtual circuits (PVCs) and switched virtual circuits (SVCs)

- An absolute maximum of 16,384 (16 K) configured VCs per ATM SPA (4,096 [4 K] per interface) with the following recommended limitations:
  - On a Cisco 7600 SIP-400, 8000 PVCs are supported on multipoint subinterfaces. The limit of 16,384 PVCs only applies to the Cisco 7600 SIP-200.
  - A recommended maximum number of 2,048 PVCs on all point-to-point subinterfaces for all ATM SPAs in a SIP.
  - A recommended maximum number of 16,380 PVCs on all multipoint subinterfaces for all ATM SPAs in a SIP, and a recommended maximum number of 200 PVCs per each individual multipoint subinterface.
  - A recommended maximum number of 400 SVCs for all ATM SPAs in a SIP.
  - A recommended maximum number of 1,024 PVCs or 400 SVCs using service policies for all ATM SPAs in a SIP.
- Up to 4,096 simultaneous segmentations and reassemblies (SARs) per interface
- Supports a maximum number of 200 PVCs or SVCs using Link Fragmentation and Interleaving (LFI) for all ATM SPAs (or other ATM modules) in a Catalyst 6500 Series switch.
- A maximum number of 1000 PVCs or 400 SVCs configured with MQC policy maps.
- Up to 1,000 maximum virtual templates per switch
- ATM adaptation layer 5 (AAL5) for data traffic
- Hardware switching of multicast packets for point-to-point subinterfaces
- SONET/SDH (software selectable) optical fiber (2-Port and 4-Port OC-3c/STM-1 ATM SPA, 1-Port OC-48c/STM-16 ATM SPA, or 1-Port OC-12c/STM-4 ATM SPA), depending on the model of ATM SPA.
- Uses small form-factor pluggable (SFP) optical transceivers, allowing the same ATM SPA hardware to support multimode (MM), single-mode intermediate (SMI), or single-mode long (SML) reach, depending on the capabilities of the SPA.
- ATM section, line, and path alarm indication signal (AIS) cells, including support for F4 and F5 flows, loopback, and remote defect indication (RDI)
- Operation, Administration, and Maintenance (OAM) cells
- Online insertion and removal (OIR) of individual ATM SPAs from the SIP, as well as OIR of the SIPs with ATM SPAs installed

SONET/SDH Error, Alarm, and Performance Monitoring

- Fiber removed and reinserted
- Signal failure bit error rate (SF-BER)
- Signal degrade bit error rate (SD-BER)
- Signal label payload construction (C2)
- Path trace byte (J1)
- Section Diagnostics:
  - Loss of signal (SLOS)
  - Loss of frame (SLOF)
  - Error counts for B1

  - Threshold crossing alarms (TCA) for B1 (B1-TCA)
- Line Diagnostics:
  - Line alarm indication signal (LAIS)
  - Line remote defect indication (LRDI)
  - Line remote error indication (LREI)
  - Error counts for B2
  - Threshold crossing alarms for B2 (B2-TCA)
- Path Diagnostics:
  - Path alarm indication signal (PAIS)
  - Path remote defect indication (PRDI)
  - Path remote error indication (PREI)
  - Error counts for B3
  - Threshold crossing alarms for B3 (B3-TCA)
  - Loss of pointer (PLOP)
  - New pointer events (NEWPTR)
  - Positive stuffing event (PSE)
  - Negative stuffing event (NSE)
- The following loopback tests are supported:
  - Network (line) loopback
  - Internal (diagnostic) loopback
- Supported SONET/SDH synchronization:
  - Local (internal) timing (for inter-switch connections over dark fiber or WDM equipment)
  - Loop (line) timing (for connecting to SONET/SDH equipment)
  - +/– 4.6 ppm clock accuracy over full operating temperature

Layer 2 Features

- Supports the following encapsulation types:
  - AAL5SNAP (LLC/SNAP)
  - LLC encapsulated Bridged protocol
  - AAL5MUX (VC multiplexing)
  - AAL5NLPID and Routed-NLPID-PDUs (ATM SPAs in a Cisco 7600 SIP-200 only)
  - AAL5CISCOPPP
- Supports the following ATM traffic classes and per-VC traffic shaping modes:
  - Constant bit rate (CBR) with peak rate
  - Unspecified bit rate (UBR) with peak cell rate (PCR)
  - Non-real-time variable bit rate (VBR-nrt)
  - Variable bit rate real-time (VBR-rt)

  - Unspecified bit rate plus (UBR+) on SVCs

Note ATM shaping is supported, but class queue-based shaping is not.

- ATM point-to-point and multipoint connections
- Explicit Forward Congestion Indication (EFCI) bit in the ATM cell header
- Frame Relay to ATM (FR-ATM) internetworking (ATM SPAs in a Cisco 7600 SIP-200 only)
- Integrated Local Management Interface (ILMI) operation, including keepalive, PVC discovery, and address registration and deregistration
- Link Fragmentation and Interleaving (LFI) performed in hardware
- VC–to–VC local switching and cell relay
- RFC 1755, *ATM Signaling Support for IP over ATM*
- ATM User-Network Interface (UNI) signalling 3.0, 3.1, and 4.0 only
- RFC 2225, *Classical IP and ARP over ATM* (obsoletes RFC 1577)
- Unspecified bit rate plus (UBR+) traffic service class on SVCs

Layer 3 Features

- ATM VC Access Trunk Emulation (multi-VLAN to VC) (ATM SPAs in a Cisco 7600 SIP-200 only)
- ATM over MPLS (AToM) in AAL5 mode (except for AToM cell packing)
- ATM over MPLS (AToM) in AAL5/AAL0 VC mode
- Bridging of Routed Encapsulations (BRE) (ATM SPAs in a Cisco 7600 SIP-200 only)
- Distributed Link Fragmentation and Interleaving (dLFI) for ATM (dLFI packet counters are supported, but dLFI byte counters are not supported)
- LFI+DCRTP
- Network-Based Application Recognition (NBAR) (ATM SPAs in a Cisco 7600 SIP-200 only)
- No limitation on the maximum number of VCs per VPI, up to the maximum number of 4,096 total VCs per interface (so there is no need to configure this limit using the **atm vc-per-vp** command, which is required on other ATM port adapters)
- OAM flow connectivity using OAM ping for segment or end-to-end loopback
- PVC multicast (PIM dense and sparse modes)
- Quality of service (QoS):
  - Policing
  - IP-to-ATM class of service (IP precedence and DSCP)
  - Per-VC class-based weighted fair queueing (CBWFQ)
  - Per-VC Layer 3 queuing
  - VC Bundling (Cisco 7600 SIP-200 only)
  - Weighted Random Early Detection (WRED)
  - Aggregate WRED

- RFC 1483, *Multiprotocol Encapsulation over ATM Adaptation Layer 5*:
  - Routed Bridge Encapsulation (RBE) (ATM SPAs in a Cisco 7600 SIP-200 only)
  - Half-bridging (ATM SPAs in a Cisco 7600 SIP-200 only)
  - PVC bridging (full-bridging) is supported on Cisco 7600 SIP-200 and Cisco 7600 SIP-400
- Supports oversubscription by default
- Routing protocols:
  - Border Gateway Protocol (BGP)
  - Enhanced Interior Gateway Routing Protocol (EIGRP)
  - Interior Gateway Routing Protocol (IGRP)
  - Integrated Intermediate System-to-Intermediate System (IS-IS)
  - Open Shortest Path First (OSPF)
  - Routing Information Protocol version 1 and version 2 (RIPv1 and RIPv2)

High Availability Features

- 1+1 Automatic Protection Switching (APS) redundancy (PVC circuits only)
- Route Processor Redundancy (RPR)
- RPR Plus (RPR+)
- OSPF Nonstop Forwarding (NSF)
- Stateful Switchover (SSO)

Enhancements to RFC 1483 Spanning Tree Interoperability

This section describes an interoperability feature for the various spanning tree implementations across 1483 Bridge Mode ATM PVCs. Historically, vendors have not implemented spanning tree across RFC 1483 encapsulation consistently. Some Cisco IOS releases also may not support the full range of spanning-tree options. This feature addresses some of the practical challenges of interworking common variations of spanning tree over RFC 1483 Bridge Mode encapsulation.

Note This feature set is only supported on RFC 1483 Bridge Mode ATM permanent virtual circuits (PVCs).

The following are basic spanning tree terms:

- *IEEE 802.1D* is a standard for interconnecting LANs through media access control (MAC) bridges. IEEE 802.1D uses the Spanning-Tree Protocol to eliminate loops in the bridge topology, which cause broadcast storms.
- *Spanning Tree Protocol (STP)* as defined in IEEE 802.1D is a link-management protocol that provides path redundancy while preventing undesirable loops in the network. An IEEE 802.1D spanning tree makes it possible to have one spanning tree instance for the whole switch, regardless of the number of VLANs configured on the switch.

- *Bridge Protocol Data Unit (BPDU)* is the generic name for the frame used by the various spanning-tree implementations. The Spanning Tree Protocol uses the BPDU information to elect the root switch and root port for the switched network, as well as the root port and designated port for each switched segment.
- *Per VLAN Spanning Tree (PVST)* is a Cisco proprietary protocol that allows a Cisco device to support multiple spanning tree topologies on a per-VLAN basis. PVST uses the BPDUs defined in IEEE 802.1D (see Figure 6-2 on page 6-12), but instead of one STP instance per switch, there is one STP instance per VLAN.
- *PVST+* is a Cisco proprietary protocol that creates one STP instance per VLAN (as in PVST). However, PVST+ enhances PVST and uses Cisco proprietary BPDUs with a special 802.2 Subnetwork Access Protocol (SNAP) Organizational Unique Identifier (OUI)[1] (see Figure 6-2 on page 6-12) instead of the standard IEEE 802.1D frame format used by PVST. PVST+ BPDUs are also known as Simple Symmetric Transmission Protocol (SSTP) BPDUs.

Note RFC 1483 is referenced throughout this section, although it has been superseded by RFC 2684.

Supported Supervisor Engines and Line Cards

The Cisco 7600 series router supports PVST to PVST+ BPDU interoperability with the following line card:

- Cisco 7600 SIP-200

Interoperability Problems

The current interoperability problems can be summarized as follows:

- When transmitting STP BPDUs, many vendors' implementations of ATM-to-Ethernet bridging are not fully compliant with the specifications of RFC 1483, Appendix B. The most common variation of the standard is to use an ATM Common Part Convergence Sublayer (CPCS) SNAP protocol data unit (PDU) with OUI: 00-80-C2 and PID: 00-07. Appendix B reserved this OUI/PID combination for generic Ethernet frames without BPDUs. Appendix B specifies OUI: 00-80-C2 and protocol identifier (PID): 00-0E for frames with BPDU contents.
- There are several varieties of the Spanning-TreeProtocol used by Cisco products on ATM interfaces. The Catalyst 5000 series supports only PVST on ATM interfaces. The Cisco 7600 router and Catalyst 6500 series switches support only PVST+ on ATM interfaces. Most other Cisco routers implement classic IEEE 802.1D on ATM interfaces.

  When the Cisco 7600 series router and the Catalyst 6500 series switch first implemented 1483 Bridging (on Cisco IOS Release 12.1E) on the Cisco 7600 FlexWAN module, the platform used OUI: 00-80-C2 and PID: 00-0E to maximize interoperability with all other Cisco IOS products.

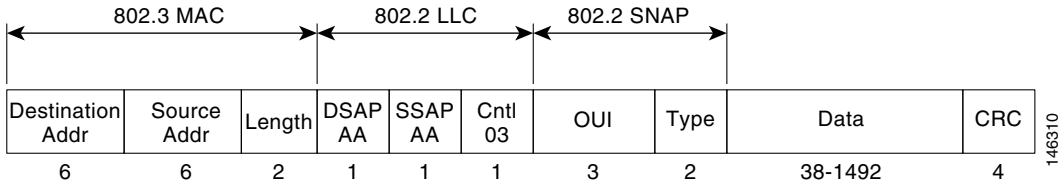
  However, there are so many implementations that do not send PVST or IEEE 802.1D BPDUs with PID: 00-0E that the Cisco 7600 series and the Catalyst 6500 series reverted to the more common implementation of RFC 1483 (with PID: 00-07) in Cisco IOS 12.2SX. This spanning tree interoperability feature provides the option of encapsulating BPDUs across RFC 1483 with either PID: 00-07 or PID: 00-0E.

1. The Organizational Unique Identifier (OUI) portion of the MAC address often identifies the vendor of the upper layer protocol or the manufacturer of the Ethernet adapter. The OUI value of 00-00-0C identifies Cisco Systems as the manufacturer of the Ethernet adapter.

BPDU Packet Formats

This section describes the various BPDU packet formats. Figure 6-1 shows the generic IEEE 802.2/802.3 frame format, which is used by PVST+,—but is not used by PVST.

Figure 6-1 IEEE 802.2/802.3 SNAP Encapsulation Frame Format



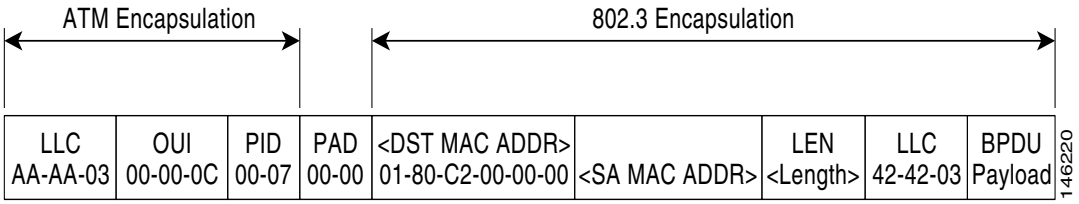
In an Ethernet SNAP frame, the SSAP and DSAP fields are always set to AA. These codes identify it as a SNAP frame. The Control field always has a value of 03, which specifies connectionless logical link control (LLC) services.

The Type field identifies the upper layer protocol to which data should be passed. For example, a Type field of hex 0800 represents IP, while a value of 8137 indicates that data is meant for IPX.

Catalyst 5000 PVST BPDU Packet Format

The Catalyst 5000 series switches send and receive BPDUs in PVST format on ATM interfaces (see Figure 6-2).

Figure 6-2 BPDU PVST Frame Format Used by the Catalyst 5000 Switch



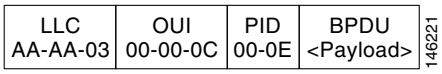
- BPDUs sent by the Catalyst 5000 switch use a PID of 0x00-07, which does not comply with RFC 1483. The Cisco 7600 series router also has the ability to send BPDUs in this data format.
- The PAD portion of the ATM encapsulation varies from 0 to 47 bytes in length to ensure complete ATM cell payloads.
- By using the **bridge-domain** command's **ignore-bpdu-pid** optional keyword, the Catalyst 5000 switch sends this frame by default.
- The Catalyst 5000 switch cannot accept the PVST+ BPDUs and blocks the ATM port, giving the following error message:

```
%SPANTREE-2-RX_1QNON1QTRUNK: Rcved 1Q-BPDU on non-1Q-trun port 6/1 vlan 10
%SPANTREE-2-RX_BLKPORTPVID: Block 6/1 on rcving vlan 10 for inc peer vlan 0
```

Cisco 7200 and Cisco 7500 Routers IEEE 802.1D BPDU Frame Format

Figure 6-3 shows the Cisco 7200 and Cisco 7500 series routers IEEE 802.1D BPDU frame format:

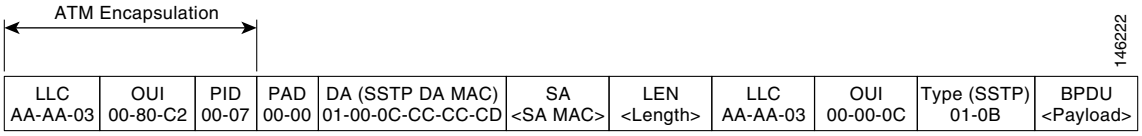
Figure 6-3 Frame Format for the Cisco 7200 and Cisco 7500 Routers IEEE 802.1D BPDU



Cisco 7600 Router PVST+ BPDU Frame Format

The Cisco 7600 series router PVST+ BPDU packet format is shown in Figure 6-4. These BPDUs are not IEEE 802.1D BPDUs, but Cisco proprietary SSTP BPDUs.

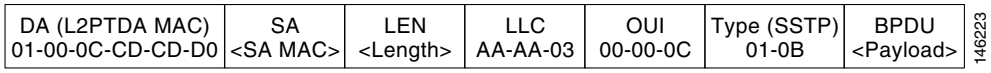
Figure 6-4 Cisco 7600 Router PVST+ BPDU Frame Format (1483 Bridge Mode)



Cisco L2PT BPDU Frame Format

Figure 6-5 shows the Cisco Layer 2 Protocol Tunneling (L2PT) BPDU SNAP frame format.

Figure 6-5 L2PT BPDU SNAP Frame Format



Unsupported Features

- The following high availability features are not supported:
  - APS N+1 redundancy is not supported
  - APS redundancy is not supported on SVCs
  - APS reflector mode (**aps reflector** interface configuration command) is not supported
- The **atm bridge-enable** command, which was used in previous releases on other ATM interfaces to enable multipoint bridging on PVCs, is not supported on ATM SPA interfaces. Instead, use the **bridge** option with the **encapsulation** command to enable RFC 1483 half-bridging on PVCs. See the "Configuring ATM Routed Bridge Encapsulation" section on page 7-20.
- PVC autoprovisioning (**create on-demand** VC class configuration command) is not supported.
- Creating SVCs with UNI signalling 4.1 is not supported (UNI signalling 3.0, 3.1, and 4.0 are supported).
- Enhanced Remote Defect Indication–Path (ERDI-P) is not supported.

- Fast Re-Route (FRR) over ATM is not supported.
- LAN Emulation (LANE) is not supported.
- Multicast SVCs are not supported.
- Available Bit Rate (ABR) traffic service class is not supported.
- Unspecified bit rate plus (UBR+) traffic service class is not supported on PVCs.
- VP–to–VP local switching and cell relay are not supported.

Prerequisites

- The 2-Port and 4-Port OC-3c/STM-1 ATM SPAs must use either the Cisco 7600 SIP-200 or Cisco 7600 SIP-400.
- The 1-Port OC-12c/STM-4 ATM SPA must use the Cisco 7600 SIP-400.
- The 1-Port OC-48c/STM-16 ATM SPA must use the Cisco 7600 SIP-400.
- The Cisco 7600 SIP-200 requires a Catalyst 6500 Series switch using a SUP-720 3B and above processor that is running Cisco IOS Release 12.2(18)SXE or later release.
- The Cisco 7600 SIP-400 requires a Catalyst 6500 Series switch using a SUP-720 processor that is running Cisco IOS Release 12.2(18)SXE or later release.
- Before beginning to configure the ATM SPA, have the following information available:
  - Protocols you plan to route on the new interfaces.
  - IP addresses for all ports on the new interfaces, including subinterfaces.
  - Bridging encapsulations you plan to use.

Restrictions

Note For other SIP-specific restrictions, see the "Restrictions" section on page 3-15.

- The 1-Port OC-48c/STM-16 ATM SPA does not support the following features: AToM, BRE, LFI, RBE, SVCs, UBR+, RFC 2225 (formerly RFC 1577), or bridging.
- The ATM SPAs in the Catalyst 6500 Series switch do not support APS reflector and reflector channel modes. (These modes require a facing PTE, which is typically a Cisco ATM switch.)
- The ATM SPA is functionally similar to other ATM port adapters on the Catalyst 6500 Series switch, such as the PA-A3, but it is a different card type, so the slot's previous configuration is lost when you replace an existing ATM port adapter with an ATM SPA.
- The following restrictions apply to the operation of QoS on the ATM SPAs:
  - The ATM SPAs do not support bandwidth-limited priority queueing, but support only strict priority policy maps (that is, the **priority** command without any parameters).
  - A maximum of one **priority** command is supported in a policy map.
  - You cannot use the **match input interface** command in policy maps and class maps that are being used for ATM SPAs.

  - Hierarchical traffic shaping (traffic shaping on both the VC and VP for a circuit) is not supported. Traffic shaping can be configured only on the VC or on the VP, but not both.
  - ATM (Layer 2) output shaping is supported, but IP (Layer 3) shaping on an output (egress) interface is not supported. In particular, this means that you cannot use any **shape** class-map configuration commands in policy maps that are being used in the output direction. This includes the **shape adaptive**, **shape average**, **shape fecn-adapt**, and **shape peak** commands.
  - The ATM SPA interfaces support a maximum of six configured precedences (using the **random-detect aggregate** command) in each class map in a policy map. The maximum number of configurable subclass groups is 7.
- For best performance, we recommend the following maximums:
  - A maximum number of 2,048 PVCs on all point-to-point subinterfaces for all ATM SPAs in a SIP.
  - A maximum number of 16,380 PVCs on all multipoint subinterfaces for all ATM SPAs in a SIP.
  - A maximum number of 400 SVCs for all ATM SPAs in a SIP carrier card.
  - A maximum number of 1024 PVCs or SVCs s using service policies for all ATM SPAs in a switch.
  - A maximum number of 200 PVCs or SVCs using Link Fragmentation and Interleaving (LFI) for all ATM SPAs in a switch.
  - A maximum number of 200 PVCs on each multipoint subinterface being used on an ATM SPA.

Note These limits are flexible and depend on all factors that affect performance in the switch, such as processor card, type of traffic, and so on.

- In the default configuration of the transmit path trace buffer, the ATM SPA does not support automatic updates of remote host name and IP address (as displayed by the **show controllers atm** command). This information is updated only when the interface is shut down and reactivated (using the **shutdown** and **no shutdown** commands). Information for the received path trace buffer, however, is automatically updated.
- The **show ppp multilink** command displays only the packet counters, and not byte counters, for a dLFI configuration on an ATM SPA interface.

Supported MIBs

The following MIBs are supported in Cisco IOS Release 12.2(18)SXE and later releases for the ATM SPAs on the Catalyst 6500 Series switch.

Common MIBs

- ENTITY-MIB
- IF-MIB
- MIB-II

Cisco-Specific Common MIBs

- CISCO-ENTITY-EXT-MIB
- OLD-CISCO-CHASSIS-MIB

- CISCO-CLASS-BASED-QOS-MIB
- CISCO-ENTITY-FRU-CONTROL-MIB
- CISCO-ENTITY-ASSET-MIB
- CISCO-ENTITY-SENSOR-MIB
- CISCO-MQC-MIB

ATM Industry MIBs

- ATM-MIB (RFC 2515)
- ATM-ACCOUNTING-INFORMATION-MIB (RFC 2512)
- SONET-MIB

Cisco-Specific ATM MIBs

- CISCO-ATM-EXT-MIB
- CISCO-ATM-PVC-MIB
- CISCO-AAL5-MIB
- CISCO-CLASS-BASED-QOS-MIB
- CISCO-IETF-ATM2-PVCTRAP-MIB
- CISCO-MQC-MIB
- CISCO-SONET-MIB

To locate and download MIBs for selected platforms, Cisco IOS releases, and feature sets, use Cisco MIB Locator found at the following URL:

http://tools.cisco.com/ITDIT/MIBS/servlet/index

If Cisco MIB Locator does not support the MIB information that you need, you can also obtain a list of supported MIBs and download MIBs from the Cisco MIBs page at the following URL:

http://www.cisco.com/public/sw-center/netmgmt/cmtk/mibs.shtml

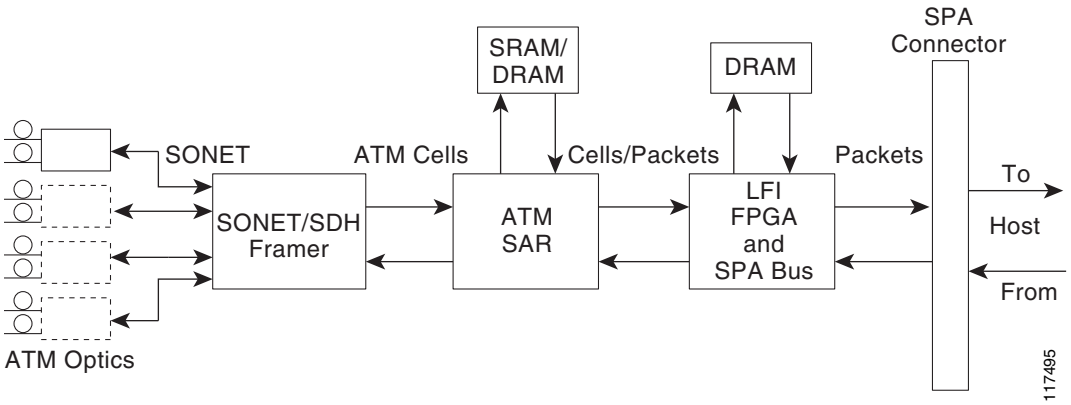
To access Cisco MIB Locator, you must have an account on Cisco.com. If you have forgotten or lost your account information, send a blank e-mail to cco-locksmith@cisco.com. An automatic check will verify that your e-mail address is registered with Cisco.com. If the check is successful, account details with a new random password will be e-mailed to you. Qualified users can establish an account on Cisco.com by following the directions found at this URL:

http://tools.cisco.com/RPF/register/register.do

SPA Architecture

This section provides an overview of the data path for the ATM SPAs, for use in troubleshooting and monitoring. Figure 6-6 shows the data path for ATM traffic as it travels between the ATM optical connectors on the front panel of the ATM SPA to the backplane connector that connects the SPA to the SIP.

Figure 6-6 ATM SPA Data Architecture



Path of Cells in the Ingress Direction

The following steps describe the path of an ingress cell as it is received from the ATM network and converted to a data packet before transmission through the SIP to the switch's processors for switching, routing, or further processing:

1. The SONET/SDH framer device receives incoming cells on a per-port basis from the SPA's optical circuitry. (The ATM SPA supports 1, 2, or 4 optical ports, depending on the model of SPA.)
2. The SONET/SDH framer removes the SONET overhead information, performs any necessary clock and data recovery, and processes any SONET/SDH alarms that might be present. The framer then extracts the 53-byte ATM cells from the data stream and forwards each cell to the ATM segmentation and re-assembly (SAR) engine.
3. The SAR engine receives the cells from the framer and reassembles them into the original packets, temporarily storing them in a per-port receive buffer until they can be forwarded to the LFI FPGA. The SAR engine discards any packets that have been corrupted in transit.
4. The LFI FPGA receives the packets from the SAR engine and forwards them to the host processor for further routing, switching, or additional processing. The FPGA also performs LFI reassembly as needed, and collects the traffic statistics for the packets that it passes.

Path of Packets in the Egress Direction

The following steps describe the path of an egress packet as the SPA receives it from the switch through the SIP and converts it to ATM cells for transmission on the ATM network:

1. The LFI FPGA receives the packets from the host processor and stores them in its packet buffers until the SAR engine is ready to receive them. The FPGA also performs any necessary LFI processing on the packets before forwarding them to the SAR engine. The FPGA also collects the traffic statistics for the packets that it passes.
2. The SAR engine receives the packets from the FPGA and supports multiple CBWFQ queues to store the packets until they can be fully segmented. The SAR engine performs the necessary WRED queue admission and CBWFQ QoS traffic scheduling on its queues before segmenting the packets into ATM cells and shaping the cells into the SONET/SDH framer.

3. The SONET/SDH framer receives the packets from the SAR engine and inserts each cell into the SONET data stream, adding the necessary clocking, SONET overhead, and alarm information. The framer then outputs the data stream out the appropriate optical port.
4. The optical port conveys the optical data onto the physical layer of the ATM network.

Displaying the SPA Hardware Type

To verify the SPA hardware type that is installed in your Catalyst 6500 Series switch, use the **show interfaces** or **show diagbus** commands. A number of other **show** commands also provide information about the SPA hardware.

Table 6-2 shows the hardware description that appears in the **show** command output for each type of ATM SPA that is supported on the Catalyst 6500 Series switch.

Table 6-2 ATM SPA Hardware Descriptions in show Commands

SPA	Description in show interfaces Command	Description in show diagbus Command
SPA-2XOC3-ATM	Hardware is SPA-2XOC3-ATM	SPA-2XOC3-ATM (0x046E)
SPA-4XOC3-ATM	Hardware is SPA-4XOC3-ATM	SPA-4XOC3-ATM (0x3E1)
SPA-1XOC12-ATM	Hardware is SPA-1XOC12-ATM	SPA-1XOC12-ATM (0x03E5)
SPA-1XOC48-ATM	Hardware is SPA-1XOC48-ATM	SPA-1XOC48-ATM (0x3E6)

Example of the show interfaces Command

The following example shows output from the **show interfaces atm** command on a Catalyst 6500 Series switch with an ATM SPA installed in the first subslot of a SIP that is installed in slot 5:

```
Router# show interfaces atm 5/0/0

ATM5/0/0 is up, line protocol is up
  Hardware is SPA-4XOC3-ATM, address is 000d.2959.d780 (bia 000d.2959.d78a)
  MTU 4470 bytes, sub MTU 4470, BW 149760 Kbit, DLY 80 usec,
     reliability 255/255, txload 1/255, rxload 1/255
  Encapsulation ATM, loopback not set
  Encapsulation(s): AAL5
  4095 maximum active VCs, 1 current VCCs
  VC idle disconnect time: 300 seconds
  0 carrier transitions
  Last input 00:00:09, output 00:00:09, output hang never
  Last clearing of "show interface" counters 00:01:26
  Input queue: 0/75/0/0 (size/max/drops/flushes); Total output drops: 0
  Queueing strategy: fifo
  Output queue: 0/40 (size/max)
  5 minute input rate 0 bits/sec, 0 packets/sec
  5 minute output rate 0 bits/sec, 0 packets/sec
     5 packets input, 540 bytes, 0 no buffer
     Received 0 broadcasts (0 IP multicast)
     0 runts, 0 giants, 0 throttles
     0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored, 0 abort
     5 packets output, 720 bytes, 0 underruns
     0 output errors, 0 collisions, 0 interface resets
     0 output buffer failures, 0 output buffers swapped out
```

Note The value for "packets output" in the default version of the **show interfaces atm** command includes the bytes used for ATM AAL5 padding, trailer and ATM cell header. To see the packet count without the padding, header, and trailer information, use the **show interfaces atm statistics** or **show atm pvc** commands.

Example of the show diagbus Command

The following example shows output from the **show diagbus** command on a Catalyst 6500 Series switch with two ATM SPAs installed in a Cisco 7600 SIP-400 that is installed in slot 4:

```
Router# show diagbus 4

Slot 4: Logical_index 8
        4-adapter SIP-400 controller
        Board is analyzed ipc ready
        HW rev 0.300, board revision 08
        Serial Number:  Part number: 73-8272-03

        Slot database information:
        Flags: 0x2004   Insertion time: 0x1961C (01:16:54 ago)

        Controller Memory Size:
                384 MBytes CPU Memory
                128 MBytes Packet Memory
                512 MBytes Total on Board SDRAM
        IOS (tm) cwlc Software (sip1-DW-M), Released Version 12.2(17)SX [BLD-sipedon2 107]

        SPA Information:
        subslot 4/0: SPA-4XOC3-ATM (0x3E1), status: ok
        subslot 4/1: SPA-1XOC12-ATM (0x3E5), status: ok
```

Example of the show controllers Command

The following example shows output from the **show controllers atm** command on a Catalyst 6500 Series switch with an ATM SPAs installed in the second subslot of a SIP that is installed in slot 5:

```
Router# show controllers atm 5/1/0

Interface ATM5/1/0 (SPA-4XOC3-ATM[4/0]) is up
 Framing mode: SONET OC3 STS-3c

SONET Subblock:
SECTION
  LOF = 0          LOS    = 0                           BIP(B1) = 603
LINE
  AIS = 0          RDI    = 2          FEBE = 2332      BIP(B2) = 1018
PATH
  AIS = 0          RDI    = 1          FEBE = 28        BIP(B3) = 228
  LOP = 0          NEWPTR = 0          PSE  = 1         NSE     = 2

Active Defects: None
Active Alarms:  None
Alarm reporting enabled for: SF SLOS SLOF B1-TCA B2-TCA PLOP B3-TCA

ATM framing errors:
  HCS (correctable):   0
  HCS (uncorrectable): 0
```

```
APS
 not configured

PATH TRACE BUFFER : STABLE

BER thresholds:  SF = 10e-3  SD = 10e-6
TCA thresholds:  B1 = 10e-6  B2 = 10e-6  B3 = 10e-6

  Clock source:  line
```