Configuring the Cisco UBR-MC20X20V Cable Interface Line Card

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The Cisco UBR-MC20X20V cable interface line card is designed specifically for the Cisco uBR10012 universal broadband router. This card transmits and receives RF signals between the subscriber and the headend over hybrid fiber-coaxial (HFC) system.

The Cisco UBR-MC20X20V card has high line card CPU speed, memory, and flash memory allowing support of Voice over IP (VoIP) at much higher call loads and a higher percentage of modems running advanced DOCSIS features that typically consume line card CPU resources.

Document Revision History

Document Revision	Date	Change Summary
OL-20959-01	November 16, 2009	Initial version.
OL-20959-02	May 10, 2010	Added information about the new available licenses (10 and 15 downstream) for the Cisco uBR-MC20X20V cable line card.

Finding Support Information for Platforms and Cisco IOS Software Images

Use Cisco Feature Navigator to find information about platform support and Cisco IOS software image support. Access Cisco Feature Navigator at http://www.cisco.com/go/fn. You must have an account on Cisco.com. If you do not have an account or have forgotten your user name or password, click **Cancel** at the login dialog box and follow the instructions that appear.

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Prerequisites for Configuring the Cisco UBR-MC20X20V Cable Interface Line Card

The Cisco UBR-MC20X20V cable interface line card is supported on the Cisco CMTS routers and follows these general prerequisites when being implemented on the Cisco CMTS.

- The Cisco UBR10012 universal broadband router must be running Cisco IOS 12.2(33)SCC release or later to support the Cisco UBR-MC20X20V cable interface line card.
- The Cisco uBR10012 universal broadband router must have two DOCSIS Timing, Communication and Control (DTCC) cards configured before installing the Cisco UBR-MC20X20V cable interface line card.

Note If you use DTCC card, verify that it has the latest firmware version (see Cisco uBR10012 Universal Broadband Router DTCC Card guide for details)

Restrictions for Configuring the Cisco UBR-MC20X20V Cable Interface Line Card

- A bonded channel must be made up of channels only from the local card and not from multiple cable line cards.
- The Cisco UBR-MC20X20V cable interface line card supports Advanced Encryption Standard (AES) encryption. This support holds good only when the BPI is enabled.
- All controllers on the Cisco UBR-MC20X20V cable interface line card must have identical annex setting.
- If Cisco uBR10-MC5X20 line card is used as working line card and Cisco uBR-MC20X20V line card used as protect line card, the HCCP feature is not supported when the working line card is replaced (using Online Insertion and Removal (OIR)) with a Cisco uBR-MC20X20V line card.

Information About the Cisco UBR-MC20X20V Cable Interface Line Card

The Cisco UBR-MC20X20V line cards have five downstream (DS) ports and twenty upstream (US) ports. The line card supports five cable interfaces, and the 20 DS and 20 US channels are dynamically associated with any of these five MAC domains. The card has twenty US spigots and five DS spigots. Each of the US spigots support either two-frequency stacked US channels across ten ports or a single US channel across twenty ports. Each of the DS spigots support four-frequency stacked channels across five ports.

Upstream data, from the subscriber, comes through the upstream ports (US0–US19) on the Cisco UBR-MC20X20V cable interface line card. The line card processes and configures the data and sends it across the backplane to the WAN/ backhaul card and out to the Internet.

Downstream data, to the subscriber, comes from the Internet through the WAN/ backhaul card, and across the backplane to the Cisco UBR-MC20X20V cable interface line card. The Cisco UBR-MC20X20V card processes and configures the data and sends it out through the appropriate radio frequency (RF) channel on a downstream port (DS0–DS4) to be combined with the rest of the downstream signals in the headend.

The Cisco UBR-MC20X20V cable interface line card supports both DOCSIS and EuroDOCSIS cable modem networks. The card supports downstream channels in the 55 to 999 MHz range, and upstream channels in the 5 to 65 MHz range. The Cisco UBR-MC20X20V cable interface line card supports Annex B and Annex A radio frequency (RF) data rates, channel widths, and modulation schemes and has DOCSIS MAC management and spectrum management capabilities. DOCSIS 3.0, A-TDMA, S-CDMA, downstream bonding, and upstream bonding rates are supported.

Figure 1 shows the Cisco UBR-MC20X20V cable interface line card faceplate.

Figure 1 Cisco UBR-MC20X20V Cable Interface Line Card

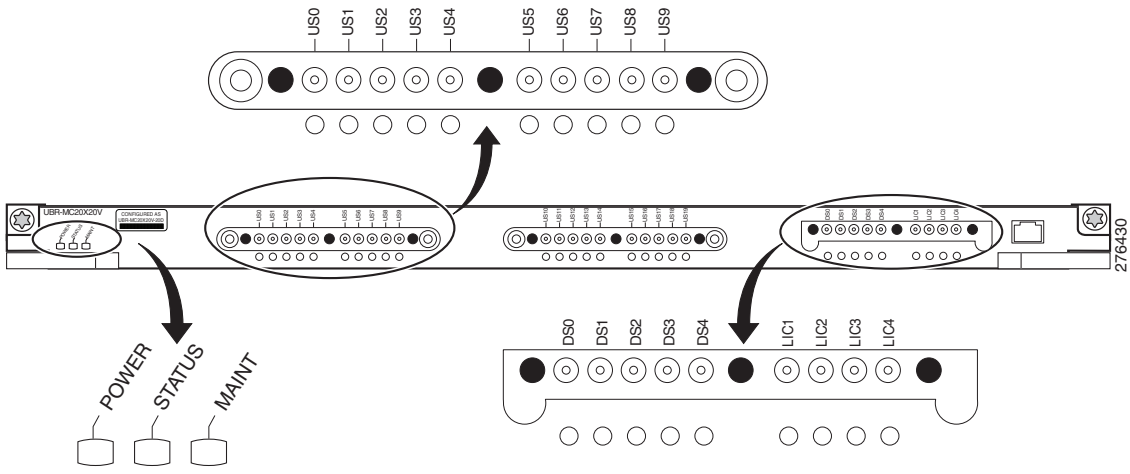

Table 1 describes the LEDs on the Cisco UBR-MC20X20V cable interface line card.

Table 1 Cisco UBR-MC20X20V Card LEDs

LED	Status	Description
POWER	Green	Card is powered on.
	Off	Card is not powered on.
STATUS	Green	Processor has booted and passed diagnostics.
	Blinking Green	Protect mode when the card is the redundant card in the system.
	Yellow	In bootup mode.
	Off	No power to the line card.
MAINT	Yellow	It is safe to remove the line card.
	Off	No action necessary.
US0 through US19	Green	Upstream-enabled path is configured and able to pass traffic.
	Off	Upstream port is not enabled.
DS0 through DS4	Green	RF-enabled downstream path is configured and able to pass traffic out through the upconverter at radio frequencies.
	Off	RF is not enabled. **Note** If the downstream port/interface is "no shut", this LED will be green even if the RF output is shut or the DS frequency is not set.
LIC1 through LIC4	**LIC1–LIC4**	
	Green	Line card supports 20 DS channels.
	Off	Line card supports 0 DS channel
	Blinking green	Invalid or no DS license.
	LIC1	
	Green	Line card supports 5 DS channels
	LIC1–LIC2[1]	
	Green	Line card supports 10 DS channels
	LIC1–LIC3[2]	
	Green	Line card supports 15 DS channels

1. In Cisco IOS Release 12.2(33)SCD2 and later releases, you can use a combination of two UBR-MC20X20V-5D line cards to get a 10 downstream channel license. For more information, see Upgrading the Cisco CMTS Line Card Software License, page 59.
2. In Cisco IOS Release 12.2(33)SCD2 and later releases, you can use a combination of three UBR-MC20X20V-5D line cards to get a 15 downstream channel license. For more information, see Upgrading the Cisco CMTS Line Card Software License, page 59.

Table 2 shows the supported DOCSIS modulation schemes.

Table 2 Supported DOCSIS and EuroDOCSIS Modulation Schemes

Cable Interface Line Card	Downstream Modulation	Upstream Modulation
Cisco UBR-MC20X20V[1]	64–QAM[2], 256–QAM	QPSK[3], 8–, 16–, 32–, 64–QAM

1. The Cisco UBR-MC20X20V cable interface line card has three variants: Cisco UBR-MC20X20V-0D, Cisco UBR-MC20X20V-5D, and Cisco UBR-MC20X20V-20D. The Cisco UBR-MC20X20V-0D line card supports 20 upstreams and zero (no) downstreams. The Cisco UBR-MC20X20V-5D line card supports 20 upstreams and 5 downstreams. However, you can also purchase 10 and 15 downstream upgrade licenses for this line card. Cisco UBR-MC20X20V-20D line card supports 20 upstreams and 20 downstreams.
2. QAM = Quadrature Amplitude Modulation
3. QPSK = Quadrature Phase Shift Keying

Benefits

The Cisco UBR-MC20X20V cable interface line card provides the following benefits:

- Expanded capacity of the Cisco uBR10012 universal broadband router, providing the highest port density available in Cisco cable interface line cards.
- Additional flexibility for cable operators in partitioning the cable plant to address growing subscriber bandwidth demands; enables cost-effective scalability of services and subscribers.
- Online insertion and removal (OIR), allowing key system components to be added or removed without powering off the chassis.
- Hardware-based support for DOCSIS 2.0 (apart from DOCSIS 1.x features) and DOCSIS 3.0 features such as S-CDMA, Multiple Logical Channels, Upstream Channel Bonding, Per Service flow DS ID, and other DOCSIS 3.0 downstream features.

Onboard Failure Logging

The On-Board Failure Logging (OBFL) feature enables storage and collection of critical failure information in the nonvolatile memory of a Field Replaceable Unit (FRU), like a Route Processor (RP) or line card. The Cisco uBR10000 series universal broadband router supports OBFL on PRE4, the Cisco SIP-600 jacket card, Cisco UBR-MC20X20V cable interface line card, and the Cisco UBR-MC5X20H cable interface line card.

The OBFL stored data assists in understanding and debugging field failures upon Return Material Authorization (RMA) of a RP or line card at repair and failure analysis sites.

OBFL records operating temperatures, voltages, hardware uptime and any other important events that assist onboard diagnosis in case of hardware failures.

For more information on the feature, see the Onboard Failure Logging feature guide located at the following URL:

http://www.cisco.com/en/US/docs/ios/12_2sx/12_2sxh/feature/guide/sxhobfl.html#wp1053048

Note The output from the CMTS router may vary slightly compared to the output samples shown in the URL mentioned above.

How to Configure the Cisco UBR-MC20X20V Cable Interface Line Card

The Cisco uBR10012 universal broadband router should be operational before beginning the following procedures to configure the Cisco UBR-MC20X20V cable interface line card.

This section describes the steps for configuring Cisco UBR-MC20X20V line card at startup. These procedures provide only the initial, basic configuration for the line card.

Configuring the Controller on Cisco UBR-MC20X20V Cable Interface Line Card

Every downstream port on the Cisco UBR-MC20X20V line card is configured as an integrated-cable controller. Every Cisco UBR-MC20X20V line card has 5 integrated-cable controllers. To configure an RF channel on the MC20X20V integrated-cable controller on the Cisco UBR-MC20X20V line card, follow the summary steps.

SUMMARY STEPS

1. **enable**
2. **configure terminal**
3. **controller integrated-cable** *slot*/*subslot*/*port*
4. **rf-channel** *rf-port* **cable downstream channel-id** *channel-id*
5. **rf-channel** *rf-port* **frequency** *freq* [**annex** {**A** | **B**} **modulation** {**64** | **256**} [**interleave-depth** {**8** | **12** | **16** | **32** | **64** | **128**}]]
6. **rf-channel** *rf-port* **rf-power** *power-level*
7. **no rf-channel** *rf-port* **rf-shutdown**
8. **Ctrl-Z**

DETAILED STEPS

	Command or Action	Purpose
Step 1	**enable** **Example:** `Router> enable`	Enables privileged EXEC mode. • Enter your password if prompted.

Step 2	**configure terminal**
	
	Example:
	`Router# configure terminal`
	`Router(config)#`
		Enters global configuration mode.

	Command or Action	Purpose
Step 3	**controller integrated-cable** *slot*/*subslot*/*port* **Example:** `Router(config)# controller integrated-cable 7/1/0`	Enters controller configuration mode to configure the MC20X20V integrated-cable controller from the global configuration mode. • *slot*—Slot where the line card resides. Allowed range is 5 to 8. • *subslot*—Subslot where the line card resides. Available sub slots are 0 or 1. • *port*—Downstream port number on the line card. The allowed port values are 0 to 4.
Step 4	**rf-channel** *rf-port* **cable downstream channel-id** *channel-id* **Example:** `Router(config-controller)# rf-channel 0 cable downstream channel-id 97`	Assigns a downstream channel ID to an RF channel in controller configuration mode. • *rf-port*— RF channel number on a physical port on the line card. Allowed range is 0 to 3. • *channel-id*—Unique channel ID. Valid values are 1 to 255. **Note** Retain the system-generated default channel IDs instead of configuring it.

Command or Action	Purpose
Step 5 **rf-channel** *rf-port* **frequency** *freq* [**annex** {**A** | **B**} **modulation** {**64** | **256**} [**interleave-depth** {**8** | **12** | **16** | **32** | **64** | **128**}]] **Example:** `Router(config-controller)# rf-channel 0 frequency 453000000 annex B modulation 256 interleave-depth 32`	Configures the frequency of an RF channel in controller configuration mode. • *freq*—Center frequency for the RF channel. Allowed range is 55 to 999 MHz. The frequency can be configured as "none" as well. • **annex** {**A** | **B**}— MPEG framing format for each RF channel: – **A**–Annex A. The downstream is compatible with the European MPEG framing format specified in ITU-TJ.83 Annex A. – **B**–Annex B. The downstream is compatible with the North American MPEG framing format specified in ITU-TJ.83 Annex B. • **modulation** {**64** | **256**}—Modulation rate for each RF channel: – **64**–64-QAM – **256**–256-QAM • **interleave-depth** {**8** | **12** | **16** | **32** | **64** | **128**}—Downstream interleave depth. The default value is 32. **Note** When the frequency, annex, or modulation is changed, it is reflected across all RF channels in the port. Frequency will be automatically assigned using the 6 Mhz or 8 Mhz range based on annex. The range of frequency depends on the RF channel being configured. **Note** All controllers on the Cisco UBR-MC20X20V cable interface line card must have identical annex setting. The following warning message is displayed when the annex value is changed for a controller on the Cisco UBR-MC20X20V cable interface line card: *% Warning:: Annex for all controllers must be the same* This warning is also displayed when a Cisco uBR10-MC5X20 cable interface line card with a mixed annex configuration is replaced with Cisco UBR-MC20X20V cable interface line card.

	Command or Action	Purpose
Step 6	**rf-channel** *rf-port* **rf-power** *power-level* **Example:** `Router(config-controller)# rf-channel 0 rf-power 50.6`	Sets the RF power output level in the controller integrated-cable or controller modular-cable mode. The rf-power for an RF channel is based on the power mode. • *rf-port*—RF channel number on a physical port of the line card. Allowed range is 0 to 3. • *power-level*—Desired RF output power level in dBmV. Allowed range is 44 to 63 dBmV. The format is XY.Z; by default, .Z is added as .0. There are four modes of power level. Mode indicates the number of RF channels that are enabled on a physical port determined by the highest numbered channel that is enabled on the port. – Single Mode: 52dBmV to 60dBmV (channel 0 is enabled while the other channels are disabled) – Dual Mode: 48dBmV to 56dBmV (channel 0 could be enabled or disabled; channel 1 is enabled; channels 2 and 3 are disabled) – Tri Mode: 46dBmV to 54dBmV (channels 0 and 1 could be enabled or disabled; channel 2 is enabled; channel 3 is disabled) – Quad Mode: 44dBmV to 52dBmV (channel 3 is enabled; channels 0, 1, and 2 can be either enabled or disabled)
Step 7	**no rf-channel** *rf-port* **rf-shutdown** **Example:** `Router(config-controller)# no rf-channel rf-port rf-shutdown`	Enables the RF channel.
Step 8	**Ctrl-Z** **Example:** `Router(config)# Ctrl^Z`	Returns to Privileged EXEC mode.

Example

The following example shows how to configure the RF channel on a controller:

```
Router# enable
Router# configure terminal
Router(config)# controller integrated-Cable 6/1/0
Router(config-controller)# rf-channel 0 cable downstream channel-id 193
Router(config-controller)# rf-channel 0 frequency 393000000 annex B modulation 256qam
interleave 128
Router(config-controller)# rf-channel 0 rf-power 50.0
Router(config-controller)# no rf-channel 0 rf-shutdown
Router(config-controller)# rf-channel 1 cable downstream channel-id 194
Router(config-controller)# rf-channel 1 frequency 399000000 annex B modulation 256qam
interleave 128
Router(config-controller)# rf-channel 1 rf-power 50.0
Router(config-controller)# no rf-channel 1 rf-shutdown
Router(config-controller)# rf-channel 2 cable downstream channel-id 195
Router(config-controller)# rf-channel 2 frequency 405000000 annex B modulation 256qam
interleave 128
```

```
Router(config-controller)# rf-channel 2 rf-power 50.0
Router(config-controller)# no rf-channel 2 rf-shutdown
Router(config-controller)# rf-channel 3 cable downstream channel-id 196
Router(config-controller)# rf-channel 3 frequency 411000000 annex B modulation 256qam
interleave 128
Router(config-controller)# rf-channel 3 rf-power 50.0
Router(config-controller)# no rf-channel 3 rf-shutdown
```

Note The parameters shared by all RF channels on the MC20X20V integrated-cable controller are auto-configured when one RF channel is configured. For example, if the frequency on rf-channel 0 is configured, the frequency on the other RF channels are automatically configured based on the frequency value of rf-channel 0. Besides frequency, the annex/modulation and rf-power parameters are automatically configured for all RF channels in a controller when any rf-channel parameter is modified.

Troubleshooting Tips

Run the **show controllers integrated-cable** *slot/subslot/port* **config** command to view the integrated cable controller configuration details. The s**how controllers integrated-cable counters rf-channel** command displays raw QAM channel traffic statistics which include both narrowband and wideband traffic for QAM channel.

The **show interfaces integrated-cable** command displays only the narrowband traffic for the QAM channel.

Configuring Wideband Cable Interfaces on Cisco UBR-MC20X20V Cable Interface Line Card

To configure the wideband cable interface on Cisco UBR-MC20X20V line card, follow the summary steps.

SUMMARY STEPS

1. **enable**
2. **configure terminal**
3. **interface wideband-cable** *slot*/*subslot*/*port*:*wb_channel_no*
4. **cable bundle** *n* [**master**]
5. **cable rf-channel** *rf-port* [**bandwidth-percent** *bw-percent*] [**remaining ratio** *excess-value*]
6. **cable rf-channel controller** *port* **channel** *rf-port* **bandwidth-percent** *bw-percent*
7. **cable bonding-group-id** *bonding-group-id*
8. **Ctrl-Z**

DETAILED STEPS

	Command or Action	Purpose
Step 1	**enable** **Example:** `Router> enable`	Enables privileged EXEC mode. • Enter your password if prompted.

Step 2	**configure terminal**
	
	Example:
	`Router# configure terminal`
	`Router(config)#`
		Enters global configuration mode.

Step 3	**interface wideband-cable** *slot*/*subslot*/*port:wb_channel_no* **Example:** `Router(config)# interface wideband-cable 7/1/0:0`	Enters the wideband cable interface mode from the global configuration mode. • *slot*—Slot where the line card resides. Allowed range is 5 to 8. • *subslot*—Subslot where the line card resides. Allowed range is 0 to 1. • *port:wb_channel_no*—Interface number on the line card. The allowed port values are 0 to 4. The number of wideband-cable interfaces that can be created on the MC20X20V card is 30. One controller can have up to 6 wideband cable interfaces. Allowed range of *wb_channel_no* is 0 to 5.
Step 4	**cable bundle** *n* [**master**] **Example:** `Router(config-if)# cable bundle 1`	Configures a cable interface to belong to an interface bundle. • *n*—Bundle identifier. Valid range is from 1 to 255. • **master**—(Optional) Interface specified as the master.
Step 5	**cable rf-channel** *rf-port* [**bandwidth-percent** *bw-percent*] [**remaining ratio** *excess-value*] **Example:** `Router(config-if)# cable rf-channel 0 bandwidth-percent 25`	Configures the RF channel's bandwidth that would be allocated to a specified wideband channel or bonding group. • *rf-port*—RF channel physical port on the FPGA. • **bandwidth-percent** *bw-percent*—(Optional) The percent of bandwidth from this RF channel that will be used for the wideband interface. The range is 0 to 100. If bandwidth-percent is not used, the default bandwidth value is 100 percent. • **remaining ratio** *excess-value*—(Optional) Ratio of the excess bandwidth that is allocated to the wideband interface. The default value is 1. The range is 1 to 100. **Note** This option is available only when dynamic bandwidth sharing (DBS) is enabled. Run the **cable dynamic-bw-sharing** command to enable DBS. For complete description of the command, refer to the *Cisco Broadband Cable Command Reference Guide* on Cisco.com.

	Command or Action	Purpose
Step 6	**cable rf-channel controller** *port* **channel** *rf-port* **bandwidth-percent** *bw-percent* **Example:** `Router(config-if)# cable rf-channel controller 2 channel 1 bandwidth-percent 50`	Configures the RF channel's bandwidth percentage on another controller on the same cable line card. • *port*—Controller port value. • **channel** *rf-port*—RF port. • **bandwidth-percent** *bw-percent*—(Optional) Percentage of bandwidth from this RF channel that will be used for the wideband interface. The valid range is 0 to 100 percent. If bandwidth-percent is not used, the default bandwidth value is 100 percent.
Step 7	**cable bonding-group-id** *bonding-group-id* **Example:** `Router(config-if)# cable bonding-group-id 40`	Configures the bonding group ID. *bonding-group-id*— Bonding group ID. Allowed range is 1 to 1536.
Step 8	**Ctrl-Z** **Example:** `Router(config)# Ctrl^Z`	Returns to Privileged EXEC mode.

Example

The following example shows how to configure wideband cable interface:

```
Router> enable
Router# configure terminal
Router(config)# interface wideband-cable 7/1/0:0
Router(config-if)# cable bundle 1
Router(config-if)# cable rf-channel 0 bandwidth-percent 25
Router(config-if)# cable rf-channel 1 bandwidth-percent 25
Router(config-if)# cable rf-channel controller 2 channel 1 bandwidth-percent 50
Router(config-if)# cable rf-channel controller 2 channel 2 bandwidth-percent 50
```

Troubleshooting Tips

Run the **show controller integrated-cable** *slot/subslot/port* **mapping wb-channel** and **show controller integrated-cable** *slot/subslot/port* **mapping rf-channel** commands to view the entire configuration of the bandwidth allocation between WB channels and RF channels.

Configuring a Cable Interface on the Cisco UBR-MC20X20V Cable Interface Line Card

To configure the cable interface on the Cisco UBR-MC20X20V cable interface line card, follow the summary steps.:

SUMMARY STEPS

1. **enable**
2. **configure terminal**

3. **interface cable** *slot*/*subslot*/*port*
4. **downstream integrated-cable** *slot*/*bay*/*port* **rf-channel** {*rf-port* | *low*-*high*} [**upstream** *grouplist*]
5. **downstream integrated-cable** *slot/subslot/port* **rf-channel** *rf-port* [**upstream** *grouplist*]
6. **downstream modular-cable** *slot*/*bay*/*port* **rf-channel** {*rf-port* | *low*-*high*} [**upstream** *grouplist*]
7. **cable upstream max-ports** *n*
8. **cable upstream** *logical-port* **connector** *physical-port*
9. **cable upstream** *n* **docsis-mode** {**atdma** | **tdma** | **tdma-atdma**}
10. **cable upstream** *n* **channel-width** *first-choice-width* [*last-choice-width*]
11. **cable upstream** *n* **minislot-size** *size*
12. **cable upstream** *n* **range-backoff** {**automatic** | *start end*}
13. **cable upstream** *n* **modulation-profile** *primary-profile-number* [*secondary-profile-number*] [*tertiary-profile-number*]
14. **no cable upstream** *n* **shutdown**
15. **Ctrl-Z**

DETAILED STEPS

	Command or Action	Purpose
Step 1	**enable** **Example:** `Router> enable`	Enables privileged EXEC mode. • Enter your password if prompted.

Step 2	**configure terminal**
	
	Example:
	`Router# configure terminal`
	`Router(config)#`
		Enters global configuration mode.

Step 3	**interface cable** *slot*/*subslot*/*port* **Example:** `Router(config)# interface cable 7/0/0`	Enters the cable interface mode from the global configuration mode. • *slot*—Cable interface slot. • *subslot*—Cable interface subslot. • *port*—Cable interface number on the MAC domain number with a range of 0 to 4.
Step 4	**downstream modular-cable** *slot*/*bay*/*port* **rf-channel** {*rf-port* | *low*-*high*}[**upstream** *grouplist*] **Example:** `Router(config-if)# downstream modular-cable 1/0/0 rf-channel 0 upstream 3`	Sets or makes the RF channels from the SPA as primary channels in the MAC domain. • *slot*—Cable interface slot. • *bay*—Cable interface subslot. • *port*—Cable interface number. • *rf-port*— RF channel number with a range of 0 to 3. • *low-high*—Range of RF channel physical ports on the FPGA. The low and high values are separated by a hyphen. • *grouplist*—Upstream channel number with a range of 0 to 7.

	Command or Action	Purpose
Step 5	**downstream integrated-cable** *slot/subslot/port* **rf-channel** *rf-port* [**upstream** *grouplist*] **Example:** `Router(config-if)# downstream integrated-cable 7/1/0 rf-channel 3 upstream 3`	Configures the RF channels from the Cisco UBR-MC20X20V cable interface line card to primary channels in a MAC domain on the same slot/subslot. • *slot*—Cable interface slot. • *subslot*—Cable interface subslot. • *port*—Cable interface number. • *rf-port*—RF channel number with a range of 0 to 3. • *grouplist*—Upstream channel number with a range of 0 to 7
Step 6	**cable upstream max-ports** *n* **Example:** `Router(config-if)# cable upstream max-ports 4`	Configures the maximum number of upstreams on a downstream (MAC domain) on a Cisco UBR-MC20X20V cable interface line card. *n*—Number of upstream ports. The valid range is from 1 to 8, with a default of 4.
Step 7	**cable upstream** *logical-port* **connector** *physical-port* **Example:** `Router(config-if)# cable upstream 0 connector 0`	Maps an upstream port to a physical port on the Cisco UBR-MC20X20V cable interface line card for use with a particular downstream. • *logical-port*—Upstream port number for the logical port assignment. The number of logical ports is configured with the **cable modulation-profile** command, and the valid range is from 0 to one less than the current value set with the **cable modulation-profile** command. • *physical-port*—Upstream port number for the actual physical port to be assigned. The valid range is 0 to 19, with no default.
Step 8	**cable upstream** *n* **docsis-mode** {**atdma** | **scdma** | **scdma-d3** | **tdma** | **tdma-atdma**} **Example:** `Router(config-if)# cable upstream 0 docsis-mode tdma`	Configures an upstream to use either DOCSIS 1.x or DOCSIS 2.0 modulation profiles. • *n*—Upstream port number. Valid values start with 0 for the upstream port on the cable interface line card. • **atdma**—Indicates the upstream for DOCSIS 2.0 Advanced Time Division Multiple Access (A-TDMA) modulation profiles only. • **scdma**—Indicates the upstream for DOCSIS 2.0 Synchronous Code Division Multiple Access (S-CDMA) modulation profiles only. • **scdma-d3**—Indicates the upstream for DOCSIS 3.0 S-CDMA modulation profiles. The **scdma-d3** option uses channel type 4SR mode. • **tdma**—Indicates the upstream for DOCSIS 1.0 and DOCSIS 1.1 Time Division Multiple Access (TDMA) modulation profiles only (default). • **tdma-atdma**—Indicates the upstream for both A-TDMA and TDMA operation (mixed mode).

	Command or Action	Purpose
Step 9	**cable upstream** *n* **channel-width** *first-choice-width* [*last-choice-width*] **Example:** `Router(config-if)# cable upstream 0 channel-width 1600000 1600000`	Specifies an upstream channel width for an upstream port. • *n*—The upstream port number. Valid values start with 0 for the first upstream port on the cable interface line card. • *first-choice-width*—Upstream channel width in hertz (Hz). Valid values for all cards are: – 200,000 (160,000 symbols/sec)—Not valid when using Unsolicited Grant Service (UGS) or UGS with Activity Detection (UGS-AD) service flows (such as PacketCable voice calls) – 400,000 (320,000 symbols/sec) – 800,000 (640,000 symbols/sec) – 1,600,000 (1,280,000 symbols/sec) – 3,200,000 (2,560,000 symbols/sec) • *last-choice-width*—Upstream channel width in hertz. The valid values are the same as those for the first-choice-width parameter, but for proper operation, the last-choice-width should be equal to or less than the first-choice-width value. Use this parameter with supported cards to enable symbol rate management algorithms. The symbol rate automatically steps up from the first-choice-width value to the highest value until a stable channel is established.
Step 10	**cable upstream** *n* **minislot-size** *size* **Example:** `Router(config-if)# cable upstream 0 minislot-size 4`	Specifies the minislot size (in ticks) for a specific upstream interface. • *n*—Upstream port number. Valid values start with 0 for the first upstream port on the cable interface line card. • *size*—Minislot size in time ticks. Valid minislot sizes are 1, 2, 4, 8, 16, 32, 64, 128.
Step 11	**cable upstream** *n* **range-backoff** {**automatic** | *start end*} **Example:** `Router(config-if)# cable upstream 0 range-backoff 3 6`	Specifies automatic or configured initial ranging backoff calculation. • *n*—Upstream port number. Valid values start with 0 for the first upstream port on the cable interface line card. • **automatic**—Fixed data backoff start and end values. • *start*—Binary exponential algorithm. Sets the start value for initial ranging backoff. Valid values are from 0 to 15. • *end*—Binary exponential algorithm. Sets the end value for initial ranging backoff. Valid values are from 0 to 15.

	Command or Action	Purpose
Step 12	**cable upstream** *n* **modulation-profile** *primary-profile-number* [*secondary-profile-number*] [*tertiary-profile-number*] **Example:** `Router(config-if)# cable upstream 0 modulation-profile 21`	Assigns one or two modulation profiles to an upstream port. • *n*—Upstream port number. Valid values start with 0 for the first upstream port on the cable interface line card. • *primary-profile-number*—Number identifying the primary modulation profile for the upstream port. • *secondary-profile-number*—Secondary modulation profile for the upstream port, which is used when noise on the upstream increases to the point that the primary modulation profile can no longer be used. The valid values are the same ranges as for the primary modulation profile. • *tertiary-profile-number*—Tertiary modulation profile for the upstream port.
Step 13	**no cable upstream** *n* **shutdown** **Example:** `Router(config-if)# no cable upstream 0 shutdown`	Enables a single upstream port. *n*—Upstream port number. Valid values start with 0 for the first upstream port on the cable interface line card.
Step 14	**Ctrl-Z** **Example:** `Router(config)# Ctrl^Z`	Returns to Privileged EXEC mode.

Example

The following example shows how to configure a cable interface.

```
Router> enable
Router# configure terminal
Router(config)# interface cable 7/0/0
Router(config-if)# downstream integrated-cable 7/0/0 rf-channel 0
Router(config-if)# downstream integrated-cable 7/0/1 rf-channel 1
Router(config-if)# downstream modular-cable 1/0/0 rf-channel 0
Router(config-if)# cable upstream max-ports 4
Router(config-if)# cable upstream 0 connector 0
Router(config-if)# cable upstream 0 docsis-mode tdma
Router(config-if)# cable upstream 0 channel-width 1600000 1600000
Router(config-if)# cable upstream 0 minislot-size 4
Router(config-if)# cable upstream 0 range-backoff 3 6
Router(config-if)# cable upstream 0 modulation-profile 21
Router(config-if)# no cable upstream 0 shutdown
```

Troubleshooting Tips

Run the **show cable mac-domain cable** *slot*/*subslot*/*port* **cgd-associations** command to view a summary of the Channel Grouping Domain associations for all cable MAC domains.

Configuring an Integrated-Cable Interface on the Cisco UBR-MC20X20V Cable Interface Line Card

An integrated-cable (IC) interface is a channel on the Cisco UBR-MC20X20V cable interface line card which is configured as the primary card in any MAC domain.

To configure the IC interface on the Cisco UBR-MC20X20V cable interface line card, follow the summary steps.

SUMMARY STEPS

1. **enable**
2. **configure terminal**
3. **interface integrated-cable** *slot/subslot/port:rf-channel*
4. **cable rf-bandwidth-percent** *percent-value* [**remaining ratio** *excess-value*]
5. **Ctrl-Z**

DETAILED STEPS

	Command or Action	Purpose
Step 1	**enable** **Example:** `Router> enable`	Enables privileged EXEC mode. • Enter your password if prompted.

Step 2	**configure terminal**
	
	Example:
	`Router# configure terminal`
	`Router(config)#`
		Enters global configuration mode.

Step 3	**interface integrated-cable** *slot/subslot/port:rf-channel* **Example:** `Router(config)# interface integrated-cable 7/0/0:0`	Enters the cable interface mode. • *slot*—Cable interface slot. • *subslot*—Cable interface subslot. • *port*—Cable interface number. • *rf-channel*—RF channel number with a range of 0 to 3.

	Command or Action	Purpose
Step 4	**cable rf-bandwidth-percent** *percent-value* [**remaining ratio** *excess-value*] **Example:** `Router(config-if)# cable rf-bandwidth-percent 96`	Enables either static or dynamic bandwidth percentage sharing for an IC interface in interface configuration mode. • *percent-value*—Static bandwidth allocation of a downstream RF channel. The range is 1 to 100%. The default is 0. • **remaining ratio**—(Optional) Ratio of the remaining or excess bandwidth that can be allocated to the modular cable channel. **Note** This option is only available when dynamic bandwidth sharing is enabled. Run the **cable dynamic-bw-sharing** command to enable DBS. For complete description of the command, refer to the *Cisco Broadband Cable Command Reference Guide* on Cisco.com. • *excess-value*—Value of excess bandwidth that can be allocated to the modular cable channel. The range is 1–100. The default value is 1.
Step 5	**Ctrl-Z** **Example:** `Router(config)# Ctrl^Z`	Returns to Privileged EXEC mode.

Example

The following example shows how to configure an integrated-cable interface.

```
Router> enable
Router# configure terminal
Router(config)# interface integrated-cable 7/0/0:0
Router(config-if)# cable rf-bandwidth-percent 96
Router(config-if)# cable bundle 1
```

Troubleshooting Tips

Run the **show controllers integrated-cable** *slot*/*subslot*/*port* **mapping rf-channel** command to view the allocation of bandwidth on the IC interfaces that use the RF channels.

The **show interfaces integrated-cable** command displays only the narrowband traffic statistics of the QAM channel. The **show controllers integrated-cable counters rf channel** displays narrowband and wideband traffic statistics for the QAM channel.

Configuring the Fiber Node on the Cisco UBR-MC20X20V Cable Interface Line Card

To configure the fiber node on Cisco UBR-MC20X20V line card, follow the summary steps.

Note The fiber node should be configured as per the physical topology of the system.

SUMMARY STEPS

1. **enable**
2. **configure terminal**
3. **cable fiber-node** *fiber-node-id*
4. **downstream integrated-cable** *slot/subslot/port* **rf-channel** {*rf-port* | *low-high*} [**upstream** *grouplist*]
5. **cable upstream** *logical-port* **connector** *physical-port*
6. **Ctrl-Z**

DETAILED STEPS

	Command or Action	Purpose
Step 1	**enable** **Example:** `Router> enable`	Enables privileged EXEC mode. • Enter your password if prompted.

Step 2	**configure terminal**
	
	Example:
	`Router# configure terminal`
	`Router(config)#`
		Enters global configuration mode.

Step 3	**cable fiber-node** *fiber-node-id* **Example:** `Router(config)# cable fiber-node 1`	Enters the cable fiber-node configuration mode to configure a fiber node. *fiber-node-id*—Unique numerical ID for the fiber node. Valid values are 1 to 256.
Step 4	**downstream integrated-cable** *slot/subslot/port* **rf-channel** {*rf-port* | *low-high*} [**upstream** *grouplist*] **Example:** `Router(config-if)# downstream integrated-cable 7/1/0 rf-channel 3 upstream 3`	Configures the downstreams on the fiber-node of the Cisco UBR-MC20X20V cable interface line card. • *slot*—Cable interface slot. • *subslot*—Cable interface subslot. • *port*—Cable interface number. • *rf-port*—RF channel number with a range of 0 to 3. • *low-high*—A range of RF channel physical ports on the FPGA. The low and high values are separated by a hyphen. • *grouplist*—Upstream channel number with a range of 0 to 7

	Command or Action	Purpose
Step 5	**cable upstream** *logical-port* **connector** *physical-port* **Example:** `Router(config-fiber-node)# upstream Cable 7/0 connector 0-3`	Maps an upstream port to a physical port on the Cisco UBR-MC20X20V cable interface line card for use with a particular downstream. • *logical-port*—Upstream port number for the logical port assigned. The number of logical ports is configured with the **cable modulation-profile** command, and the valid range is from 0 to one less than the current value set using the **cable modulation-profile** command. • *physical-port*—Upstream port number for the actual physical port to be assigned. The valid range is from 0 to 19, with no default.
Step 6	**Ctrl-Z** **Example:** `Router(config)# Ctrl^Z`	Returns to Privileged EXEC mode.

Example

The following example shows how to configure the fiber node on the Cisco UBR-MC20X20V cable interface line card.

```
Router> enable
Router# configure terminal
Router(config)# cable fiber-node 1
Router(config-fiber-node)# downstream integrated-cable 7/0/0 rf-channel 0 2-3
Router(config-fiber-node)# upstream Cable 7/0 connector 0-3
```

Note For complete descriptions of the above software configuration commands, refer to the *Cisco Broadband Cable Command Reference Guide* on Cisco.com.

Troubleshooting Tips

- Run **show cable fiber-node** command to list all channels associated with the fiber node and to indicate if the fiber node is valid.
- To always have a valid fiber node:
  - Downstream channels in fiber node should have unique frequency and downstream channel ID.
  - All downstream channels in fiber node should belong to the same bundle.
  - Upstream with distinct frequency must be specified.

Configuring Global HCCP N+1 Line Card Redundancy on the Cisco uBR10012 Router

The Cisco IOS Release 12.2(33)SCC supports global N+1 line card redundancy feature on the Cisco uBR100012 routers. This feature implements a simpler command line interface (CLI) to establish the working and protect line card relationships. The HCCP interface commands are not supported any more. The Cisco UBR-MC20X20V cable interface line card can be configured as protect card to protect either the Cisco UBR-MC20X20V line card or the Cisco MC5X20U/H line card.

This feature allows plug-and-play operation of the Cisco RF switch in 7+1 or 4+1 HCCP Redundancy configuration with the Cisco uBR10012 universal broadband router. In this configuration, the Cisco uBR100012 router is configured with either one or two Cisco RF switches using HCCP. Some configuration of the router is required.

See *N+1 Redundancy for the Cisco CMTS Routers* for more information.

PREREQUISITES

- An external DHCP server must be installed and operational on the network, or an internal DHCP server must be operational within the Cisco uBR100012 router.
- Configure the RF switch name using the **rf-switch name** line card redundancy configuration command, and the RF switch IP addresses prior to configuring line card redundancy.

SUMMARY STEPS

1. **enable**
2. **configure terminal**
3. **ip host rf-sw1** *ip_addr*
4. **ip host rf-sw2** *ip_addr*
5. **redundancy**
6. **linecard-group 1 cable**
7. **member subslot** *slot/card* **working**
8. **member subslot** *slot/card* **protect** [**config** *slot/card*]
9. **Ctrl-Z**
10. **write memory**

DETAILED STEPS

	Command or Action	Purpose
Step 1	**enable** **Example:** `Router> enable`	Enables privileged EXEC mode. • Enter your password if prompted.

Step 2	**configure terminal**
	
	Example:
	`Router# configure terminal`
	`Router(config)#`
		Enters global configuration mode.

	Command or Action	Purpose
Step 3	**ip host rf-sw1** *ip_addr* **Example:** `Router(config)# ip host rf-sw1 10.4.4.1`	Assigns the Domain Name System (DNS) entry to the first or only Cisco RF switch in the redundancy scheme. *ip_addr*—IP address of the RF switch.
Step 4	**ip host rf-sw2** *ip_addr* **Example:** `Router(config)# ip host rf-sw2 10.4.4.2`	(Required when using two Cisco RF Switches) Assigns the DNS entry to the second Cisco RF switch in the redundancy scheme.

Step 5	**redundancy**
	Example:
	`Router(config)# redundancy`
	`Router(config-red)#`
		Enters redundancy configuration mode.

Step 6	**linecard-group 1 cable** **Example:** `Router(config-red)# linecard-group 1 cable`	Enters cable line card redundancy mode. This command assigns the HCCP group to all interfaces on the cable interface line card, or Cisco Broadband Processing Engine.
Step 7	**member subslot** *slot/card* **working** **Example:** `Router(config-red)# member subslot 8/0 working`	This command configures all interfaces on the specified line card to function as HCCP working interfaces in the redundancy scheme. Repeat this step for each working line card in the Cisco router.

Step 8	**member subslot** *slot/card* **protect**
	Example:
	`Router(config-red)# member subslot 8/1 protect`
	member subslot *slot/card* **protect config** *slot/card*
	Example:
	`Router(config-red)# member subslot 8/1 protect config 8/0`
		Configures all interfaces on the specified line card to function as HCCP protect interfaces in the redundancy scheme.
		or
		For faster switchover results, configures the protect interface for the most appropriate working interface configuration.

Step 9	**Ctrl-Z**
	Example:
	`Router(config-red)# Ctrl^Z`
	`Router#`
		Exits global and redundancy configuration modes and returns to Privileged EXEC mode.

Step 10	**write memory**
	Example:
	`Router# copy running-config startup-config`
	`or`
	`Router# write memory`
		After configuring all domains, save your settings to the nonvolatile random access memory (NVRAM) to ensure that the system retains the settings after a power cycle.

Note Cisco uBR-MC20X20V line card is configured as protect line card for a Cisco uBR-MC20X20V working line card. Hot-Standby Connection-to-Connection Protocol (HCCP) N+1 Redundancy and high availability features are enabled. The downstream channels of this Cisco uBR-MC20X20V protect line card will be muted. When the protect line card is removed from HCCP line card redundancy group, the downstream channels continue to be in muted state, regardless of the state displayed in the running configuration.
To prevent the inconsistency between the state of the hardware channels and the state displayed in the running configuration, when the Cisco uBR-MC20X20V protect line card is used as working line card, reconfigure the Cisco uBR-MC20X20V line card.

Example

The following example of the **show running configuration** command illustrates the N+1 redundancy scheme configured on the Cisco uBR10012 universal broadband router with two Cisco RF Switches:

```
Router# show running config
...

ip host rfsw-1 10.4.4.1
ip host rfsw-2 10.4.4.2

redundancy
 main-cpu
  auto-sync standard
 linecard-group 1 cable
  rf-switch name 1 rf-switch-1
  rf-switch name 2 rf-switch-2
rf-switch snmp-community private123
  member subslot 6/1 working
  member subslot 5/1 protect
member subslot 8/0 working
...
```

Monitoring and Maintaining the Cisco UBR-MC20X20V Cable Interface Line Card

The following sections describe the **show** commands that provide more information about the Cisco UBR-MC20X20V cable interface line card:

- Viewing the Cisco UBR-MC20X20V Cable Interface Line Card Statistics
- Viewing Information about the Cable Interface Controllers
- Viewing Information about the Cable Modems

Viewing the Cisco UBR-MC20X20V Cable Interface Line Card Statistics

To view information about the Cisco UBR-MC20X20V line card statistics, use the **show controller integrated-cable** command in privileged EXEC mode.

show controller integrated-cable {*slot/subslot/port*} [**all | association | brief | config | counters | errors | mapping | registers | status**]

This command allows the user to view the following line card statistics.

- Interface association
- JIB hardware downstream configuration
- Channel counters
- Errors
- Mapping of WB/RF channels
- JIB hardware downstream registers
- JIB hardware downstream status

Syntax Description

slot/subslot/port	Identifies the cable interface on the Cisco uBR10012 router. The following are the valid values: • *slot*—Slot where the line card resides. Allowed range is 5 to 8. • *subslot*—Subslot where the line card resides. Available sub slots are 0 or 1. • *port*—Controller number on the line card. The allowed port values are 0 to 4.
all	Displays the complete information about the line card statistics.
association	Displays the controller association information.
brief	Displays a brief information about the line card statistics.
config	Displays statistics about the JIB hardware downstream configuration.
counters	Displays information about the RF and WB channel counters.
errors	Displays information about the error counters such as DOCSIS processor error counters, BPI error counters, Queue Manager error counters, and so on.
mapping	Displays mapping statistics of the WB and RF channels.
registers	Displays the list of JIB hardware downstream register values.
status	Displays the JIB hardware status for downstream ports.

Examples

The following example shows a typical display for the **show controller integrated-cable** command and the **all** keyword.

```
Router# show controller integrated-Cable 6/0/0 all

Load for five secs: 9%/0%; one minute: 17%; five minutes: 14%
Time source is NTP, *15:06:02.838 EDT Sun Mar 21 2010

Integrated Cable Controller 6/0/0:
---------------------------------
  Channel 1  Annex = B  Modulation = 256 QAM
  Channel 2  Annex = B  Modulation = 256 QAM
  Channel 3  Annex = B  Modulation = 256 QAM
  Channel 4  Annex = B  Modulation = 256 QAM

JIB3_DS BPI registers (base address 0xF8880000)

bpi_int_isr_0                       [0x00000000] = 0x00000000
bpi_int_ier_0                       [0x00000004] = 0x0000000F
```

```
glb_int_isr_0                       [0x00000010] = 0x00000000
glb_int_ier_0                       [0x00000014] = 0x000003FF
glb_int_isr_1                       [0x00000020] = 0x00000000
glb_int_ier_1                       [0x00000024] = 0x000003FF
bpi_int_fesr_0                      [0x00000040] = 0x00000000
bpi_tst_tp_sel_reg                  [0x00000050] = 0x00000000
bpi_tst_tp_reg                      [0x00000054] = 0x00000000
bpi_cnt_good_packet_in_cnt          [0x00000064] = 0x61308806
bpi_cnt_bad_packet_in_cnt           [0x00000068] = 0x00006538
bpi_cnt_good_packet_out_cnt         [0x0000006C] = 0x61308806
bpi_cnt_bad_packet_out_cnt          [0x00000070] = 0x00006538
bpi_ecc_sbit_err_cnt                [0x00000074] = 0x00000000
glb_sw_rev_id                       [0x00000078] = 0x00020002
glb_hw_rev_id                       [0x0000007C] = 0x00010008
frz_reg                             [0x00000080] = 0x00000000
frz_en                              [0x00000084] = 0x00000001
glb_dcm_status                      [0x00000088] = 0x00000007
glb_sw_rst                          [0x0000008C] = 0x00000000

JIB3_DS ERP registers (base address 0xF8881000)

erp_irq_src_reg                     [0x00000000] = 0x00000000
erp_irq_en_reg                      [0x00000004] = 0x80000FFF
erp_tp_sel_reg                      [0x00000050] = 0x00000000
erp_tp_reg                          [0x00000054] = 0x00000000
erp_cfg_reg                         [0x00000060] = 0x00000000
erp_err_record_reg                  [0x00000064] = 0x00000000
erp_err_addr_record_reg             [0x00000068] = 0x00000000
erp_err_wd_record_reg               [0x0000006C] = 0x00000000
erp_proc_err_addr_record_reg        [0x00000090] = 0x00000000

JIB3_DS RX SPI registers (base address 0xF8882000)

rxspi_irq_src_reg                   [0x00000000] = 0x00000000
rxspi_irq_en_reg                    [0x00000004] = 0x000001FF
rxspi_ferr_src_reg                  [0x00000040] = 0x00000000
rxspi_testpoint_sel_reg             [0x00000050] = 0x00000000
rxspi_testpoint_reg                 [0x00000054] = 0x00000000
rxspi_rst_cntl_reg                  [0x00000060] = 0x00000000
rxspi_cntl_status_reg               [0x00000064] = 0x00000005
rxspi_cfg_cntl_reg                  [0x00000068] = 0x00000021
rxspi_afthres_reg                   [0x0000006C] = 0x01C00180
rxspi_cal_dur_reg                   [0x00000070] = 0x00030000
rxspi_non_drop_err_cnt_reg          [0x00000088] = 0x00000000
rxspi_drop_byte_cnt_reg             [0x0000008C] = 0x00000000
rxspi_rx_byte_cnt_reg[0]            [0x000000B0] = 0xFFFFFFFF
rxspi_rx_byte_cnt_reg[1]            [0x000000B4] = 0xFFFFFFFF
rxspi_rx_byte_cnt_reg[2]            [0x000000B8] = 0x14B49467
rxspi_rx_pkt_cnt_reg[0]             [0x000000C0] = 0x3FF2F36C
rxspi_rx_pkt_cnt_reg[1]             [0x000000C4] = 0x20F3AFA9
rxspi_rx_pkt_cnt_reg[2]             [0x000000C8] = 0x004A4A35
rxspi_fifo_pkt_drop_cnt_reg[0]      [0x000000E0] = 0x00000000
rxspi_fifo_pkt_drop_cnt_reg[1]      [0x000000E4] = 0x00000000
rxspi_fifo_pkt_drop_cnt_reg[2]      [0x000000E8] = 0x00000000
rxspi_calendar_table_reg[0]         [0x00000800] = 0x00000000
rxspi_calendar_table_reg[1]         [0x00000804] = 0x00000001
rxspi_calendar_table_reg[2]         [0x00000808] = 0x00000002
rxspi_calendar_table_reg[3]         [0x0000080C] = 0x00000003

JIB3_DS TX SPI registers (base address 0xF8883000)

txspi_irq_src_reg                   [0x00000000] = 0x00000000
txspi_irq_en_reg                    [0x00000004] = 0x0000001F
txspi_ferr_src_reg                  [0x00000040] = 0x00000000
```

```
txspi_testpoint_sel_reg             [0x00000050] = 0x00000000
txspi_testpoint_reg                 [0x00000054] = 0x00000000
txspi_rst_cntl_reg                  [0x00000060] = 0x00000000
txspi_cntl_status_reg               [0x00000064] = 0x00000009
txspi_cfg_cntl_reg                  [0x00000068] = 0x00000001
txspi_afthres_reg                   [0x0000006C] = 0x01EC01E8
txspi_cal_dur_reg                   [0x00000070] = 0x00040000
txspi_train_cntl_reg                [0x00000074] = 0x00000000
txspi_nonfatalerr_cnt_reg           [0x00000080] = 0x00000000
txspi_eop_abort_pkt_cnt_reg[0]      [0x00000090] = 0x00000000
txspi_eop_abort_pkt_cnt_reg[1]      [0x00000094] = 0x00000000
txspi_eop_abort_pkt_cnt_reg[2]      [0x00000098] = 0x00000000
txspi_eop_abort_pkt_cnt_reg[3]      [0x0000009C] = 0x00000000
txspi_eop_abort_byte_cnt_reg[0]     [0x000000A0] = 0x00000000
txspi_eop_abort_byte_cnt_reg[1]     [0x000000A4] = 0x00000000
txspi_eop_abort_byte_cnt_reg[2]     [0x000000A8] = 0x00000000
txspi_eop_abort_byte_cnt_reg[3]     [0x000000AC] = 0x00000000
txspi_tx_byte_cnt_reg[0]            [0x000000C0] = 0x00000000
txspi_tx_byte_cnt_reg[1]            [0x000000C4] = 0x00000000
txspi_tx_byte_cnt_reg[2]            [0x000000C8] = 0x00000000
txspi_tx_byte_cnt_reg[3]            [0x000000CC] = 0x00000000
txspi_tx_pkt_cnt_reg[0]             [0x00000100] = 0x00000000
txspi_tx_pkt_cnt_reg[1]             [0x00000104] = 0x00000000
txspi_tx_pkt_cnt_reg[2]             [0x00000108] = 0x00000000
txspi_tx_pkt_cnt_reg[3]             [0x0000010C] = 0x00000000
txspi_calendar_table_reg[0]         [0x00000800] = 0x00000000
txspi_calendar_table_reg[1]         [0x00000804] = 0x00000001
txspi_calendar_table_reg[2]         [0x00000808] = 0x00000002
txspi_calendar_table_reg[3]         [0x0000080C] = 0x00000003
txspi_calendar_table_reg[4]         [0x00000810] = 0x00000004

JIB3_DS DOC registers (base address 0xF8884000)

doc_int_err0                        [0x00000000] = 0x00000000
doc_int_err0_ier                    [0x00000004] = 0xFFBFBFFD
doc_int_err1                        [0x00000010] = 0x00000000
doc_int_err1_ier                    [0x00000014] = 0x003FFFF8
doc_int_fesr                        [0x00000040] = 0x00000000
doc_test_sel                        [0x00000050] = 0x00000000
doc_testpoint                       [0x00000054] = 0x00000000
doc_cfg_ctrl                        [0x00000060] = 0x031A0000
doc_err_cap_ctrl                    [0x00000064] = 0x001F0001
doc_err_cap_addr                    [0x00000068] = 0x00000000
doc_err_cap_data                    [0x0000006C] = 0x000080F7
doc_seg_num                         [0x00000070] = 0x00000001
doc_wb_chan_stats_sel               [0x00000074] = 0x00000077
doc_wb_pkt_cnt                      [0x00000078] = 0x00000000
doc_wb_byte_cnt                     [0x0000007C] = 0x00000000
doc_wb_police_sel                   [0x00000080] = 0x00000000
doc_wb_police_data                  [0x00000084] = 0x00000000
doc_wb_police_intv                  [0x00000088] = 0x00000000
doc_nb_chan_stats_sel               [0x0000008C] = 0x0000004C
doc_nb_pkt_cnt                      [0x00000090] = 0x00000000
doc_nb_byte_cnt                     [0x00000094] = 0x00000000
doc_nb_police_sel                   [0x00000098] = 0x00000000
doc_nb_police_data                  [0x0000009C] = 0x00000000
doc_nb_police_intv                  [0x000000A0] = 0x00000000
doc_int_doc_cnt                     [0x000000D4] = 0x00000000
doc_int_ecc_sbiterr_cnt             [0x000000D8] = 0x00000000
doc_pkt_good_in_cnt                 [0x000000DC] = 0x6130ED6F
doc_pkt_good_out_cnt                [0x000000E0] = 0x61308837
doc_pkt_err_in_cnt                  [0x000000E4] = 0x00000000
doc_pkt_err_out_cnt                 [0x000000E8] = 0x00006538
doc_pkt_drop_cnt                    [0x000000EC] = 0x00000000
```

```
doc_efc_all_cnt                     [0x000000F0] = 0x00000000
doc_efc_hi_cnt                      [0x000000F4] = 0x00000000
doc_efc_me_cnt                      [0x000000F8] = 0x00000000
doc_efc_lo_cnt                      [0x000000FC] = 0x00000000
doc_efc_ch_sel                      [0x00000100] = 0x00000000
doc_efc_debug_ctrl                  [0x00000104] = 0x00000000
doc_rldram_ext_ecc                  [0x00000114] = 0x00000000
doc_rldram_cfg                      [0x00000118] = 0x00101544
doc_rldram_ctrl                     [0x0000011C] = 0x00100389
doc_rldram_status                   [0x00000120] = 0x039D7403
doc_rldram_blk_clr                  [0x00000124] = 0x0B7FFFFF
doc_rldram_cal_match_win_h          [0x00000128] = 0x00000000
doc_rldram_cal_match_win_l          [0x0000012C] = 0x1FFFFFFF
doc_rldram_ecc_err_rec_addr         [0x00000130] = 0x00000000
doc_magic_num_err_pkt_ctrl          [0x00000150] = 0x00000000
doc_magic_num_err_pkt_addr          [0x00000154] = 0x00000000
doc_magic_num_err_pkt_data          [0x00000158] = 0x00000000

JIB3_DS RIF registers (base address 0xF8885000)

rif_int_err0                        [0x00000000] = 0x00000000
rif_int_ier0                        [0x00000004] = 0x00000007
rif_int_fesr0                       [0x00000040] = 0x00000000
rif_tp_sel                          [0x00000050] = 0x00000000
rif_tp                              [0x00000054] = 0x00000000
rif_cfg_ctrl                        [0x00000060] = 0x00000000
rif_cnt_in_mpeg_cnt                 [0x00000064] = 0xFFFFFFFF
rif_cnt_out_good_mpeg_cnt           [0x00000068] = 0xFFFFFFFF
rif_cnt_out_bad_mpeg_cnt            [0x0000006C] = 0x00000000
rif_cnt_drop_mpeg_cnt               [0x00000070] = 0x00000000
rif_1bit_ecc_err_stat               [0x00000074] = 0x00000000

JIB3_DS RTN registers (base address 0xF8886000)

return_int_isr                      [0x00000000] = 0x00000000
return_int_ier                      [0x00000004] = 0x000001FF
return_int_fesr                     [0x00000040] = 0x00000000
return_tp_sel                       [0x00000050] = 0x00000000
return_tp                           [0x00000054] = 0x00000000
return_ctrl_reg                     [0x00000060] = 0x00000000
return_pif_loopback_chnl            [0x00000064] = 0x00000000
return_sniffer_nonbonded_en         [0x00000068] = 0x00000000
return_sniffer_bonded_en            [0x0000006C] = 0x00000000
return_spi_chnl_sel                 [0x00000070] = 0x0000013A
return_err_drop_en                  [0x00000074] = 0x0000000F
return_snf_macda_cfg_addr           [0x00000078] = 0x00000000
return_snf_macda_cfg_data_hi        [0x0000007C] = 0x00000000
return_snf_macda_cfg_data_lo        [0x00000080] = 0x00000000
return_in_pifrx_good_cnt            [0x000000A0] = 0x00000000
return_in_pifrx_bad_cnt             [0x000000A4] = 0x00000000
return_in_piflp_good_cnt            [0x000000A8] = 0xFFFFFFFF
return_in_piflp_bad_cnt             [0x000000AC] = 0x00000000
return_in_sniffer_good_cnt          [0x000000B0] = 0x61308845
return_in_sniffer_bad_cnt           [0x000000B4] = 0x00006538
return_in_spi_loop_good_cnt         [0x000000B8] = 0x00000000
return_in_spi_loop_bad_cnt          [0x000000BC] = 0x00000000
return_out_spi0_cnt                 [0x000000C0] = 0x00000000
return_out_spi1_cnt                 [0x000000C4] = 0x00000000
return_out_spi2_cnt                 [0x000000C8] = 0x00000000
return_out_spi3_cnt                 [0x000000CC] = 0x00000000
return_out_spi4_cnt                 [0x000000D0] = 0x00000000
return_pifrx_if_par_err_drop_cnt    [0x000000D4] = 0x00000000
return_pifrx_if_len_err_drop_cnt    [0x000000D8] = 0x00000000
return_piflp_if_err_drop_cnt        [0x000000DC] = 0x00000000
```

```
return_piflp_if_chnl_drop_cnt       [0x000000E0] = 0x00000000
return_snf_pb_err_drop_cnt          [0x000000E4] = 0x00006538
return_snf_pkt_type_err_drop_cnt    [0x000000E8] = 0x61308845
return_spilp_if_err_drop_cnt        [0x000000EC] = 0x00000000
return_pifrx_traffic_mux_drop_cnt   [0x000000F0] = 0x00000000
return_piflp_traffic_mux_drop_cnt   [0x000000F4] = 0x00000000
return_snf_traffic_mux_drop_cnt     [0x000000F8] = 0x00000000
return_spilp_traffic_mux_drop_cnt   [0x000000FC] = 0x00000000
return_pifrx_fifo_overflow_drop_cnt [0x00000100] = 0x00000000
return_piflp_fifo_overflow_drop_cnt [0x00000104] = 0x00000000
return_snf_fifo_overflow_drop_cnt   [0x00000108] = 0x00000000
return_spilp_fifo_overflow_drop_cnt [0x0000010C] = 0x00000000
return_pifrx_if_par_err_cnt         [0x00000110] = 0x00000000
return_pifrx_if_len_err_cnt         [0x00000114] = 0x00000000
return_pifrx_fifo_ecc_1berr_cnt     [0x00000118] = 0x00000000
return_piflp_fifo_ecc_1berr_cnt     [0x0000011C] = 0x00000000
return_snf_fifo_ecc_1berr_cnt       [0x00000120] = 0x00000000
return_spilp_fifo_ecc_1berr_cnt     [0x00000124] = 0x00000000

JIB3_DS DLM registers (base address 0xF8890000)

dlm_int_isr_0                       [0x00000000] = 0x00000005
dlm_int_ier_0                       [0x00000004] = 0x00000000
dlm_cnt_local_ts_reg                [0x00000064] = 0x5B00EB07
dlm_cfg_tss_comp_reg                [0x00000068] = 0x00000027
dlm_cfg_tss_ctrl_reg                [0x0000006C] = 0x00000000
dlm_cfg_tss_cmd_reg                 [0x00000070] = 0x00000000
dlm_cnt_ts_load_cnt                 [0x000000BC] = 0x00000000
dlm_cnt_ts_chk_failed_cnt           [0x000000C4] = 0x00000000
dlm_cnt_tss_perr_cnt                [0x000000C8] = 0x00000000
dlm_cnt_load_ts_reg                 [0x000000D0] = 0x003F52EF

JIB3_DS SEQ registers (base address 0xF8892000)

seq_int_err0                        [0x00000000] = 0x0000000F
seq_int_ier0                        [0x00000004] = 0x000FFFFF
seq_int_err3                        [0x00000030] = 0x00000000
seq_int_ier3                        [0x00000034] = 0x00000001
seq_int_fatal_err                   [0x00000040] = 0x00000000
seq_tp_sel                          [0x00000050] = 0x00000000
seq_tp                              [0x00000054] = 0x00000000
seq_cfg_en                          [0x00000060] = 0x00000001
seq_cfg_sync_timer_sel              [0x00000064] = 0x00000004
seq_cfg_sync_timer_data             [0x00000068] = 0x00000000
seq_cfg_sync_sa_sel                 [0x0000006C] = 0x00000004
seq_cfg_sync_sa_data_lo             [0x00000070] = 0x70CC0B91
seq_cfg_sync_sa_data_hi             [0x00000074] = 0x00000000
seq_cfg_tkb_timer_sel               [0x00000078] = 0x00000014
seq_cfg_tkb_timer_data              [0x0000007C] = 0x00000000
seq_cfg_tkb_max                     [0x00000080] = 0x00000000
seq_hwdbg_dpv_proc_table_addr       [0x00000090] = 0x00000000
seq_hwdbg_dpv_ptr_mod_table         [0x00000094] = 0x00000000
seq_hwdbg_dpv_timestamp_table       [0x00000098] = 0x00000000
seq_hwdbg_dpv_hcs_table             [0x0000009C] = 0x00000000
seq_cnt_blkram_oecc_err_stat        [0x000000A4] = 0x00000000
seq_cnt_tran_mpeg_stat              [0x000000A8] = 0xFFFFFFFF
seq_cnt_tran_mpeg_sync_stat         [0x000000AC] = 0x00000000
seq_cnt_tran_only_sync_stat         [0x000000B0] = 0x00000000
seq_cnt_tran_dpv_stat               [0x000000B8] = 0x00000000

JIB3_DS QM registers (base address 0xF8893000)

qm_int_isr0                         [0x00000000] = 0x00000000
qm_int_ier0                         [0x00000004] = 0x0000007F
```

```
qm_int_isr1                          [0x00000010] = 0x00000000
qm_int_ier1                          [0x00000014] = 0x000FFFFF
qm_int_fat_err_isr                   [0x00000040] = 0x00000000
qm_tst_tp_sel                        [0x00000050] = 0x00000000
qm_tst_tp                            [0x00000054] = 0x00000000
qm_cfg_chnl_rst_0                    [0x00000060] = 0x00000000
qm_cfg_ctl                           [0x0000006C] = 0x00000011
qm_cfg_sqf_fac_addr                  [0x0000008C] = 0x00000014
qm_cfg_sqf_fac_data                  [0x00000090] = 0x00000000
qm_cfg_bond_chnl_map_addr            [0x00000094] = 0x00000020
qm_cfg_bond_chnl_map_data_lo         [0x00000098] = 0x00000000
qm_cfg_flt_thr_addr                  [0x000000A4] = 0x0000024F
qm_cfg_flt_thr_data                  [0x000000A8] = 0x00000000
qm_cfg_repl_addr                     [0x000000AC] = 0x0000002D
qm_cfg_repl_data_lo                  [0x000000B0] = 0x00000000
qm_hwdbg_buf_mag_addr                [0x000000BC] = 0x00000000
qm_hwdbg_wptr_data_lo                [0x000000C0] = 0x00000C60
qm_hwdbg_wptr_data_mi                [0x000000C4] = 0x00016080
qm_hwdbg_wptr_data_hi                [0x000000C8] = 0x000012A0
qm_hwdbg_rptr_data_lo                [0x000000CC] = 0x00000C60
qm_hwdbg_rptr_data_mi                [0x000000D0] = 0x00016080
qm_hwdbg_rptr_data_hi                [0x000000D4] = 0x000012A0
qm_hwdbg_qulen_data_lo               [0x000000D8] = 0x00000000
qm_hwdbg_qulen_data_mi               [0x000000DC] = 0x00000000
qm_hwdbg_qulen_data_hi               [0x000000E0] = 0x00000000
qm_hwdbg_contex_data                 [0x000000E4] = 0x00000000
qm_cfg_dir_stat_addr                 [0x000000E8] = 0x0000004E
qm_cnt_dir_pkt_stat                  [0x000000EC] = 0x00000000
qm_cnt_dir_byte_stat                 [0x000000F0] = 0x00000000
qm_cfg_qam_stat_addr                 [0x000000F4] = 0x0000004C
qm_cnt_qam_chnl_pkt_stat             [0x000000F8] = 0x00000000
qm_cnt_qam_chnl_byte_stat            [0x000000FC] = 0x00000000
qm_cnt_qam_chnl_sync_stat            [0x00000100] = 0x00000000
qm_cnt_bpram_ovrflw_stat             [0x00000108] = 0x00000000
qm_cnt_que_ovrflw_stat               [0x0000010C] = 0x00000000
qm_cnt_good_bpi_pkt_stat             [0x00000110] = 0x6130886C
qm_cnt_bad_bpi_pkt_stat              [0x00000114] = 0x000000FF
qm_cnt_bpram_out_good_pkt_stat       [0x0000011C] = 0xC38C8639
qm_cnt_bpram_out_dir_pkt_stat        [0x00000120] = 0x213DFA0E
qm_cnt_bpram_out_bonded_pkt_stat     [0x00000124] = 0x3486CDA6
qm_cnt_replicated_pkt_stat           [0x00000128] = 0x8399F7DB
qm_cnt_bpram_bad_type_pkt_stat       [0x00000134] = 0x00000000
qm_cnt_bpram_bad_eop_pkt_stat        [0x00000138] = 0x00000000
qm_cnt_bpram_bad_dir_pkt_stat        [0x0000013C] = 0x00000000
qm_cnt_bpram_bad_bonded_pkt_stat     [0x00000140] = 0x00000000
qm_cnt_bpram_oecc_err_pkt_stat       [0x00000144] = 0x00000000
qm_cnt_bpram_bad_pkt_stat            [0x00000148] = 0x000000FF
qm_cnt_wr_good_pkt_stat              [0x0000014C] = 0xC38C863A
qm_cnt_wr_bad_pkt_stat               [0x00000150] = 0x00000000
qm_cnt_drop_bad_pkt_stat             [0x00000154] = 0x000000FF
qm_cnt_drop_ovrflw_pkt_stat          [0x00000158] = 0x00000000
qm_cnt_rd_pkt_stat                   [0x0000015C] = 0xC38C8664
qm_cnt_rd_mpeg_stat                  [0x00000160] = 0xFFFFFFFF
qm_cnt_rd_mpeg_sync_stat             [0x00000164] = 0x06A0FC65
qm_cnt_rd_mpeg_only_sync_stat        [0x00000168] = 0x0620376C
qm_cnt_tran_pkt_stat                 [0x00000170] = 0xC38C8664
qm_cnt_tran_oecc_err_pkt_stat        [0x00000174] = 0x00000000
qm_cnt_tran_mpeg_stat                [0x00000178] = 0xFFFFFFFF
qm_cnt_tran_mpeg_sync_stat           [0x0000017C] = 0x06A0FC65
qm_cnt_tran_mpeg_only_sync_stat      [0x00000180] = 0x0620376C
qm_cnt_tran_dpv_stat                 [0x00000188] = 0x00000000
qm_rldram_ext_ecc                    [0x00000198] = 0x00000000
qm_rldram_cfg                        [0x0000019C] = 0x00101544
qm_rldram_ctrl                       [0x000001A0] = 0x00100389
```

```
qm_rldram_status                    [0x000001A4] = 0x03DF7C03
qm_rldram_cal_match_win_h           [0x000001A8] = 0x00000000
qm_rldram_cal_match_win_l           [0x000001AC] = 0x7FFFFFFF

JIB3_DS PG registers (base address 0xF8898000)

pg_mod                              [0x00000050] = 0x00000000
pg_dhs                              [0x00000054] = 0x00000000
pg_ipg                              [0x0000005C] = 0x00000000
pg_num                              [0x00000058] = 0x00000000
pg_payload_length                   [0x00000060] = 0x00000000
pg_payload_value                    [0x00000064] = 0x00000000
pg_pkt_hdr_prog_0                   [0x00000068] = 0x00000000
pg_pkt_hdr_prog_1                   [0x0000006C] = 0x00000000
pg_pkt_hdr_1                        [0x00000070] = 0x00000000
pg_pkt_hdr_2                        [0x00000074] = 0x00000000
pg_pkt_hdr_3                        [0x00000078] = 0x00000000
pg_pkt_hdr_4                        [0x0000007C] = 0x00000000
pg_pkt_hdr_5                        [0x00000080] = 0x00000000
pg_pkt_hdr_6                        [0x00000084] = 0x00000000

JIB3_DS PMBIST registers (base address 0xF8899000)

pmbist_ena_addr                     [0x00000060] = 0x00000002
pmbist_din_addr                     [0x00000064] = 0x00000000
pmbist_dout_addr                    [0x0000006C] = 0x00008101
pmbist_trgt_select_addr             [0x00000074] = 0x00000000
pmbist_ff_status                    [0x00000078] = 0x00000000
pmbist_num_wr_fr_pmbist             [0x0000007C] = 0x00000000
pmbist_num_rd_fr_pmbist             [0x00000080] = 0x00000000
pmbist_um_wr_2cmd_ff                [0x00000084] = 0x00000000
pmbist_num_rd_2cmd_ff               [0x00000088] = 0x00000000
pmbist_num_rd_rtn_pmbist            [0x0000008C] = 0x00000000
pmbist_num_wr_2dram                 [0x00000090] = 0x00000000
pmbist_num_rd_2dram                 [0x00000094] = 0x00000000
pmbist_num_rd_fr_dram               [0x00000098] = 0x00000000

DS PHY Configuration of Controller 0:
---------------------
  Base Frequency = 555000000Hz
  RF-Power = 52.0dBmV
  Annex = B Modulation = 256QAM
  Channel Status Interleave
  ------- ------ ----------
     0   Active     32
     1   Active     32
     2   Active     32
     3   Active     32
  DS_PHY PLL set for Annex-B

  DS PHY Device Information:
  -------------------
    Remora Version = 3.10
    UPX SW Version = 0x10D
    Upconverter Type:Unknown
    UPX Part Number =

  Device Status:
  --------------
    UPX Alarm Status = 0x3FF
    UPX Alarm Mask   = 0x19000
Remora registers (base address 0xF8900000)
-----------------------------------------
```

```
Remora General Registers (0xF8900000):
--------------------------------------
revision                            [0x00000000] = 0x00000003
hw_fpga_rev_id                      [0x00000004] = 0x0000000A
erp_scratch_pad0                    [0x00000008] = 0x00000000
erp_scratch_pad1                    [0x0000000C] = 0x00000000

Remora Reset and DCM Lock Registers (0xF8900100):
-------------------------------------------------
reset_ctrl                          [0x00000100] = 0x00000000
dcm_lock                            [0x00000104] = 0x0000000F

Remora Configuration Registers (0xF8900200):
--------------------------------------------
port_cfg[0]                         [0x00000200] = 0x00155549
port_cfg[1]                         [0x00000204] = 0x00155548
port_cfg[2]                         [0x00000208] = 0x00155548
port_cfg[3]                         [0x0000020C] = 0x00155548
port_cfg[4]                         [0x00000210] = 0x00155548
core_config_status                  [0x00000214] = 0x00000020
port_rm2tififo_prog_flags[0]        [0x00000218] = 0xBBA20C0D
port_rm2tififo_prog_flags[1]        [0x0000021C] = 0xBBA20C0D
port_rm2tififo_prog_flags[2]        [0x00000220] = 0xBBA20C0D
port_rm2tififo_prog_flags[3]        [0x00000224] = 0xBBA20C0D
port_rm2tififo_prog_flags[4]        [0x00000228] = 0xBBA20C0D

Remora DFT/Pattern Inject Registers (0xF8900300):
-------------------------------------------------
alt_sym_tst_mode                    [0x00000300] = 0x00005A69
alt_sym_tst_en_reg                  [0x00000304] = 0x00000000
qdr_mem_test_en_reg                 [0x00000308] = 0x00000000
qdr_mem_test_rd_wr_reg              [0x0000030C] = 0x00000A12
ready_for_data_input                [0x00000318] = 0x0000001F

Remora ECC Registers (0xF8900400):
----------------------------------
debug_cfg                           [0x00000400] = 0x00000000
sniff_frame_cnt                     [0x00000404] = 0x00000000
ecc_parity_conf_reg                 [0x00000408] = 0x00000003
ecc_uncorrect_data_log_reg          [0x0000040C] = 0x00002814
ecc_uncorrect_log_reg               [0x00000410] = 0x00000020
ecc_correctable_data_log_reg        [0x00000414] = 0x00002C14
ecc_correctable_log_reg             [0x00000418] = 0x00000028
qdr_ecc_corr_cnt_reg                [0x0000041C] = 0x00000000
fatal_err_log                       [0x00000420] = 0x00000000
err_inj_reg                         [0x00000424] = 0x00000000

Remora QDR Registers (0xF8900500):
----------------------------------
qdr_phy_idelayctrl_rst_reg          [0x00000500] = 0x00000000
qdr_phy_idelayctrl_rdy_err_reg      [0x00000504] = 0x00000261
qdr_phy_cal_tap_dly_reg             [0x00000508] = 0x00000ADB
qdr_phy_idelayctrl_ctrl_reg         [0x0000050C] = 0x00000002
qdr_init_ctrl_reg                   [0x00000510] = 0x801FFFFF

Remora Interrupt Status Registers (0xF8900600):
-----------------------------------------------
glb_int_stat_reg                    [0x00000600] = 0x00000000
int_stat_gr_reg[0]                  [0x00000604] = 0x00000000
int_stat_gr_reg[1]                  [0x00000608] = 0x00000000
int_stat_gr_reg[2]                  [0x0000060C] = 0x00000000
int_stat_gr_reg[3]                  [0x00000610] = 0x00000000
int_stat_gr_reg[4]                  [0x00000614] = 0x00000000
```

```
misc_int_stat_reg                   [0x00000618] = 0x00000001
fatal_err_src_reg                   [0x0000061C] = 0x00000000
port_local_interrupt_enable[0]      [0x00000620] = 0x0001FFFF
port_local_interrupt_enable[1]      [0x00000624] = 0x0001FFFF
port_local_interrupt_enable[2]      [0x00000628] = 0x0001FFFF
port_local_interrupt_enable[3]      [0x0000062C] = 0x0001FFFF
port_local_interrupt_enable[4]      [0x00000630] = 0x0001FFFF
misc_int_en_reg                     [0x00000634] = 0x00001FF8
fatal_err_en_reg                    [0x00000638] = 0x00000EFF
port_local_interrupt_override[0]    [0x0000063C] = 0x00000000
port_local_interrupt_override[1]    [0x00000640] = 0x00000000
port_local_interrupt_override[2]    [0x00000644] = 0x00000000
port_local_interrupt_override[3]    [0x00000648] = 0x00000000
port_local_interrupt_override[4]    [0x0000064C] = 0x00000000
misc_int_override                   [0x00000650] = 0x00000000
fatal_err_override                  [0x00000654] = 0x00000000

Remora Counts Registers (0xF8900800):
-------------------------------------
illegal_ch_num_pkt_drop_count       [0x00000800] = 0x00000000
fifo_full_mpeg_pkt_drop_count_hi    [0x00000804] = 0x00000000
fifo_full_mpeg_pkt_drop_count_lo    [0x00000808] = 0x00000000
channel_mpeg_pkt_count[0]           [0x0000080C] = 0x00000EE7
channel_mpeg_pkt_count[1]           [0x00000810] = 0x00000E8C
channel_mpeg_pkt_count[2]           [0x00000814] = 0x00000839
channel_mpeg_pkt_count[3]           [0x00000818] = 0x000009DF
channel_mpeg_pkt_count[4]           [0x0000081C] = 0x00000000
channel_mpeg_pkt_count[5]           [0x00000820] = 0x00000000
channel_mpeg_pkt_count[6]           [0x00000824] = 0x00000000
channel_mpeg_pkt_count[7]           [0x00000828] = 0x00000000
channel_mpeg_pkt_count[8]           [0x0000082C] = 0x00000000
channel_mpeg_pkt_count[9]           [0x00000830] = 0x00000000
channel_mpeg_pkt_count[10]          [0x00000834] = 0x00000000
channel_mpeg_pkt_count[11]          [0x00000838] = 0x00000000
channel_mpeg_pkt_count[12]          [0x0000083C] = 0x00000000
channel_mpeg_pkt_count[13]          [0x00000840] = 0x00000000
channel_mpeg_pkt_count[14]          [0x00000844] = 0x00000000
channel_mpeg_pkt_count[15]          [0x00000848] = 0x00000000
channel_mpeg_pkt_count[16]          [0x0000084C] = 0x00000000
channel_mpeg_pkt_count[17]          [0x00000850] = 0x00000000
channel_mpeg_pkt_count[18]          [0x00000854] = 0x00000000
channel_mpeg_pkt_count[19]          [0x00000858] = 0x00000000
port_re_timestamp_count[0]          [0x0000085C] = 0x97979796
port_re_timestamp_count[1]          [0x00000860] = 0x00000000
port_re_timestamp_count[2]          [0x00000864] = 0x00000000
port_re_timestamp_count[3]          [0x00000868] = 0x00000000
port_re_timestamp_count[4]          [0x0000086C] = 0x00000000
port_rx_fifo_overflow_drop_count[0] [0x00000870] = 0x00000000
port_rx_fifo_overflow_drop_count[1] [0x00000874] = 0x00000000
port_rx_fifo_overflow_drop_count[2] [0x00000878] = 0x00000000
port_rx_fifo_overflow_drop_count[3] [0x0000087C] = 0x00000000
port_rx_fifo_overflow_drop_count[4] [0x00000880] = 0x00000000
channel_jib_if_pkt_count[0]         [0x00000884] = 0x4AFC8612
channel_jib_if_pkt_count[1]         [0x00000888] = 0x44C96772
channel_jib_if_pkt_count[2]         [0x0000088C] = 0x42A048EA
channel_jib_if_pkt_count[3]         [0x00000890] = 0x43E61FF6
channel_jib_if_pkt_count[4]         [0x00000894] = 0x00000000
channel_jib_if_pkt_count[5]         [0x00000898] = 0x00000000
channel_jib_if_pkt_count[6]         [0x0000089C] = 0x00000000
channel_jib_if_pkt_count[7]         [0x000008A0] = 0x00000000
channel_jib_if_pkt_count[8]         [0x000008A4] = 0x00000000
channel_jib_if_pkt_count[9]         [0x000008A8] = 0x00000000
channel_jib_if_pkt_count[10]        [0x000008AC] = 0x00000000
channel_jib_if_pkt_count[11]        [0x000008B0] = 0x00000000
```

```
channel_jib_if_pkt_count[12]        [0x000008B4] = 0x00000000
channel_jib_if_pkt_count[13]        [0x000008B8] = 0x00000000
channel_jib_if_pkt_count[14]        [0x000008BC] = 0x00000000
channel_jib_if_pkt_count[15]        [0x000008C0] = 0x00000000
channel_jib_if_pkt_count[16]        [0x000008C4] = 0x00000000
channel_jib_if_pkt_count[17]        [0x000008C8] = 0x00000000
channel_jib_if_pkt_count[18]        [0x000008CC] = 0x00000000
channel_jib_if_pkt_count[19]        [0x000008D0] = 0x00000000

Remora Timestamp Registers (0xF8900900):
----------------------------------------
local_1024_ts_ctrl                  [0x00000900] = 0x00000039
local_1024_current_ts               [0x00000904] = 0xC354FFA0
local_1024_tcc_ts_latch             [0x00000908] = 0x7291125F
doc_ts_offset_ch_0_1                [0x0000090C] = 0x04AF04AF
doc_ts_offset_ch_2_3                [0x00000910] = 0x04AF04AF
doc_ts_offset_ch_4_5                [0x00000914] = 0x04F704F7
doc_ts_offset_ch_6_7                [0x00000918] = 0x04F704F7
doc_ts_offset_ch_8_9                [0x0000091C] = 0x04F704F7
doc_ts_offset_ch_10_11              [0x00000920] = 0x04F704F7
doc_ts_offset_ch_12_13              [0x00000924] = 0x04F704F7
doc_ts_offset_ch_14_15              [0x00000928] = 0x04F704F7
doc_ts_offset_ch_16_17              [0x0000092C] = 0x04F704F7
doc_ts_offset_ch_18_19              [0x00000930] = 0x04F704F7

Remora PRATE/SRATE Registers (0xF8900A00):
------------------------------------------
port_prate_regs[0].prate_ctrl       [0x00000A00] = 0x00000003
port_prate_regs[0].prate_m_prime_lo [0x00000A04] = 0x0005971E
port_prate_regs[0].prate_n_prime_lo [0x00000A08] = 0x08AA5B88
port_prate_regs[0].prate_m_prime_hi [0x00000A0C] = 0x00000000
port_prate_regs[1].prate_ctrl       [0x00000A10] = 0x00000003
port_prate_regs[1].prate_m_prime_lo [0x00000A14] = 0x00000191
port_prate_regs[1].prate_n_prime_lo [0x00000A18] = 0x00037E78
port_prate_regs[1].prate_m_prime_hi [0x00000A1C] = 0x00000000
port_prate_regs[2].prate_ctrl       [0x00000A20] = 0x00000003
port_prate_regs[2].prate_m_prime_lo [0x00000A24] = 0x00000191
port_prate_regs[2].prate_n_prime_lo [0x00000A28] = 0x00037E78
port_prate_regs[2].prate_m_prime_hi [0x00000A2C] = 0x00000000
port_prate_regs[3].prate_ctrl       [0x00000A30] = 0x00000003
port_prate_regs[3].prate_m_prime_lo [0x00000A34] = 0x00000191
port_prate_regs[3].prate_n_prime_lo [0x00000A38] = 0x00037E78
port_prate_regs[3].prate_m_prime_hi [0x00000A3C] = 0x00000000
port_prate_regs[4].prate_ctrl       [0x00000A40] = 0x00000003
port_prate_regs[4].prate_m_prime_lo [0x00000A44] = 0x00000191
port_prate_regs[4].prate_n_prime_lo [0x00000A48] = 0x00037E78
port_prate_regs[4].prate_m_prime_hi [0x00000A4C] = 0x00000000
port_srate_regs[0].srate_ctrl       [0x00000A50] = 0x00000003
port_srate_regs[0].srate_mn         [0x00000A54] = 0x004E0095
port_srate_regs[1].srate_ctrl       [0x00000A58] = 0x00000003
port_srate_regs[1].srate_mn         [0x00000A5C] = 0x0191032C
port_srate_regs[2].srate_ctrl       [0x00000A60] = 0x00000003
port_srate_regs[2].srate_mn         [0x00000A64] = 0x0191032C
port_srate_regs[3].srate_ctrl       [0x00000A68] = 0x00000003
port_srate_regs[3].srate_mn         [0x00000A6C] = 0x0191032C
port_srate_regs[4].srate_ctrl       [0x00000A70] = 0x00000003
port_srate_regs[4].srate_mn         [0x00000A74] = 0x0191032C
```

The following example shows a typical display for the **show controller integrated-cable** command and the **association** keyword.

```
Router# show controller integrated-Cable 7/1/0 association
```

```
WB Association Info for 7/1 No of WB 30
WB                      BG   Bundle  NB          NB chan  Reserved  Total
channel                 ID   num     channel     ID       CIR       CIR
Wideband-Cable7/1/0:0   1057 1       Cable7/1/0  121      0         21751500
                                     Multicast           0         21751500
Wideband-Cable7/1/3:0   1153 1       Cable7/1/3  133      0         12481000
                                     Multicast           0         12481000
```

The following example shows a typical display for the **show controller integrated-cable** command and the **brief** keyword.

```
Router# show controller integrated-Cable 6/0/0 brief

Integrated Cable Controller 6/0/0:
----------------------------------
  Channel 1  Annex = B  Modulation = 256 QAM
  Channel 2  Annex = B  Modulation = 256 QAM
  Channel 3  Annex = B  Modulation = 256 QAM
  Channel 4  Annex = B  Modulation = 256 QAM

Jib3-DS Device Information:
---------------------------
   Jib3-DS Version = 2.2.1.8
   SW Rev ID = 0x00020002 HW Rev ID = 0x00010008
   Device Type: Coldplay
   Driver State: 3

Channel Resources:
------------------
   Total Non-bonded Channels..........= 20
   Per-Controller Non-bonded Channels = 4
   Total Bonded Channels..............= 32
   Per-Controller Bonded Channels.....= 6

Slot-Wide Resources:
--------------------
   Number of PHS Rules...........= 12K (0x3000)
   Number of BPI Table Entries...= 24K (0x6000)
   Number of Service Flows.......= 64K (0x10000)


DS PHY Device Information:
  -------------------
    Remora Version = 3.10
    UPX Board Revision = Toucan Rev-B
    UPX SW Version = 0x109
    Toucan FPGA Version = 0x27

  Device Status:
  --------------
    UPX Alarm Status = 0x3FF
    UPX Alarm Mask   = 0x19000
```

The following example shows a typical display for the **show controller integrated-cable** command and the **config** keyword.

```
Router# show controller integrated-Cable 6/0/0 config

Load for five secs: 16%/1%; one minute: 15%; five minutes: 14%
Time source is NTP, *15:06:26.476 EDT Sun Mar 21 2010


Integrated Cable Controller 6/0/0:
----------------------------------
  Channel 1  Annex = B  Modulation = 256 QAM
  Channel 2  Annex = B  Modulation = 256 QAM
  Channel 3  Annex = B  Modulation = 256 QAM
  Channel 4  Annex = B  Modulation = 256 QAM

Jib3-DS Device Information:
---------------------------
   Jib3-DS Version = 2.2.1.8
```

```
   SW Rev ID = 0x00020002 HW Rev ID = 0x00010008
   Device Type: Coldplay
   Driver State: 3

Channel Resources:
------------------
   Total Non-bonded Channels.........= 20
   Per-Controller Non-bonded Channels = 4
   Total Bonded Channels.............= 32
   Per-Controller Bonded Channels.....= 6

Slot-Wide Resources:
--------------------
   Number of PHS Rules...........= 12K (0x3000)
   Number of BPI Table Entries...= 24K (0x6000)
   Number of Service Flows.......= 64K (0x10000)



Sniffer Configuration:
----------------------
Non-Bonded Channel Mask = 0x00000000
Bonded Channel Mask.....= 0x00000000
Sniff All Enable........= False

Configured Sniffer MAC Addresses:
Entry     MAC Address     Enabled
-----   ---------------   -------
0       0000.0000.0000     False
1       0000.0000.0000     False
2       0000.0000.0000     False
3       0000.0000.0000     False
4       0000.0000.0000     False
5       0000.0000.0000     False
6       0000.0000.0000     False
7       0000.0000.0000     False
8       0000.0000.0000     False
9       0000.0000.0000     False
10      0000.0000.0000     False
11      0000.0000.0000     False
12      0000.0000.0000     False
13      0000.0000.0000     False
14      0000.0000.0000     False
15      0000.0000.0000     False


Replication Table:
------------------

Replication Entry Index   Channel Mask
-----------------------   ------------
41                        0x0000000F
42                        0x0000000F
43                        0x0000000F
44                        0x0000000F


Configured Bonding Groups:
--------------------------
Bonded Channel   Channels in Bonding Group
--------------   -------------------------
00               0, 1, 2, 3
```

```
Sync Configuration:
-------------------

Channel   MAC Address      Interval
-------   --------------   --------
0         001d.70cc.0b90      10 ms
1         001d.70cc.0b90      10 ms
2         001d.70cc.0b90      10 ms
3         001d.70cc.0b90      10 ms

DS PHY Configuration of Controller 0:
---------------------
  Base Frequency = 555000000Hz
  RF-Power = 52.0dBmV
  Annex = B Modulation = 256QAM
  Channel Status Interleave
  ------- ------ ----------
     0   Active     32
     1   Active     32
     2   Active     32
     3   Active     32
  DS_PHY PLL set for Annex-B
```

The following example shows a typical display for the **show controller integrated-cable** command and the **counters** keyword with **rf-channel** and **wb-channel** options.

```
Router# show controllers integrated-Cable 6/0/0 counters rf-channel

Load for five secs: 3%/0%; one minute: 13%; five minutes: 13%
Time source is NTP, *15:06:36.267 EDT Sun Mar 21 2010

Controller  RF    MPEG       MPEG       MPEG       Sync       MAP/UCD
            Chan  Packets    bps        Mbps       Packets    Packets
                  Tx                               Tx         Tx
6/0/0       0     1258146418   3561772    3.561772   27806521   552546936
6/0/0       1     1154122165   3026599    3.26599    27806521   552248538
6/0/0       2     1117840977   1707741    1.707741   27806521   551490577
6/0/0       3     1139201813   1981820    1.981820   27806520   551866145

Router# show controllers integrated-Cable 6/0/0 counters wb-channel

Load for five secs: 4%/1%; one minute: 12%; five minutes: 13%
Time source is NTP, *15:06:43.114 EDT Sun Mar 21 2010

Controller      WB channel       Tx packets       Tx octets
6/0/0           0                881249714         466143984373
6/0/0           1                0                0
6/0/0           2                0                0
6/0/0           3                0                0
6/0/0           4                0                0
6/0/0           5                0                0
```

The following example shows a typical display for the **show controller integrated-cable** command and the **errors** keyword.

```
Router# show controller integrated-Cable 6/0/0 errors

Load for five secs: 2%/1%; one minute: 10%; five minutes: 13%
Time source is NTP, *15:06:59.788 EDT Sun Mar 21 2010


Rx SPI Error Counters:
```

```
----------------------
Non-Droppable Errors Channel 0 = 00  FIFO Pkt Drop Count Channel 0 = 00000000
Non-Droppable Errors Channel 1 = 00  FIFO Pkt Drop Count Channel 1 = 00000000
Non-Droppable Errors Channel 2 = 00  FIFO Pkt Drop Count Channel 2 = 00000000
Non-Droppable Errors Channel 3 = 00  Dropped Bytes                 = 00000000


Tx SPI Error Counters:
----------------------
DIP2 Errors              = 00        Illegal Src Pattern Errs  = 00
EOP Abort Pkts Channel 0 = 00000000  EOP Abort Bytes Channel 0 = 00000000
EOP Abort Pkts Channel 1 = 00000000  EOP Abort Bytes Channel 1 = 00000000
EOP Abort Pkts Channel 2 = 00000000  EOP Abort Bytes Channel 2 = 00000000
EOP Abort Pkts Channel 3 = 00000000  EOP Abort Bytes Channel 3 = 00000000

DOCSIS Processor Error Counters:
--------------------------------
EFC and Stats Errors = 00000000  DOCSIS Engine Errors = 00025934
PHS Errors           = 00000000  Parser Errors        = 00000000
Output Packet Errors = 00000000  Dropped Packets      = 00000000
Input Packet Errors  = 00000000  ECC Errors           = 00000000

BPI Error Counters:
-------------------
Bad Input Pkts  = 22  Single-bit ECC Errors = 0
Bad Output Pkts = 22

Queue Manager Error Counters:
-----------------------------
BPRAM Bad End of Packets..= 00000000  Bonded Map Errors............= 00000000
BPRAM Overflows...........= 00000000  BPRAM Bad Packet Type Errors = 00000000
Directed Map Error Counts = 00000000  BPRAM ECC Errors.............= 00000000
RLDRAM ECC Errors.........= 00000000  Queue Overflows..............= 00000000

Sequencer Error Counters:
-------------------------
BlkRAM ECC Errors = 00000000

ERP Error Counters:
-------------------
Processor Bus Errored Address = 0x00000000

Return Interface Error Counters:
--------------------------------
Phys If Rx FIFO Oflow Drops = 00000000  Phys If LB FIFO Oflow Drops = 00000000
Sniffer FIFO Oflow Drops....= 00000000  Phys If Rx Parity Errors....= 00000000
Phys If Length Errors.......= 00000000  Phys If Rx FIFO ECC Errors..= 00000000
Phys If LB FIFO ECC Errors..= 00000000  Sniffer FIFO ECC Errors.....= 00000000
SPI LB FIFO ECC Errors......= 00000000


Jib3-DS (Coldplay) interrupt events
      count
 current   total    bursts  Event name
      21     25921       0  DOCSIS Processing Block: DSID Valid Error


Internal error packet buffer:
-----------------------------

IPH Header:
Packet type......... = 0x00
Flags............... = 0x00
Packet Length....... = 33015 (0x80F7)
```

```
DOCSIS Header Length = 11
Replication Index... = 0
Stats Index......... = 0x0546
Flags2.............. = 0x01040000
Service Flow........ = 0x00000000

Packet Body:
0x010500E1 0x4411C0FA 0x00895500 0x118072C7
0x6A001D70 0xCC0BE208 0x0045B800 0xCA000000
0x003F1121 0x42AC2200 0x63AC2200 0x82C004C0
0x0200B600 0x008000F1 0x318FF541 0x1BA16AE2
0xB303AF17 0x1652643F 0x4498F48E 0xE278F16B
0x167521EC 0x3CBF34DD 0xDCBEA10E 0x0B5AA70C
0xE6B9B77F 0x8E3590ED 0x4EC9388A 0x9B886A51

Internal magic number error packet buffer:
-----------------------------------------
No magic number errored packet available
```

The following example shows a typical display for the **show controller integrated-cable** command and the **mapping** keyword with **rf-channel** and **wb-channel** options.

```
Router# show controller integrated-Cable 6/0/0 mapping rf-channel

Load for five secs: 9%/1%; one minute: 11%; five minutes: 13%
Time source is NTP, *15:07:13.079 EDT Sun Mar 21 2010
Ctrlr    RF       MC         MC Rem.    WB         WB         WB Rem.
         channel  BW %       Ratio      channel    BW %       Ratio
6/0/0    0        33         1          6/0/0:0     63        1
6/0/0    1        33         1          6/0/0:0     63        1
6/0/0    2        33         1          6/0/0:0     63        1
6/0/0    3        33         1          6/0/0:0     63        1

Router# show controllers integrated-Cable 6/0/0 mapping wb-channel

Load for five secs: 18%/1%; one minute: 11%; five minutes: 13%
Time source is NTP, *15:07:17.566 EDT Sun Mar 21 2010
Ctrlr    WB       RF         BW %       Remaining
         channel  channel               Ratio
6/0/0    0        6/0/0:0     63        1
                  6/0/0:1     63        1
                  6/0/0:2     63        1
                  6/0/0:3     63        1
```

The following example shows a typical display for the **show controller integrated-cable** command and the **registers** keyword.

```
Router# show controller integrated-Cable 6/0/0 registers

Load for five secs: 12%/2%; one minute: 11%; five minutes: 13%
Time source is NTP, *15:07:25.549 EDT Sun Mar 21 2010

JIB3_DS BPI registers (base address 0xF8880000)

bpi_int_isr_0                      [0x00000000] = 0x00000000
bpi_int_ier_0                      [0x00000004] = 0x0000000F
glb_int_isr_0                      [0x00000010] = 0x00000000
glb_int_ier_0                      [0x00000014] = 0x000003FF
glb_int_isr_1                      [0x00000020] = 0x00000000
glb_int_ier_1                      [0x00000024] = 0x000003FF
bpi_int_fesr_0                     [0x00000040] = 0x00000000
bpi_tst_tp_sel_reg                 [0x00000050] = 0x00000000
bpi_tst_tp_reg                     [0x00000054] = 0x00000000
```

```
bpi_cnt_good_packet_in_cnt          [0x00000064] = 0x00045B37
bpi_cnt_bad_packet_in_cnt           [0x00000068] = 0x0000000D
bpi_cnt_good_packet_out_cnt         [0x0000006C] = 0x00045B37
bpi_cnt_bad_packet_out_cnt          [0x00000070] = 0x0000000D
bpi_ecc_sbit_err_cnt                [0x00000074] = 0x00000000
glb_sw_rev_id                       [0x00000078] = 0x00020002
glb_hw_rev_id                       [0x0000007C] = 0x00010008
frz_reg                             [0x00000080] = 0x00000000
frz_en                              [0x00000084] = 0x00000001
glb_dcm_status                      [0x00000088] = 0x00000007
glb_sw_rst                          [0x0000008C] = 0x00000000

JIB3_DS ERP registers (base address 0xF8881000)

erp_irq_src_reg                     [0x00000000] = 0x00000000
erp_irq_en_reg                      [0x00000004] = 0x80000FFF
erp_tp_sel_reg                      [0x00000050] = 0x00000000
erp_tp_reg                          [0x00000054] = 0x00000000
erp_cfg_reg                         [0x00000060] = 0x00000000
erp_err_record_reg                  [0x00000064] = 0x00000000
erp_err_addr_record_reg             [0x00000068] = 0x00000000
erp_err_wd_record_reg               [0x0000006C] = 0x00000000
erp_proc_err_addr_record_reg        [0x00000090] = 0x00000000

JIB3_DS RX SPI registers (base address 0xF8882000)

rxspi_irq_src_reg                   [0x00000000] = 0x00000000
rxspi_irq_en_reg                    [0x00000004] = 0x000001FF
rxspi_ferr_src_reg                  [0x00000040] = 0x00000000
rxspi_testpoint_sel_reg             [0x00000050] = 0x00000000
rxspi_testpoint_reg                 [0x00000054] = 0x00000000
rxspi_rst_cntl_reg                  [0x00000060] = 0x00000000
rxspi_cntl_status_reg               [0x00000064] = 0x00000005
rxspi_cfg_cntl_reg                  [0x00000068] = 0x00000021
rxspi_afthres_reg                   [0x0000006C] = 0x01C00180
rxspi_cal_dur_reg                   [0x00000070] = 0x00030000
rxspi_non_drop_err_cnt_reg          [0x00000088] = 0x00000000
rxspi_drop_byte_cnt_reg             [0x0000008C] = 0x00000000
rxspi_rx_byte_cnt_reg[0]            [0x000000B0] = 0x01A499EF
rxspi_rx_byte_cnt_reg[1]            [0x000000B4] = 0x00CF4ED0
rxspi_rx_byte_cnt_reg[2]            [0x000000B8] = 0x0001F030
rxspi_rx_pkt_cnt_reg[0]             [0x000000C0] = 0x0001D242
rxspi_rx_pkt_cnt_reg[1]             [0x000000C4] = 0x0002828C
rxspi_rx_pkt_cnt_reg[2]             [0x000000C8] = 0x00000684
rxspi_fifo_pkt_drop_cnt_reg[0]      [0x000000E0] = 0x00000000
rxspi_fifo_pkt_drop_cnt_reg[1]      [0x000000E4] = 0x00000000
rxspi_fifo_pkt_drop_cnt_reg[2]      [0x000000E8] = 0x00000000
rxspi_calendar_table_reg[0]         [0x00000800] = 0x00000000
rxspi_calendar_table_reg[1]         [0x00000804] = 0x00000001
rxspi_calendar_table_reg[2]         [0x00000808] = 0x00000002
rxspi_calendar_table_reg[3]         [0x0000080C] = 0x00000003

JIB3_DS TX SPI registers (base address 0xF8883000)

txspi_irq_src_reg                   [0x00000000] = 0x00000000
txspi_irq_en_reg                    [0x00000004] = 0x0000001F
txspi_ferr_src_reg                  [0x00000040] = 0x00000000
txspi_testpoint_sel_reg             [0x00000050] = 0x00000000
txspi_testpoint_reg                 [0x00000054] = 0x00000000
txspi_rst_cntl_reg                  [0x00000060] = 0x00000000
txspi_cntl_status_reg               [0x00000064] = 0x00000009
txspi_cfg_cntl_reg                  [0x00000068] = 0x00000001
txspi_afthres_reg                   [0x0000006C] = 0x01EC01E8
txspi_cal_dur_reg                   [0x00000070] = 0x00040000
```

```
txspi_train_cntl_reg                [0x00000074] = 0x00000000
txspi_nonfatalerr_cnt_reg           [0x00000080] = 0x00000000
txspi_eop_abort_pkt_cnt_reg[0]      [0x00000090] = 0x00000000
txspi_eop_abort_pkt_cnt_reg[1]      [0x00000094] = 0x00000000
txspi_eop_abort_pkt_cnt_reg[2]      [0x00000098] = 0x00000000
txspi_eop_abort_pkt_cnt_reg[3]      [0x0000009C] = 0x00000000
txspi_eop_abort_byte_cnt_reg[0]     [0x000000A0] = 0x00000000
txspi_eop_abort_byte_cnt_reg[1]     [0x000000A4] = 0x00000000
txspi_eop_abort_byte_cnt_reg[2]     [0x000000A8] = 0x00000000
txspi_eop_abort_byte_cnt_reg[3]     [0x000000AC] = 0x00000000
txspi_tx_byte_cnt_reg[0]            [0x000000C0] = 0x00000000
txspi_tx_byte_cnt_reg[1]            [0x000000C4] = 0x00000000
txspi_tx_byte_cnt_reg[2]            [0x000000C8] = 0x00000000
txspi_tx_byte_cnt_reg[3]            [0x000000CC] = 0x00000000
txspi_tx_pkt_cnt_reg[0]             [0x00000100] = 0x00000000
txspi_tx_pkt_cnt_reg[1]             [0x00000104] = 0x00000000
txspi_tx_pkt_cnt_reg[2]             [0x00000108] = 0x00000000
txspi_tx_pkt_cnt_reg[3]             [0x0000010C] = 0x00000000
txspi_calendar_table_reg[0]         [0x00000800] = 0x00000000
txspi_calendar_table_reg[1]         [0x00000804] = 0x00000001
txspi_calendar_table_reg[2]         [0x00000808] = 0x00000002
txspi_calendar_table_reg[3]         [0x0000080C] = 0x00000003
txspi_calendar_table_reg[4]         [0x00000810] = 0x00000004

JIB3_DS DOC registers (base address 0xF8884000)

doc_int_err0                        [0x00000000] = 0x00000000
doc_int_err0_ier                    [0x00000004] = 0xFFBFBFFD
doc_int_err1                        [0x00000010] = 0x00000000
doc_int_err1_ier                    [0x00000014] = 0x003FFFF8
doc_int_fesr                        [0x00000040] = 0x00000000
doc_test_sel                        [0x00000050] = 0x00000000
doc_testpoint                       [0x00000054] = 0x00000000
doc_cfg_ctrl                        [0x00000060] = 0x031A0000
doc_err_cap_ctrl                    [0x00000064] = 0x001F0001
doc_err_cap_addr                    [0x00000068] = 0x00000020
doc_err_cap_data                    [0x0000006C] = 0x000080F7
doc_seg_num                         [0x00000070] = 0x00000001
doc_wb_chan_stats_sel               [0x00000074] = 0x00000077
doc_wb_pkt_cnt                      [0x00000078] = 0x00000000
doc_wb_byte_cnt                     [0x0000007C] = 0x00000000
doc_wb_police_sel                   [0x00000080] = 0x00000001
doc_wb_police_data                  [0x00000084] = 0x00000000
doc_wb_police_intv                  [0x00000088] = 0x00000000
doc_nb_chan_stats_sel               [0x0000008C] = 0x0000004C
doc_nb_pkt_cnt                      [0x00000090] = 0x00000000
doc_nb_byte_cnt                     [0x00000094] = 0x00000000
doc_nb_police_sel                   [0x00000098] = 0x00000001
doc_nb_police_data                  [0x0000009C] = 0x00000000
doc_nb_police_intv                  [0x000000A0] = 0x00000000
doc_int_doc_cnt                     [0x000000D4] = 0x00000000
doc_int_ecc_sbiterr_cnt             [0x000000D8] = 0x00000000
doc_pkt_good_in_cnt                 [0x000000DC] = 0x00045B5C
doc_pkt_good_out_cnt                [0x000000E0] = 0x00045B39
doc_pkt_err_in_cnt                  [0x000000E4] = 0x00000000
doc_pkt_err_out_cnt                 [0x000000E8] = 0x00000023
doc_pkt_drop_cnt                    [0x000000EC] = 0x00000000
doc_efc_all_cnt                     [0x000000F0] = 0x00000000
doc_efc_hi_cnt                      [0x000000F4] = 0x00000000
doc_efc_me_cnt                      [0x000000F8] = 0x00000000
doc_efc_lo_cnt                      [0x000000FC] = 0x00000000
doc_efc_ch_sel                      [0x00000100] = 0x00000000
doc_efc_debug_ctrl                  [0x00000104] = 0x00000000
doc_rldram_ext_ecc                  [0x00000114] = 0x00000000
```

```
doc_rldram_cfg                      [0x00000118] = 0x00101544
doc_rldram_ctrl                     [0x0000011C] = 0x00100389
doc_rldram_status                   [0x00000120] = 0x039D7403
doc_rldram_blk_clr                  [0x00000124] = 0x0B7FFFFF
doc_rldram_cal_match_win_h          [0x00000128] = 0x00000000
doc_rldram_cal_match_win_l          [0x0000012C] = 0x1FFFFFFF
doc_rldram_ecc_err_rec_addr         [0x00000130] = 0x00000000
doc_magic_num_err_pkt_ctrl          [0x00000150] = 0x00000000
doc_magic_num_err_pkt_addr          [0x00000154] = 0x00000001
doc_magic_num_err_pkt_data          [0x00000158] = 0x00000000

JIB3_DS RIF registers (base address 0xF8885000)

rif_int_err0                        [0x00000000] = 0x00000000
rif_int_ier0                        [0x00000004] = 0x00000007
rif_int_fesr0                       [0x00000040] = 0x00000000
rif_tp_sel                          [0x00000050] = 0x00000000
rif_tp                              [0x00000054] = 0x00000000
rif_cfg_ctrl                        [0x00000060] = 0x00000000
rif_cnt_in_mpeg_cnt                 [0x00000064] = 0x000A6226
rif_cnt_out_good_mpeg_cnt           [0x00000068] = 0x000A6226
rif_cnt_out_bad_mpeg_cnt            [0x0000006C] = 0x00000000
rif_cnt_drop_mpeg_cnt               [0x00000070] = 0x00000000
rif_1bit_ecc_err_stat               [0x00000074] = 0x00000000

JIB3_DS RTN registers (base address 0xF8886000)

return_int_isr                      [0x00000000] = 0x00000000
return_int_ier                      [0x00000004] = 0x000001FF
return_int_fesr                     [0x00000040] = 0x00000000
return_tp_sel                       [0x00000050] = 0x00000000
return_tp                           [0x00000054] = 0x00000000
return_ctrl_reg                     [0x00000060] = 0x00000000
return_pif_loopback_chnl            [0x00000064] = 0x00000000
return_sniffer_nonbonded_en         [0x00000068] = 0x00000000
return_sniffer_bonded_en            [0x0000006C] = 0x00000000
return_spi_chnl_sel                 [0x00000070] = 0x0000013A
return_err_drop_en                  [0x00000074] = 0x0000000F
return_snf_macda_cfg_addr           [0x00000078] = 0x0000000F
return_snf_macda_cfg_data_hi        [0x0000007C] = 0x00000000
return_snf_macda_cfg_data_lo        [0x00000080] = 0x00000000
return_in_pifrx_good_cnt            [0x000000A0] = 0x00000000
return_in_pifrx_bad_cnt             [0x000000A4] = 0x00000000
return_in_piflp_good_cnt            [0x000000A8] = 0x000A6224
return_in_piflp_bad_cnt             [0x000000AC] = 0x00000000
return_in_sniffer_good_cnt          [0x000000B0] = 0x00045B3A
return_in_sniffer_bad_cnt           [0x000000B4] = 0x00000023
return_in_spi_loop_good_cnt         [0x000000B8] = 0x00000000
return_in_spi_loop_bad_cnt          [0x000000BC] = 0x00000000
return_out_spi0_cnt                 [0x000000C0] = 0x00000000
return_out_spi1_cnt                 [0x000000C4] = 0x00000000
return_out_spi2_cnt                 [0x000000C8] = 0x00000000
return_out_spi3_cnt                 [0x000000CC] = 0x00000000
return_out_spi4_cnt                 [0x000000D0] = 0x00000000
return_pifrx_if_par_err_drop_cnt    [0x000000D4] = 0x00000000
return_pifrx_if_len_err_drop_cnt    [0x000000D8] = 0x00000000
return_piflp_if_err_drop_cnt        [0x000000DC] = 0x00000000
return_piflp_if_chnl_drop_cnt       [0x000000E0] = 0x00000000
return_snf_pb_err_drop_cnt          [0x000000E4] = 0x00000023
return_snf_pkt_type_err_drop_cnt    [0x000000E8] = 0x00045B3A
return_spilp_if_err_drop_cnt        [0x000000EC] = 0x00000000
return_pifrx_traffic_mux_drop_cnt   [0x000000F0] = 0x00000000
return_piflp_traffic_mux_drop_cnt   [0x000000F4] = 0x00000000
return_snf_traffic_mux_drop_cnt     [0x000000F8] = 0x00000000
```

```
return_spilp_traffic_mux_drop_cnt   [0x000000FC] = 0x00000000
return_pifrx_fifo_overflow_drop_cnt [0x00000100] = 0x00000000
return_piflp_fifo_overflow_drop_cnt [0x00000104] = 0x00000000
return_snf_fifo_overflow_drop_cnt   [0x00000108] = 0x00000000
return_spilp_fifo_overflow_drop_cnt [0x0000010C] = 0x00000000
return_pifrx_if_par_err_cnt         [0x00000110] = 0x00000000
return_pifrx_if_len_err_cnt         [0x00000114] = 0x00000000
return_pifrx_fifo_ecc_1berr_cnt     [0x00000118] = 0x00000000
return_piflp_fifo_ecc_1berr_cnt     [0x0000011C] = 0x00000000
return_snf_fifo_ecc_1berr_cnt       [0x00000120] = 0x00000000
return_spilp_fifo_ecc_1berr_cnt     [0x00000124] = 0x00000000

JIB3_DS DLM registers (base address 0xF8890000)

dlm_int_isr_0                       [0x00000000] = 0x00000004
dlm_int_ier_0                       [0x00000004] = 0x00000000
dlm_cnt_local_ts_reg                [0x00000064] = 0x8D7DF4CD
dlm_cfg_tss_comp_reg                [0x00000068] = 0x00000027
dlm_cfg_tss_ctrl_reg                [0x0000006C] = 0x00000000
dlm_cfg_tss_cmd_reg                 [0x00000070] = 0x00000000
dlm_cnt_ts_load_cnt                 [0x000000BC] = 0x00000000
dlm_cnt_ts_chk_failed_cnt           [0x000000C4] = 0x00000000
dlm_cnt_tss_perr_cnt                [0x000000C8] = 0x00000000
dlm_cnt_load_ts_reg                 [0x000000D0] = 0x003F52EF

JIB3_DS SEQ registers (base address 0xF8892000)

seq_int_err0                        [0x00000000] = 0x0000000F
seq_int_ier0                        [0x00000004] = 0x000FFFFF
seq_int_err3                        [0x00000030] = 0x00000000
seq_int_ier3                        [0x00000034] = 0x00000001
seq_int_fatal_err                   [0x00000040] = 0x00000000
seq_tp_sel                          [0x00000050] = 0x00000000
seq_tp                              [0x00000054] = 0x00000000
seq_cfg_en                          [0x00000060] = 0x00000001
seq_cfg_sync_timer_sel              [0x00000064] = 0x00000014
seq_cfg_sync_timer_data             [0x00000068] = 0x00000000
seq_cfg_sync_sa_sel                 [0x0000006C] = 0x00000014
seq_cfg_sync_sa_data_lo             [0x00000070] = 0x00000000
seq_cfg_sync_sa_data_hi             [0x00000074] = 0x00000000
seq_cfg_tkb_timer_sel               [0x00000078] = 0x00000015
seq_cfg_tkb_timer_data              [0x0000007C] = 0x00000000
seq_cfg_tkb_max                     [0x00000080] = 0x00000000
seq_hwdbg_dpv_proc_table_addr       [0x00000090] = 0x00000001
seq_hwdbg_dpv_ptr_mod_table         [0x00000094] = 0x00000000
seq_hwdbg_dpv_timestamp_table       [0x00000098] = 0x00000000
seq_hwdbg_dpv_hcs_table             [0x0000009C] = 0x00000000
seq_cnt_blkram_oecc_err_stat        [0x000000A4] = 0x00000000
seq_cnt_tran_mpeg_stat              [0x000000A8] = 0x000A6224
seq_cnt_tran_mpeg_sync_stat         [0x000000AC] = 0x00000000
seq_cnt_tran_only_sync_stat         [0x000000B0] = 0x00000000
seq_cnt_tran_dpv_stat               [0x000000B8] = 0x00000000

JIB3_DS QM registers (base address 0xF8893000)

qm_int_isr0                         [0x00000000] = 0x00000000
qm_int_ier0                         [0x00000004] = 0x0000007F
qm_int_isr1                         [0x00000010] = 0x00000000
qm_int_ier1                         [0x00000014] = 0x000FFFFF
qm_int_fat_err_isr                  [0x00000040] = 0x00000000
qm_tst_tp_sel                       [0x00000050] = 0x00000000
qm_tst_tp                           [0x00000054] = 0x00000000
qm_cfg_chnl_rst_0                   [0x00000060] = 0x00000000
qm_cfg_ctl                          [0x0000006C] = 0x00000011
```

```
qm_cfg_sqf_fac_addr                [0x0000008C] = 0x00000015
qm_cfg_sqf_fac_data                [0x00000090] = 0x00000000
qm_cfg_bond_chnl_map_addr          [0x00000094] = 0x00000020
qm_cfg_bond_chnl_map_data_lo       [0x00000098] = 0x00000000
qm_cfg_flt_thr_addr                [0x000000A4] = 0x00000250
qm_cfg_flt_thr_data                [0x000000A8] = 0x00000000
qm_cfg_repl_addr                   [0x000000AC] = 0x00000000
qm_cfg_repl_data_lo                [0x000000B0] = 0x00000000
qm_hwdbg_buf_mag_addr              [0x000000BC] = 0x00000001
qm_hwdbg_wptr_data_lo              [0x000000C0] = 0x00014F60
qm_hwdbg_wptr_data_mi              [0x000000C4] = 0x000033A0
qm_hwdbg_wptr_data_hi              [0x000000C8] = 0x00000AA0
qm_hwdbg_rptr_data_lo              [0x000000CC] = 0x00014F60
qm_hwdbg_rptr_data_mi              [0x000000D0] = 0x000033A0
qm_hwdbg_rptr_data_hi              [0x000000D4] = 0x00000AA0
qm_hwdbg_qulen_data_lo             [0x000000D8] = 0x00000000
qm_hwdbg_qulen_data_mi             [0x000000DC] = 0x000000E7
qm_hwdbg_qulen_data_hi             [0x000000E0] = 0x00000000
qm_hwdbg_contex_data               [0x000000E4] = 0x00000000
qm_cfg_dir_stat_addr               [0x000000E8] = 0x0000004E
qm_cnt_dir_pkt_stat                [0x000000EC] = 0x00000000
qm_cnt_dir_byte_stat               [0x000000F0] = 0x00000000
qm_cfg_qam_stat_addr               [0x000000F4] = 0x0000004C
qm_cnt_qam_chnl_pkt_stat           [0x000000F8] = 0x00000000
qm_cnt_qam_chnl_byte_stat          [0x000000FC] = 0x00000000
qm_cnt_qam_chnl_sync_stat          [0x00000100] = 0x00000000
qm_cnt_bpram_ovrflw_stat           [0x00000108] = 0x00000000
qm_cnt_que_ovrflw_stat             [0x0000010C] = 0x00000000
qm_cnt_good_bpi_pkt_stat           [0x00000110] = 0x00045B3C
qm_cnt_bad_bpi_pkt_stat            [0x00000114] = 0x0000000D
qm_cnt_bpram_out_good_pkt_stat     [0x0000011C] = 0x000BD95D
qm_cnt_bpram_out_dir_pkt_stat      [0x00000120] = 0x00028918
qm_cnt_bpram_out_bonded_pkt_stat   [0x00000124] = 0x00000029
qm_cnt_replicated_pkt_stat         [0x00000128] = 0x000A0738
qm_cnt_bpram_bad_type_pkt_stat     [0x00000134] = 0x00000000
qm_cnt_bpram_bad_eop_pkt_stat      [0x00000138] = 0x00000000
qm_cnt_bpram_bad_dir_pkt_stat      [0x0000013C] = 0x00000000
qm_cnt_bpram_bad_bonded_pkt_stat   [0x00000140] = 0x00000000
qm_cnt_bpram_oecc_err_pkt_stat     [0x00000144] = 0x00000000
qm_cnt_bpram_bad_pkt_stat          [0x00000148] = 0x0000000D
qm_cnt_wr_good_pkt_stat            [0x0000014C] = 0x000BD95D
qm_cnt_wr_bad_pkt_stat             [0x00000150] = 0x00000000
qm_cnt_drop_bad_pkt_stat           [0x00000154] = 0x0000000D
qm_cnt_drop_ovrflw_pkt_stat        [0x00000158] = 0x00000000
qm_cnt_rd_pkt_stat                 [0x0000015C] = 0x000BD933
qm_cnt_rd_mpeg_stat                [0x00000160] = 0x000A6226
qm_cnt_rd_mpeg_sync_stat           [0x00000164] = 0x00008140
qm_cnt_rd_mpeg_only_sync_stat      [0x00000168] = 0x00007E93
qm_cnt_tran_pkt_stat               [0x00000170] = 0x000BD95E
qm_cnt_tran_oecc_err_pkt_stat      [0x00000174] = 0x00000000
qm_cnt_tran_mpeg_stat              [0x00000178] = 0x000A6226
qm_cnt_tran_mpeg_sync_stat         [0x0000017C] = 0x00008140
qm_cnt_tran_mpeg_only_sync_stat    [0x00000180] = 0x00007E93
qm_cnt_tran_dpv_stat               [0x00000188] = 0x00000000
qm_rldram_ext_ecc                  [0x00000198] = 0x00000000
qm_rldram_cfg                      [0x0000019C] = 0x00101544
qm_rldram_ctrl                     [0x000001A0] = 0x00100389
qm_rldram_status                   [0x000001A4] = 0x03DF7C03
qm_rldram_cal_match_win_h          [0x000001A8] = 0x00000000
qm_rldram_cal_match_win_l          [0x000001AC] = 0x7FFFFFFF


JIB3_DS PG registers (base address 0xF8898000)
```

```
pg_mod                                  [0x00000050] = 0x00000000
pg_dhs                                  [0x00000054] = 0x00000000
pg_ipg                                  [0x0000005C] = 0x00000000
pg_num                                  [0x00000058] = 0x00000000
pg_payload_length                       [0x00000060] = 0x00000000
pg_payload_value                        [0x00000064] = 0x00000000
pg_pkt_hdr_prog_0                       [0x00000068] = 0x00000000
pg_pkt_hdr_prog_1                       [0x0000006C] = 0x00000000
pg_pkt_hdr_1                            [0x00000070] = 0x00000000
pg_pkt_hdr_2                            [0x00000074] = 0x00000000
pg_pkt_hdr_3                            [0x00000078] = 0x00000000
pg_pkt_hdr_4                            [0x0000007C] = 0x00000000
pg_pkt_hdr_5                            [0x00000080] = 0x00000000
pg_pkt_hdr_6                            [0x00000084] = 0x00000000

JIB3_DS PMBIST registers (base address 0xF8899000)

pmbist_ena_addr                         [0x00000060] = 0x00000002
pmbist_din_addr                         [0x00000064] = 0x00000000
pmbist_dout_addr                        [0x0000006C] = 0x00008101
pmbist_trgt_select_addr                 [0x00000074] = 0x00000000
pmbist_ff_status                        [0x00000078] = 0x00000000
pmbist_num_wr_fr_pmbist                 [0x0000007C] = 0x00000000
pmbist_num_rd_fr_pmbist                 [0x00000080] = 0x00000000
pmbist_um_wr_2cmd_ff                    [0x00000084] = 0x00000000
pmbist_num_rd_2cmd_ff                   [0x00000088] = 0x00000000
pmbist_num_rd_rtn_pmbist                [0x0000008C] = 0x00000000
pmbist_num_wr_2dram                     [0x00000090] = 0x00000000
pmbist_num_rd_2dram                     [0x00000094] = 0x00000000
pmbist_num_rd_fr_dram                   [0x00000098] = 0x00000000

Remora registers (base address 0xF8900000)
------------------------------------------


Remora General Registers (0xF8900000):
--------------------------------------
revision                                [0x00000000] = 0x00000003
hw_fpga_rev_id                          [0x00000004] = 0x0000000A
erp_scratch_pad0                        [0x00000008] = 0x00000000
erp_scratch_pad1                        [0x0000000C] = 0x00000000

Remora Reset and DCM Lock Registers (0xF8900100):
-------------------------------------------------
reset_ctrl                              [0x00000100] = 0x00000000
dcm_lock                                [0x00000104] = 0x0000000F

Remora Configuration Registers (0xF8900200):
--------------------------------------------
port_cfg[0]                             [0x00000200] = 0x00155549
port_cfg[1]                             [0x00000204] = 0x00155548
port_cfg[2]                             [0x00000208] = 0x00155548
port_cfg[3]                             [0x0000020C] = 0x00155548
port_cfg[4]                             [0x00000210] = 0x00155548
core_config_status                      [0x00000214] = 0x00000020
port_rm2tififo_prog_flags[0]            [0x00000218] = 0xBBA20C0D
port_rm2tififo_prog_flags[1]            [0x0000021C] = 0xBBA20C0D
port_rm2tififo_prog_flags[2]            [0x00000220] = 0xBBA20C0D
port_rm2tififo_prog_flags[3]            [0x00000224] = 0xBBA20C0D
port_rm2tififo_prog_flags[4]            [0x00000228] = 0xBBA20C0D

Remora DFT/Pattern Inject Registers (0xF8900300):
-------------------------------------------------
alt_sym_tst_mode                        [0x00000300] = 0x00005A69
```

```
alt_sym_tst_en_reg                  [0x00000304] = 0x00000000
qdr_mem_test_en_reg                 [0x00000308] = 0x00000000
qdr_mem_test_rd_wr_reg              [0x0000030C] = 0x00000A12
ready_for_data_input                [0x00000318] = 0x0000001F

Remora ECC Registers (0xF8900400):
----------------------------------
debug_cfg                           [0x00000400] = 0x00000000
sniff_frame_cnt                     [0x00000404] = 0x00000000
ecc_parity_conf_reg                 [0x00000408] = 0x00000003
ecc_uncorrect_data_log_reg          [0x0000040C] = 0x00002814
ecc_uncorrect_log_reg               [0x00000410] = 0x00000020
ecc_correctable_data_log_reg        [0x00000414] = 0x00002C14
ecc_correctable_log_reg             [0x00000418] = 0x00000028
qdr_ecc_corr_cnt_reg                [0x0000041C] = 0x00000000
fatal_err_log                       [0x00000420] = 0x00000000
err_inj_reg                         [0x00000424] = 0x00000000

Remora QDR Registers (0xF8900500):
----------------------------------
qdr_phy_idelayctrl_rst_reg          [0x00000500] = 0x00000000
qdr_phy_idelayctrl_rdy_err_reg      [0x00000504] = 0x00000261
qdr_phy_cal_tap_dly_reg             [0x00000508] = 0x00000ADB
qdr_phy_idelayctrl_ctrl_reg         [0x0000050C] = 0x00000002
qdr_init_ctrl_reg                   [0x00000510] = 0x801FFFFF

Remora Interrupt Status Registers (0xF8900600):
-----------------------------------------------
glb_int_stat_reg                    [0x00000600] = 0x00000000
int_stat_gr_reg[0]                  [0x00000604] = 0x00000000
int_stat_gr_reg[1]                  [0x00000608] = 0x00000000
int_stat_gr_reg[2]                  [0x0000060C] = 0x00000000
int_stat_gr_reg[3]                  [0x00000610] = 0x00000000
int_stat_gr_reg[4]                  [0x00000614] = 0x00000000
misc_int_stat_reg                   [0x00000618] = 0x00000001
fatal_err_src_reg                   [0x0000061C] = 0x00000000
port_local_interrupt_enable[0]      [0x00000620] = 0x0001FFFF
port_local_interrupt_enable[1]      [0x00000624] = 0x0001FFFF
port_local_interrupt_enable[2]      [0x00000628] = 0x0001FFFF
port_local_interrupt_enable[3]      [0x0000062C] = 0x0001FFFF
port_local_interrupt_enable[4]      [0x00000630] = 0x0001FFFF
misc_int_en_reg                     [0x00000634] = 0x00001FF8
fatal_err_en_reg                    [0x00000638] = 0x00000EFF
port_local_interrupt_override[0]    [0x0000063C] = 0x00000000
port_local_interrupt_override[1]    [0x00000640] = 0x00000000
port_local_interrupt_override[2]    [0x00000644] = 0x00000000
port_local_interrupt_override[3]    [0x00000648] = 0x00000000
port_local_interrupt_override[4]    [0x0000064C] = 0x00000000
misc_int_override                   [0x00000650] = 0x00000000
fatal_err_override                  [0x00000654] = 0x00000000

Remora Counts Registers (0xF8900800):
-------------------------------------
illegal_ch_num_pkt_drop_count       [0x00000800] = 0x00000000
fifo_full_mpeg_pkt_drop_count_hi    [0x00000804] = 0x00000000
fifo_full_mpeg_pkt_drop_count_lo    [0x00000808] = 0x00000000
channel_mpeg_pkt_count[0]           [0x0000080C] = 0x00001118
channel_mpeg_pkt_count[1]           [0x00000810] = 0x0000106B
channel_mpeg_pkt_count[2]           [0x00000814] = 0x00000913
channel_mpeg_pkt_count[3]           [0x00000818] = 0x00000A6D
channel_mpeg_pkt_count[4]           [0x0000081C] = 0x00000000
channel_mpeg_pkt_count[5]           [0x00000820] = 0x00000000
channel_mpeg_pkt_count[6]           [0x00000824] = 0x00000000
channel_mpeg_pkt_count[7]           [0x00000828] = 0x00000000
```

```
channel_mpeg_pkt_count[8]           [0x0000082C] = 0x00000000
channel_mpeg_pkt_count[9]           [0x00000830] = 0x00000000
channel_mpeg_pkt_count[10]          [0x00000834] = 0x00000000
channel_mpeg_pkt_count[11]          [0x00000838] = 0x00000000
channel_mpeg_pkt_count[12]          [0x0000083C] = 0x00000000
channel_mpeg_pkt_count[13]          [0x00000840] = 0x00000000
channel_mpeg_pkt_count[14]          [0x00000844] = 0x00000000
channel_mpeg_pkt_count[15]          [0x00000848] = 0x00000000
channel_mpeg_pkt_count[16]          [0x0000084C] = 0x00000000
channel_mpeg_pkt_count[17]          [0x00000850] = 0x00000000
channel_mpeg_pkt_count[18]          [0x00000854] = 0x00000000
channel_mpeg_pkt_count[19]          [0x00000858] = 0x00000000
port_re_timestamp_count[0]          [0x0000085C] = 0xA6A5A6A6
port_re_timestamp_count[1]          [0x00000860] = 0x00000000
port_re_timestamp_count[2]          [0x00000864] = 0x00000000
port_re_timestamp_count[3]          [0x00000868] = 0x00000000
port_re_timestamp_count[4]          [0x0000086C] = 0x00000000
port_rx_fifo_overflow_drop_count[0] [0x00000870] = 0x00000000
port_rx_fifo_overflow_drop_count[1] [0x00000874] = 0x00000000
port_rx_fifo_overflow_drop_count[2] [0x00000878] = 0x00000000
port_rx_fifo_overflow_drop_count[3] [0x0000087C] = 0x00000000
port_rx_fifo_overflow_drop_count[4] [0x00000880] = 0x00000000
channel_jib_if_pkt_count[0]         [0x00000884] = 0x00038EA2
channel_jib_if_pkt_count[1]         [0x00000888] = 0x00031ADE
channel_jib_if_pkt_count[2]         [0x0000088C] = 0x0001B869
channel_jib_if_pkt_count[3]         [0x00000890] = 0x00020053
channel_jib_if_pkt_count[4]         [0x00000894] = 0x00000000
channel_jib_if_pkt_count[5]         [0x00000898] = 0x00000000
channel_jib_if_pkt_count[6]         [0x0000089C] = 0x00000000
channel_jib_if_pkt_count[7]         [0x000008A0] = 0x00000000
channel_jib_if_pkt_count[8]         [0x000008A4] = 0x00000000
channel_jib_if_pkt_count[9]         [0x000008A8] = 0x00000000
channel_jib_if_pkt_count[10]        [0x000008AC] = 0x00000000
channel_jib_if_pkt_count[11]        [0x000008B0] = 0x00000000
channel_jib_if_pkt_count[12]        [0x000008B4] = 0x00000000
channel_jib_if_pkt_count[13]        [0x000008B8] = 0x00000000
channel_jib_if_pkt_count[14]        [0x000008BC] = 0x00000000
channel_jib_if_pkt_count[15]        [0x000008C0] = 0x00000000
channel_jib_if_pkt_count[16]        [0x000008C4] = 0x00000000
channel_jib_if_pkt_count[17]        [0x000008C8] = 0x00000000
channel_jib_if_pkt_count[18]        [0x000008CC] = 0x00000000
channel_jib_if_pkt_count[19]        [0x000008D0] = 0x00000000

Remora Timestamp Registers (0xF8900900):
----------------------------------------
local_1024_ts_ctrl                  [0x00000900] = 0x00000039
local_1024_current_ts               [0x00000904] = 0xF5D27575
local_1024_tcc_ts_latch             [0x00000908] = 0x7291125F
doc_ts_offset_ch_0_1                [0x0000090C] = 0x04AF04AF
doc_ts_offset_ch_2_3                [0x00000910] = 0x04AF04AF
doc_ts_offset_ch_4_5                [0x00000914] = 0x04F704F7
doc_ts_offset_ch_6_7                [0x00000918] = 0x04F704F7
doc_ts_offset_ch_8_9                [0x0000091C] = 0x04F704F7
doc_ts_offset_ch_10_11              [0x00000920] = 0x04F704F7
doc_ts_offset_ch_12_13              [0x00000924] = 0x04F704F7
doc_ts_offset_ch_14_15              [0x00000928] = 0x04F704F7
doc_ts_offset_ch_16_17              [0x0000092C] = 0x04F704F7
doc_ts_offset_ch_18_19              [0x00000930] = 0x04F704F7

Remora PRATE/SRATE Registers (0xF8900A00):
------------------------------------------
port_prate_regs[0].prate_ctrl       [0x00000A00] = 0x00000003
port_prate_regs[0].prate_m_prime_lo [0x00000A04] = 0x0005971E
port_prate_regs[0].prate_n_prime_lo [0x00000A08] = 0x08AA5B88
```

```
port_prate_regs[0].prate_m_prime_hi [0x00000A0C] = 0x00000000
port_prate_regs[1].prate_ctrl       [0x00000A10] = 0x00000003
port_prate_regs[1].prate_m_prime_lo [0x00000A14] = 0x00000191
port_prate_regs[1].prate_n_prime_lo [0x00000A18] = 0x00037E78
port_prate_regs[1].prate_m_prime_hi [0x00000A1C] = 0x00000000
port_prate_regs[2].prate_ctrl       [0x00000A20] = 0x00000003
port_prate_regs[2].prate_m_prime_lo [0x00000A24] = 0x00000191
port_prate_regs[2].prate_n_prime_lo [0x00000A28] = 0x00037E78
port_prate_regs[2].prate_m_prime_hi [0x00000A2C] = 0x00000000
port_prate_regs[3].prate_ctrl       [0x00000A30] = 0x00000003
port_prate_regs[3].prate_m_prime_lo [0x00000A34] = 0x00000191
port_prate_regs[3].prate_n_prime_lo [0x00000A38] = 0x00037E78
port_prate_regs[3].prate_m_prime_hi [0x00000A3C] = 0x00000000
port_prate_regs[4].prate_ctrl       [0x00000A40] = 0x00000003
port_prate_regs[4].prate_m_prime_lo [0x00000A44] = 0x00000191
port_prate_regs[4].prate_n_prime_lo [0x00000A48] = 0x00037E78
port_prate_regs[4].prate_m_prime_hi [0x00000A4C] = 0x00000000
port_srate_regs[0].srate_ctrl       [0x00000A50] = 0x00000003
port_srate_regs[0].srate_mn         [0x00000A54] = 0x004E0095
port_srate_regs[1].srate_ctrl       [0x00000A58] = 0x00000003
port_srate_regs[1].srate_mn         [0x00000A5C] = 0x0191032C
port_srate_regs[2].srate_ctrl       [0x00000A60] = 0x00000003
port_srate_regs[2].srate_mn         [0x00000A64] = 0x0191032C
port_srate_regs[3].srate_ctrl       [0x00000A68] = 0x00000003
port_srate_regs[3].srate_mn         [0x00000A6C] = 0x0191032C
port_srate_regs[4].srate_ctrl       [0x00000A70] = 0x00000003
port_srate_regs[4].srate_mn         [0x00000A74] = 0x0191032C

Router# show controllers integrated-Cable 6/0/0 status

Load for five secs: 9%/0%; one minute: 11%; five minutes: 13%
Time source is NTP, *15:07:31.309 EDT Sun Mar 21 2010

Jib3-DS Status:
---------------
   Rx SPI..............: OK
   Tx SPI..............: OK
   DCM Status..........: OK
   ERP Status..........: OK
   DOCSIS RLDRAM Status: OK
   QM RLDRAM Status....: OK


  DS PHY Device Information:
  -------------------
    Remora Version = 3.10
    UPX SW Version = 0x10D
    Upconverter Type:Unknown
    UPX Part Number =

  Device Status:
  --------------
    UPX Alarm Status = 0x3FF
    UPX Alarm Mask   = 0x19000
```

Viewing Information about the Interface Controllers

To view information about the interface controllers, use the following commands in privileged EXEC mode.

show controller integrated-cable *slot/subslot/port*

show interfaces integrated-cable *slot/subslot/port*

For complete descriptions of the above configuration commands, refer to the *Cisco Broadband Cable Command Reference Guide* on Cisco.com.

Examples

The following example shows a typical display for the **show controllers integrated-cable** command.

```
Router# show controllers integrated-Cable 6/0/0 all

Integrated Cable Controller 6/0/0:
----------------------------------
  Channel 1  Annex = B  Modulation = 256 QAM
  Channel 2  Annex = B  Modulation = 256 QAM
  Channel 3  Annex = B  Modulation = 256 QAM
  Channel 4  Annex = B  Modulation = 256 QAM

JIB3_DS BPI registers (base address 0xF8880000)

bpi_int_isr_0                       [0x00000000] = 0x00000000
bpi_int_ier_0                       [0x00000004] = 0x0000000F
glb_int_isr_0                       [0x00000010] = 0x00000000
glb_int_ier_0                       [0x00000014] = 0x000003FF
glb_int_isr_1                       [0x00000020] = 0x00000000
glb_int_ier_1                       [0x00000024] = 0x000003FF
bpi_int_fesr_0                      [0x00000040] = 0x00000000
bpi_tst_tp_sel_reg                  [0x00000050] = 0x00000000
bpi_tst_tp_reg                      [0x00000054] = 0x00000000
bpi_cnt_good_packet_in_cnt          [0x00000064] = 0x61308806
bpi_cnt_bad_packet_in_cnt           [0x00000068] = 0x00006538
bpi_cnt_good_packet_out_cnt         [0x0000006C] = 0x61308806
bpi_cnt_bad_packet_out_cnt          [0x00000070] = 0x00006538
bpi_ecc_sbit_err_cnt                [0x00000074] = 0x00000000
glb_sw_rev_id                       [0x00000078] = 0x00020002
glb_hw_rev_id                       [0x0000007C] = 0x00010008
frz_reg                             [0x00000080] = 0x00000000
frz_en                              [0x00000084] = 0x00000001
glb_dcm_status                      [0x00000088] = 0x00000007
glb_sw_rst                          [0x0000008C] = 0x00000000

JIB3_DS ERP registers (base address 0xF8881000)

erp_irq_src_reg                     [0x00000000] = 0x00000000
erp_irq_en_reg                      [0x00000004] = 0x80000FFF
erp_tp_sel_reg                      [0x00000050] = 0x00000000
erp_tp_reg                          [0x00000054] = 0x00000000
erp_cfg_reg                         [0x00000060] = 0x00000000
erp_err_record_reg                  [0x00000064] = 0x00000000
erp_err_addr_record_reg             [0x00000068] = 0x00000000
erp_err_wd_record_reg               [0x0000006C] = 0x00000000
erp_proc_err_addr_record_reg        [0x00000090] = 0x00000000

JIB3_DS RX SPI registers (base address 0xF8882000)

rxspi_irq_src_reg                   [0x00000000] = 0x00000000
```

```
rxspi_irq_en_reg                    [0x00000004] = 0x000001FF
rxspi_ferr_src_reg                  [0x00000040] = 0x00000000
rxspi_testpoint_sel_reg             [0x00000050] = 0x00000000
rxspi_testpoint_reg                 [0x00000054] = 0x00000000
rxspi_rst_cntl_reg                  [0x00000060] = 0x00000000
rxspi_cntl_status_reg               [0x00000064] = 0x00000005
rxspi_cfg_cntl_reg                  [0x00000068] = 0x00000021
rxspi_afthres_reg                   [0x0000006C] = 0x01C00180
rxspi_cal_dur_reg                   [0x00000070] = 0x00030000
rxspi_non_drop_err_cnt_reg          [0x00000088] = 0x00000000
rxspi_drop_byte_cnt_reg             [0x0000008C] = 0x00000000
rxspi_rx_byte_cnt_reg[0]            [0x000000B0] = 0xFFFFFFFF
rxspi_rx_byte_cnt_reg[1]            [0x000000B4] = 0xFFFFFFFF
rxspi_rx_byte_cnt_reg[2]            [0x000000B8] = 0x14B49467
rxspi_rx_pkt_cnt_reg[0]             [0x000000C0] = 0x3FF2F36C
rxspi_rx_pkt_cnt_reg[1]             [0x000000C4] = 0x20F3AFA9
rxspi_rx_pkt_cnt_reg[2]             [0x000000C8] = 0x004A4A35
rxspi_fifo_pkt_drop_cnt_reg[0]      [0x000000E0] = 0x00000000
rxspi_fifo_pkt_drop_cnt_reg[1]      [0x000000E4] = 0x00000000
rxspi_fifo_pkt_drop_cnt_reg[2]      [0x000000E8] = 0x00000000
rxspi_calendar_table_reg[0]         [0x00000800] = 0x00000000
rxspi_calendar_table_reg[1]         [0x00000804] = 0x00000001
rxspi_calendar_table_reg[2]         [0x00000808] = 0x00000002
rxspi_calendar_table_reg[3]         [0x0000080C] = 0x00000003

JIB3_DS TX SPI registers (base address 0xF8883000)

txspi_irq_src_reg                   [0x00000000] = 0x00000000
txspi_irq_en_reg                    [0x00000004] = 0x0000001F
txspi_ferr_src_reg                  [0x00000040] = 0x00000000
txspi_testpoint_sel_reg             [0x00000050] = 0x00000000
txspi_testpoint_reg                 [0x00000054] = 0x00000000
txspi_rst_cntl_reg                  [0x00000060] = 0x00000000
txspi_cntl_status_reg               [0x00000064] = 0x00000009
txspi_cfg_cntl_reg                  [0x00000068] = 0x00000001
txspi_afthres_reg                   [0x0000006C] = 0x01EC01E8
txspi_cal_dur_reg                   [0x00000070] = 0x00040000
txspi_train_cntl_reg                [0x00000074] = 0x00000000
txspi_nonfatalerr_cnt_reg           [0x00000080] = 0x00000000
txspi_eop_abort_pkt_cnt_reg[0]      [0x00000090] = 0x00000000
txspi_eop_abort_pkt_cnt_reg[1]      [0x00000094] = 0x00000000
txspi_eop_abort_pkt_cnt_reg[2]      [0x00000098] = 0x00000000
txspi_eop_abort_pkt_cnt_reg[3]      [0x0000009C] = 0x00000000
txspi_eop_abort_byte_cnt_reg[0]     [0x000000A0] = 0x00000000
txspi_eop_abort_byte_cnt_reg[1]     [0x000000A4] = 0x00000000
txspi_eop_abort_byte_cnt_reg[2]     [0x000000A8] = 0x00000000
txspi_eop_abort_byte_cnt_reg[3]     [0x000000AC] = 0x00000000
txspi_tx_byte_cnt_reg[0]            [0x000000C0] = 0x00000000
txspi_tx_byte_cnt_reg[1]            [0x000000C4] = 0x00000000
txspi_tx_byte_cnt_reg[2]            [0x000000C8] = 0x00000000
txspi_tx_byte_cnt_reg[3]            [0x000000CC] = 0x00000000
txspi_tx_pkt_cnt_reg[0]             [0x00000100] = 0x00000000
txspi_tx_pkt_cnt_reg[1]             [0x00000104] = 0x00000000
txspi_tx_pkt_cnt_reg[2]             [0x00000108] = 0x00000000
txspi_tx_pkt_cnt_reg[3]             [0x0000010C] = 0x00000000
txspi_calendar_table_reg[0]         [0x00000800] = 0x00000000
txspi_calendar_table_reg[1]         [0x00000804] = 0x00000001
txspi_calendar_table_reg[2]         [0x00000808] = 0x00000002
txspi_calendar_table_reg[3]         [0x0000080C] = 0x00000003
txspi_calendar_table_reg[4]         [0x00000810] = 0x00000004

JIB3_DS DOC registers (base address 0xF8884000)

doc_int_err0                        [0x00000000] = 0x00000000
```

```
doc_int_err0_ier                    [0x00000004] = 0xFFBFBFFD
doc_int_err1                        [0x00000010] = 0x00000000
doc_int_err1_ier                    [0x00000014] = 0x003FFFF8
doc_int_fesr                        [0x00000040] = 0x00000000
doc_test_sel                        [0x00000050] = 0x00000000
doc_testpoint                       [0x00000054] = 0x00000000
doc_cfg_ctrl                        [0x00000060] = 0x031A0000
doc_err_cap_ctrl                    [0x00000064] = 0x001F0001
doc_err_cap_addr                    [0x00000068] = 0x00000000
doc_err_cap_data                    [0x0000006C] = 0x000080F7
doc_seg_num                         [0x00000070] = 0x00000001
doc_wb_chan_stats_sel               [0x00000074] = 0x00000077
doc_wb_pkt_cnt                      [0x00000078] = 0x00000000
doc_wb_byte_cnt                     [0x0000007C] = 0x00000000
doc_wb_police_sel                   [0x00000080] = 0x00000000
doc_wb_police_data                  [0x00000084] = 0x00000000
doc_wb_police_intv                  [0x00000088] = 0x00000000
doc_nb_chan_stats_sel               [0x0000008C] = 0x0000004C
doc_nb_pkt_cnt                      [0x00000090] = 0x00000000
doc_nb_byte_cnt                     [0x00000094] = 0x00000000
doc_nb_police_sel                   [0x00000098] = 0x00000000
doc_nb_police_data                  [0x0000009C] = 0x00000000
doc_nb_police_intv                  [0x000000A0] = 0x00000000
doc_int_doc_cnt                     [0x000000D4] = 0x00000000
doc_int_ecc_sbiterr_cnt             [0x000000D8] = 0x00000000
doc_pkt_good_in_cnt                 [0x000000DC] = 0x6130ED6F
doc_pkt_good_out_cnt                [0x000000E0] = 0x61308837
doc_pkt_err_in_cnt                  [0x000000E4] = 0x00000000
doc_pkt_err_out_cnt                 [0x000000E8] = 0x00006538
doc_pkt_drop_cnt                    [0x000000EC] = 0x00000000
doc_efc_all_cnt                     [0x000000F0] = 0x00000000
doc_efc_hi_cnt                      [0x000000F4] = 0x00000000
doc_efc_me_cnt                      [0x000000F8] = 0x00000000
doc_efc_lo_cnt                      [0x000000FC] = 0x00000000
doc_efc_ch_sel                      [0x00000100] = 0x00000000
doc_efc_debug_ctrl                  [0x00000104] = 0x00000000
doc_rldram_ext_ecc                  [0x00000114] = 0x00000000
doc_rldram_cfg                      [0x00000118] = 0x00101544
doc_rldram_ctrl                     [0x0000011C] = 0x00100389
doc_rldram_status                   [0x00000120] = 0x039D7403
doc_rldram_blk_clr                  [0x00000124] = 0x0B7FFFFF
doc_rldram_cal_match_win_h          [0x00000128] = 0x00000000
doc_rldram_cal_match_win_l          [0x0000012C] = 0x1FFFFFFF
doc_rldram_ecc_err_rec_addr         [0x00000130] = 0x00000000
doc_magic_num_err_pkt_ctrl          [0x00000150] = 0x00000000
doc_magic_num_err_pkt_addr          [0x00000154] = 0x00000000
doc_magic_num_err_pkt_data          [0x00000158] = 0x00000000

JIB3_DS RIF registers (base address 0xF8885000)

rif_int_err0                        [0x00000000] = 0x00000000
rif_int_ier0                        [0x00000004] = 0x00000007
rif_int_fesr0                       [0x00000040] = 0x00000000
rif_tp_sel                          [0x00000050] = 0x00000000
rif_tp                              [0x00000054] = 0x00000000
rif_cfg_ctrl                        [0x00000060] = 0x00000000
rif_cnt_in_mpeg_cnt                 [0x00000064] = 0xFFFFFFFF
rif_cnt_out_good_mpeg_cnt           [0x00000068] = 0xFFFFFFFF
rif_cnt_out_bad_mpeg_cnt            [0x0000006C] = 0x00000000
rif_cnt_drop_mpeg_cnt               [0x00000070] = 0x00000000
rif_1bit_ecc_err_stat               [0x00000074] = 0x00000000

JIB3_DS RTN registers (base address 0xF8886000)
```

```
return_int_isr                       [0x00000000] = 0x00000000
return_int_ier                       [0x00000004] = 0x000001FF
return_int_fesr                      [0x00000040] = 0x00000000
return_tp_sel                        [0x00000050] = 0x00000000
return_tp                            [0x00000054] = 0x00000000
return_ctrl_reg                      [0x00000060] = 0x00000000
return_pif_loopback_chnl             [0x00000064] = 0x00000000
return_sniffer_nonbonded_en          [0x00000068] = 0x00000000
return_sniffer_bonded_en             [0x0000006C] = 0x00000000
return_spi_chnl_sel                  [0x00000070] = 0x0000013A
return_err_drop_en                   [0x00000074] = 0x0000000F
return_snf_macda_cfg_addr            [0x00000078] = 0x00000000
return_snf_macda_cfg_data_hi         [0x0000007C] = 0x00000000
return_snf_macda_cfg_data_lo         [0x00000080] = 0x00000000
return_in_pifrx_good_cnt             [0x000000A0] = 0x00000000
return_in_pifrx_bad_cnt              [0x000000A4] = 0x00000000
return_in_piflp_good_cnt             [0x000000A8] = 0xFFFFFFFF
return_in_piflp_bad_cnt              [0x000000AC] = 0x00000000
return_in_sniffer_good_cnt           [0x000000B0] = 0x61308845
return_in_sniffer_bad_cnt            [0x000000B4] = 0x00006538
return_in_spi_loop_good_cnt          [0x000000B8] = 0x00000000
return_in_spi_loop_bad_cnt           [0x000000BC] = 0x00000000
return_out_spi0_cnt                  [0x000000C0] = 0x00000000
return_out_spi1_cnt                  [0x000000C4] = 0x00000000
return_out_spi2_cnt                  [0x000000C8] = 0x00000000
return_out_spi3_cnt                  [0x000000CC] = 0x00000000
return_out_spi4_cnt                  [0x000000D0] = 0x00000000
return_pifrx_if_par_err_drop_cnt     [0x000000D4] = 0x00000000
return_pifrx_if_len_err_drop_cnt     [0x000000D8] = 0x00000000
return_piflp_if_err_drop_cnt         [0x000000DC] = 0x00000000
return_piflp_if_chnl_drop_cnt        [0x000000E0] = 0x00000000
return_snf_pb_err_drop_cnt           [0x000000E4] = 0x00006538
return_snf_pkt_type_err_drop_cnt     [0x000000E8] = 0x61308845
return_spilp_if_err_drop_cnt         [0x000000EC] = 0x00000000
return_pifrx_traffic_mux_drop_cnt    [0x000000F0] = 0x00000000
return_piflp_traffic_mux_drop_cnt    [0x000000F4] = 0x00000000
return_snf_traffic_mux_drop_cnt      [0x000000F8] = 0x00000000
return_spilp_traffic_mux_drop_cnt    [0x000000FC] = 0x00000000
return_pifrx_fifo_overflow_drop_cnt  [0x00000100] = 0x00000000
return_piflp_fifo_overflow_drop_cnt  [0x00000104] = 0x00000000
return_snf_fifo_overflow_drop_cnt    [0x00000108] = 0x00000000
return_spilp_fifo_overflow_drop_cnt  [0x0000010C] = 0x00000000
return_pifrx_if_par_err_cnt          [0x00000110] = 0x00000000
return_pifrx_if_len_err_cnt          [0x00000114] = 0x00000000
return_pifrx_fifo_ecc_1berr_cnt      [0x00000118] = 0x00000000
return_piflp_fifo_ecc_1berr_cnt      [0x0000011C] = 0x00000000
return_snf_fifo_ecc_1berr_cnt        [0x00000120] = 0x00000000
return_spilp_fifo_ecc_1berr_cnt      [0x00000124] = 0x00000000

JIB3_DS DLM registers (base address 0xF8890000)

dlm_int_isr_0                        [0x00000000] = 0x00000005
dlm_int_ier_0                        [0x00000004] = 0x00000000
dlm_cnt_local_ts_reg                 [0x00000064] = 0x5B00EB07
dlm_cfg_tss_comp_reg                 [0x00000068] = 0x00000027
dlm_cfg_tss_ctrl_reg                 [0x0000006C] = 0x00000000
dlm_cfg_tss_cmd_reg                  [0x00000070] = 0x00000000
dlm_cnt_ts_load_cnt                  [0x000000BC] = 0x00000000
dlm_cnt_ts_chk_failed_cnt            [0x000000C4] = 0x00000000
dlm_cnt_tss_perr_cnt                 [0x000000C8] = 0x00000000
dlm_cnt_load_ts_reg                  [0x000000D0] = 0x003F52EF

JIB3_DS SEQ registers (base address 0xF8892000)
```

```
seq_int_err0                        [0x00000000] = 0x0000000F
seq_int_ier0                        [0x00000004] = 0x000FFFFF
seq_int_err3                        [0x00000030] = 0x00000000
seq_int_ier3                        [0x00000034] = 0x00000001
seq_int_fatal_err                   [0x00000040] = 0x00000000
seq_tp_sel                          [0x00000050] = 0x00000000
seq_tp                              [0x00000054] = 0x00000000
seq_cfg_en                          [0x00000060] = 0x00000001
seq_cfg_sync_timer_sel              [0x00000064] = 0x00000004
seq_cfg_sync_timer_data             [0x00000068] = 0x00000000
seq_cfg_sync_sa_sel                 [0x0000006C] = 0x00000004
seq_cfg_sync_sa_data_lo             [0x00000070] = 0x70CC0B91
seq_cfg_sync_sa_data_hi             [0x00000074] = 0x00000000
seq_cfg_tkb_timer_sel               [0x00000078] = 0x00000014
seq_cfg_tkb_timer_data              [0x0000007C] = 0x00000000
seq_cfg_tkb_max                     [0x00000080] = 0x00000000
seq_hwdbg_dpv_proc_table_addr       [0x00000090] = 0x00000000
seq_hwdbg_dpv_ptr_mod_table         [0x00000094] = 0x00000000
seq_hwdbg_dpv_timestamp_table       [0x00000098] = 0x00000000
seq_hwdbg_dpv_hcs_table             [0x0000009C] = 0x00000000
seq_cnt_blkram_oecc_err_stat        [0x000000A4] = 0x00000000
seq_cnt_tran_mpeg_stat              [0x000000A8] = 0xFFFFFFFF
seq_cnt_tran_mpeg_sync_stat         [0x000000AC] = 0x00000000
seq_cnt_tran_only_sync_stat         [0x000000B0] = 0x00000000
seq_cnt_tran_dpv_stat               [0x000000B8] = 0x00000000

JIB3_DS QM registers (base address 0xF8893000)

qm_int_isr0                         [0x00000000] = 0x00000000
qm_int_ier0                         [0x00000004] = 0x0000007F
qm_int_isr1                         [0x00000010] = 0x00000000
qm_int_ier1                         [0x00000014] = 0x000FFFFF
qm_int_fat_err_isr                  [0x00000040] = 0x00000000
qm_tst_tp_sel                       [0x00000050] = 0x00000000
qm_tst_tp                           [0x00000054] = 0x00000000
qm_cfg_chnl_rst_0                   [0x00000060] = 0x00000000
qm_cfg_ctl                          [0x0000006C] = 0x00000011
qm_cfg_sqf_fac_addr                 [0x0000008C] = 0x00000014
qm_cfg_sqf_fac_data                 [0x00000090] = 0x00000000
qm_cfg_bond_chnl_map_addr           [0x00000094] = 0x00000020
qm_cfg_bond_chnl_map_data_lo        [0x00000098] = 0x00000000
qm_cfg_flt_thr_addr                 [0x000000A4] = 0x0000024F
qm_cfg_flt_thr_data                 [0x000000A8] = 0x00000000
qm_cfg_repl_addr                    [0x000000AC] = 0x0000002D
qm_cfg_repl_data_lo                 [0x000000B0] = 0x00000000
qm_hwdbg_buf_mag_addr               [0x000000BC] = 0x00000000
qm_hwdbg_wptr_data_lo               [0x000000C0] = 0x00000C60
qm_hwdbg_wptr_data_mi               [0x000000C4] = 0x00016080
qm_hwdbg_wptr_data_hi               [0x000000C8] = 0x000012A0
qm_hwdbg_rptr_data_lo               [0x000000CC] = 0x00000C60
qm_hwdbg_rptr_data_mi               [0x000000D0] = 0x00016080
qm_hwdbg_rptr_data_hi               [0x000000D4] = 0x000012A0
qm_hwdbg_qulen_data_lo              [0x000000D8] = 0x00000000
qm_hwdbg_qulen_data_mi              [0x000000DC] = 0x00000000
qm_hwdbg_qulen_data_hi              [0x000000E0] = 0x00000000
qm_hwdbg_contex_data                [0x000000E4] = 0x00000000
qm_cfg_dir_stat_addr                [0x000000E8] = 0x0000004E
qm_cnt_dir_pkt_stat                 [0x000000EC] = 0x00000000
qm_cnt_dir_byte_stat                [0x000000F0] = 0x00000000
qm_cfg_qam_stat_addr                [0x000000F4] = 0x0000004C
qm_cnt_qam_chnl_pkt_stat            [0x000000F8] = 0x00000000
qm_cnt_qam_chnl_byte_stat           [0x000000FC] = 0x00000000
qm_cnt_qam_chnl_sync_stat           [0x00000100] = 0x00000000
qm_cnt_bpram_ovrflw_stat            [0x00000108] = 0x00000000
```

```
qm_cnt_que_ovrflw_stat              [0x0000010C] = 0x00000000
qm_cnt_good_bpi_pkt_stat            [0x00000110] = 0x6130886C
qm_cnt_bad_bpi_pkt_stat             [0x00000114] = 0x000000FF
qm_cnt_bpram_out_good_pkt_stat      [0x0000011C] = 0xC38C8639
qm_cnt_bpram_out_dir_pkt_stat       [0x00000120] = 0x213DFA0E
qm_cnt_bpram_out_bonded_pkt_stat    [0x00000124] = 0x3486CDA6
qm_cnt_replicated_pkt_stat          [0x00000128] = 0x8399F7DB
qm_cnt_bpram_bad_type_pkt_stat      [0x00000134] = 0x00000000
qm_cnt_bpram_bad_eop_pkt_stat       [0x00000138] = 0x00000000
qm_cnt_bpram_bad_dir_pkt_stat       [0x0000013C] = 0x00000000
qm_cnt_bpram_bad_bonded_pkt_stat    [0x00000140] = 0x00000000
qm_cnt_bpram_oecc_err_pkt_stat      [0x00000144] = 0x00000000
qm_cnt_bpram_bad_pkt_stat           [0x00000148] = 0x000000FF
qm_cnt_wr_good_pkt_stat             [0x0000014C] = 0xC38C863A
qm_cnt_wr_bad_pkt_stat              [0x00000150] = 0x00000000
qm_cnt_drop_bad_pkt_stat            [0x00000154] = 0x000000FF
qm_cnt_drop_ovrflw_pkt_stat         [0x00000158] = 0x00000000
qm_cnt_rd_pkt_stat                  [0x0000015C] = 0xC38C8664
qm_cnt_rd_mpeg_stat                 [0x00000160] = 0xFFFFFFFF
qm_cnt_rd_mpeg_sync_stat            [0x00000164] = 0x06A0FC65
qm_cnt_rd_mpeg_only_sync_stat       [0x00000168] = 0x0620376C
qm_cnt_tran_pkt_stat                [0x00000170] = 0xC38C8664
qm_cnt_tran_oecc_err_pkt_stat       [0x00000174] = 0x00000000
qm_cnt_tran_mpeg_stat               [0x00000178] = 0xFFFFFFFF
qm_cnt_tran_mpeg_sync_stat          [0x0000017C] = 0x06A0FC65
qm_cnt_tran_mpeg_only_sync_stat     [0x00000180] = 0x0620376C
qm_cnt_tran_dpv_stat                [0x00000188] = 0x00000000
qm_rldram_ext_ecc                   [0x00000198] = 0x00000000
qm_rldram_cfg                       [0x0000019C] = 0x00101544
qm_rldram_ctrl                      [0x000001A0] = 0x00100389
qm_rldram_status                    [0x000001A4] = 0x03DF7C03
qm_rldram_cal_match_win_h           [0x000001A8] = 0x00000000
qm_rldram_cal_match_win_l           [0x000001AC] = 0x7FFFFFFF

JIB3_DS PG registers (base address 0xF8898000)

pg_mod                              [0x00000050] = 0x00000000
pg_dhs                              [0x00000054] = 0x00000000
pg_ipg                              [0x0000005C] = 0x00000000
pg_num                              [0x00000058] = 0x00000000
pg_payload_length                   [0x00000060] = 0x00000000
pg_payload_value                    [0x00000064] = 0x00000000
pg_pkt_hdr_prog_0                   [0x00000068] = 0x00000000
pg_pkt_hdr_prog_1                   [0x0000006C] = 0x00000000
pg_pkt_hdr_1                        [0x00000070] = 0x00000000
pg_pkt_hdr_2                        [0x00000074] = 0x00000000
pg_pkt_hdr_3                        [0x00000078] = 0x00000000
pg_pkt_hdr_4                        [0x0000007C] = 0x00000000
pg_pkt_hdr_5                        [0x00000080] = 0x00000000
pg_pkt_hdr_6                        [0x00000084] = 0x00000000

JIB3_DS PMBIST registers (base address 0xF8899000)

pmbist_ena_addr                     [0x00000060] = 0x00000002
pmbist_din_addr                     [0x00000064] = 0x00000000
pmbist_dout_addr                    [0x0000006C] = 0x00008101
pmbist_trgt_select_addr             [0x00000074] = 0x00000000
pmbist_ff_status                    [0x00000078] = 0x00000000
pmbist_num_wr_fr_pmbist             [0x0000007C] = 0x00000000
pmbist_num_rd_fr_pmbist             [0x00000080] = 0x00000000
pmbist_um_wr_2cmd_ff                [0x00000084] = 0x00000000
pmbist_num_rd_2cmd_ff               [0x00000088] = 0x00000000
pmbist_num_rd_rtn_pmbist            [0x0000008C] = 0x00000000
pmbist_num_wr_2dram                 [0x00000090] = 0x00000000
```

```
pmbist_num_rd_2dram                 [0x00000094] = 0x00000000
pmbist_num_rd_fr_dram               [0x00000098] = 0x00000000

DS PHY Configuration of Controller 0:
---------------------
  Base Frequency = 555000000Hz
  RF-Power = 52.0dBmV
  Annex = B Modulation = 256QAM
  Channel Status Interleave
  ------- ------ ----------
     0   Active     32
     1   Active     32
     2   Active     32
     3   Active     32
  DS_PHY PLL set for Annex-B

  DS PHY Device Information:
  -------------------
    Remora Version = 3.10
    UPX SW Version = 0x10D
    Upconverter Type:Unknown
    UPX Part Number =

  Device Status:
  --------------
    UPX Alarm Status = 0x3FF
    UPX Alarm Mask   = 0x19000
Remora registers (base address 0xF8900000)
-----------------------------------------


Remora General Registers (0xF8900000):
--------------------------------------
revision                            [0x00000000] = 0x00000003
hw_fpga_rev_id                      [0x00000004] = 0x0000000A
erp_scratch_pad0                    [0x00000008] = 0x00000000
erp_scratch_pad1                    [0x0000000C] = 0x00000000

Remora Reset and DCM Lock Registers (0xF8900100):
-------------------------------------------------
reset_ctrl                          [0x00000100] = 0x00000000
dcm_lock                            [0x00000104] = 0x0000000F

Remora Configuration Registers (0xF8900200):
--------------------------------------------
port_cfg[0]                         [0x00000200] = 0x00155549
port_cfg[1]                         [0x00000204] = 0x00155548
port_cfg[2]                         [0x00000208] = 0x00155548
port_cfg[3]                         [0x0000020C] = 0x00155548
port_cfg[4]                         [0x00000210] = 0x00155548
core_config_status                  [0x00000214] = 0x00000020
port_rm2tififo_prog_flags[0]        [0x00000218] = 0xBBA20C0D
port_rm2tififo_prog_flags[1]        [0x0000021C] = 0xBBA20C0D
port_rm2tififo_prog_flags[2]        [0x00000220] = 0xBBA20C0D
port_rm2tififo_prog_flags[3]        [0x00000224] = 0xBBA20C0D
port_rm2tififo_prog_flags[4]        [0x00000228] = 0xBBA20C0D

Remora DFT/Pattern Inject Registers (0xF8900300):
-------------------------------------------------
alt_sym_tst_mode                    [0x00000300] = 0x00005A69
alt_sym_tst_en_reg                  [0x00000304] = 0x00000000
qdr_mem_test_en_reg                 [0x00000308] = 0x00000000
qdr_mem_test_rd_wr_reg              [0x0000030C] = 0x00000A12
ready_for_data_input                [0x00000318] = 0x0000001F
```

```
Remora ECC Registers (0xF8900400):
----------------------------------
debug_cfg                           [0x00000400] = 0x00000000
sniff_frame_cnt                     [0x00000404] = 0x00000000
ecc_parity_conf_reg                 [0x00000408] = 0x00000003
ecc_uncorrect_data_log_reg          [0x0000040C] = 0x00002814
ecc_uncorrect_log_reg               [0x00000410] = 0x00000020
ecc_correctable_data_log_reg        [0x00000414] = 0x00002C14
ecc_correctable_log_reg             [0x00000418] = 0x00000028
qdr_ecc_corr_cnt_reg                [0x0000041C] = 0x00000000
fatal_err_log                       [0x00000420] = 0x00000000
err_inj_reg                         [0x00000424] = 0x00000000

Remora QDR Registers (0xF8900500):
----------------------------------
qdr_phy_idelayctrl_rst_reg          [0x00000500] = 0x00000000
qdr_phy_idelayctrl_rdy_err_reg      [0x00000504] = 0x00000261
qdr_phy_cal_tap_dly_reg             [0x00000508] = 0x00000ADB
qdr_phy_idelayctrl_ctrl_reg         [0x0000050C] = 0x00000002
qdr_init_ctrl_reg                   [0x00000510] = 0x801FFFFF

Remora Interrupt Status Registers (0xF8900600):
-----------------------------------------------
glb_int_stat_reg                    [0x00000600] = 0x00000000
int_stat_gr_reg[0]                  [0x00000604] = 0x00000000
int_stat_gr_reg[1]                  [0x00000608] = 0x00000000
int_stat_gr_reg[2]                  [0x0000060C] = 0x00000000
int_stat_gr_reg[3]                  [0x00000610] = 0x00000000
int_stat_gr_reg[4]                  [0x00000614] = 0x00000000
misc_int_stat_reg                   [0x00000618] = 0x00000001
fatal_err_src_reg                   [0x0000061C] = 0x00000000
port_local_interrupt_enable[0]      [0x00000620] = 0x0001FFFF
port_local_interrupt_enable[1]      [0x00000624] = 0x0001FFFF
port_local_interrupt_enable[2]      [0x00000628] = 0x0001FFFF
port_local_interrupt_enable[3]      [0x0000062C] = 0x0001FFFF
port_local_interrupt_enable[4]      [0x00000630] = 0x0001FFFF
misc_int_en_reg                     [0x00000634] = 0x00001FF8
fatal_err_en_reg                    [0x00000638] = 0x00000EFF
port_local_interrupt_override[0]    [0x0000063C] = 0x00000000
port_local_interrupt_override[1]    [0x00000640] = 0x00000000
port_local_interrupt_override[2]    [0x00000644] = 0x00000000
port_local_interrupt_override[3]    [0x00000648] = 0x00000000
port_local_interrupt_override[4]    [0x0000064C] = 0x00000000
misc_int_override                   [0x00000650] = 0x00000000
fatal_err_override                  [0x00000654] = 0x00000000

Remora Counts Registers (0xF8900800):
-------------------------------------
illegal_ch_num_pkt_drop_count       [0x00000800] = 0x00000000
fifo_full_mpeg_pkt_drop_count_hi    [0x00000804] = 0x00000000
fifo_full_mpeg_pkt_drop_count_lo    [0x00000808] = 0x00000000
channel_mpeg_pkt_count[0]           [0x0000080C] = 0x00000EE7
channel_mpeg_pkt_count[1]           [0x00000810] = 0x00000E8C
channel_mpeg_pkt_count[2]           [0x00000814] = 0x00000839
channel_mpeg_pkt_count[3]           [0x00000818] = 0x000009DF
channel_mpeg_pkt_count[4]           [0x0000081C] = 0x00000000
channel_mpeg_pkt_count[5]           [0x00000820] = 0x00000000
channel_mpeg_pkt_count[6]           [0x00000824] = 0x00000000
channel_mpeg_pkt_count[7]           [0x00000828] = 0x00000000
channel_mpeg_pkt_count[8]           [0x0000082C] = 0x00000000
channel_mpeg_pkt_count[9]           [0x00000830] = 0x00000000
channel_mpeg_pkt_count[10]          [0x00000834] = 0x00000000
channel_mpeg_pkt_count[11]          [0x00000838] = 0x00000000
```

```
channel_mpeg_pkt_count[12]          [0x0000083C] = 0x00000000
channel_mpeg_pkt_count[13]          [0x00000840] = 0x00000000
channel_mpeg_pkt_count[14]          [0x00000844] = 0x00000000
channel_mpeg_pkt_count[15]          [0x00000848] = 0x00000000
channel_mpeg_pkt_count[16]          [0x0000084C] = 0x00000000
channel_mpeg_pkt_count[17]          [0x00000850] = 0x00000000
channel_mpeg_pkt_count[18]          [0x00000854] = 0x00000000
channel_mpeg_pkt_count[19]          [0x00000858] = 0x00000000
port_re_timestamp_count[0]          [0x0000085C] = 0x97979796
port_re_timestamp_count[1]          [0x00000860] = 0x00000000
port_re_timestamp_count[2]          [0x00000864] = 0x00000000
port_re_timestamp_count[3]          [0x00000868] = 0x00000000
port_re_timestamp_count[4]          [0x0000086C] = 0x00000000
port_rx_fifo_overflow_drop_count[0] [0x00000870] = 0x00000000
port_rx_fifo_overflow_drop_count[1] [0x00000874] = 0x00000000
port_rx_fifo_overflow_drop_count[2] [0x00000878] = 0x00000000
port_rx_fifo_overflow_drop_count[3] [0x0000087C] = 0x00000000
port_rx_fifo_overflow_drop_count[4] [0x00000880] = 0x00000000
channel_jib_if_pkt_count[0]         [0x00000884] = 0x4AFC8612
channel_jib_if_pkt_count[1]         [0x00000888] = 0x44C96772
channel_jib_if_pkt_count[2]         [0x0000088C] = 0x42A048EA
channel_jib_if_pkt_count[3]         [0x00000890] = 0x43E61FF6
channel_jib_if_pkt_count[4]         [0x00000894] = 0x00000000
channel_jib_if_pkt_count[5]         [0x00000898] = 0x00000000
channel_jib_if_pkt_count[6]         [0x0000089C] = 0x00000000
channel_jib_if_pkt_count[7]         [0x000008A0] = 0x00000000
channel_jib_if_pkt_count[8]         [0x000008A4] = 0x00000000
channel_jib_if_pkt_count[9]         [0x000008A8] = 0x00000000
channel_jib_if_pkt_count[10]        [0x000008AC] = 0x00000000
channel_jib_if_pkt_count[11]        [0x000008B0] = 0x00000000
channel_jib_if_pkt_count[12]        [0x000008B4] = 0x00000000
channel_jib_if_pkt_count[13]        [0x000008B8] = 0x00000000
channel_jib_if_pkt_count[14]        [0x000008BC] = 0x00000000
channel_jib_if_pkt_count[15]        [0x000008C0] = 0x00000000
channel_jib_if_pkt_count[16]        [0x000008C4] = 0x00000000
channel_jib_if_pkt_count[17]        [0x000008C8] = 0x00000000
channel_jib_if_pkt_count[18]        [0x000008CC] = 0x00000000
channel_jib_if_pkt_count[19]        [0x000008D0] = 0x00000000

Remora Timestamp Registers (0xF8900900):
----------------------------------------
local_1024_ts_ctrl                  [0x00000900] = 0x00000039
local_1024_current_ts               [0x00000904] = 0xC354FFA0
local_1024_tcc_ts_latch             [0x00000908] = 0x7291125F
doc_ts_offset_ch_0_1                [0x0000090C] = 0x04AF04AF
doc_ts_offset_ch_2_3                [0x00000910] = 0x04AF04AF
doc_ts_offset_ch_4_5                [0x00000914] = 0x04F704F7
doc_ts_offset_ch_6_7                [0x00000918] = 0x04F704F7
doc_ts_offset_ch_8_9                [0x0000091C] = 0x04F704F7
doc_ts_offset_ch_10_11              [0x00000920] = 0x04F704F7
doc_ts_offset_ch_12_13              [0x00000924] = 0x04F704F7
doc_ts_offset_ch_14_15              [0x00000928] = 0x04F704F7
doc_ts_offset_ch_16_17              [0x0000092C] = 0x04F704F7
doc_ts_offset_ch_18_19              [0x00000930] = 0x04F704F7

Remora PRATE/SRATE Registers (0xF8900A00):
------------------------------------------
port_prate_regs[0].prate_ctrl       [0x00000A00] = 0x00000003
port_prate_regs[0].prate_m_prime_lo [0x00000A04] = 0x0005971E
port_prate_regs[0].prate_n_prime_lo [0x00000A08] = 0x08AA5B88
port_prate_regs[0].prate_m_prime_hi [0x00000A0C] = 0x00000000
port_prate_regs[1].prate_ctrl       [0x00000A10] = 0x00000003
port_prate_regs[1].prate_m_prime_lo [0x00000A14] = 0x00000191
port_prate_regs[1].prate_n_prime_lo [0x00000A18] = 0x00037E78
```

```
port_prate_regs[1].prate_m_prime_hi [0x00000A1C] = 0x00000000
port_prate_regs[2].prate_ctrl       [0x00000A20] = 0x00000003
port_prate_regs[2].prate_m_prime_lo [0x00000A24] = 0x00000191
port_prate_regs[2].prate_n_prime_lo [0x00000A28] = 0x00037E78
port_prate_regs[2].prate_m_prime_hi [0x00000A2C] = 0x00000000
port_prate_regs[3].prate_ctrl       [0x00000A30] = 0x00000003
port_prate_regs[3].prate_m_prime_lo [0x00000A34] = 0x00000191
port_prate_regs[3].prate_n_prime_lo [0x00000A38] = 0x00037E78
port_prate_regs[3].prate_m_prime_hi [0x00000A3C] = 0x00000000
port_prate_regs[4].prate_ctrl       [0x00000A40] = 0x00000003
port_prate_regs[4].prate_m_prime_lo [0x00000A44] = 0x00000191
port_prate_regs[4].prate_n_prime_lo [0x00000A48] = 0x00037E78
port_prate_regs[4].prate_m_prime_hi [0x00000A4C] = 0x00000000
port_srate_regs[0].srate_ctrl       [0x00000A50] = 0x00000003
port_srate_regs[0].srate_mn         [0x00000A54] = 0x004E0095
port_srate_regs[1].srate_ctrl       [0x00000A58] = 0x00000003
port_srate_regs[1].srate_mn         [0x00000A5C] = 0x0191032C
port_srate_regs[2].srate_ctrl       [0x00000A60] = 0x00000003
port_srate_regs[2].srate_mn         [0x00000A64] = 0x0191032C
port_srate_regs[3].srate_ctrl       [0x00000A68] = 0x00000003
port_srate_regs[3].srate_mn         [0x00000A6C] = 0x0191032C
port_srate_regs[4].srate_ctrl       [0x00000A70] = 0x00000003
port_srate_regs[4].srate_mn         [0x00000A74] = 0x0191032C
```

The following example shows a typical display for the **show interfaces integrated-cable** command.

```
Router# show interfaces integrated-cable 7/1/3:1
Integrated-Cable7/1/3:1 is down, line protocol is down
  Hardware is CMTS IC interface, address is 0013.5f06.93b7 (bia 0013.5f06.93b7)
  MTU 1764 bytes, BW 13000 Kbit, DLY 1000 usec,
     reliability 255/255, txload 1/255, rxload 1/255
  Encapsulation MCNS, loopback not set
  Keepalive set (10 sec)
  ARP type: ARPA, ARP Timeout 04:00:00
  Last input never, output never, output hang never
  Last clearing of "show interface" counters never
  Input queue: 0/75/0/0 (size/max/drops/flushes); Total output drops: 0
  Interface Integrated-Cable7/1/3:1 queueing strategy: PXF Class-based
  5 minute input rate 0 bits/sec, 0 packets/sec
  5 minute output rate 0 bits/sec, 0 packets/sec
     0 packets input, 0 bytes, 0 no buffer
     Received 0 broadcasts (0 multicasts)
     0 runts, 0 giants, 0 throttles
     0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored, 0 abort
     0 packets output, 0 bytes, 0 underruns
     0 output errors, 0 collisions, 0 interface resets
     0 output buffer failures, 0 output buffers swapped out
```

Viewing Information about the Cable Modems

To view information about the registered and unregistered cable modems, use the **show cable modem** command in privileged EXEC mode.

For a complete description of the command, see the *Cisco Broadband Cable Command Reference Guide* on Cisco.com.

Example

The following example shows a typical display for the **show cable modem** command.

```
Router# show cable modem
```

```
MAC Address    IP Address      I/F          MAC           Prim RxPwr  Timing Num I
                                            State         Sid  (dBmv) Offset CPE P
0011.808d.1d9a 80.23.0.2       C6/1/0/U0    online        1    -0.75  1701   0   N
0006.53b6.581f 80.23.0.3       C7/1/0/U0    online        1    0.00   2104   0   N
001e.6bfb.3a08 80.23.0.4       C7/1/0/UB    w-online      2    1.00   2588   0   N
001e.6bfb.388c 80.23.0.5       C7/1/0/UB    w-online      3   *2.25   3050   0   N
001e.6bfc.cfaa 80.23.0.7       C7/1/0/UB    w-online      4    0.50   2587   0   N
0000.39a0.fe4f 80.23.0.6       C7/1/3/U0    online        1    0.00   1632   0   N
0000.3961.8059 80.23.0.8       C7/1/3/U0    online        2    0.00   1607   0   N
0000.39f2.2e58 80.23.0.9       C7/1/3/U0    online        3    0.50   1610   0   N
```

The following example shows a typical display of the **show cable modem primary** command:

```
Router# show cable modem primary

MAC Address    IP Address      Host         MAC           Prim Num Primary    DS
                               Interface    State         Sid  CPE Downstream RfId
0011.808d.1d9a 80.23.0.2       C6/1/0/U0    online        1     0   C6/1/0      600
0006.53b6.581f 80.23.0.3       C7/1/0/U0    online        1     0   Mo3/0/0:3   123
001e.6bfb.3a08 80.23.0.4       C7/1/0/UB    w-online      2     0   In7/1/0:0   840
001e.6bfb.388c 80.23.0.5       C7/1/0/UB    w-online      3     0   Mo3/0/0:3   123
001e.6bfc.cfaa 80.23.0.7       C7/1/0/UB    w-online      4     0   In7/1/0:0   840
0000.39a0.fe4f 80.23.0.6       C7/1/3/U0    online        1     0   In7/1/3:0   912
0000.3961.8059 80.23.0.8       C7/1/3/U0    online        2     0   In7/1/3:0   912
0000.39f2.2e58 80.23.0.9       C7/1/3/U0    online        3     0   In7/1/3:1   913
```

Upgrading the Cisco CMTS Line Card Software License

To enable all software features, all new or upgraded Cisco devices that require software activation must be registered with Cisco. The registration process requires a Product Authorization Key (PAK), which is an 11-character alphanumeric key printed on the purchase order document shipped with your device hardware. The registration process converts the PAK to an electronic license file containing a unique key for your device hardware. The license file must then be installed on your device to unlock the product and its features.

Note To upgrade to a 10DS or 15DS license, you can purchase either a Cisco UBR-MC20X20V-0D or Cisco UBR-MC20X20V-5D cable interface line cards and then purchase multiples of +5DS licenses. Alternatively, you could directly purchase +10DS or +15DS licenses.

To upgrade and install a license, perform these steps:

1. Purchase a PAK for the required type of license. For example, the UBR-MC20X20V-5D (which provides the 5 downstream channel license for the uBR-MC20X20V cable line card.)
2. Submit the PAK code and UDI of the line card to the Cisco Product License Registration portal.

   The portal retrieves the stock keeping units (SKUs) associated with the PAK. Select the SKU and enter the UDI—a unique and unchangeable identifier of the device where the license should be installed. A license key is then e-mailed to you, which you can use to upgrade the license.
3. Install the license file returned from the license portal by using Cisco IOS commands. (This step can also be completed using the Cisco License Manager application, which can be downloaded at http://www.cisco.com/go/clm.)

Note If you use Microsoft Entourage and receive the license file from Cisco in an e-mail attachment, the license file will contain UTF-8 marking. These extra bytes in the license file makes it unusable during license installation. To work around this issue, you can use a text editor to remove the extra characters and then install the license file. For more information about UTF-8 encoding, go to this URL: http://www.w3.org/International/questions/qa-utf8-bom

4. Reset the line card with the **hw-module subslot** *slot/subslot* **reset** command.

You can manually upgrade a license by using the **install license** command. However, before you upgrade the license you must have already received the license file from Cisco Product License Registration at http://www.cisco.com/go/license.

SUMMARY STEPS

1. Obtain the PAK.
2. **enable**
3. **show license udi**
4. Convert the PAK to a license.
5. **license install** *stored-location-url*
6. Reset the line card.

DETAILED STEPS

Step 1 Obtain the PAK.

PAKs are purchasable items, ordered in the same manner as other Cisco equipment. PAKs are used to obtain license files for feature sets on specific classes of Cisco devices.

Step 2 **enable**

This command enables privileged EXEC mode.

```
Router> enable
```

Enter password, if prompted.

Step 3 **show license udi**

This command displays all licensable UDIs in the system. The following is sample output from this command:

```
Router# show license udi

SlotID   PID                    SN                      UDI
-------------------------------------------------------------------------------
 5       UBR-MC88U              CSJ13054214     UBR-MC88U:CSJ13054214
```

Step 4 Convert the PAK to a license (http://www.cisco.com/go/license).

After entering the appropriate information, you will receive an e-mail with the license information that you can use to install the license.

Step 5 **license install** *stored-location-url*

This command installs the license. Follow the instructions on the screen.

When a license is successfully installed, a message confirms the installation and states whether or not the licensed feature is present in the current image.

```
Router# license install tftp://223.255.254.254/<user>/licenses/CSJ13462916_72X60.lic

Installing licenses from tftp://223.255.254.254/<user>/licenses/CSJ13462916_72X60.lic
Loading <user>/licenses/CSJ13462916_72X60.lic from 223.255.254.254 (via
FastEthernet0/0/0):!
[OK - 2239 bytes]
*Apr 25 12:33:22.823Installing...Feature:US_License...Successful:Supported
Installing...Feature:DS_License...Successful:Supported
2/2 licenses were successfully installed
0/2 licenses were existing licenses
0/2 licenses were failed to install
Router#
```

Step 6 **hw-module subslot** *slot/subslot* **reset**

This command resets the line card.

Verifying the License Upgrade

You can verify the license upgrade by using the following commands:

- **show running-config | include license**

  This command displays the running configuration for each cable interface.The following is sample output from this command:

```
Router> show running-config | include license

card 6/0 ubr10k-clc-mc2020v license 10X20
card 7/0 ubr10k-clc-mc2020v license invalid
Router>
```

- **show diag** *slot/subslot*

  This command displays diagnostic information for port adapters/modules. The following is the sample output from this command:

```
Router# show diag 6/1

Slot/Subslot 6/1:
    ubr10k-clc-mc2020v card, 5 ports
    Card is half slot size
    Card is analyzed
    Card detected 02:05:40 ago
    Card uptime 0 days, 2 hours, 6 minutes, 40 seconds
    Card idle time N/A
    Voltage status: 3.3V Nominal 2.5V Nominal 1.8V Nominal 1.5V Nominal 1.2V Nominal
1.1V Nominal 1.0V Nominal 0.95V Nominal 1.05V Nominal
EEPROM contents, slot 6/1:
    Controller Type          : 1601
    Hardware Revision        : 8.6
    Top Assy. Part Number    : 800-32154-01
    Top Assy. Revision       : 10
    Product Identifier (PID) : UBR-MC20X20V
    Version Identifier (VID) : V01
```

```
    CLEI Code                : NOCLEICODE
    Deviation Number         : 104645
    Fab Version              : 03
    PCB Serial Number        : CAT1329E099
    RMA Test History         : 00
    RMA Number               : 0-0-0-0
    RMA History              : 00
    Licensing Transaction ID : 20
    License                  : 10X20
    Bundle PID               : UBR-MC20X20V-5D
```

- **show license detail**

  This command displays the details of the license. The following is the sample output from this command:

```
Router# show license detail subslot 6/0

Load for five secs: 1%/0%; one minute: 1%; five minutes: 1%
Time source is hardware calendar, *16:55:22.394 UTC Mon Apr 26 2010
Index: 1        Feature: DS_License                      Version: 1.0
    License Type: Permanent
    License State: Active, In Use
    License Count: 20/20/0  (Active/In-use/Violation)
    License Priority: Medium
    Store Index: 0
    Store Name: Primary License Storage
Index: 2        Feature: DS_License                      Version: 1.0
    License Type: Evaluation
    License State: Inactive
        Evaluation total period: 8  weeks 4  days
        Evaluation period left: 8  weeks 4  days
    License Count: 20/0/0  (Active/In-use/Violation)
    License Priority: None
    Store Index: 1
    Store Name: Evaluation License Storage
Index: 3        Feature: US_License                      Version: 1.0
    License Type: Permanent
    License State: Active, In Use
    License Count: 20/20/0  (Active/In-use/Violation)
    License Priority: Medium
    Store Index: 1
    Store Name: Primary License Storage
Index: 4        Feature: US_License                      Version: 1.0
    License Type: Evaluation
    License State: Inactive
        Evaluation total period: 8  weeks 4  days
        Evaluation period left: 8  weeks 4  days
    License Count: 20/0/0  (Active/In-use/Violation)
    License Priority: None
    Store Index: 0
    Store Name: Evaluation License Storage
```

Upgrading the License When Line Card is in LCHA Mode

If the Cisco uBR-MC20X20V line card is in the line card high availability (LCHA) mode, perform the following steps while upgrading:

1. Ensure that the working line card is active.
2. Install the license on the protect line card.

3. Verify the installed license by running the **show license detail** *subslot* command.
4. Reload the protect line card.
5. Verify the effective license by running the **show running-config | include license** command.
6. Install the license on the working line card.
7. Verify the installed license by running the **show license detail** *subslot* command.
8. Reload the working line card to cause the line card switchover to the upgraded protect line card.
9. Verify the effective license by running the **show running-config | include license** command.
10. Revert to the upgraded working line card.
11. Repeat steps 6 through 10 for each working line card to be upgraded.

Return Materials Authorization

When a line card in service fails, a replacement card is required with equivalent licenses for restoring the services completely. If the failed line card has the same license as the shipping order, the return materials authorization (RMA) replacement and spares will also have the same license as the failed line card.

If the failed line card has an upgrade license after shipping, the RMA replacement and spares will have lower license. To work around this:

- Rehost the upgrade licenses from the failed line card.
- Follow the procedure for hitless replacement with RMA of the working line card with LCHA. Failure to follow the procedure results in Loss of Service.

Restrictions for RMA

- If the line card is not part of the LCHA, follow the steps in Upgrading the Cisco CMTS Line Card Software License, page 59.
- If the line card is part of the LCHA, and the RMA is for the protect line card, follow the steps in Upgrading the License When Line Card is in LCHA Mode, page 62.
- If the RMA is for the working line card, the service automatically switches over to the protect line card. To verify this:
  - Insert the replacement line card.
  - Verify the effective license for the working line card by running the **show running-config | include license** command.
- If effective license is not the same as previous license in slot, do the following:
  - Upgrade the working line card. For more information, see Upgrading the Cisco CMTS Line Card Software License, page 59.
  - Verify the installed license on the working line card by running the **show license detail** *subslot* command.
  - Ensure that the working line card continues to be on the HCCP standby.
  - Reload the working line card.
  - Verify the effective license by running the **show running-config | include license** command.

- Revert to the upgraded line card.
- Run the **no shut** command on all upstream and downstream channels.

Troubleshooting the Cisco UBR-MC20X20V Cable Interface Line Card

The following MAC domain commands are useful for troubleshooting bonding operations.

- **show cable mac-domain cable** *slot/subslot/domain* **rcc**
- **show cable mac-domain cable** slot/subslot/domain **downstream-service-group**
- **show cable mac-domain cable** slot/subslot/domain **upstream-service-group**
- **show cable mac-domain cable** slot/subslot/domain **cgd-associations**

For complete descriptions of the above configuration commands, refer to the *Cisco Broadband Cable Command Reference Guide* on Cisco.com.

Upgrading Cisco uBR10-MC5X20S/U/H Line Cards to Cisco UBR-MC20X20V Line Card

Cisco IOS Release 12.2(33)SCC, by default, supports OIR compatibility for the Cisco UBR-MC20X20V line card.

Note Run the **no platform oir-compatibility** command to specifically disable OIR for all slots in the line card.

With HCCP Group

The following procedure provides information about upgrading Cisco uBR10-MC5X20S/U/H line cards to the Cisco UBR-MC20X20V line card with the HCCP configuration.

1. Upgrade the protect cable line card from Cisco uBR10-MC5X20S/U/H to Cisco UBR-MC20X20V line card.
2. OIR the working Cisco uBR10-MC5X20S/U/H line card. CMTS switches over to the protect mode.
3. Replace the working card with the Cisco UBR-MC20X20V line card.

Repeat steps 2 and 3 for other slots that need an upgrade from Cisco uBR10-MC5X20S/U/H to Cisco UBR-MC20X20V line card.

Without the HCCP Group

The following procedure provides information about upgrading Cisco uBR10-MC5X20S/U/H line cards to the Cisco UBR-MC20X20V line card without the HCCP configuration.

1. OIR the working Cisco uBR10-MC5X20S/U/H line card.
2. Replace it with the Cisco UBR-MC20X20V line card.

Repeat steps 1 and 2 for other slots that need an upgrade from Cisco uBR10-MC5X20S/U/H to Cisco UBR-MC20X20V line card.

Note The OIR-compatibility enables automatic translation of the Cisco uBR10-MC5X20S/U/H line card config to the UBR-MC20X20V line card config. The related error message is:
%UBR10K-6-COMPAT_NEW_CARD: The 5cable-mc520h-d in slot 6/0 has been replaced by a ubr10k-clc-mc2020v.
If the automatic translation of the config fails, then the MAC domains or cable interfaces are placed in the shutdown mode. The following error message will be displayed.
%UBR10K-6-COMPAT_SHUTDOWN_CARD: Failed to restore the configuration for Cable6/1/0.

When No Licenses are Available

If you cannot communicate with the Swift License Server, enable the in-built temporary evaluation license.

Note Use this temporary license only until the permanent license becomes available.

Install the permanent license as soon as it is available because the temporary license is valid only for 60 days.

To enable the temporary license, run the following commands:

license modify priority US_License high subslot *slot/subslot*

license modify priority DS_License high subslot *slot/subslot*

Additional References

For more information about the Cisco UBR-MC20X20V cable interface line cards, Cisco uBR10012 router chassis, and software configuration, refer the following documents:

Related Documents

Document Title	URL
Cisco UBR-MC20X20V Cable Interface Line Card Hardware Installation Guide	http://www.cisco.com/en/US/docs/interfaces_modules/cable/broadband_processing_engines/ubr_mc20x20v/installation/guide/mc20x20v_hig.html
Cisco uBR10012 Universal Broadband Router Hardware Installation Guide	http://www.cisco.com/en/US/docs/cable/cmts/ubr10012/installation/guide/hig.html
Cisco uBR10000 Series Universal Broadband Router Release Notes	http://www.cisco.com/en/US/products/hw/cable/ps2209/prod_release_notes_list.html
Cisco IOS Commands for the Cisco CMTS Routers	http://www.cisco.com/en/US/docs/ios/cable/command/reference/cbl_book.html
Cisco uBR10012 Universal Broadband Router Software Configuration Guide	http://www.cisco.com/en/US/docs/cable/cmts/ubr10012/configuration/guide/scg.html
Cisco uBR10012 Router Software Features	http://www.cisco.com/en/US/products/hw/cable/ps2209/products_feature_guides_list.html
Cisco IOS CMTS Cable Software Configuration Guide, Release 12.2SC	http://www.cisco.com/web/techdoc/cable/Config/Sw_conf.html

Standards

Standard	Title
CableLabs™ DOCSIS 1.1 specifications	http://www.cablelabs.com/cablemodem/
CableLabs™ PacketCable specifications	http://www.cablelabs.com/packetcable/
CableLabs™ PacketCable MultiMedia specifications	http://www.cablelabs.com/packetcable/specifications/multimedia.html

MIBs

MIB	MIBs Link
MIBs for the Cisco Cable Modem Termination System	*Cisco CMTS Universal Broadband Series Router MIB Specifications Guide 12.2 SC* http://www.cisco.com/en/US/docs/cable/cmts/mib/12_2sc/reference/guide/ubrmibv5.html
MIBs Supporting Cisco IOS	To locate and download MIBs for selected platforms, Cisco IOS releases, and feature sets, use Cisco MIB Locator found at the following URL: http://www.cisco.com/go/mibs

Technical Assistance

Description	Link
The Cisco Support website provides extensive online resources, including documentation and tools for troubleshooting and resolving technical issues with Cisco products and technologies. To receive security and technical information about your products, you can subscribe to various services, such as the Product Alert Tool (accessed from Field Notices), the Cisco Technical Services Newsletter, and Really Simple Syndication (RSS) Feeds. Access to most tools on the Cisco Support website requires a Cisco.com user ID and password.	http://www.cisco.com/techsupport

Feature Information for Configuring the Cisco UBR-MC20X20V Cable Interface Line Card

Table 3 lists the release history for this feature.

Not all commands may be available in your Cisco IOS software release. For release information about a specific command, see the command reference documentation.

Use Cisco Feature Navigator to find information about platform support and software image support. Cisco Feature Navigator enables you to determine which Cisco IOS and Catalyst OS software images support a specific software release, feature set, or platform. To access Cisco Feature Navigator, go to http://www.cisco.com/go/cfn. An account on Cisco.com is not required.

Note Table 3 lists only the Cisco IOS software release that introduced support for a given feature in a given Cisco IOS software release train. Unless noted otherwise, subsequent releases of that Cisco IOS software release train also support that feature.

Table 3 Feature Information for the Cisco UBR-MC20X20V Cable Interface Line Card

Feature Name	Releases	Feature Information
Configuring the Cisco UBR-MC20X20V Cable Interface Line Card	12.2(33)SCC	The Cisco UBR-MC20X20V line card was introduced on the Cisco uBR10012 Universal Broadband Router.
Configuring the Cisco UBR-MC20X20V Cable Interface Line Card	12.2(33)SCD2	Two new licenses for 10 and 15 downstream channels were added for the Cisco uBR-MC20X20V cable line card.