Hardware Troubleshooting for Catalyst 8540/8510 MSRs and LightStream 1010 ATM Switch: IOS upgrade

Document ID: 21445

IOS Upgrade

Contents

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Cisco offers several Cisco IOS® Software Releases for LightStream 1010 and the Catalyst 8500 ATM switch routers. Each release offers a different combination of functionality and hardware support. This section provides general Cisco IOS software release suggestions for these platforms and discusses factors to consider when choosing a release.

Overview of Cisco IOS Release Model

Since IOS release 11.3 (and more fully since release 12.0) Cisco has followed an IOS release model that generally uses two types of release:

- Main releases − Identified by a version name that does not end with a capital letter. For example, release 12. 0(15) is available on the Software Center for the LightStream 1010. Cisco IOS main releases seek greater stability and quality. For that reason, main releases do not accept the addition of features or platforms. Each maintenance revision provides bug fixes only.

- Early deployment (ED) releases − Unlike main Cisco IOS releases, Cisco IOS ED releases are vehicles that bring new development to the marketplace. Each maintenance revision of an ED release includes not only bug fixes, but a set of new features, new platform support, and general enhancements to protocols and the Cisco IOS infrastructure. Every one to two years, the features and platforms of the ED releases are ported to the next main Cisco IOS release. Among the types of ED releases are the following:
    - ♦ Consolidated Technology Early Deployment (CTED) releases are easily identifiable by their name, which always ends with a "T" (technology). Examples of consolidated technology releases are Cisco IOS 11.3T, 12.0T, and 12.1T.

- Specific Technology Early Deployment (STED) releases target a specific technology or market theater. They are always released on specific platforms. STED releases are identified using two letters appended to the major release version. The first letter identifies the targeted technology. For example, "W" indicates that the release is targeted to ATM, LAN switching, and layer 3 switching technology. Cisco IOS releases 11.2WA3, 11.3WA4 and 12.0W5 for Cisco ATM switch routers are all examples of STED releases.

Further information on Cisco release trains and the release model is available on Cisco.com in White Paper: Cisco IOS Reference Guide. A more detailed version of this white paper also is available in Cisco IOS Releases: The Complete Reference.

12.0 Mainline and 12.0W5 for the LightStream 1010

The LightStream 1010 supports two major trains of Cisco IOS images: 12.0 mainline and 12.0W5. Normally, a mainline image provides the most stable release for a platform running Cisco IOS. However, this guideline does not apply to 12.0 mainline for the LightStream 1010.

The 12.0 mainline image is derived from the 11.3WA4 train, specifically the 11.3(5)WA4(8) release. After the first few maintenance releases, the 12.0 mainline image does not contain any new LightStream 1010−specific features. New features that specifically enhance the functionality of the LightStream 1010 are integrated in the 12.0W5 train. Thus, if you only need the 11.3WA4 features, Cisco recommends the 12.0 mainline image as the general−deployment maintenance path. Otherwise, Cisco recommends the latest 12.0W5 image.

In addition, Cisco releases a maintenance image for every platform that runs 12.0 mainline. It is important to understand that only a few LightStream 1010−specific bug fixes are integrated in 12.0 mainline releases. Thus, a later 12.0 mainline release for the LightStream 1010 may or may not contain a bug that specifically applies to the LightStream 1010. The following table presents some of these fixes, but is not meant to be a complete list.

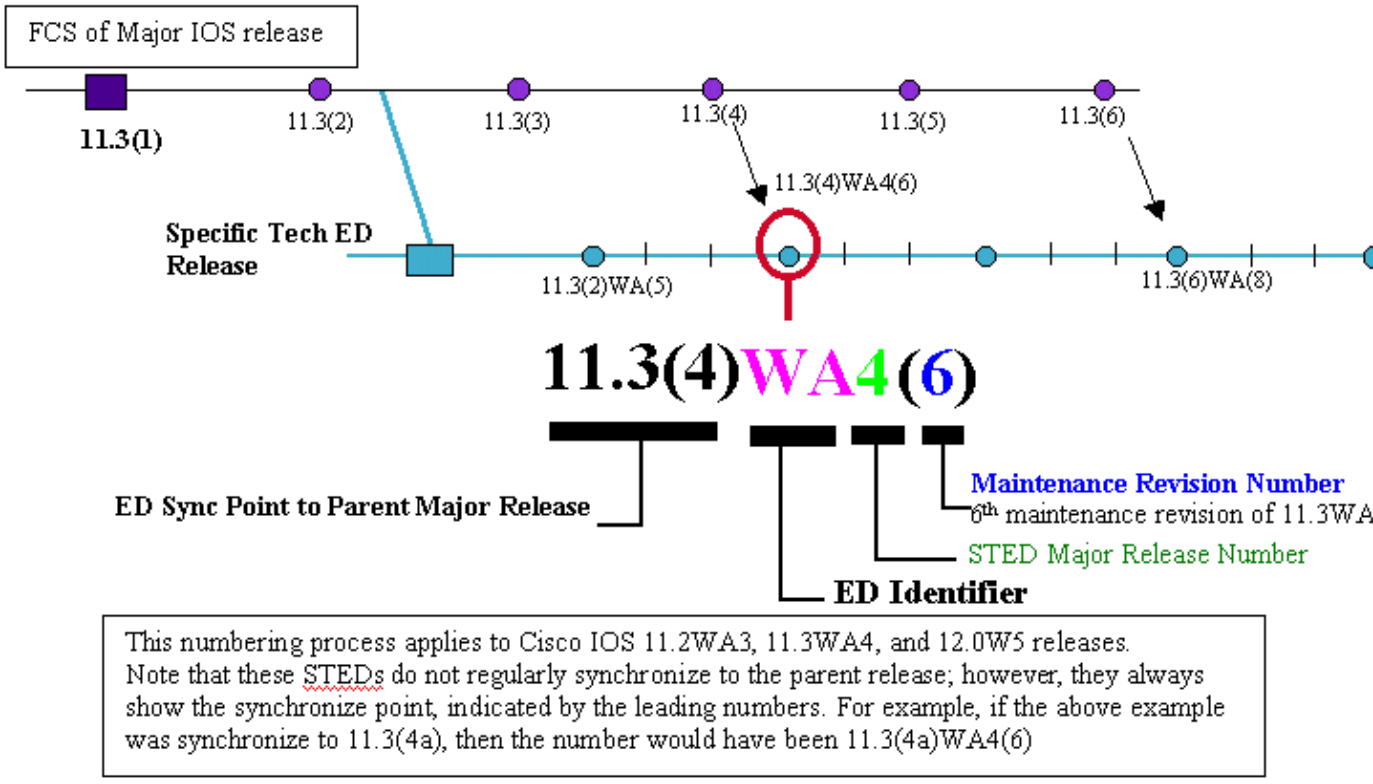
Cisco Bug ID	Fixed−In Release	Description
CSCdr68425	12.0(13)	Resolves a problem with creating a soft VC with 95 percent of the PVP bandwidth. On VBR virtual path (VP) tunnels, the PCR traffic parameters of a call are now checked against the PCR of the tunnel rather than against the maximum equivalent bandwidth of the tunnel.
CSCdr16095	12.0(13)	Resolves a problem with switched virtual circuit (SVC) call setups failing even when physical connectivity is fine. Also includes the following MIB objects: • csfSigCallTotalSetupAttempts: total number of call setup attempts. • csfSigCallTotalFailAttempts: total number of failed call setup attempts. • csfSigCallFilterFailAttempts: number of failed call setup attempts that match the diagnostic filter.
CSCdr96649	12.0(14)	

		Resolves software−forced crash on Catalyst 8510 MSR platform at PC 0x600B3A60.
CSCdp90229	12.0(15)	Applies fix in ATM signaling code running on *routers*. Resolves crash on 7507 platform due to a bus error at address 0xD0D0D19.
CSCdk87932	12.0(16)	Implements SSCOP state level changes. Resolves SSCOP BGN/END PDU conformance issue, and allows switches and routers to interoperate with SVC redundancy features in 12.1E images.

Cisco IOS Software Release 12.0W5

The 12.0W5 technology release for the LightStream 1010 as well as for the Catalyst 8500 series is based on and maintains synchronization with the Cisco IOS 12.0 mainline image. Synchronization means that a particular 12.0(X)W5 image includes the same bug fixes as the matching 12.0(X) mainline image. For example, the 12.0(16)W5 image includes the same bug fixes as the 12.0(16) mainline image.

As a technology release, the 12.0W5 train integrates new hardware support, such as the eight−port T1/E1 IMA port adapter, and new software support, such as IP MultiLayer Switching (MLS) over ATM and Fast Simple Server Redundancy Protocol (FSSRP).



The 12.0W5 release uses the following naming scheme:

12.0(1)W5(X)
12.0(1)W5(Y)
12.0(x)W5(Z)
12.0(y)W5(Zb)

- Lowercase x and y − Indicates the version of the parent IOS mainline release.
- Uppercase X, Y, and Z − Indicates the maintenance level of the release. Maintenance releases integrate new features and new software fixes. Maintenance releases typically are released every seven to eight weeks.

An important concept to understand about Cisco IOS is general deployment (GD) status, which refers to the point at which Cisco declares a release to be stable on all platforms and in all network environments. A release reaches GD status if it meets certain quality criteria, including positive feedback from actual customers. Only mainline releases, which do not integrate new hardware and software support, are designed to reach GD status. Technology releases like the 12.0W5 do not reach GD status.

You can view more information about the 12.0W5(X) releases by clicking here and by checking the Release Notes for your ATM switch router.

Cisco IOS Software Release 12.1(5)EY

The Catalyst 8500 series and the LightStream 1010 are now supported by Cisco IOS® Software Release 12.1(x)EY train. You can view more information about this train by clicking on the following links:

- Cisco IOS Software Release 12.1(5)EY
- Catalyst 8540 Cisco IOS Release 12.1 Documents
- Catalyst 8500 MSR Documents

The 12.0W5 train effectively went into maintenance mode for the LightStream 1010 and Catalyst 8500 after release 12.0(10)W5(18b). The 12.1(x)EY train is an X or short−lived technology release through which new features and new hardware support are being introduced. The 12.1(x)EY train will merge back into a main 12.1E release and ultimately into a 12.2E release.

Image Memory Requirements

Before upgrading your ATM switch router, ensure that your system has sufficient memory resources to support 12.0W5 images. The internal architecture of your switch router uses the following memory components.

- Flash memory stores a copy of the Cisco IOS software and is retained when you power down or restart. The 8540 MSR requires 16 MB of flash memory, while the 8510 MSR and LightStream1010 require eight MB of flash memory.

- On power on, the system loads the operating image into DRAM, from which the image runs. DRAM also stores dynamic configuration information and state tables such as routing tables and virtual circuit (VC) tables. The Catalyst 8540 MSR now requires 256 MB of dynamic random−access memory (DRAM), while the 8510 MSR and LightStream1010 require 64 MB of DRAM.

Use the **show version** command to determine your current amount of DRAM and flash memory. In the following output, the LightStream1010 has 64 MB of DRAM and eight MB of flash memory.

```
ls1010−3.8#show version
Cisco Internetwork Operating System Software
IOS (tm) LightStream1010 WA4−5 Software (LightStream1010−WP−M), Version 12.0(10)W5(18b) RELEAS
Copyright (c) 1986−2000 by cisco Systems, Inc.
Compiled Thu 03−Aug−00 08:33 by integ
Image text−base: 0x60010930, data−base: 0x60AC4000

ROM: System Bootstrap, Version 11.2(1.4.WA3.0) [integ 1.4.WA3.0], RELEASE SOFTWARE
ROM: LightStream1010 WA4−5 Software (LightStream1010−WP−M), Version 12.0(4a)W5(11a) RELEASE SO
```

```
ls1010−3.8 uptime is 4 weeks, 4 days, 2 hours, 47 minutes
System restarted by power−on
System image file is "slot0:ls1010−wp−mz_120−10_W5_18b.bin"

cisco LightStream1010 (R4600) processor with 65536K bytes of memory.
R4700 processor, Implementation 33, Revision 1.0
Last reset from power−on
1 Ethernet/IEEE 802.3 interface(s)
18 ATM network interface(s)
123K bytes of non−volatile configuration memory.
8192K bytes of Flash internal SIMM (Sector size 256K).

Configuration register is 0x2102
```

Other Firmware Code

On the ATM switch router, you can reprogram the functional images on the route processors, rommon, switch processors, switch processor feature cards, carrier modules, full−width modules, and network clock modules. Functional images provide the low−level operating functionality for various hardware controllers. On hardware controllers with insystem programmable devices, such as field programmable gate arrays (FPGAs) and Erasable Programmable Logic Devices (EPLDs), the hardware functional images can be reprogrammed independently of loading the system image and without removing the devices from the controller.

The FPGA and functional images include caveat fixes, but in most cases, it is not necessary to upgrade. The release notes that describe the caveats from the FPGA and functional images are available here.

Before Deploying a Release

In general, Cisco recommends the latest image because of the amount of software features and hardware support and high number of bug fixes. Before deploying a Cisco IOS software release in a production network, always consult appropriate product−specific documentation and perform acceptance testing in your own test environment, as well as consult the following resources on the Cisco website:

- Field Notices
- Cisco Bug Toolkit − Cisco's defect tracking system. You must be a registered user and be logged in to Cisco.com in order to access this tool.

Other practices to consider when making network changes, like upgrading, are outlined in the Change Management: Best Practices White Paper.

Upgrading Redundant Route Processors on the Catalyst 8540

The Catalyst 8540 consists of a 13−slot chassis that accepts both ATM and Ethernet interface modules. The five middle slots of the chassis are reserved for two sets of processor cards:

- Switch Processors (SPs) − Form the high−speed switch fabric that provides the physical pathway from ingress port to egress port.

- Route Processors (RPs) − Provide standard system components, such as the CPU, DRAM, and onboard flash memory as well as PCMCIA card slots to store the system image.

The Catalyst 8540 supports redundant RPs. This document explains how to upgrade the Cisco IOS software image on a system using two RPs.

Primary and Secondary RPs

Primary and secondary are terms used to describe which RP is active and which RP is standby. The RP in slot 4 or slot 8 can be primary; in other words, the RP in slot 4 is not always the primary. Use the **show redundancy** command to determine the current primary and secondary RPs in your system.

```
8540MSR# show redundancy

        This CPU is the PRIMARY
        Primary
        -------
        Slot:                          4
        CPU Uptime:                    14 hours, 59 minutes
        ILMI sysUpTime:                15 weeks, 12 minutes
        Image:                         PNNI Software (cat8540m-WPK2-M), Version 12.1(FAE

        Time Since :
          Last Running Config. Sync:   Never
          Last Startup Config. Sync:   Never
        Module Syncs are ENABLED
        Init Sync is NOT Complete
        Last Restart Reason:           Switch Over
        Time since switchover:         14 hours, 50 minutes


        Secondary
        ---------
        State:                         DOWN

8540MSR#
```

Use the **show version** command to ensure that a primary RP recognizes the secondary RP:

```
8540MSR# show version
Cisco Internetwork Operating System Software
IOS (tm) PNNI Software (cat8540m-WPK2-M), Version 12.1(FALCON.29)
Copyright (c) 1986-2002 by cisco Systems, Inc.
Compiled Sat 12-Jan-02 00:49 by
Image text-base: 0x60010958, data-base: 0x60F46000

ROM: System Bootstrap, Version 12.0(0.19)W5(5), RELEASE SOFTWARE

8540MSR uptime is 2 weeks, 1 day, 20 hours, 27 minutes
System returned to ROM by reload at 18:28:41 UTC Mon Mar 4 2002
System image file is "slot0:cat8540m-wpk2-mz.121-99.FALCON_DEVTEST_UBLDIT29"

cisco C8540MSR (R5000) processor with 262144K/256K bytes of memory.
R5000 CPU at 200Mhz, Implementation 35, Rev 2.1, 512KB L2 Cache
Last reset from power-on
3 Ethernet/IEEE 802.3 interface(s)
16 FastEthernet/IEEE 802.3 interface(s)
15 ATM network interface(s)
505K bytes of non-volatile configuration memory.

20480K bytes of Flash PCMCIA card at slot 0 (Sector size 128K).
8192K bytes of Flash internal SIMM (Sector size 256K).
Secondary is up
Secondary has 262144K bytes of memory.

Configuration register is 0x0

8540MSR#
```

The primary RP on the Catalyst 8540 serves as the system master. The secondary RP runs in standby mode. In this mode, the secondary RP is partially booted with the Cisco IOS software; however, no configuration is loaded. The following sample output of the **show run** command was captured from a secondary RP. Note how the command returns an essentially blank running configuration for the secondary RP.

```
8540MSR# show running-config
Building configuration...

Current configuration : 7709 bytes
!
version 12.1
service config
no service pad
service timestamps debug uptime
service timestamps log uptime
no service password-encryption
!
hostname 8540MSR
!
logging buffered 4096 debugging
no logging console
enable password lab
!
spd headroom 1024
no facility-alarm core-temperature major
no facility-alarm core-temperature minor
redundancy
 main-cpu
  sync dynamic-info
  sync config startup
  sync config running
network-clock-select revertive
network-clock-select 2 system
no diag online access
sdm ipqos zero
sdm policy 0
ip subnet-zero
ip host-routing
!
[Information Deleted]
!
line con 0
line aux 0
line vty 0 4
!
end
```

In standby mode, the secondary RP caches configuration information provided by the master. On actual failover, the secondary RP enables higher−layer protocols such as spanning tree and CDP as well as routing protocols and related CEF adjacency and FIB tables.

Each RP supports an internal port and an external Ethernet port assigned one of the following names depending on the redundancy status:

- Primary RP − controller0 and ethernet0
- Secondary RP − controller−sec0 and ethernetsec−0

Console access to the secondary RP must be done directly through the secondary's own console port and not via the primary. Telnet access to the secondary RP is not possible since the two RPs share a single IP and MAC address pair that is "owned" by the primary RP.

Before You Begin

Step 1 Ensure that your Catalyst 8540 meets the requirements for full redundancy status:

- Both route processors must be the same hardware version. Use the **show hardware** command to verify that the two RPs are the same hardware version.

Note: Both RPs must either have or not have a clock module.

```
8540MSR# show hardware

C8540 named 8540MSR, Date: 09:48:07 UTC Tue Mar 5 2002

Slot Ctrlr-Type    Part No.  Rev  Ser No  Mfg Date   RMA No. Hw Vrs  Tst EEP
---- ------------  --------- -- -------- --------- -------- ------- --- ---
 0/* Super Cam     73-2739-03 D0 03170TAL May 03 99 0          3.1
 0/0 8T1 IMA PAM   73-3367-02 B2 03100061 Mar 15 99 00-00-00   2.0     0   0
 0/1 155UTP PAM    73-1572-03 A0 09005149 Oct 22 98 00-00-00   3.2     0   2
 2/* ARM PAM       73-4208-01 05 03150016 Apr 18 99            1.0
 3/* ETHERNET PAM  73-3754-06 B0 03282WBF Jul 13 99 0          5.1
 4/* Route Proc    73-2644-05 A0 03140NXK Apr 04 99 0          5.7
 4/0 Netclk Modul  73-2868-03 A0 03140NSU Apr 04 99 0          3.1
 5/* Switch Card   73-3315-08 B0 03170SMB May 03 99 0          8.3
 5/0 Feature Card  73-3408-04 B0 03160S4H May 03 99 0          4.1
 7/* Switch Card   73-3315-08 B0 03160SDT May 03 99 0          8.3
 7/0 Feature Card  73-3408-04 B0 03160RQV May 03 99 0          4.1
 8/* Route Proc    73-2644-05 A0 03140NXH Apr 04 99 0          5.7
 8/0 Netclk Modul  73-2868-03 A0 03140NVT Apr 04 99 0          3.1
 9/* OC48c PAM     73-3745-02 12 03190UXC Jun 28 99            2.1
10/* OCM Board     73-4165-01 04 03230ZZ2 Jun 28 99           10.1
10/0 QUAD 622 Gen  73-2851-05 A0 03160RVS Jun 16 99            5.0
11/* OC48c PAM     73-3745-02 12 03100015 Jun 28 99            2.1
12/* OCM Board     73-4165-01 04 03190UJV Jun 28 99           10.1
12/0 QUAD 622 Gen  73-2851-05 A0 03160S9J Jun 16 99 0          5.0

DS1201 Backplane EEPROM:
Model  Ver.  Serial  MAC-Address  MAC-Size  RMA  RMA-Number   MFG-Date
------ ---- -------- ------------ --------  ---  ----------  -----------
 C8540  2   6315484 00902156D800   1024      0        0      Mar 23 1999
 cubi version : 11

Power Supply:
Slot Part No.          Rev  Serial No.  RMA No.     Hw Vrs  Power Consumption
---- ----------------- ---- ----------- ----------- ------- -----------------
0          34-0918-02 B0   ACP03220289 00-00-00-00   2.1             2746 cA

8540MSR#
```

- Both route processors must use the same functional images. Use the **show functional-image-info slot [4,8]** command to verify that the FPGA versions are identical.

```
8540MSR# show functional-image-info slot 4

Details for cpu Image on slot: 4

Functional Version of the FPGA Image: 4.8
 #Jtag-Distribution-Format-B
 #HardwareRequired: 100(3.0-19,4.0-19,5.0-19)
 #FunctionalVersion: 4.8
 #Sections: 1
 #Section1Format: MOTOROLA_EXORMAX

  Copyright (c) 1996-00 by cisco Systems, Inc.
```

```
  All rights reserved.
  generated by:       holliday
  on:                 Mon Mar  6 13:59:17 PST 2000
  using:              /vob/cougar/bin/jtag_script Version 1.13
  config file:        cpu.jcf

  Chain description:
  Part type Bits Config file
  10k50     10   ../cidrFpga2/max/cidr_fpga.ttf
  xcs4062   3    ../cubiFpga2/xil/cubi.bit
  xcs4062   3    ../cubiFpga2/xil/cubi.bit
  generic   2
  XC4005    3    /vob/cougar/custom/common/jtcfg/xil/jtcfg_r.bit
  Number devices             = 5
  Number of instruction bits = 21

  FPGA config file information:
  Bitgen date/time  Sum   File
  100/03/02 19:14:49 7068  ../cidrFpga2/max/cidr_fpga.ttf
  1999/04/15 18:46:32 36965 ../cubiFpga2/xil/cubi.bit
  1999/04/15 18:46:32 36965 ../cubiFpga2/xil/cubi.bit
  98/06/11 16:56:44 49904 /vob/cougar/custom/common/jtcfg/xil/jtcfg_r.bit

 #End-Of-Header


Details for Network Clock Module Image on slot: 4

Functional Version of the FPGA Image: 8.0
 #Jtag-Distribution-Format-B
 #HardwareRequired: 101(3.0-9)
 #FunctionalVersion: 8.0
 #Sections: 1
 #Section1Format: MOTOROLA_EXORMAX

  Copyright (c) 1996-98 by cisco Systems, Inc.
  All rights reserved.
  generated by:       pirooz
  on:                 Tue Oct 27 16:39:34 PST 1998
  using:              /cougar/bin/jtag_script Version 1.08
  config file:        nclkm.jcf

  Chain description:
  Part type Bits Config file
  10k30     10   /cougar/custom/nclkm/nclkm_cnt_dpll/max/PLL_WRAPPER.ttf
  xc40      3    /cougar/custom/nclkm/DPLL/xilinx/DPLL_r.bit
  XC4005    3    /cougar/custom/common/jtcfg/xil/jtcfg_r.bit
  Number devices             = 3
  Number of instruction bits = 16

  FPGA config file information:
  Bitgen date/time  Sum   File
  98/10/26 16:08:39 60395 /cougar/custom/nclkm/nclkm_cnt_dpll/max/PLL_WRAPPER.tf
  1998/10/21 17:17:12 15339 /cougar/custom/nclkm/DPLL/xilinx/DPLL_r.bit
  98/06/11 16:56:44 49904 /cougar/custom/common/jtcfg/xil/jtcfg_r.bit

 #End-Of-Header

8540MSR#

8540MSR# show functional-image-info slot 8

Details for cpu Image on slot: 8

Functional Version of the FPGA Image: 4.8
 #Jtag-Distribution-Format-B
```

```
 #HardwareRequired: 100(3.0-19,4.0-19,5.0-19)
 #FunctionalVersion: 4.8
 #Sections: 1
 #Section1Format: MOTOROLA_EXORMAX

  Copyright (c) 1996-00 by cisco Systems, Inc.
  All rights reserved.
  generated by:       holliday
  on:                 Mon Mar  6 13:59:17 PST 2000
  using:              /vob/cougar/bin/jtag_script Version 1.13
  config file:        cpu.jcf

  Chain description:
  Part type Bits Config file
  10k50     10   ../cidrFpga2/max/cidr_fpga.ttf
  xcs4062   3    ../cubiFpga2/xil/cubi.bit
  xcs4062   3    ../cubiFpga2/xil/cubi.bit
  generic   2
  XC4005    3    /vob/cougar/custom/common/jtcfg/xil/jtcfg_r.bit
  Number devices             = 5
  Number of instruction bits = 21

  FPGA config file information:
  Bitgen date/time  Sum   File
  100/03/02 19:14:49 7068  ../cidrFpga2/max/cidr_fpga.ttf
  1999/04/15 18:46:32 36965 ../cubiFpga2/xil/cubi.bit
  1999/04/15 18:46:32 36965 ../cubiFpga2/xil/cubi.bit
  98/06/11 16:56:44 49904 /vob/cougar/custom/common/jtcfg/xil/jtcfg_r.bit

 #End-Of-Header


Details for Network Clock Module Image on slot: 8

Functional Version of the FPGA Image: 8.0
 #Jtag-Distribution-Format-B
 #HardwareRequired: 101(3.0-9)
 #FunctionalVersion: 8.0
 #Sections: 1
 #Section1Format: MOTOROLA_EXORMAX

  Copyright (c) 1996-98 by cisco Systems, Inc.
  All rights reserved.
  generated by:       pirooz
  on:                 Tue Oct 27 16:39:34 PST 1998
  using:              /cougar/bin/jtag_script Version 1.08
  config file:        nclkm.jcf

  Chain description:
  Part type Bits Config file
  10k30     10   /cougar/custom/nclkm/nclkm_cnt_dpll/max/PLL_WRAPPER.ttf
  xc40      3    /cougar/custom/nclkm/DPLL/xilinx/DPLL_r.bit
  XC4005    3    /cougar/custom/common/jtcfg/xil/jtcfg_r.bit
  Number devices             = 3
  Number of instruction bits = 16

  FPGA config file information:
  Bitgen date/time  Sum   File
  98/10/26 16:08:39 60395 /cougar/custom/nclkm/nclkm_cnt_dpll/max/PLL_WRAPPER.tf
  1998/10/21 17:17:12 15339 /cougar/custom/nclkm/DPLL/xilinx/DPLL_r.bit
  98/06/11 16:56:44 49904 /cougar/custom/common/jtcfg/xil/jtcfg_r.bit

 #End-Of-Header


8540MSR#
```

- Both route processors must have the same amount of memory and must be running the same system image. Use the **show version** command to verify this.

```
8540MSR# show version
Cisco Internetwork Operating System Software
IOS (tm) PNNI Software (cat8540m-WPK2-M), Version 12.1(FALCON.29), MAINTENANCE E
Copyright (c) 1986-2002 by cisco Systems, Inc.
Compiled Sat 12-Jan-02 00:49 by
Image text-base: 0x60010958, data-base: 0x60F46000

ROM: System Bootstrap, Version 12.0(0.19)W5(5), RELEASE SOFTWARE

8540MSR uptime is 16 hours, 5 minutes
System returned to ROM by reload at 18:28:41 UTC Mon Mar 4 2002
System image file is "slot0:cat8540m-wpk2-mz.121-99.FALCON_DEVTEST_UBLDIT29"

cisco C8540MSR (R5000) processor with 262144K/256K bytes of memory.
R5000 CPU at 200Mhz, Implementation 35, Rev 2.1, 512KB L2 Cache
Last reset from power-on
3 Ethernet/IEEE 802.3 interface(s)
16 FastEthernet/IEEE 802.3 interface(s)
15 ATM network interface(s)
505K bytes of non-volatile configuration memory.

20480K bytes of Flash PCMCIA card at slot 0 (Sector size 128K).
8192K bytes of Flash internal SIMM (Sector size 256K).
Configuration register is 0x0

8540MSR#
```

Step 2 Verify that an IP address is assigned to the RP.

```
8540MSR# show ip interface Ethernet 0
Ethernet0 is up, line protocol is up
  Internet address is 172.20.52.11/27
  Broadcast address is 255.255.255.255
  Address determined by configuration file
  MTU is 1500 bytes
  Helper address is not set
  Directed broadcast forwarding is disabled
  Multicast reserved groups joined: 224.0.0.5 224.0.0.6
  Outgoing access list is not set
  Inbound  access list is not set
  Proxy ARP is enabled
  Local Proxy ARP is disabled
  Security level is default
  Split horizon is enabled
  ICMP redirects are always sent
  ICMP unreachables are always sent
  ICMP mask replies are never sent
  IP fast switching is disabled
  IP fast switching on the same interface is disabled
  IP Null turbo vector
  IP multicast fast switching is disabled
  IP multicast distributed fast switching is disabled
  IP route-cache flags are Fast, No CEF
  Router Discovery is disabled
  IP output packet accounting is disabled
  IP access violation accounting is disabled
  TCP/IP header compression is disabled
  RTP/IP header compression is disabled
  Probe proxy name replies are disabled
  Policy routing is disabled
  Network address translation is disabled
  WCCP Redirect outbound is disabled
```

```
  WCCP Redirect exclude is disabled
  BGP Policy Mapping is disabled
8540MSR#
```

If necessary, assign an IP address.

```
8540# configure terminal
8540(config)# ip address 10.0.0.1 255.255.255.0
```

Step 3 Ensure that you can connect to your TFTP server by pinging its IP address. If the TFTP server is on a different IP network, then you will need to configure the address of the default gateway for the Ethernet port's IP address.

Step−by−Step Upgrade Process

Note: This example assumes that you want to download a Cisco IOS image to the PCMCIA card in slot0 of the RPs.

Step 1 Download the Cisco IOS image for the 8540 you wish to upgrade from the Cisco Software Center Software page to your TFTP server. To download software from the software center, you must be a registered user and you must be logged in.

Step 2 Copy the Cisco IOS image from your TFTP server to the flash memory on each RP.

- Specify the device named **slot0:** to copy the image to the PC card slot0 on the primary RP.

```
8540# dir slot0:
8540# delete slot0:
8540# squeeze slot0:
8540# copy tftp ?
  atm−acct−active:  Copy to atm−acct−active: file system
  atm−acct−ready:   Copy to atm−acct−ready: file system
  bootflash:        Copy to bootflash: file system
  disk0:            Copy to disk0: file system
  disk1:            Copy to disk1: file system
  flash:            Copy to flash: file system
  ftp:              Copy to ftp: file system
  null:             Copy to null: file system
  nvram:            Copy to nvram: file system
  rcp:              Copy to rcp: file system
  rcsf:             Copy to rcsf: file system
  running−config    Update (merge with) current system configuration
  slot0:            Copy to slot0: file system
  slot1:            Copy to slot1: file system
  startup−config    Copy to startup configuration
  system:           Copy to system: file system
  tftp:             Copy to tftp: file system

8540#

8540# copy tftp slot0:
Address or name of remote host []? 10.0.0.1
Source filename []? cat8540m−wp−mz.121−6.EY.bin
Destination filename [cat8540m−wp−mz.121−6.EY.bin]?
```

- Specify the device named **sec−slot0:** to copy the image to PC card slot0 on the secondary RP.

```
8540# copy tftp sec−slot0:
Address or name of remote host [10.0.0.1]?
```

```
Source filename [cat8540m-wp-mz.121-6.EY.bin]?
Destination filename [cat8540m-wp-mz.121-6.EY.bin]?
```

Important: The only time that you specify a **sec-x** device name is when you are downloading a Cisco IOS image to the secondary RP. Each RP boots only from its own flash memory devices. The primary sees the contents of the secondary`s flash to support loading an image from your TFTP server. The secondary RP does not see the primary`s flash contents.

Note: With the current bootloader image, only the primary RP supports network booting via a TFTP server. The secondary must boot from the bootflash or from a flash card.

Step 3 Each RP uses the boot variables from the configuration in its own onboard NVRAM. The primary RP automatically synchronizes both the running and the startup configurations. Thus, the redundant RP has and uses the same boot statements (if any) as the primary. If your configuration file on the primary RP specifies an image in slot0, then the secondary RP also specifies an image in slot0 since it's using the same (synced) configuration file.

- Specify the Cisco IOS image in slot0 as the image that each RP should boot from with the following command:

```
8540(config)# boot system flash slot0:cat8540m-wp-mz.121-6.EY.bin
```

- Verify your configuration change with the **show running** and **show bootvar** commands.

```
8540# show bootvar
BOOT variable = slot0:cat8540m-wp-mz.121-6.EY.bin
CONFIG_FILE variable =
BOOTLDR variable =
Configuration register is 0x0
```

Step 4 In this example, let's assume the primary RP is in slot 4 and the secondary RP is in slot 8. When ready, soft-reset slot 4 with the **reload** command. After the reboot, execute the **show redundancy** command and confirm that the reloaded RP in slot 4 is running the image that you need. The RP in slot 8 is now the primary RP.

Step 5 When a secondary RP becomes the primary, it loads a full configuration and does not load a new version of Cisco IOS. Thus, execute the **reload** command again and force slot 8 (the new primary RP) to load the new software version. Again use the **show redundancy** command to confirm the expected results.

Frequently Asked Questions about 8540 RP Redundancy

Q. Can I load different versions of Cisco IOS on the two route processors?

A. Yes, your Catalyst 8540 can have different versions on the two RPs. However, your system must have the same image on both RPs to be considered redundant. If Cisco IOS detects a mismatch in versions, you will see log messages warning of a "conditionally redundant" system that requires a software upgrade.

Q. Which RP becomes the primary and which RP becomes the secondary after a power cycle?

A. The answer depends on whether RP switchover commands were executed before the power cycle:

1. If you did not execute the **redundancy force−failover main−cpu** command before power cycling, the RP which was primary before the power cycle will again come up as primary. The reason is that the redundancy status is saved through power on−off cycles via a master−slave register on each RP.
2. If you did execute the **redundancy force−failover main−cpu** command before power cycling, then one of the following results will happen, depending on whether the new primary (after the switchover) was reloaded:
    - ◊ If the new primary was not reloaded and you perform a power cycle just after switchover, the original primary will come up as new primary.
    - ◊ If the new primary was reloaded with the secondary still in rommon, the new primary will come up as primary after power cycle.

When the secondary RP in slot 8 becomes primary, it continues to serve as the system master, and there is no preempt command that causes the RP in slot 4 to take over again.

Related Information

- **Rebooting a Router**
- **Software Installation and Upgrade Procedure**
- **Managing Configuration Files, System Images, and Functional Images on the Catalyst 8540**
- **Configuring Redundancy and Extended High System Availability (Catalyst 8540 MSR)**
- **Upgrading Redundant Route Processors on the Catalyst 8540**
- **Technical Support &Documentation − Cisco Systems**

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