

Explanation of an Abort 1M3 (1000003)

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Introduction

This document explains the abort 1M3 (1000003) error message, as this example shows:

```
#define ADDRESS_ERROR      1000003  /* Address error      */
```

Prerequisites

Requirements

There are no specific requirements for this document.

Components Used

This document is not restricted to specific software and hardware versions.

Conventions

Refer to Cisco Technical Tips Conventions for more information on document conventions.

Abort 1M3 (1000003) Error Message

This abort is logged when the MC680x0 processor does not receive a signal from an external device such as a memory device to indicate that the data transfer has taken place. This is usually because the software specifies an invalid address (invalid because the pointer has not been initialized) or because a hardware device fails to provide the transfer acknowledge signal.

The service switching point (SSP) portion of the software error stack has this format for MC68040 processors like network processor cards (NPC) or broadband controller cards (BCC):

```
No.  Type      Number      Data(Hex)  PC(Hex)    PROC      SwRev      Date      Time
   1.  Abort    1000003      00000000  3001565C   TRNS      9.3.45     08/04/03  03:14:53

SSP 30330660 10 00 30 15 10 9A 70 08  30 32 FD C0 01 01 00 01  ..0...p.02.....
SSP 30330670 00 01 00 01 A4 22 C3 88  30 32 FD BC 00 00 00 0A  .....".02.....

      (Address error exception stack frame; p9-4 in MC68040 User's Manual)
      1000      = status register
```

```
3015 109A = program counter
7         = stack frame type (access error)
0 08     = vector offset (8 = bus error)
3032 FDC0 = effective address
0101     = special status word
0001     = writeback 3 status
0001     = writeback 2 status
0001     = writeback 1 status
A422 C388 = fault address
3032 FD8C = writeback 3 address
0000 000A = writeback 3 data
```

The most important information in this stack is the location of the abort (program counter) and the address that cannot be accessed, which is the fault address.

You can check the **Nmemmap.h** file to determine if the fault address is a valid hardware register. In this example, the address **0xA422C388** is not a valid hardware register, so the software attempts to access an invalid address. One example of a hardware failure is the failure of one of the parallel port registers to respond. The base address of PAR_PTS is 0xA0000000.

You can use the program counter to determine the location that the software attempts to access. The expected assembly instruction is to move to a memory location that an address register specifies. This might not be the instruction at the program counter because the processor reads instructions ahead of the execution of the instructions. It has a pipelined architecture.

This instruction sequence generates a 1M3 abort error when an attempt is made to read from address 1:

```
cmp.w    #1234,Abort_Now
BNE      CK_PSOS
move.l   #1,A0
move.l   (A0),D0           ;generate a bus error
```

Related Information

- [Cisco WAN Switching Solutions – Cisco Documentation](#)
- [Guide to New Names and Colors for WAN Switching Products](#)
- [Downloads – WAN Switching Software \(registered customers only\)](#)
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