Understanding MDS Congestion Counters and Commands - reference document

Contents

Introduction

This document describes the various counters and indications that apply to congestion diagnosis in current MDS platforms.

Details

Congestion related counters and descriptions for the MDS switches and modules:

- MDS 9700 –
  - 16G FC linecard - DS-X9448-768K9
  - 24/10 10G/40G FCIP linecard - DS-X9334-K9
  - 32G FC linecard - DS-X9648-1536K9
  - 64G FC linecard - DS-X9748-3072K9
- MDS 9250i Multiservice Fabric Switch
- MDS 9148S 16G Fabric switch
- MDS 9396S 16G Fabric switch
- MDS 9132T 32G Fabric switch
- MDS 9148T 32G Fabric switch
- MDS 9396T 32G Fabric switch
- MDS 9220i 32G Fabric switch
- MDS 9124V 64G Fabric switch
- MDS 9148V 64G Fabric switch
- MDS 9396V 64G Fabric switch

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Superscripts indicate linecard generation or switch type. See the list located after Table 6.

Table 1 – FC - Counters indicating delay only

Counter Name	**Description**
F16_RCM_RCP0_RBBZ_CH0[5,96S,2410] F16_RCM_RCP0_RBBZ_CH1[5,96S,2410] F16_RCM_RCP0_RBBZ_CH2[5,96S,2410] F16_RCM_RCP0_RBBZ_CH3[5,96S,2410] VIP_RCM_RBBZ_CH0_CNT [50i, 48S] F32_RCM_P8_P15_RCP_RBBZ_CH0[6,32T,48T,96T,20i] F32_RCM_P8_P15_RCP_RBBZ_CH1[6,32T,48T,96T,20i] F32_RCM_P8_P15_RCP_RBBZ_CH2[6,32T,48T,96T,20i] F32_RCM_P8_P15_RCP_RBBZ_CH3[6,32T,48T,96T,20i] F64_RCM_P0_P7_RCP_RBBZ_CH0[7,24V,48V,96V] F64_RCM_P0_P7_RCP_RBBZ_CH1[7,24V,48V,96V] F64_RCM_P0_P7_RCP_RBBZ_CH2[7,24V,48V,96V] F64_RCM_P0_P7_RCP_RBBZ_CH3[7,24V,48V,96V]	Total count of transitions to zero for R indicate that the switch is applying bac perceived congestion, and this perceiv credits being returned on an interface c There is no indication of time at zero f instant or for an extended duration of t Also shown in the output of show inter xxxx receive B2B credit transitions fro or xxxx Receive B2B credit transitions t *show interface counters* “from” was ch CSCug35184 show interface counte For F16, F32, F64, CH0 – CHx indicat R_RDY mode then only VL0(CH0) w will increment according to which VL CH0 – VL0 – This is the Control virtu CH1 – VL1 – This is the High priority CH2 – VL2 – This is the Slow device CH3 – VL3 – This is the Normal virtu Pxx_Pxx indicates the port group
F16_TMM_PORT_TBBZ_CH0[5,96S,2410] F16_TMM_PORT_TBBZ_CH1[5,96S,2410] F16_TMM_PORT_TBBZ_CH2[5,96S,2410] F16_TMM_PORT_TBBZ_CH3[5,96S,2410] VIP_TMM_TBBZ_CH0_CNT[50i, 48S]	Total count of transitions to zero for T typically the result of the attached dev due to congestion in that device. There is no indication of time at zero f instant or for an extended duration of t Also shown in the output of show inter

VIP_TMM_TBBZ_CH1_CNT[50i, 48S] F32_TMM_PORT_TBBZ_CH0[6,32T,48T,96T,20i] F32_TMM_PORT_TBBZ_CH1[6,32T,48T,96T,20i] F32_TMM_PORT_TBBZ_CH2[6,32T,48T,96T,20i] F32_TMM_PORT_TBBZ_CH3[6,32T,48T,96T,20i] F64_TMM_PORT_TBBZ_CH0[7,24V,48V,96V] F64_TMM_PORT_TBBZ_CH1[7,24V,48V,96V] F64_TMM_PORT_TBBZ_CH2[7,24V,48V,96V] F64_TMM_PORT_TBBZ_CH3[7,24V,48V,96V]	xxxx transmit B2B credit transitions fr or xxxx Transmit B2B credit transitions *show interface counters* "from" was cl CSCug35184 show interface coun For F16, F32 and F64, CH0 – CH3 inc in R_RDY mode then only VL0(CH0) they will increment according to whicl CH0 – VL0 – This is the Control virtu CH1 – VL1 – This is the High priority CH2 – VL2 – This is the Slow device CH3 – VL3 – This is the Normal virtu
F16_TMM_PORT_TWAIT_CNT[5,2410,96S] VIP_TMM_TXWAIT_CH0_CNT[50i, 48S] VIP_TMM_TXWAIT_CH1_CNT[50i, 48S] F32_TMM_PORT_TWAIT[6,32T,48T,96T,20i] F64_TMM_PORT_TWAIT[7,24V,48V,96V]	Packet is available to send, but no cred Gen5(F16): increments every clock cy 1) Port in 2/4/8/16G mode: cycle = 2.353 nanoseconds 425Mhz) 2) Port in 10G mode: Cycle = 3.14ns 320Mhz 9250i/9148s: Increments every clock c F32: increments every clock cycle 850 F64: increments every clock cycle 1.1 F16/F32/F64: To calculate actual time Seconds = Twait / clock_rate See Table 3 SNMP variable fcIfTxWa
F32_ENI_PORT_CWAIT_CH0[6,32T,48T,96T,20i] F32_ENI_PORT_CWAIT_CH1[6,32T,48T,96T,20i] F32_ENI_PORT_CWAIT_CH2[6,32T,48T,96T,20i] F32_ENI_PORT_CWAIT_CH3[6,32T,48T,96T,20i] F64_ENI_PORT_CWAIT_CH0[7,24V,48V,96V]	Packet is available to send, but no cred Count of time in 1.33ns that a specific there is a frame to send on that VL. For F32 CH0 – CH3 indicates the virt mode then the F32_TMM_PORT_TW cycle 750 Mhz (1.333 ns) for ENI.

F64_ENI_PORT_CWAIT_CH1[7,24V,48V,96V] F64_ENI_PORT_CWAIT_CH2[7,24V,48V,96V] F64_ENI_PORT_CWAIT_CH3[7,24V,48V,96V] F64_ENI_PORT_CWAIT_CH4[7,24V,48V,96V] F64_ENI_PORT_CWAIT_CH5[7,24V,48V,96V] F64_ENI_PORT_CWAIT_CH6[7,24V,48V,96V] F64_ENI_PORT_CWAIT_CH7[7,24V,48V,96V]	For F64 CH0 – CH7 indicates the virtu are in use in ER_RDY mode. If the lir F64_TMM_PORT_TWAIT counter w (0.909ns) for ENI. If the link is in ER_RDY mode then th CH0 – VL0 – This is the Control virtu CH1 – VL1 – This is the High priority CH2 – VL2 – This is the Slow device CH3 – VL3 – This is the Normal virtu
FCP_SW_CNTR_RX_WT_AVG_B2B_ZERO[5,2410,48S,50i,96S, note1] F32_MAC_KLM_CNTR_RX_WT_AVG_B2B_ZERO[6,32T,48T,96T,20i] F64_CMON_RX_WT_100MS_CH0_CNT1[7,24V,48V,96V] F64_CMON_RX_WT_100MS_CH3_TMR1_HIT[7,24V,48V,96V]	Count of the number of times an interf status typically indicates that the switc attached on that interface due to conge communicating CH0 is channel zero when the link is i CH3 is the ‘normal’ VL when the link Incremented by the software creditmon F64) incremented by HW timers.

FCP_SW_CNTR_TX_WT_AVG_B2B_ZERO[5,2410,50i,48S,96S] F32_MAC_KLM_CNTR_TX_WT_AVG_B2B_ZERO[6,32T,48T,96T,20i] F64_CMON_TX_WT_100MS_CH0_TMR1_HIT[7,24V,48V,96V] F64_CMON_TX_WT_100MS_CH3_TMR1_HIT[7,24V,48V,96V]	Count of the number of times that an i status typically indicates congestion at CH0 is channel zero when the link is i CH3 is the 'normal' VL when the link NX-OS 6.2(1) through 6.2(7) on the 9 this was incremented based on F16_FCP_INTR_TMM_P_CWAIT_F VIPER_FCP_INTR_TMM_CWAIT_ interrupts. Consequently, this only occurred once 100ms interval like in prior instances. MDS 9700, 9250i and 9148S: In NX- software creditmon process. They will port remains at 0 Tx credits. Starting w
F16_TMM_PORT_STUCK_FORCE_TIMEOUT_L_H_CNT[5,96S,note1,note3] F32_TMM_PORT_STUCK_FORCE_TIMEOUT_L_H[6,32T,48T,96T,20i,Note4] F64_TMM_PORT_STUCK_FORCE_TIMEOUT_L_H[7,24V,48V,96V]	Count of times port was at zero Tx cre threshold). NX-OS 6.2(1) through 6.2(7) on the 9 to 1s(F port)/1.5s(E port). Needs to be configured via: System timeout no-credit-drop <ms> Or in 8.1(1) and later: System timeout no-credit-drop <ms> This counter will increment even if "sy it defaults to 500ms. If no-credit-drop simply indicates the port was at zero T

	This is similar to the viper counter: VIP_TMM_STK_PRT_TO_TRANSI
F16_TMM_PORT_STUCK_FORCE_TIMEOUT_H_L_CNT[5,96S,note1] F32_TMM_PORT_STUCK_FORCE_TIMEOUT_H_L[6,32T,48T,96T,20i,Note3] F64_TMM_PORT_STUCK_FORCE_TIMEOUT_H_L[7,24V,48V,96V]	Count of times port received a credit a

F16_TMM_PORT_CWAIT_FORCE_TIMEOUT_L_H_CNT[5,2410,96S] F32_TMM_CH0_TMR1_HIT[6,32T,48T,96T,20i,Note2] F64_TMM_PORT_CWAIT_FORCE_TIMEOUT_L_H[7,24V,48V,96V]	Count of times port was at zero Tx cre NX-OS 6.2(1) through 6.2(7) on the 9 this was used to increment the FCP_S counter. Consequently, this only occurred once 100ms interval like in prior instances. In NX-OS 6.2(9) this is used for the sl Needs to be configured via: System timeout slowport-monitor <m Slowport-monitor events can be displa show process creditmon slowport-mo show logging onboard slowport-mon This is similar to the viper counter: VIP_TMM_SLO_PRT_TO_TRANSI
F16_TMM_PORT_CWAIT_FORCE_TIMEOUT_H_L_CNT[5,2410,96S] None[6,32T,48T,96T,20i] F64_TMM_PORT_CWAIT_FORCE_TIMEOUT_H_L[7,24V,48V,96V]	Count of times a credit was received a triggered.
VIP_TMM_STK_PRT_TO_TRANSITION_CH0_CNT[48S,50i,note2] VIP_TMM_STK_PRT_TO_TRANSITION_CH1_CNT[48S,50i,note2]	Count of times port was at zero Tx cre - channel 0 (high priority queue) - channel 1 (low priority queue) NX-OS 6.2(5) through 6.2(7) on the 9 to 1s(F port)/1.5s(E port).

	In NX-OS 6.2(9) the software creditm and the stuck force timout is used for ' with no action taken (no packets are dr Needs to be configured via: System timeout no-credit-drop <ms> This counter will increment even if "sy it defaults to 500ms. If no-credit-drop simply indicates the port was at zero T This is similar to the Gen5 counter F16_TMM_PORT_STUCK_FORCE_
VIP_TMM_SLO_PRT_TO_TRANSITION_CH0_CNT[48S,50i] VIP_TMM_SLO_PRT_TO_TRANSITION_CH1_CNT[48S,50i]	Count of times port was at zero Tx cre - channel 0 (high priority queue) - channel 1 (low priority queue) NX-OS 6.2(5) through 6.2(7) on the 92 FCP_SW_CNTR_TX_WT_AVG_B2I Consequently, this only occurred once 100ms interval like in prior instances. In NX-OS 6.2(9) this is used for the sl Needs to be configured via: System timeout slowport-monitor <m Slowport-monitor events can be displa show process creditmon slowport-mo show logging onboard slowport-moni This is similar to the Gen5 counter; F16_FCP_INTR_TMM_P_CWAIT_F
F64_RCM_RWAIT_CH0_CNT2[7,24V,48V,96V] F64_RCM_RWAIT_CH1_CNT2[7,24V,48V,96V] F64_RCM_RWAIT_CH2_CNT2[7,24V,48V,96V] F64_RCM_RWAIT_CH3_CNT2[7,24V,48V,96V] F64_RCM_RWAIT_CH4_CNT2[7,24V,48V,96V] F64_RCM_RWAIT_CH5_CNT2[7,24V,48V,96V]	**RxWait counters (2.5us interva Manager. As compared to TxW TWAIT, it will miss intervals o means that RxWait will always other side of the link.**

F64_RCM_RWAIT_CH6_CNT2[7,24V,48V,96V] F64_RCM_RWAIT_CH7_CNT2[7,24V,48V,96V]	

Table 2 – FC - Counters indicating frame drops

Counter Name	**Description**
F16_TMM_PORT_FRM_DROP_CNT[5,2410,96S] FCP_CNTR_TMM_NORMAL_DROP[48] VIP_TMM_NORMAL_DROP_CNT[50i, 48S, note1] VIP_TMM_TOTAL_DROP_ CNT[50i, 48S, note1] F32_TMM_PORT_FRAME_DROP[6,32T,48T,96T,20i] F64_TMM_PORT_FRAME_DROP[7,24V,48V,96V]	Number of frames dropp or np path by the Transm Manager(TMM); these d types of packet drops: tir abort drops, dummy fra egress, and so on. These counters are the ag for all the underlying cou For example for F32 this F32_TMM_PORT_ABC F32_TMM_PORT_LB_ F32_TMM_PORT_TIM F32_TMM_PORT_OFF F32_TMM_PORT_ABC F32_TMM_PORT_TO_ F32_TMM_PORT_TO_ F32_TMM_PORT_TO_ F32_TMM_PORT_TO_ F32_TMM_PORT_TO_ For F64 the list is similar

F16_TMM_TOLB_TIMEOUT_DROP_CNT[5,2410,96S] VIP_TMM_TO_DROP_CNT[50i,48S,note1,note3] F32_TMM_PORT_TIMEOUT_DROP[6,32T,48T,96T,20i] F64_TMM_PORT_TIMEOUT_DROP[7,24V,48V,96V]	Total number of Timeou includes frames timed ou congestion drop, HW stu timeout(no-credit-drop), force timeout(we don't e Congestion drop thresho *system timeout congesti* command. It is on at 500 all "modes" (port types): system timeout congestio mode e|f or system timeout congestio logical-type edge|core

F16_TMM_TOLB_LB_DROP_CNT[5,2410,96S] F32_TMM_PORT_LB_DROP[6,32T,48T,96T] F64_TMM_PORT_LB_DROP[7,24V,48V,96V]	Loopback test frames tha due to congestion. These frames. They are aggrega Fxx_TMM_PORT_FRA
F16_TMM_PORT_STUCK_FORCE_TIMEOUT_CNT[5,2410,96S] VIP_TMM_STUCK_PORT_TO_CNT [48S,50i] F32_TMM_PORT_STUCK_FORCE_TIMEOUT [6,32T,48T,96T,20i] F64_TMM_PORT_STUCK_FORCE_TIMEOUT [7,24V,48V,96V]	Total number of frames f dropped by Stuck port pr credit-drop)

VIP_TMM_TO_CNT [48S,50i,note1]	Total number of timeout congestion drop only. See VIP_TMM_STUCK_PC for the total timeout drops due t See VIP_TMM_TO_DR number of timeout drops congestion-drop and no-
F16_TMM_PORT_CWAIT_FORCE_TIMEOUT_CNT[5] VIP_TMM_SLOW_PORT_TO_CNT [48S,50i]	Total timeout packets dr slow-port-monitor proce doesn't increment since monitor feature doesn't i drop function
VIP_RHP_CNAV_DRP_CNT[48S,50i] VIP_RHP_CNAV_DROP_CNT[48S,50i,Note2] F16_RHP_CNAV_DRP_CNT [5,2410,96S] F16_RHP_CNAV_DROP_CNT [5,2410,96S,Note2]	Frame received but Cred in Ingress. These frame(dropped as CNAV_DRC ingress frame drops.

F32_RHP_CIP_CNAV_DRP_CNT [6,32T,48T,96T,20i] F32_RHP_CNAV_DROP_CNT[6,32T,48T,96T,20i,Note2] F64_RHP_CIP_CNAV_DRP_CNT [7,24V,48V,96V] F64_RHP_CNAV_DROP_CNT [7,24V,48V,96V,Note2]	
IP_FCMAC_CNT_STATS_ERRORS_RX_BAD_WORDS_FROM_DECODER [48S,50i,5,2410,96S] F32_MAC_KLM_CNTR_RX_BAD_WORDS_FROM_DECODER[6 ,32T,48T,96T,20i] F64_MAC_KLM_CNTR_RX_BAD_WORDS_FROM_DECODER [7,24V,48V,96V]	Invalid, non-decodeable, word(ITW) received. Th primitive signals, primiti parts of actual data frame

None[48S,50i,Note2] F32_MAC_KLM_CNTR_RX_FEC_UNCORRECTED_BLOCKS[6 ,32T,48T,96T,20i] F64_MAC_KLM_CNTR_RX_FEC_UNCORRECTED_BLOCKS[7,24V,48V,96V]	Number of Forward Erro Correction(FEC) blocks corrected due to bit error then passed up to the FC can result in Invalid Tran Words(ITWs), lost FC pr R_RDY) and/or CRCs if was part of an actual data FEC Is optional on 16G mandatory on 32G and h FEC_Uncorrected errors recorded in OBFL – Not In some cases these seem increments of about 33,0 Note4

IP_FCMAC_CNT_STATS_ERRORS_RX_CRC [5,2410,96S,48S,50i] IP_FCMAC_ERRORS_RX_CRC[6,7,32T,48T,96T,20i,24V,48V,96Vj]	Frames received with a b FCMAC layer.
F16_RHP_NP_RCRC [5,2410,96S] F32_RHP_NP_RCRC [6,32T,48T,96T,20i]	Total normal packets rec error or mac err that did error EOF ordered set

F64_RHP_NP_RCRC [7,24V,48V,96V]	
IP_FCMAC_CNT_STATS_ERRORS_RX_EOFA [5,2410,96S] IP_FCMAC_ERRORS_RX_EOFA [6,32T,48T,96T,20i,6,32T,48T,96T,20i]	Frames with EOF Abort FC MAC from the extern indicates the MDS actual frames with EOFa on the to the Fxx_RHP_NP_EC which is at the higher RH These errors typically me device, like a UCS Fabri detecting Ethernet CRCs forwarding them up to th interfaces as ‘stomped C Because of this, when th CRCs and also EOFA th indicate physical layer is links. They indicate phys Ethernet errors within th

F16_RHP_NP_EOFA [5,2410,96S] F32_RHP_NP_EOFA [6,32T,48T,96T,20i] F64_RHP_NP_EOFA [6,32T,48T,96T,20i]	Frame with EOF Abort r Receive Header Processo in the Fxx ASIC. Norma frame is received at the F have an EOFn (Normal). CRC does not match the frame then the frame is c will be dropped. To facil FCMAC replaces the EC EOFa (Abort). If a frame is received that also has example from a cut-throu has 'stomped' a frame, th IP_FCMAC_ERRORS_ increment *and* the Fxx_RHP_NP_EOFA co increment.
IP_FCMAC_CNT_STATS_ERRORS_RX_MAX_FRAME_TRUNCATE[5,2410,96S,48S,50i] IP_FCMAC_ERRORS_RX_MAX_FRAME_TRUNCATE	FCMAC received a fram than the 2142 (I think) m This occurs when an EO

CRC[6,7,32T,48T,96T,20i,24V,48V,96Vj]	detected. The frame will with an EOFabort so it is RHP clock.
IP_FCMAC_CNT_STATS_ERRORS_RX_MIN_FRAME_PAD[5,2410,96S,48S,50i] IP_FCMAC_ERRORS_RX_MIN_FRAME_PAD [6,7,32T,48T,96T,20i,24V,48V,96Vj]	FCMAC received a fram before the minimum num I think). The frame will b with an EOF abort so it i the RHP clock.

F16_TMM_TOLB_OFFLINE_CNT [5,2410,96S] VIP_TMM_OFFLINE_DROP_CNT [48S,50i] F32_TMM_PORT_OFFLINE [6,32T,48T,96T,20i] F64_TMM_PORT_OFFLINE_DROP [7,24V,48V,96V]	These are packets that ar interface to be transmitte can be sent the interface occurs when ports go do warning. Normally it is j at a time.

Table 3 – FC - Counters indicating action on or for an interface

Counter Name	**Description**
FCP_SW_CNTR_CREDIT_LOSS[5,2410,96S,48S,50i] F32_MAC_KLM_CNTR_CREDIT_LOSS[6,32T,48T,96T,20i] F64_CMON_CREDIT_LOSS_CH0_TMR2_HIT[7,24V,48V,96V] F64_CMON_CREDIT_LOSS_CH3_TMR2_HIT[7,24V,48V,96V]	Count of the number of times that creditmon credit l recovery has been invoked on a port This is set to 1 full second on F ports and 1.5 second ports. CH0 is channel zero when the link is in R_RDY mo CH3 is the ‘normal’ VL when the link is in ER_RD

FCP_SW_CNTR_FORCE_TIMEOUT_ON[5,50i,48S,note2]	Count of the number of times the "system timeout n drop threshold" has been reached by this port; when zero Tx B2B credits for the time specified, the port drop packets at line rate Note 1: For the 9700 and 9250i these counters will increment prior to the introduction of the HW slow feature in 6.2(9). Since the 9148S was first supporte OS 6.2(9) it will never have it increment. Reference F16_TMM_PORT_STUCK_FORCE_TIMEOUT_ and VIP_TMM_STK_PRT_TO_TRANSITION_CH0_ counters which indicate the same thing (but are not
FCP_SW_CNTR_FORCE_TIMEOUT_OFF[5,50i,96S,48s,note 2]	Count of the number of times that the port has recov the system timeout no-credit-drop condition; this sta typically means that R_Rdy primitive has been retu possibly that an LR and LRR even has occurred. Note 1: For the 9700 and 9250i these counters will

	increment prior to the introduction of the HW slow feature in 6.2(9). Since the 9148S was first supporte OS 6.2(9) they will never increment. They are re-ad hardware internal statistics and logging onboard err bug CSCus93140: CSCus93140 no-credit-drop SW counters not inc on MDS 9700, 9250i, 9148S F16_TMM_PORT_STUCK_FORCE_TIMEOUT_ indicates the same thing.
FCP_SW_CNTR_LINK_RESET_OUT[5,2410,96S,50i,48S, note 1] F32_MAC_KLM_CNTR_LINK_RESET_OUT[6,32T,48T,96T,20i] F64_MAC_KLM_CNTR_LINK_RESET_OUT[7,24V,48V,96V]	Count of times a Link Credit Reset(LR) was transm the interface. This occurs during credit loss recovery Also shown in the output of “show interface counte as: “Tx Link Reset(LR) while link is active” Note: Link Resets that are transmitted are only cou the link is active.

FCP_SW_CNTR_LINK_RESET_IN[5,2410,96S,50i,48S,Note 1] F32_MAC_KLM_CNTR_LINK_RESET_IN[6,32T,48T,96T,20i] F64_MAC_KLM_CNTR_LINK_RESET_IN[7,24V,48V,96V]	Count of times a Link Credit Reset(LR) was receive interface. Note 1: These are not incremented. Also shown in the output of “show interface counte as: “Rx Link Reset(LR) while link is active” Note: Link Resets that are received are only counte link is active.

FCP_SW_CNTR_LRR_OUT[5,48,50i,48S,Note1] F32_MAC_KLM_CNTR_LRR_OUT[6,32T,48T,96T,20i] F64_MAC_KLM_CNTR_LRR_OUT[7,24V,48V,96V]	Count of times a Link Credit Reset Response(LRR) transmitted from the interface.
FCP_SW_CNTR_LRR_IN[5,48,50i,48S,Note1] F32_MAC_KLM_CNTR_LRR_IN[6,32T,48T,96T,20i] F64_MAC_KLM_CNTR_LRR_IN[7,24V8V,96V]	Count of times a Link Credit Reset Response(LRR) received on the interface.

FCP_SW_CNTR_OLS_OUT[5,48,60i,48S,Note1] F32_MAC_KLM_CNTR_OLS_OUT[6,32T,48T,96T,20i] F64_MAC_KLM_CNTR_OLS_OUT[7,24V,48V,96V]	Count of times an Off Line Sequence(OLS) was tra from the interface.

FCP_SW_CNTR_OLS_IN[5,48,50i,48S,Note1] F32_MAC_KLM_CNTR_OLS_IN[6,32T,48T,96T,20i] F64_MAC_KLM_CNTR_OLS_IN[7,24V,48V,96V]	Count of times an Off Line Sequence(OLS) was rec the interface.

FCP_SW_CNTR_NOS_OUT[5,48,50i,48S,Note1] F32_MAC_KLM_CNTR_NOS_OUT[6,32T,48T,96T,20i] F64_MAC_KLM_CNTR_NOS_OUT[7,24V,48V,96V]	Count of times an Not Operational Sequence(NOS) transmitted from the interface.
FCP_SW_CNTR_NOS_IN[5,48,50i,48S,Note1] F32_MAC_KLM_CNTR_NOS_IN[6,32T,48T,96T,20i] F64_MAC_KLM_CNTR_NOS_IN[7,24V,48V,96V]	Count of times an Not Operational Sequence(NOS) received on the interface.

Table 4 – FC - Counters representing normal flow

Counter Name	Description	Command
F16_TMM_CH_CNT_CH0[5,2410,96S] F16_TMM_CH_CNT_CH1[5,2410,96S] F16_TMM_CH_CNT_CH2[5,2410,96S] F16_TMM_CH_CNT_CH3[5,2410,96S] F32_TMM_PORT_CH0_TX_NP[6,32T,48T,96T,20i] F32_TMM_PORT_CH1_TX_NP[6,32T,48T,96T,20i] F32_TMM_PORT_CH2_TX_NP[6,32T,48T,96T,20i]	Total transmitted frame counts on CHx (or VLx). For F16 and F32 CH0 – CH3 indicates the virtual channel or virtual link. If the link is in	**Sup Hard** None (not **Sup Hard** show hard module-all 5,2410,6,7,N

F32_TMM_PORT_CH3_TX_NP[6,32T,48T,96T,20i] F64_TMM_PORT_CH0_TX_NP[7,24V,48V,96V] F64_TMM_PORT_CH1_TX_NP[7,24V,48V,96V] F64_TMM_PORT_CH2_TX_NP[7,24V,48V,96V] F64_TMM_PORT_CH3_TX_NP[7,24V,48V,96V]	R_RDY mode then only VL0(CH0) will be used. If the link is in ER_RDY mode then they will increment according to which VL it is occurring on. Specifically: CH0 – VL0 – This is the Control virtual link CH1 – VL1 – This is the High priority virtual link (currently not used) CH2 – VL2 – This is the Slow device virtual link CH3 – VL3 – This is the Normal virtual link	show hard | all> all < **Linecard** None (not **Linecard** show hard all <port x>[5,2410,96
F16_RHP_NP_TOTRG_CH0[5,96S] F16_RHP_NP_TOTRG_CH1[5,96S] F16_RHP_NP_TOTRG_CH2[5,96S] F16_RHP_NP_TOTRG_CH3[5,96S] F32_RHP_NP_TOTRG_CH0[6] F32_RHP_NP_TOTRG_CH1[6] F32_RHP_NP_TOTRG_CH2[6] F32_RHP_NP_TOTRG_CH3[6] F64_RHP_NP_TOTRG_CH0[7,24V,48V,96V] F64_RHP_NP_TOTRG_CH1[7,24V,48V,96V]	Total received frame counts on CHx (or VLx). CH0 – CH3 indicates the virtual channel or virtual link. If the link is in R_RDY mode then only VL0(CH0)	**Sup Hard** None (not **Sup Hard** show hard module-all 5,2410,6,7,N show hard | all> all <

F64_RHP_NP_TOTRG_CH2[7,24V,48V,96V] F64_RHP_NP_TOTRG_CH3[7,24V,48V,96V]	will be used. If the link is in ER_RDY mode then they will increment according to which VL it is occurring on. Specifically: CH0 – VL0 – This is the Control virtual link CH1 – VL1 – This is the High priority virtual link (currently not used) CH2 – VL2 – This is the Slow device virtual link CH3 – VL3 – This is the Normal virtual link	**Linecard** None (not **Linecard** show hard all <port x>[5,2410,96
VIP_RHP_FRM_CNT[48S,50i]	Total received frame counts	**Sup Hard** None (not **Sup Hard** show hard module-all [5,2410,6,7,N show hard | all> all < **Linecard**

		None (not **Linecard** show hard all <port x>5,2410,96
VIP_TMM_CH0_CNT48S,50i	Total transmitted frame counts	**Sup Hard** None **Sup Hard** show hard | all> all < **Linecard** None (not **Linecard** show hard all <port x>5,2410,96
IP_FCMAC_CNT_STATS_CREDIT_IG_XG_MUX_SEND48S,50i, 5,2410,96S IP_FCMAC_CREDIT_IG_XG_MUX_SEND_RRDY_REQ6,32T,48T,96T,20i,7,24V,48V,96V	Count of RRDYs sent out by the port to the peer. Ideally equal to the TOTAL_RX frame count.	**Sup Hard** None (not **Sup Hard** show hard module-all 5,2410,6,7,N

		show hard | all> all < 96S,48S,50i, **Linecard** None (not **Linecard** show hard all <port x>5,2410,96
IP_FCMAC_CNT_STATS_CREDIT_EG_DEC_RRDY48S,50i, 5,2410,96S IP_FCMAC_CREDIT_EG_DEC_RRDY6,32T,48T,96T,20i,7,24V,48V,96V	Count of RRDYs received by the port from the peer. Ideally be equal to the TOTAL_TX frame count.	**Sup Hard** None (not **Sup Hard** show hard module-all 5,2410,6,7,N show hard | all> all < 96S,48S,50i, **Linecard** None (not **Linecard** show hard all <port x>5,2410,96

Table 5 – FC - SNMP variables applicable to congestion

Counter Name	**Description**

fcIfTxWaitCount[5,note1] fcIfTxWaitCount[50i,48S,note2] fcIfTxWaitCount[2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V	OID 1.3.6.1.4.1.9.9.289.1.2.1.1.15 The number of times the FC-port w due to lack of transmit credits **and** were packets queued for transmit. units of 2.5us. To calculate seconds user: txwait * /1000000 There is no OID for the Rx directio Not generated by port-monitor Based on the counters: F16_TMM_PORT_TWAIT_CNT[5] VIP_TMM_TXWAIT_CH0_CNT[5] VIP_TMM_TXWAIT_CH1_CNT[5] F32_TMM_PORT_TWAIT RRDY[6,32T,48T,96T,20i] F64_TMM_PORT_TWAIT[7,24V,4
fcIfRxWaitCount[6,24V,48V,96V,Note1]	OID 1.3.6.1.4.1.9.9.289.1.2.1.1.48 The amount of time in 2.5us (micro intervals that the interface was at 0 credits remaining. This indicates th switchport was preventing further i frames for a time. Unlike TxWait, which uses the mu granular than 2.5us, underlying TW counter, RxWait will only increme the duration of time is 2.5us or lon Small durations of 0 Rx B2B credi remaining will not be counted. Thi that TxWait on the adjacent side w

	always be a better measure if it is a Not currently used by port-monitor Only available on 64G capable inte
fcIfCreditLoss[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	OID 1.3.6.1.4.1.9.9.289.1.2.1.1.37 The number of link resets that have occurred due to unavailable credits from the peer side of the lin
fcIfLinkResetOuts[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	OID 1.3.6.1.4.1.9.9.289.1.2.1.1.10 The number of link reset protocol e issued by the FC-Port to the attached FC-Por
fcIfLinkResetIns[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	OID 1.3.6.1.4.1.9.9.289.1.2.1.1.9 The number of link reset protocol e received by the FC-Port from the a FC-port
fcIfTimeOutDiscards[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	OID 1.3.6.1.4.1.9.9.289.1.2.1.1.35 The number of packets that are dro to time-out at the FC-port or due to port going offline.
fcIfOutDiscards[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	OID 1.3.6.1.4.1.9.9.289.1.2.1.1.36 The total number of packets that ar discarded in the egress side of the I This is an aggregate counter compr several types of drops.
fcIfTxWtAvgBBCreditTransitionToZero[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	OID 1.3.6.1.4.1.9.9.289.1.2.1.1.38 Count of the number of times that a interface was at zero Tx B2B credi 100 ms. This status typically indica congestion at the device attached o interface.

fcIfBBCreditTransistionFromZero[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	OID 1.3.6.1.4.1.9.9.289.1.2.1.1.28 Increments if the transmit B2B cre zero There is no indication of time at ze this counter. It could stay at zero fo instant or for an extended duration Also shown in the output of show i counters: xxxx Transmit B2B credit transitio zero
fcHCIfBBCreditTransistionFromZero[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	OID 1.3.6.1.4.1.9.9.289.1.2.1.1.40 Increments if the transmit B2B cre zero There is no indication of time at ze this counter. It could stay at zero fo instant or for an extended duration Also shown in the output of show i counters: xxxx Transmit B2B credit transitio zero
fcIfBBCreditTransistionToZero[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	OID 1.3.6.1.4.1.9.9.289.1.2.1.1.39 Increments if the receive B2B cred There is no indication of time at ze this counter. It could stay at zero fo instant or for an extended duration Also shown in the output of show i counters: xxxx Receive B2B credit transition
fcHCIfBBCreditTransistionToZero[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	OID 1.3.6.1.4.1.9.9.289.1.2.1.1.41 Increments if the receive B2B cred

	There is no indication of time at ze this counter. It could stay at zero fo instant or for an extended duration Also shown in the output of show i counters: xxxx Receive B2B credit transition

Table 6 – FC – Interrupts related to congestion

Counter Name	**Description**
F16_FCP_INTR_TMM_P_CWAIT_FORCE_TIMEOUT_L_H[5,2410]	Slowport conditio High transition: T threshold) NX-OS 6.2(1) thr port was at zero T increments on the these “pre-slowpo counter was used FCP_SW_CNTR counter incremen NX-OS 6.2(9) an
F16_FCP_INTR_TMM_P_CWAIT_FORCE_TIMEOUT_H_L[5,2410]	Slowport conditio transition: ie cred NX-OS 6.2(1) thr port received a cr credits for 100ms slowport-monitor used to re-arm the FCP_SW_CNTR counter incremen NX-OS 6.2(9) an
F16_FCP_INTR_TMM_P_STUCK_FORCE_TIMEOUT_L_H[5,2410]	Stuck port condit High transition.

	Configured via: “system timeout s mode|f” Defaults to 500m
F16_FCP_INTR_TMM_P_STUCK_FORCE_TIMEOUT_H_L[5,2410]	Count of times st
VIPER_FCP_INTR_TMM_CWAIT_AVG_LIVE_CH0_OVER_THRESHOLD_RAISING[48s,50i] VIPER_FCP_INTR_TMM_CWAIT_AVG_LIVE_CH1_OVER_THRESHOLD_RAISING[48s,50i]	Slowport conditio High transition: T threshold) NX-OS 6.2(5) thr port was at zero T increments on the these “pre-slowpo counter was used FCP_SW_CNTR counter incremen NX-OS 6.2(9) an
VIPER_FCP_INTR_TMM_CWAIT_AVG_LIVE_CH0_OVER_THRESHOLD_FALLING[48s,50i] VIPER_FCP_INTR_TMM_CWAIT_AVG_LIVE_CH1_OVER_THRESHOLD_FALLING[48s,50i]	Slowport conditio
VIPER_FCP_INTR_TMM_STUCK_PORT_TIMEOUT_CH0_RAISING[48s,50i] VIPER_FCP_INTR_TMM_STUCK_PORT_TIMEOUT_CH1_RAISING[48s,50i]	Count of times po the stuck port tim (default value 500 NX-OS 6.2(5) thr port was at zero T 1.5s(E port). In th

	releases this inter FCP_SW_CNTF increment. NX-OS 6.2(9) an
VIPER_FCP_INTR_TMM_STUCK_PORT_TIMEOUT_CH0_FALLING[48s,50i] VIPER_FCP_INTR_TMM_STUCK_PORT_TIMEOUT_CH1_FALLING[48s,50i]	Count of times st
IP_FCMAC_INTR_PRIM_RX_SEQ_NOS[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	Not Operational S interface. NOS is a primitiv continuously unti
IP_FCMAC_INTR_PRIM_RX_SEQ_OLS[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	Off Line Sequenc OLS is a sequenc continuously unti
IP_FCMAC_INTR_PRIM_RX_SEQ_LR[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	Link Reset receiv sent under two co 1) Link bringu

	2) Credit Loss bring each side u B2B credits. This link but just resto
IP_FCMAC_INTR_PRIM_RX_SEQ_LRR[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	Link Reset receiv sent in response t
IP_FCMAC_INTR_ERR_BB_SCR_INCREMENT [5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	Credit recovery a This interrupt cou the port detected BB_SCr checkpo accounting by int B2B credit count many credits wer Defined in FC-FS **17.4.9 BB_Credi** Note: BBSCN is ports that is enabl Interface fcx/y no switchport fcb NX-OS 8.2(1) ad NX-OS 8.4(1) ad On NX-OS 8.4(1 shows this: B2B State Chang

	Negotiated Value Does not function ER_RDY mode.
IP_FCMAC_INTR_ERR_BB_SCS_RESEND[5,2410,6,96S,32T,48T,96T,20i,7,24V,48V,96V]	Credit recovery a (SOF corruption) This interrupt cou the port detected BB_SCs checkpo ports credit accou R_RDY(s) to the number of frame(the actual numbe Defined in FC-FS **17.4.9 BB_Credi** Note: BBSCN is ports that is enabl Interface fcx/y no switchport fcb NX-OS 8.2(1) ad NX-OS 8.4(1) ad On NX-OS 8.4(1 shows this: B2B State Chang Negotiated Value Does not function ER_RDY mode.

F32_FCP_INTR_RCM_PORTxx_CH0_SLOW_STUCK1 [6,32T,48T,96T]	In R_RDY mode Increments fcIfRxWtAvgBB This is the 100ms In ER_RDY mod Increments chann zero Port number is th F64 ASIC as seen fcmac drv-info`.
F64_FCP_INTR_TMM4_Px_CH0_TMR2_THR	Increments fcIfCr In R_RDY mode Indicates the cred 1 second(F) or 1.5 Credit-loss-recov In ER_RDY mod Indicates the cred 1 second or 1.5 se channel 0 (VL0). Port number is th F64 ASIC as seen fcmac drv-info`.

Superscripts:

[5]: Cisco MDS 9706/9710/9718 DS-X9448-768K9 module

[2410]: Cisco MDS 9700 – FC/FCIP 24/10 DS-X9334-K9 module

[6]: Cisco MDS 9706/9710/9718 DS-X9648-1536K9 module

[7]: Cisco MDS 9706/9710/9718 DS-X9748-3072K9 module

50i: Cisco MDS 9250i

48S: Cisco MDS 9148s

96S: Cisco MDS 9396s

32T: Cisco MDS 9132T

48T: Cisco MDS 9148T

96T: Cisco MDS 9396T

20i: Cisco MDS 9220i

24V: Cisco MDS 9124V

48V: Cisco MDS 9148V

96V: Cisco MDS 9396V

F16: F16 (Generation 5 ASIC)

VIP: Viper ASIC for MDS 9250i and 9148S

F32: F32 (Generation 6 ASIC)

F64: F64 (Generation 7 ASIC)

Flanker – N7K F3/MDS 40G FCoE ASIC

RI: Request Interface

TMM: Transmit Memory Manager

FCP_SW: These indicate software counters

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