

# High-Speed Serial Interface (HSSI) Design Specification

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## Introduction

This document specifies the physical layer interface that exists between a DTE such as a high speed router or similar data device and a DCE such as a DS3 (44.736 Mbps) or SONET STS-1 (51.84 Mbps) DSU.

## Prerequisites

## Requirements

There are no specific requirements for this document.

## Components Used

This document is not restricted to specific software and hardware versions.

## Conventions

Refer to Cisco Technical Tips Conventions for more information on document conventions.

## Notice and Authors

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### Joint Authors

John T. Chapman  
cisco Systems, Inc.  
1525 O'Brien Drive  
Menlo Park, Ca 94025

jchapman@cisco.com  
TEL: (415) 688-7651

Mitri Halabi T3plus Networking, Inc. mitri@t3plus.com 2840 San Tomas Expressway TEL: (408) 727-4545  
Santa Clara, Ca, 95051 FAX: (408) 727-5151

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## HSSI Addendum Issue 1

This is a set of 3 addenda to the HSSI specification to document additions and clarifications to the HSSI specification since the 2.11 release and to enhance the operating and diagnostic capabilities for the Data Circuit-Terminating Equipment (DCEs) and Data Service Units (DSUs).

### Addendum #1

Delete all references to "clock must be maintained for n cycles after the last valid data." This is consistent with HSSI being a layer 1 specification, and therefore having no knowledge of data validity.

Replace with the following phrasing:

"To facilitate various bit/byte/frame DCE multiplexor implementations, the clock may be gapped to allow the deletion of framing pulses and to allow bandwidth limiting of the HSSI.

The maximum gapping interval is not specified. However, the clock sources ST and RT are expected to be generally continuous when both TA and CA are asserted. A gapping interval is measured as the amount of time between two consecutive clock edges of the same slope.

The instantaneous data transfer rate must never exceed 52 Mbps."

## **Addendum #2**

1.5 kohm resistors are to be used instead of 10 kohm resistor for pullup and pull down functions on all receivers. This allows the proper 150 mvolts minimum to be developed across the 110 ohms terminating resistors.

## **Addendum #3**

An optional signal, LC, has been added from the DCE to the Data Terminal Equipment (DTE) on the reserved signal pair pins 5 (+) & 30 (-). LC is a loopback request signal from the DCE to DTE, to request that the DTE provide a loopback path to the DCE. More specifically, the DTE would set TT=RT and SD=RD. ST would not be used, and could not be relied upon as a valid clock source under these circumstances.

This would then allow the DCE/DSU network management diagnostics to test the DCE/DTE interface independent of the DTE. This follows the HSSI philosophy that both the DCE and the DTE are intelligent independent peers, and that the DCE is capable of and responsible for maintaining its own data communications channel.

In the event that both the DTE and DCE asserted loopback requests, the DTE will be given preference.

# **1.0 Intended Usage**

This document specifies the physical layer interface that exists between a DTE such as a high speed router or similar data device and a DCE such as a DS3 (44.736 Mbps) or SONET STS-1 (51.84 Mbps) DSU. Future extensions to this specification may include support for rates up to SONET STS-3 (155.52 Mbps).

## **1.1 Document Organization**

Section 1 introduces HSSI and relates it to other specifications. Section 2 contains a list of the terms and definitions used in this specification. Section 3 defines the electrical specifications, including signal names, definitions, characteristics, operation, and timing. Section 4 describes the physical properties including connector types, cable types, and pin assignments. Appendix A graphically relates timing relationships. Appendix B graphically defines polarity conventions. Appendix C has a detailed analysis of ECL noise immunity.

## **1.2 Comparison to Existing Standards**

With respect to the ANSI/EIA series of standards, EIA-232-D, EIA-422-A, EIA-423-A, EIA-449, and EIA-530, this specification is distinct in that it:

- supports serial bit rates up to 52 Mbps

- uses Emitter Coupled Logic (ECL) transmission levels
- allows the timing signals to be gapped, i.e., discontinuous
- uses a simplified control signal protocol
- uses a more detailed loopback signal protocol
- uses a different connector

## 2.0 Terms and Definitions

This specification adheres to the following definitions:

### **Analog Loopback:**

A loopback in either direction that is associated with the line side of a DCE.

### **Assertion:**

The (+side) of a given signal will be at potential  $V_{oh}$  while the (–side) of the same signal will be at potential  $V_{ol}$ . (ref: section 3.2 and Appendix B)

### **Deassertion:**

The (+side) of a given signal will be at potential  $V_{ol}$  while the (–side) of the same signal will be at potential  $V_{oh}$ .

### **Data Communications Channel:**

The transmission media and intervening equipment involved in the transfer of information between DCEs. In this specification, the data communications channel is assumed to be full duplex.

### **DCE:**

Data Communications Equipment. The devices and connections of a communications network which connect the data communications channel with the end device (DTE). This will be used to describe the CSU/DSU.

### **Digital Loopback:**

A loopback in either direction that is associated with the DTE port of a DCE.

### **DS3:**

Digital Signal level 3. Also known as T3. Equivalent in bandwidth to 28 T1's. The bit rate is 44.736 Mbps.

### **DSU:**

Data Service Unit. Provides a DTE with access to digital telecommunications facilities.

### **DTE:**

Data Terminal Equipment. The part of a data station that serves as a data source, destination, or both and that provides for the data communications control function according to protocols. This will be used to describe a router or similar device.

### **Gapped Clock:**

A clock stream at a nominal bit rate which may be missing clock pulses at arbitrary intervals for arbitrary lengths of time.

**OC-N:**

The optical signal that results from an optical conversion of an STS-N signal.

**SONET:**

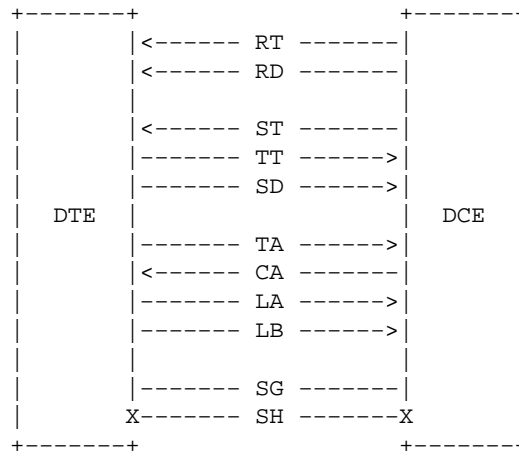
Synchronous Optical NETWORK. An ANSI/CCITT standard for standardizing the use of optical communication systems.

**STS-N:**

Synchronous Transport Signal level n, where n = 1,3,9,12,18,24,36,48. STS-1 is the basic logical building block signal for SONET with a rate of 51.84 Mbps. STS-N are obtained by byte interleaving N STS-1 signals together with a rate of N times 51.84 Mbps.

### 3.0 Electrical Specification

#### 3.1 Signal Definitions



**RT: Receive Timing**

**Direction: from DCE**

RT is a gapped clock with a maximum bit rate of 52 Mbps, and provides receive signal element timing information for RD.

**RD: Receive Data**

**Direction: from DCE**

The data signals generated by the DCE, in response to data channel line signals received from a remote data station, are transferred on this circuit to the DTE. RD is synchronous with RT.

**ST: Send Timing**

**Direction: from DCE**

ST is a gapped clock with a maximum bit rate of 52 Mbps, and provides transmit signal element timing information to the DTE.

**TT: Terminal Timing****Direction: to DCE**

TT provides transmit signal element timing information to the DCE. TT is the ST signal echoed back to the DCE by the DTE. TT should be buffered by the DTE only, and not gated with any other signal.

**SD: Send Data****Direction: to DCE**

The data signals originated by the DTE, to be transmitted via the data channel to a far end data station. SD is synchronous with TT.

**TA: data Terminal equipment Available****Direction: to DCE**

TA will be asserted by the DTE, independently of CA, when the DTE is prepared to both send and receive data to and from the DCE. Data transmission should not commence until CA has also been asserted by the DCE.

If the data communications channel requires a keep alive data pattern when the DTE is disconnected, then the DCE shall supply this pattern while TA is deasserted.

**CA: data Communications equipment Available****Direction: from DCE**

CA will be asserted by the DCE, independently of TA, when the DCE is prepared to both send and receive data to and from the DTE. This indicates that the DCE has obtained a valid data communications channel. Data transmission should not commence until TA has also been asserted by the DTE.

**LA: Loopback circuit A****LB: Loopback circuit B****Direction: to DCE**

LA and LB are asserted by the DTE to cause the DCE and its associated data communications channel to provide one of three diagnostic loopback modes. Specifically,

- LB = 0, LA = 0: no loopback
- LB = 1, LA = 1: local DTE loopback
- LB = 0, LA = 1: local line loopback
- LB = 1, LA = 0: remote line loopback

A 1 represents assertion, and a 0 represents deassertion.

A local DTE (digital) loopback occurs at the DTE port of the DCE and is used to test the link between the DTE and DCE. A local line (analog) loopback occurs at the line side port of the DCE and is used to test the DCE functionality. A remote line (analog) loopback occurs at the line port of the remote DCE and is used to test the functionality of the data communications channel. These three loopbacks are initiated in this sequence. The remote DCE is tested by remotely commanding its local loopbacks. Note that LA and LB are direct supersets of the EIA signals LL (Local Loopback) and RL (Remote Loopback).

The local DCE continues to assert CA during all three loopback modes. The remote DCE will deassert CA when remote loopback is in effect. If the remote DCE can detect a local loopback at the local DCE, the remote DCE will deassert its CA; otherwise, the remote DCE will assert its CA when there is a local loopback at the local DCE.

The DCE implements the loopback towards the commanding DTE only. Receive data from the data communications channel is ignored. Send data to the data communications channel is filled with either the commanding DTE's send data stream or with a keep alive data pattern, depending upon the data communications channel's specific requirements.

There is no explicit hardware status signal to indicate that the DCE has entered a loopback mode. The DTE waits for an appropriate amount of time after asserting LA and LB before assuming the loopback to be valid. The appropriate amount of time is application dependent and is not a part of this specification.

The loopback mode applies to both timing and data signals. Thus, on the DTE – DCE link, the same timing signal could traverse the link three times, first as ST, then as TT, and finally as RT.

### **SG: Signal Ground**

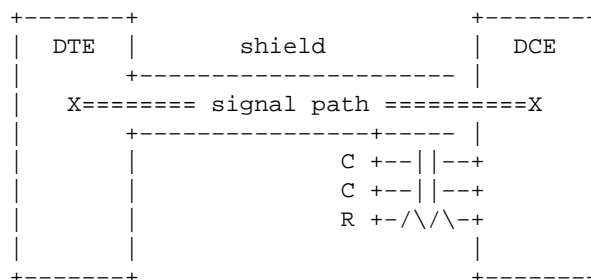
#### **Direction: Not Applicable**

SG signifies a connection to circuit ground at both ends. SG ensures that the transmit signal levels stay within the common mode input range of the receivers.

### **SH: Shield**

#### **Direction: Not Applicable**

The shield encapsulates the cable for EMI purposes, and is not implicitly intended to carry signal return currents. The shield is connected to DTE frame ground directly and may choose one of two options at the DCE frame ground. The first option is to connect the shield to DCE frame ground directly. The second option is to connect the shield to DCE frame ground through a parallel combination of a 470 ohm, +/- 10%, 1/2 watt resistor, 0.1 uF, +/- 10%, 50 volt, monolithic ceramic capacitor, and a 0.01 uF, +/- 10%, 50 volt, monolithic ceramic capacitor. This is shown below:



The R-C-C network should be located as close to the shield/chassis junction as possible. Because the shield is terminated directly to the DTE and DCE chassis, the shield is not given a pin assignment within the

connector. Shield continuity between connecting cables is maintained by the connector housing.

## 3.2 Electrical Characteristics

All signals are balanced, differentially driven, and received at standard ECL levels. The ECL negative supply voltage, V<sub>ee</sub>, may be either -5.2 V<sub>dc</sub> +/- 10% or -5.0 V<sub>dc</sub> +/- 10% at either end. Rise times and fall times are measured from 20% to 80% threshold levels.

### TRANSMITTER:

driver type:	ECL 10KH with differential outputs (MC10H109, MC10H124 or equivalent)			
signal levels:	minimum	typical	maximum	
V <sub>oh</sub> :	-1.02	-0.90	-0.73	V <sub>dc</sub>
V <sub>ol</sub> :	-1.96	-1.75	-1.59	V <sub>dc</sub>
V <sub>diff</sub> :	0.59	0.85	1.21	V <sub>dc</sub>
trise:	0.50	-	2.30	ns
t <sub>fall</sub> :	0.50	-	2.30	ns
transmission rate:	52 Mbps maximum			
signal type:	electrically balanced with Non Return to Zero (NRZ) encoding.			
termination:	330 ohms low inductance resistance from each side to V <sub>ee</sub> .			

### RECEIVER:

receiver type:	ECL 10KH differential line receiver (MC10H115, MC10H116, MC10H125, or equivalent)		
termination:	110 ohms (carbon composition) differential, 5 Kohms common-mode (optional)		
min. signal level:	150 mvolts peak-to-peak differential		
max. signal level:	1.0 volt peak-to-peak differential		
common mode input range:	-2.85 volts to -0.8 volts (-0.5 volts max)		

Values apply over an ambient temperature range of 0 to 75 degrees Celcius and have been adjusted for the broader V<sub>ee</sub> range.

## 3.3 Fail Safe Operation

In the event that the interface cable is not present, the differential ECL receivers must default to a known state. To guarantee this, it is necessary when using the 10H115 or 10H116 to add a 10 kohm, +/-1%, pull-up resistor to the (-side) of the receiver and a 10 kohm, +/-1%, pull-down resistor to the (+side) of the receiver. This will create a longitudinal termination of 5 kilohms. The default state of all interface signals is deasserted.

It is not necessary to use external resistors when using the 10H125, since it has an internal bias network that will force an output low state when the inputs are left floating.

The interface must not be damaged by an open circuit or short circuit connection on any combination of pins.

## 3.4 Timing

Source timing is defined as timing waveforms generated at a transmitter. Destination timing is defined as timing waveforms incident at a receiver. Pulse widths are measured between 50% points of the final pulse amplitude. The leading edge of the timing pulse shall be defined as the boundary between deassertion and assertion. The trailing edge of the timing pulse shall be defined as the boundary between assertion and deassertion. RT, TT, and ST minimum positive source timing pulse width shall be 7.7 ns. This allows a source duty cycle tolerance of +/- 10%. This value is obtained from:

$$10\% = ((9.61 \text{ ns} - 7.7 \text{ ns}) / 19.23 \text{ ns}) \times 100\%$$

where:

$$19.23 \text{ ns} = 1 / (52 \text{ Mbps})$$



$$9.61 \text{ ns} = 19.23 \text{ ns} * 1/2 \text{ cycle}$$

Data will change to its new state within +/- 3 ns of the leading edge of the source timing pulse.

RT, TT, and ST minimum positive destination timing pulse width shall be 6.7 ns. Data will change to its new state within +/- 5 ns of the leading edge of the destination timing pulse. These numbers allow for transmission distortion elements of 1.0 ns of pulse width distortion and 2.0 ns of clock to data skew. This leaves 1.7 ns for receiver setup time.

The data will be considered valid on the trailing edge. Thus, transmitters clock data out on the leading edge, and receivers clock data in on the trailing edge. This allows an acceptance window for clock-data skew error.

The delay from the ST port to the TT port within the DTE shall be less than 25 ns. The DCE must be able to tolerate a delay of at least 100 ns between its ST port and its TT port. This allows for a 75 ns delay for 15 meters of cable.

RT and ST may be gapped. In the event they become disabled by the DCE, RT disabling must not occur until 23 clock pulses after the last valid data on RD, and ST disabling must not occur until 1 clock pulse after the last valid data on SD. The definition of valid data is application dependent and not a subject of this specification.

CA and TA are asynchronous of each other. Upon assertion of CA, the signals ST, RT, and RD will not be considered valid for at least 40 ns. Upon the assertion of TA, the signals TT and SD will not be considered valid for at least 40 ns. This is intended to allow the receiving end sufficient setup time.

TA should not be deasserted until at least one clock pulse after the last valid data bit on SD has been transmitted. This does not apply to CA since the data is transparent to the DCE.

## 4.0 Physical Specification

The cable connecting the DCE and DTE consists of 25 twisted pairs with an overall foil/braid shield. The cable connectors are both male connectors. The DTE and DCE have female receptacles. Dimensions are given in meters (m) and feet (ft).

### 4.1 Physical

cable type:	multi-conductor cable, consisting of 25 twisted pairs cabled together with an overall double shield and PVC jacket
gauge:	28 AWG, 7 strands of 36 AWG, tinned annealed copper, nominal 0.015 in. diameter
insulation:	polyethylene or polypropylene; 0.24 mm, .0095 in. nominal wall thickness; 0.86 mm +/- 0.025 mm, .034 in. +/- 0.001 in. outside diameter
foil shield:	0.051 mm, 0.002 in. nominal aluminum/polyester/aluminum laminated tape spiral wrapped around the cable core with a 25% minimum overlap
braid shield:	braided 36 AWG, tinned plated copper in accordance with 80% minimum coverage
jacket:	75 degrees C flexible polyvinylchloride
jacket wall:	0.51 mm, 0.020 in. minimum thickness
dielectric strength:	1000 VAC for 1 minute
outside diameter:	10.41 mm +/- 0.18 mm, 0.405 in. +/- 0.015 in.
agency compliance:	CL2, UL Subject 13, NEC 725-51(c) + 53(e)
manufacturer p/n:	QUINTEC (Madison Cable 4084) ICONTEC RTF-40-25P-2 (Berk-tek, C&M)

## 4.2 Electrical

maximum length:	15 m	50 ft	
nominal length:	2 m	6 ft	
maximum DCR at 20 C:	23 ohms/km	70 ohms/1000ft	
differential impedance at 50 MHz:			
nominal: (95% or more pairs)	110 ohms	(+/- 11 ohms)	
maximum:	110 ohms	(+/- 15 ohms)	
signal attenuation at 50 MHz:	0.28 dB/m	0.085 dB/ft	
mutual capacitance within pair,			
minimum:	34 pF/m	10.5 pF/ft	
nominal: (95% or more pairs)	41 pF/m	12.5 pF/ft	(+/- 10%)
maximum:	48 pF/m	15.0 pF/ft	
capacitance, pair to shield,			
maximum:	78 pF/m	24 pF/ft	
delta:	2.6 pF/m	0.8 pF/ft	
propagation delay,			
maximum: (65% of c)	5.18 ns/m	1.58 ns/ft	
delta:	0.13 ns/m	0.04 ns/ft	

## 4.3 Connector

plug connector type: 2 row, 50 pin, shielded tab connectors  
 AMP plug part number 749111-4 or equivalent  
 AMP shell part number 749193-2 or equivalent

receptacle type: 2 row, 50 pin, receptical header with rails and latch  
 blocks. AMP part number 749075-5, 749903-5 or  
 equivalent

## 4.4 Pin Assignment

Signal Name	Dir.	Pin # (+side)	Pin # (-side)
SG - Signal Ground	---	1	26
RT - Receive Timing	<--	2	27
CA - DCE Available	<--	3	28
RD - Receive Data	<--	4	29
- reserved	<--	5	30
ST - Send Timing	<--	6	31
SG - Signal Ground	---	7	32
TA - DTE Available	-->	8	33
TT - Terminal Timing	-->	9	34
LA - Loopback circuit A	-->	10	35
SD - Send Data	-->	11	36
LB - Loopback circuit B	-->	12	37
SG - Signal Ground	---	13	38
5 ancillary to DCE	-->	14 - 18	39 - 43
SG - Signal Ground	---	19	44
5 ancillary from DCE	<--	20 - 24	45 - 49
SG - Signal Ground	---	25	50

Pin pairs 5&30, 14&30 to 18&43, and 20&45 to 24&49 are reserved for future use. To allow future backward compatibility, no signals or receivers of any kind should be connected to these pins.

(Appendices A&B not available)

## Appendix C: Noise Immunity

This appendix calculates the noise immunity of this interface. The normal specified 150 mvolts of noise immunity for 10KH ECL is not applicable here because the differential inputs do not use the internal ECL bias  $V_{bb}$ .

The common mode (NMcm) and differential mode (NMdiff) noise margins for the 10H115 and 10H116 differential line receivers are:

$$NM_{cm+} = V_{cm\_max} - V_{oh\_max} = -0.50 V_{dc} - (-0.81 V_{dc}) = 310 \text{ mVdc}$$

$$NM_{cm-} = V_{ol\_min} - V_{cm\_min} = -1.95 V_{dc} - (-2.85 V_{dc}) = 900 \text{ mVdc}$$

$$NM_{diff} = V_{od\_min} * \text{length} * \text{attenuation/length} - V_{id\_min}$$

$$= 10^{((20\log(.59) - 50(.085))/20)} - 150 \text{ mv} = 361 \text{ mv}$$

in dB:

$$= 20\log(.361) - 20\log(.15)$$

Voltages are at 25 degrees Celcius.  $V_{cm\_max}$  was chosen to be 100 mv below the saturation point of  $V_{ih} = -0.4$  volts.

The 10H125 differential receiver has a +5 Vdc supply and can handle a larger positive excursion on its input. The noise margin performance of the 10H125 is:

$$NM_{cm+} = V_{cm\_max} - V_{oh\_max} = 1.19 V_{dc} - (-0.81 V_{dc})$$

$NM_{cm-}$  and  $NM_{diff}$  are the same for all parts. To allow the use of all receivers, the worst case common mode noise at the receiver must be limited to 310 mvdc.

Interpret the common mode range,  $V_{cm\_max}$  to  $V_{cm\_min}$ , as the maximum range of absolute voltages that may be applied to the receiver's input, independent of the applied differential voltage. The signal voltage range,  $V_{oh\_max}$  to  $V_{ol\_min}$ , represents the maximum range of absolute voltages that the transmitter will produce. The difference between these two ranges represents the common mode noise margins,  $NM_{cm+}$  and  $NM_{cm-}$ , with  $NM_{cm+}$  being the maximum excursion for additive common mode noise, and  $NM_{cm-}$  being the maximum excursion for subtractive common mode noise.

With five 50-foot twisted pair grounds, the amount of ground loop current required to use up the common mode noise margin is:

$$\begin{aligned} I_{ground} &= NM_{cm+} / (\text{cable\_resistance}/5 \text{ pairs}) \\ &= (310 \text{ mVdc}) / (70 \text{ mohms/foot} \times 50 \text{ feet} / 10 \text{ wires}) \\ &= 0.9 \text{ amps dc} \end{aligned}$$

This amount of current should never be present under normal operating conditions.

Common mode noise will have a negligible effect on the differential noise margin,  $V_{df\_app}$ . Rather,  $V_{df\_app}$  would be affected by noise being introduced by one side of the power rails at the transmitter. ECL  $V_{cc}$  has a power supply rejection ratio (PSRR) of 0 dB while ECL  $V_{ee}$  has a PSRR on the order of 38 dB. Thus, to minimize differential noise,  $V_{cc}$  is grounded and  $V_{ee}$  is connected to a negative power supply.

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