

# Understanding the Cisco ONS 15454 XC and XC-VT Switching Matrix

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## Introduction

The Cisco Optical Networking System (ONS) 15454 provides a maximum switching capability of 336 Virtual Tributary level 1.5 (VT1.5) circuits. This number may be unreachable if running Unidirectional Path Switched Ring (UPSR) or Linear 1 + 1. As transverseing these architechures provides a lower maximum switching capability of 224 VT1.5 circuits. This document explains how to provision (or groom) VT1.5 circuits to achieve these values and demonstrates why users of the Cisco ONS 15454 may run out of available VT1.5 circuits before these maximum values are reached.

**Note:** The first VT connection on any port or card to any other port or card uses two Synchronous Transport Signal level 1 (STS-1) ports on the VT Cross Connection (VTX) matrix one from the STS Cross Connection (STSX) matrix to the VTX matrix and another from the VTX matrix back to the STSX matrix. If one of the terminations for that circuit happens to be an optical line card, protected by UPSR or Linear 1+1, there is an additional port burned from the VTX matrix to the STSX matrix. Once a port or card is connected to an STS-1 port on the VTX matrix, up to 28 VT1.5 circuits can be connected without reducing any further bandwidth (that is, without consuming additional STS-1 ports on the VTX matrix).

# Prerequisites

## Requirements

There are no specific requirements for this document.

## Components Used

This document is not restricted to specific software and hardware versions.

## Conventions

For more information on document conventions, see the Cisco Technical Tips Conventions.

## Background Information

Specifically, this document explains the VT1.5 switching capabilities of individual line cards; the architecture of the Cisco ONS 15454 Cross Connect (XC) cards and Cross Connect VT (XC-VT and XC10G) cards responsible for switching VT1.5 circuits; and how these cards operate with Bidirectional Line Switched Ring (BLSR), UPSR, Linear 1 + 1, and standard STS-1 connections. Sample configurations show how to achieve the maximum switching capabilities and how to exhaust the available STS-1 ports on the (VTX is used frequently and in many of the diagrams...) matrix before these maximums are reached.

## Line Card Capacities for VT1.5 Traffic

The table below shows which Cisco ONS 15454 line cards the XC-VT and XC10G can use for switching VT1.5 traffic and the maximum number of VT1.5 circuits that can be configured on each card.

Card Type	DS-1	DS-3	Enhanced DS-3 PM	EC-1	DS-3 TMUX*	OC-3	OC-12	OC-48	OC-48 ELR ITU	LS OC-48 IR	OC-48 LR
DS-1	14			14	14	14	14	14	14	14	14
DS-3											
Enhanced DS-3 PM											
EC-1	14			336	168	336	336	336	336	336	336
DS-3 XM-6/TMUX	14			168	168	168	168	168	168	168	168
OC-3	14			336	168	336	336	336	336	336	336
OC-12	14			336	168	336	336	336	336	336	336
OC-48	14			336	168	336	336	336	336	336	336
OC-48 ELR ITU	14			336	168	336	336	336	336	336	336
LS OC-48 IR	14			336	168	336	336	336	336	336	336
LS OC-48 LR	14			336	168	336	336	336	336	336	336

<b>OC 192 LR</b>	14			336	168	336	336	336	336	336	336
<b>10/100 Ethernet</b>											
<b>Gigabit Ethernet</b>											

\* TMUX = Transport Multiplexing Protocol

**Note:** Not all versions of each card are represented by this chart but no major changes are reflected.

## Line Card Characteristics

The table below shows the I/O format, internal SONET mapping, and port capabilities of the Cisco ONS 15454 line cards. Cards that have the same internal format can be cross connected.

**Note:** Internally, the Digital Signal Level 3 (DS-3) and DS-3 TMUX cannot be cross connected, because the DS-3 card is DS-3 mapped and the DS-3 TMUX card is VT1.5 mapped. However, these cards can be connected by their I/O ports when both are M13 mapped.

Card Type	I/O Format	I/O Ports	Internal SONET Mapping	STS Ports
<b>DS-1</b>	DS-1	14	VT1.5 mapped in an STS	1
<b>DS-3</b>	DS-3 <sup>1</sup>	12	DS-3 mapped in an STS	12
<b>Enhanced DS-3 PM</b>	DS-3	12	DS-3 mapped in an STS	12
<b>EC-1</b>	DS-3 mapped STS, VT1.5 mapped STS or clear channel STS (Electrical) <sup>1</sup>	12	DS-3, VT1.5s mapped in an STS or an	12
<b>DS-3 TMUX</b>	M13 mapped DS-3	6	STS-1 VT1.5 mapped in an STS	6
<b>*OC-3</b>	DS-3 mapped STS, VT1.5 mapped STS, clear channel STS or OC-nc ATM (Optical)	4	DS-3, VT1.5s mapped in an STS, or an	12 <sup>3</sup>
<b>OC-12</b>	DS-3 mapped STS, VT1.5 mapped STS, clear channel STS or OC-nc ATM	1	DS-3n/nc <sup>2</sup> VT1.5s mapped in an STS, or an STS-n/nc <sup>2</sup>	12 <sup>4</sup>

	(Optical) <sup>1</sup>			
<b>OC-48</b>	DS-3 mapped STS, VT1.5 mapped STS, clear channel STS or OC-nc ATM (Optical) <sup>1</sup>	1	DS-3, VT1.5s mapped in an STS, or an	48 <sup>5</sup>
<b>OC-48 ELR ITU</b>	18 OC-48 IYU cards based on 200 GHz spacing operate in the red and blue bands <sup>1</sup>	1	STS-n/nc <sup>2</sup> DS-3, VT1.5s mapped in an STS, or an STS-n/nc <sup>2</sup>	48 <sup>5</sup>
<b>LS OC-48 IR</b>	DS-3 mapped STS, VT1.5 mapped STS, clear channel STS or OC-nc ATM (Optical) <sup>1</sup>	1	DS-3, VT1.5s mapped in an STS, or an STS-n/nc <sup>2</sup>	48 <sup>5</sup>
<b>LS OC-48 LR</b>	DS-3 mapped STS, VT1.5 mapped STS, clear channel STS or OC-nc ATM (Optical) <sup>1</sup>	1	DS-3, VT1.5s mapped in an STS, or an STS-n/nc <sup>2</sup>	48 <sup>5</sup>
<b>OC-192 LR</b>	DS-3 mapped STS, VT1.5 mapped STS, clear channel STS or OC-nc ATM (Optical) <sup>1</sup>	1	DS-3, VT1.5s mapped in an STS, or an STS-n/nc <sup>2</sup>	192
<b>10/100 Ethernet</b>	Ethernet (Electrical)	12	Ethernet in *HDLC mapped in an STS-nc	12 <sup>4</sup>
<b>Gigabit Ethernet</b>	Ethernet (Electrical)	2	Ethernet in HDLC mapped in an STS-nc	12 <sup>4</sup>

\* OC = Optical Carrier

\* HDLC = High-Level Data Link Control

## Table Notes

<sup>1</sup> This card can accept any type of DS-3 mapping, M13, M23, clear channel, DS-3 ATM.

<sup>2</sup> This card's SONET mapping can be a DS-3 mapped STS or a VT1.5 mapped STS. However, it does not convert between the two different mappings.

<sup>3</sup> Each of the four STS streams can be configured in multiples of STS-1s or STS-3c.

<sup>4</sup> The STS stream can be configured in multiples of STS-1s, STS-3cs, STS-6cs, or STS-12c.

<sup>5</sup> The STS stream can be configured in multiples of STS-1s, STS-3cs, STS-6cs, STS-12cs, or STS-48.

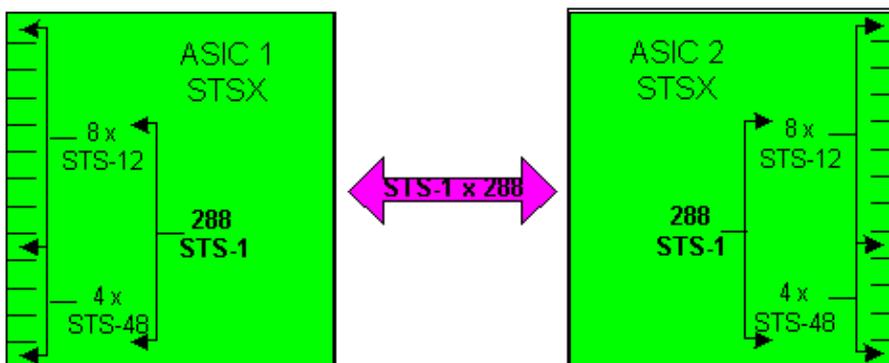
## Line Card Architecture

**Note:** To follow the circuit diagrams contained in this document, download the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

### XC Architecture

The XC card switches all traffic at the STS-1 level between the Cisco ONS 15454 traffic cards. There is no loss or degradation of traffic passing through the XC card, but the traffic passed consumes some of the available STS-1 circuits. For example, the OC-12 consumes 12 STS ports, the 12-port DS-3 consumes 12 STS ports, and the 14-port DS-1 consumes one STS port.

An XC card consists of two main STS application-specific integrated circuits (ASICs), as shown below.



Each XC card has 24 ports, 12 input ports, and 12 output ports. One input and one output port represent each available line card slot of the Cisco ONS 15454's shelf. Four input and output ports pairs, that can operate as high as the STS-48 line rate, this matches the high speed slots of 5,6,12, and 13. The remaining eight input and output ports pairs operate at a maximum of an STS-12 line rate. This provides a maximum bandwidth of  $(4 \times 48) + (8 \times 12)$  or 288 STS-1 circuits. But each connection requires two circuits, *so the effective simultaneous number of STS-1 connections that can pass through the XC card is 144*. An STS-1 on any input port can be mapped to any output port. The XC card is designed to be nonblocking, which means that all 144 STS-1 connections can be used simultaneously to their maximum capacity.

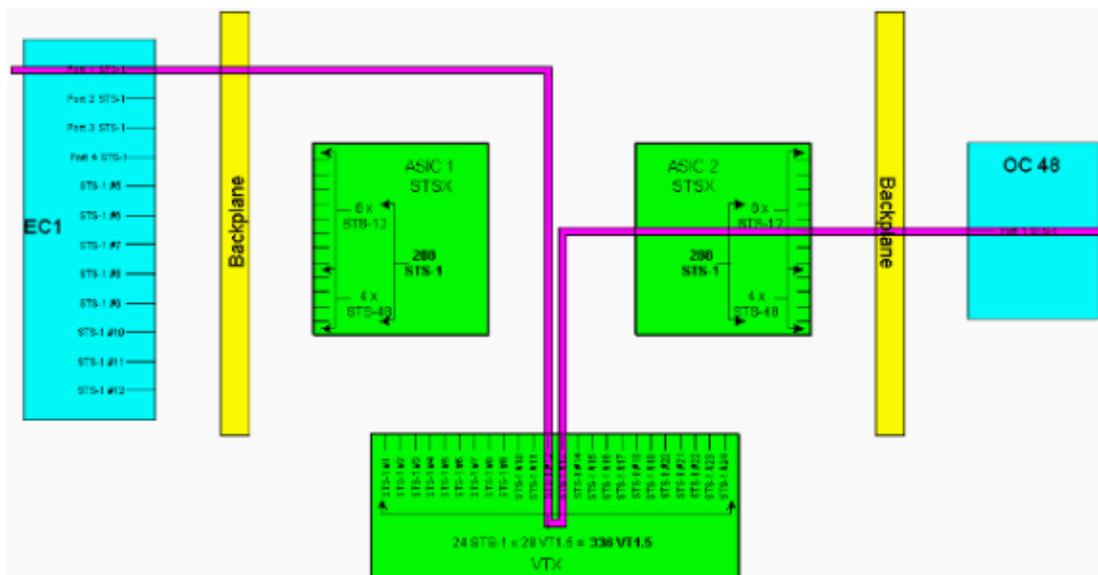
### XC-VT and XC10G Architecture

The XC-VT card provides the same functionality as the XC card. It also provides an additional 24 STS-1 level ports that interface with a sub-matrix called the VTX matrixes. This allows you to go beneath the STS-1 level and cross-connect circuits at the VT1.5 level. While the XC10G card is functionally the same as the XC-VT card, it has some enhancements on both the XC and the XC-VT cards. These enhancements come in an increased ability in handling STS-1 level connections. The XC10G provides a maximum bandwidth of  $(4 \times 192) + (8 \times 48)$  or 1152 STS-1 circuits, again because as a STS-1 goes into the STSX matrixes it must also go out. This leaves *the effective simultaneous number of STS-1 connections that may pass through the XC10G card as 576 STS-1s*.

In both the XC-VT and the XC10G, users often view the maximum number of VT1.5 circuits they can cross connect in terms of VTs, or a total of 336 VTs. The best way to approach this, however, is to relate to the 24 STS-1 ports that connect to the VTX matrix instead of the VTs. This limitation is the key factor in understanding this process.

The first VT connection on any port or card to any other port or card uses two STS-1 ports on the VTX matrix one from the STSX matrix to the VTX matrix and another from the VTX matrix back to the STSX matrix. If one of the terminations for that circuit happens to be an optical line card, protected by UPSR or Linear 1+1, there is an additional port burned from the VTX matrix to the STSX matrix. Once a port or card is connected to an STS-1 port on the VTX matrix, up to 28 VT1.5 circuits can be connected without reducing any further bandwidth (that is, without consuming additional STS-1 ports on the VTX matrix).

Either an XC-VT or XC10G card provides a third VTX ASIC as shown below.



**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

As shown above, the VTX ASIC provides 24 STS-1 circuits, each of which can be groomed with up to 28 VT1.5 circuits. This provides a theoretical bandwidth of 672 VT1.5 circuits, but since each VT1.5 connection requires a minimum of two circuits, the *simultaneous number of VT1.5 connections that can pass through the XC-VT or XC10G card is 336.*

**Note:** The XC10G has expanded capabilities on the STSX matrix only. The VTX matrix remains the same as the XC-VT card and is limited to 336 VT1.5

A VT1.5 on any VTX input port can be mapped to any VTX output port. The XC-VT/XC10G card is designed to be nonblocking, which means that all 336 VT1.5 connections can simultaneously be used to maximum capacity. Even if an STS-1 is only partially filled, every VT1.5 in the STS-1 is terminated on the VTX. When every VT1.5 in an STS is used, and all of the VTX ASIC's STS-1 ports are consumed, there is enough capacity on the VTX to switch every VT1.5 in every terminated STS. Therefore, count STS-1 terminations on the VTX instead of VT1.5 terminations.

In other words, the XC-VT/XC10G card provides the equivalent of a bidirectional STS-12 for VT1.5 traffic. The VT1.5-level signals can be cross connected, dropped, or rearranged. The Timing Communications and Control (TCC) card assigns bandwidth to each slot on a per STS-1 basis or per VT1.5 basis. When all 24 of the STS-1 ports on the VTX ASIC are used, no additional VT1.5 circuits can have access to the VTX matrix.

## Architecture Summary

Here is a brief synopsis of the circuit architecture and capacity of the XC and XC-VT line cards.

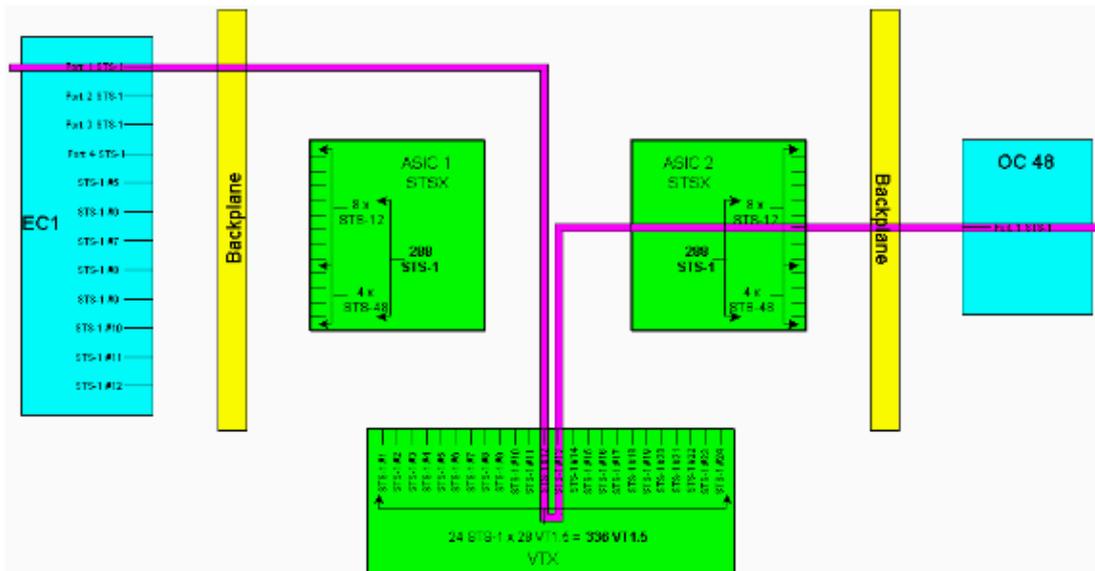
- The maximum number of simultaneous STS-1 circuits that can pass through an XC or XC-VT card is 144.
- All 144 STS-1 circuits on an XC or XC-VT card can be used to maximum capacity.
- The maximum number of simultaneous STS-1 circuits that can pass through an XC10G card is 576.
- All 576 STS-1 circuits on an XC10G card can be used to maximum capacity.
- The maximum number of VT1.5 connections that can pass through an XC-VT or XC10G card is 336.
- All 336 VT1.5 connections on an XC-VT or XC10G card can simultaneously be used to maximum capacity.
- When calculating the capacity of a VTX ASIC, count the number of STS-1 circuits that terminate on the VTX ASIC.
- The maximum number of STS-1 ports on a VTX ASIC is 24. When all 24 ports are used, no additional VT1.5 circuits can be created.
- An XC card performs STS-to-STS switching only. There is no switching at the VT level, but the card can tunnel VT1.5s through STS-1 circuits.
- When tunneling VT1.5 circuits, an XC card provides direct mapping and no Time Slot Interchange (TSI) between the incoming and outgoing VTs in an STS flow.
- An XC-VT or XC10G card allows you to map VT1.5 connections from one STS to multiple STSs, or to perform TSI on the VT 1.5s.
- If VT1.5s are tunneled through an XC-VT or a XC10G card, they do not pass through the VTX ASIC or consume any of its 24 STS-1 bandwidth.

## VT 1.5 Bandwidth with BLSR, UPSR and Linear 1 + 1 Configurations

### BLSR

The behavior when using BLSR is the same as when creating normal STS-1 connections on the VTX ASIC. For every STS-1 circuit that is terminated from source STSX ASIC 1 onto the VTX, a second STS-1 is required from the VTX to destination STSX ASIC 2.

This means that a maximum switching capacity of 336 circuits can be achieved; 2 STS-1 circuits filled with a maximum of 28 VT1.5s each using 24 ports, resulting in a total of 336 circuits ( $12 \times 28 = 336$ ).



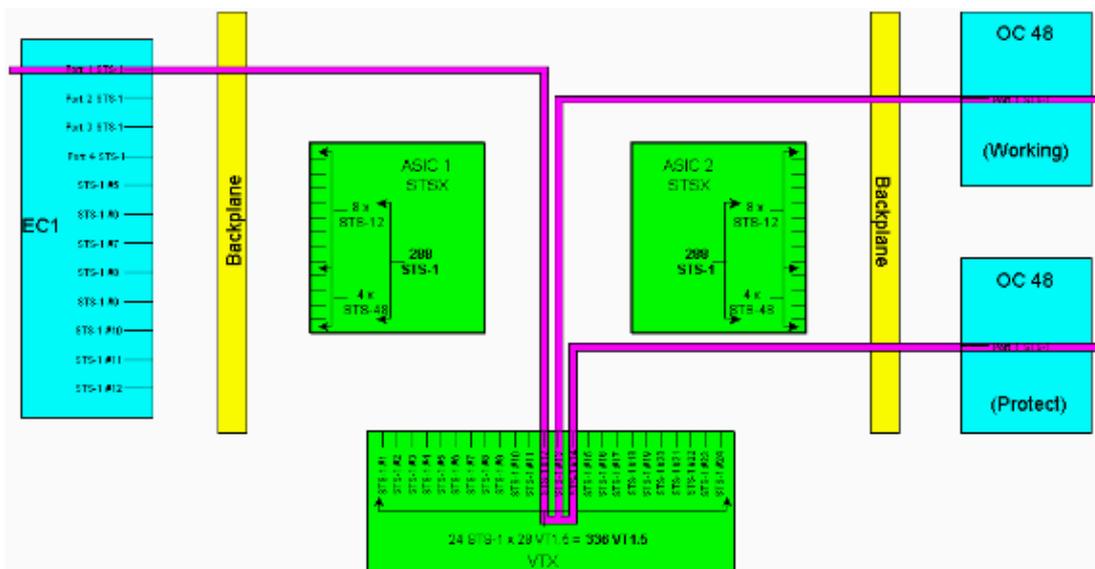
**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

**Note:** Remember the use of STS-1 to and from the VTX matrix is not on a per node basis. Two STS-1 connections are used on each and every node that the VT1.5 circuit is provisioned on.

## UPSR and Linear 1+1

The behavior when using UPSR or Linear 1 + 1 provides a lower maximum switching capability of 224 VT1.5 circuits. For every STS-1 connection that is terminated from source STSX ASIC 1 onto the VTX, two additional STS-1 connections (working and protect) are required from the VTX to destination STSX ASIC 2.

This means that a maximum switching capacity of 224 circuits can be achieved eight STS-1 circuits filled with a maximum of 28 VT1.5s each using 24 ports, resulting in a total of 224 circuits (8 x 28 = 224).



**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

**Note:** Remember the use of STS-1s to and from the VTX matrix is not on a per node bases. Two STS-1

connections are used on each and every node that the VT1.5 circuit is provisioned on. Three at nodes where the VT 1.5 is dropped, and four could be used when crossing from one UPSR ring to another.

## Point-to-Multipoint Circuits

In a point-to-multipoint connection, the ratio of ports to connections is not two-to-one as in a point-to-point connection. It is important to count the number of physical STS-1 ports that terminate instead of the number of circuit connections. Point-to-multipoint connections are used for broadcast video (unidirectional) and drop-and-continue sites in UPSR/BLSR matched nodes.

When creating point-to-point Connection A from slot 1/port 3/STS 2 (1/3/2) to slot 2/port 2/STS 4 (2/2/4), two ports are consumed. When a point-to-multipoint Connection B with 2/2/2 mapped to 4/4/4 and 5/5/5 is created, three ports are consumed. Subtracting the sum of Connection A and Connection B (five ports) from the 288 total available ports yields 283 logical ports remaining on the STSX. If these were unidirectional flows, Connection A would use one port and Connection B would use 1.5 ports.

**Note:** Unidirectional connections are measured in 0.5 increments because the cross-connected card views a bidirectional flow as two unidirectional connections. The line card capacities and characteristics tables state limits in bidirectional terms.

Currently these calculations do not have to be performed because the STSX is nonblocking. The STSX has the capacity to switch all ports/STSs to all ports/STSs.

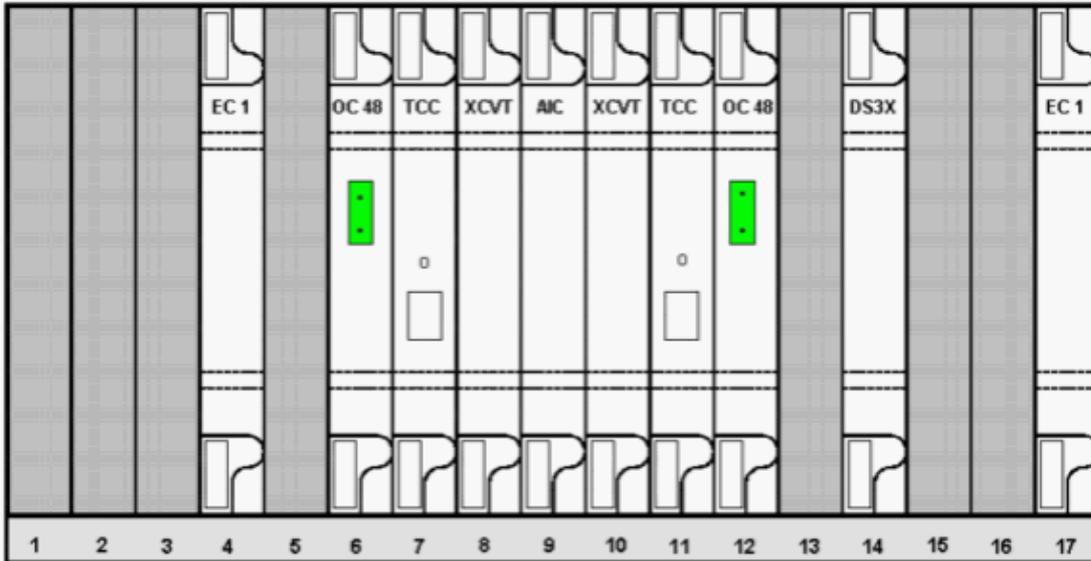
## Examples of Creating Circuits

Many of the concepts discussed above are illustrated in the following examples. The first example demonstrates how VT1.5 connections are properly provisioned over an STS-1 circuit. The second example shows how incorrect provisioning can cause errors by exceeding the available bandwidth.

### Correct Provisioning: Grooming VT1.5 Connections Over an STS-1 Circuit

In this example, two Electrical Cards (EC)-1 cards have been installed in physical slots 4 and 17, as shown in the image below. Each EC-1 card provides 12 STS-1 ports. Port 1 on the source EC-1 card in physical slot 4 is connected to port 1 on the destination EC-1 card in physical slot 17. This requires two STS-1 circuits (one source and one destination) to be terminated on the VTX ASIC, reducing the available bandwidth on the VTX ASIC from 24 STS-1 ports to 22 STS-1 ports.

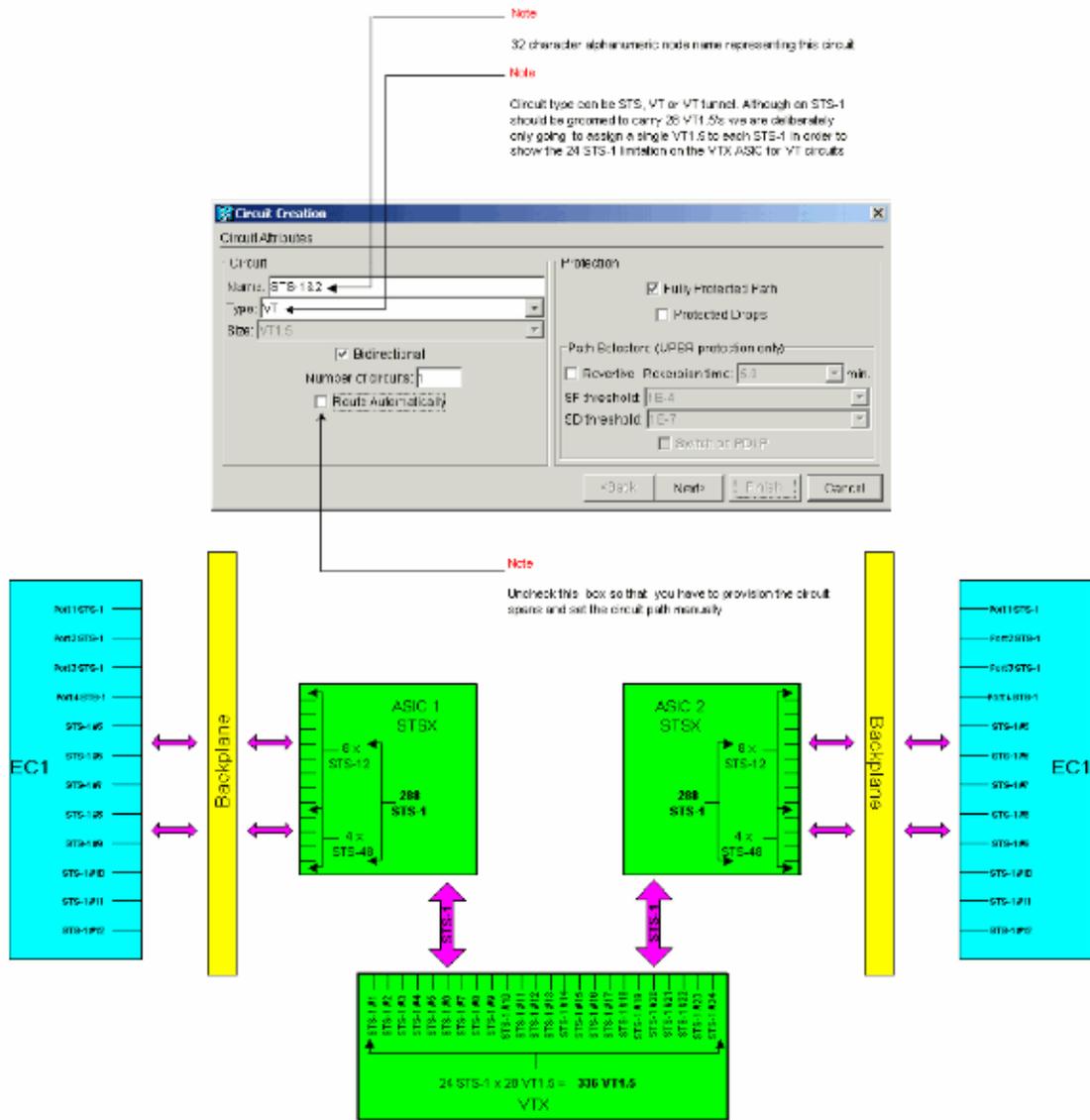
This example demonstrates how to provision multiple VT1.5 connections onto two STS-1 ports (source and destination) on the VTX ASIC. The process, called grooming, allows you to use all 28 available VT1.5 circuits on each of the 24 STS-1 ports on the VTX ASIC. This yields a total bandwidth of 672 circuits (28 x 24), but each VT1.5 connection requires both a source circuit and a destination circuit, so the maximum number of VT1.5 connections available on the XC-VT is 336.



To provision the VT1.5 circuits, follow the procedure below.

1. To provision the VT1.5 circuits, the Circuit Creation window prompts you for Circuit Attributes.

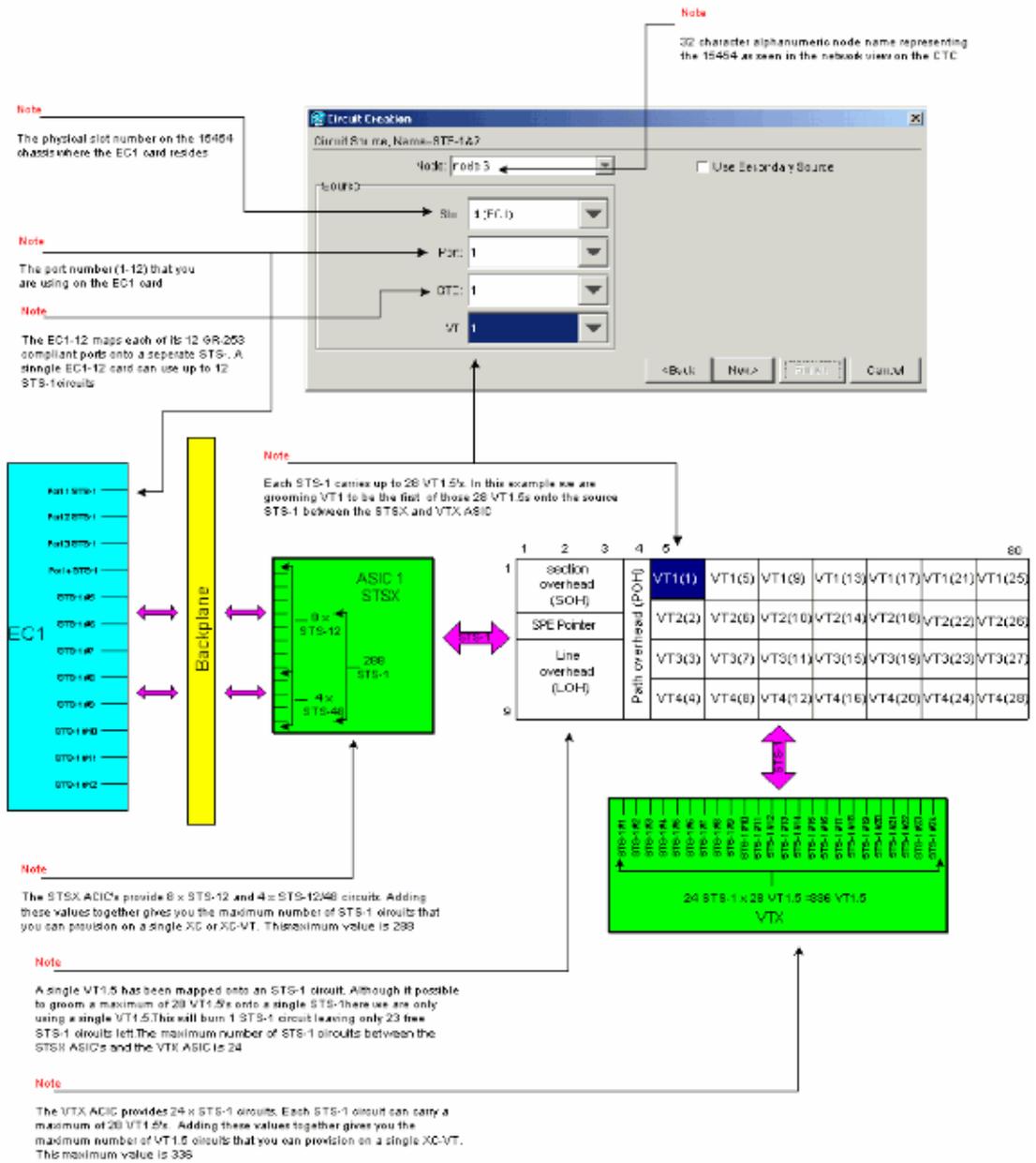
Select **VT** to provision VT1.5 circuits, then uncheck the **Route Automatically** box to manually configure the path the VT1.5 circuits follow. Click **Next**.



**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

2. In the **Circuit Creation > Circuit Source** window, set the source node, physical slot number, and port of the EC-1 card on which the VT1.5 circuits are to travel.

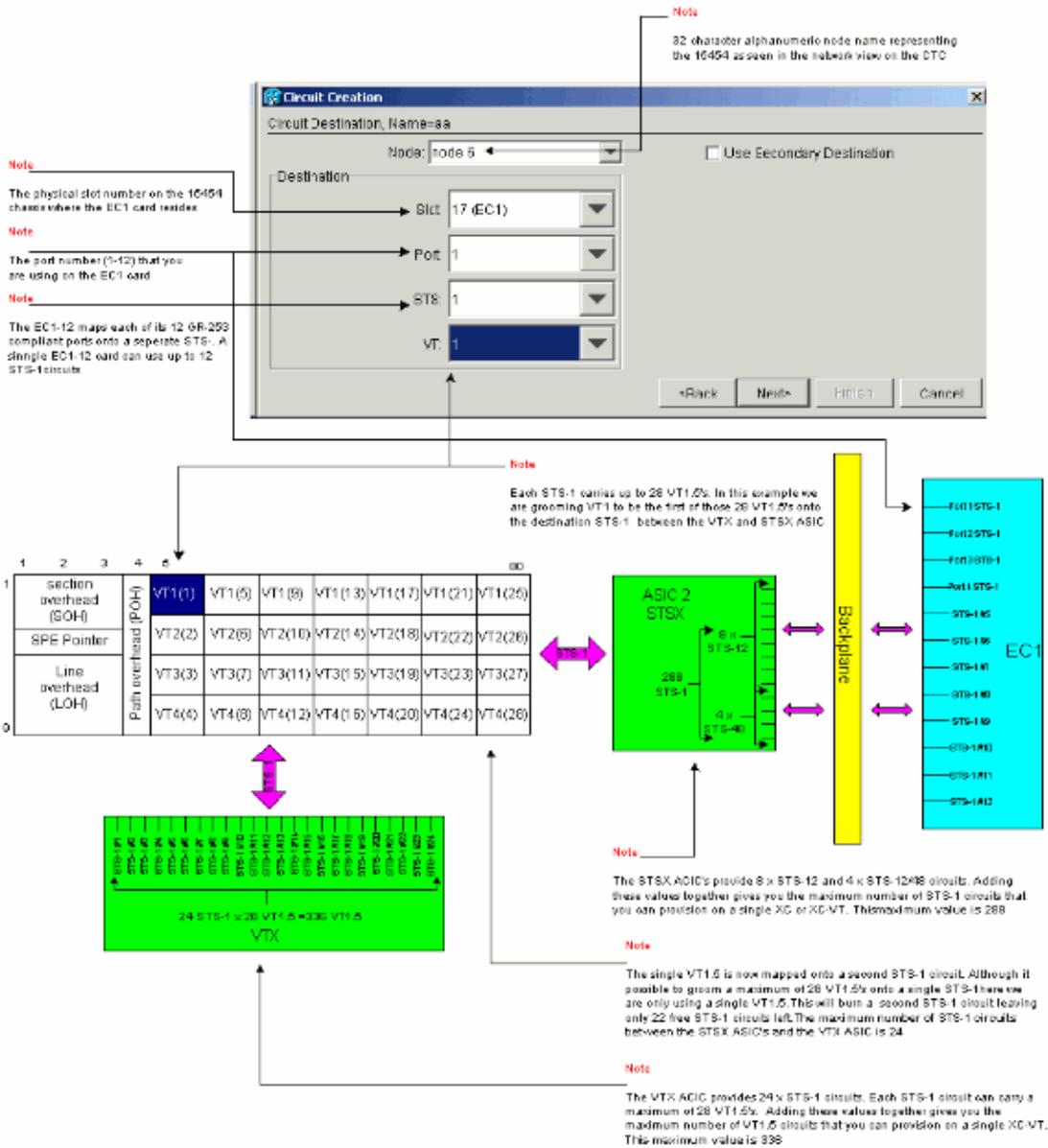
To groom the first VT1.5 on the STS-1 circuit for the first port on the source EC-1 card, select **slot 4**, **port 1**, and **VT 1**. The STS-1 does not need to be selected, since each of the EC-1 ports maps to a single source STS-1. Click **Next**.



**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

3. In the **Circuit Creation > Circuit Destination** window, set the destination node, physical slot number, and port of the EC-1 card on which the VT1.5 circuits are to travel.

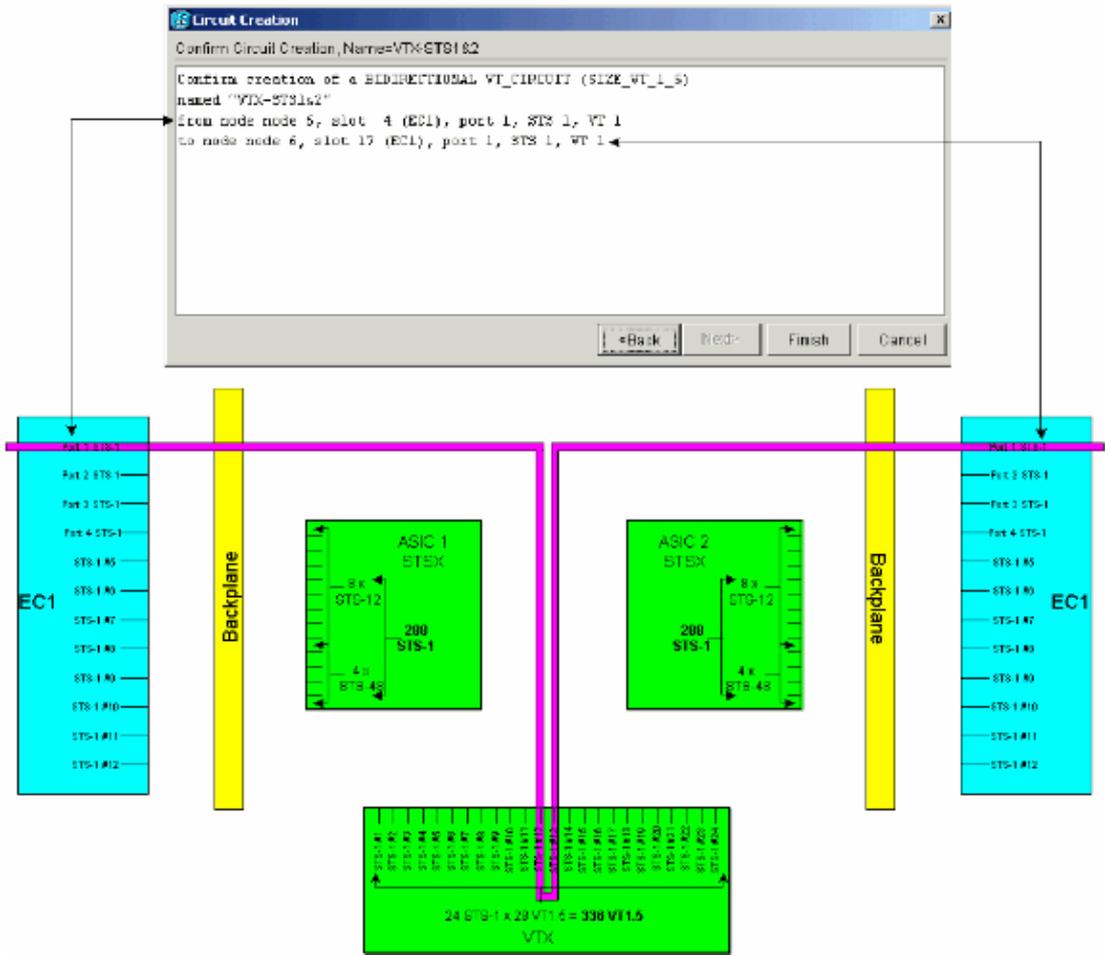
To groom the first VT1.5 on the STS-1 circuit for the first port on the destination EC-1 card, select **slot 17, port 1**, and **VT 1**. There is no need to select the STS-1, since each of the EC-1 ports maps to a single destination STS-1. Click **Next**.



**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

4. In the Circuit Creation confirmation window, verify the settings for the circuit being groomed.

The window below confirms the grooming of a VT1.5 connection on the source STS-1 circuit from port 1 of the EC-1 card in slot 4 going to a VT1.5 on the destination STS-1 circuit to port 1 of the EC-1 card in slot 17. Click **Finish** to create the circuit.

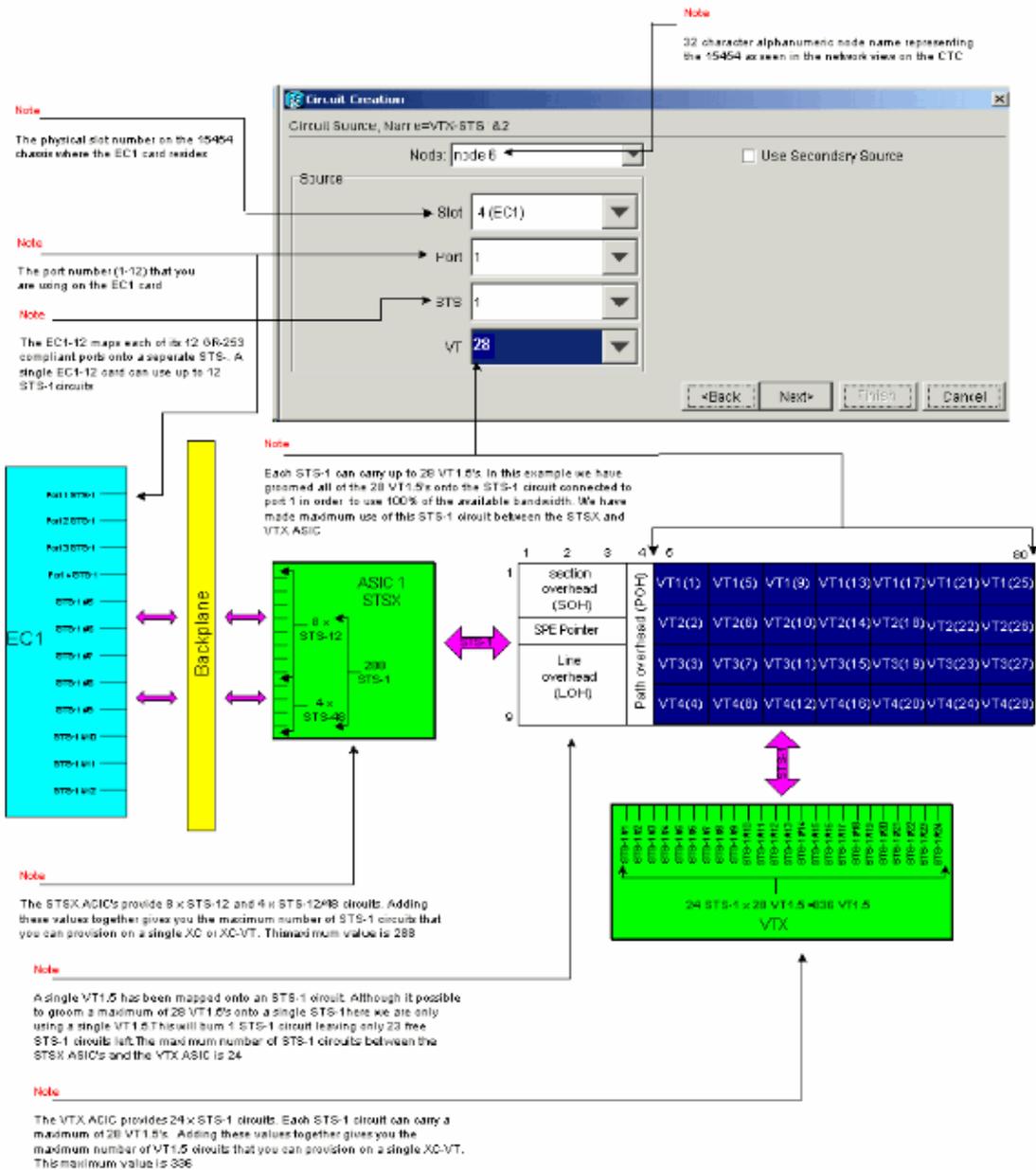


**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

- Repeat Steps 1 through 4 for the remaining 27 VT1.5s so they are groomed onto the source and destination STS-1 circuits connecting port 1 of both the EC-1 cards.

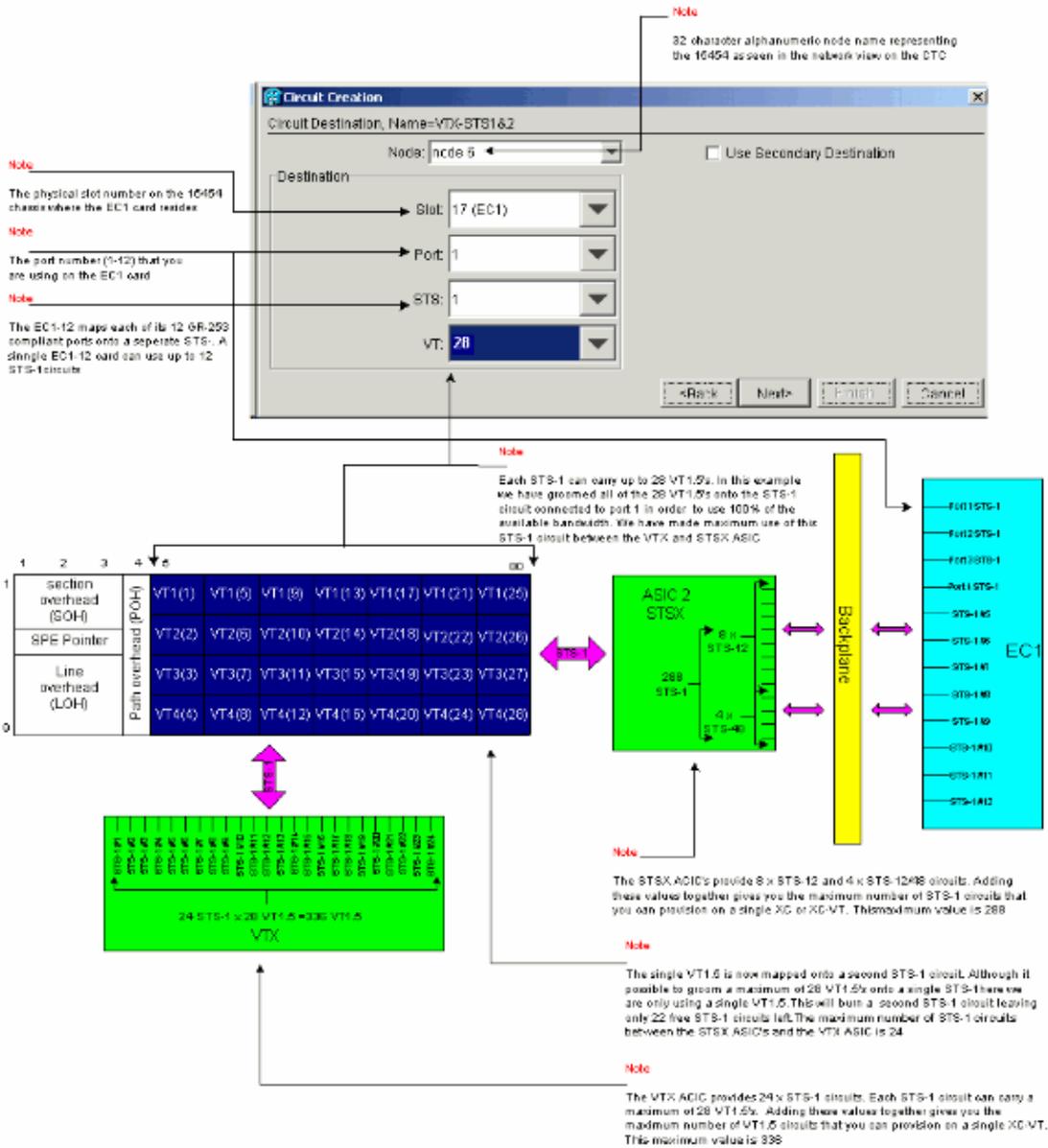
This may be done either, each circuit individually, or by multiples. Multiple circuits may be created by placing the number of desired circuits in the box of the first screen of **Circuit Creation > Circuit Attributes** (refer to Step 1). At the end of this grooming process, all 28 VT1.5 circuits should be provisioned onto the source and destination STS-1 circuits.

The **Circuit Creation > Circuit Destination** window shown below is for the last circuit destination panel that is being provisioned. All 28 VT1.5 circuits have been mapped onto the single destination STS-1 attached to port 1 of the EC-1 card in physical slot 4. By correctly grooming these 28 VT1.5 circuits, 100 percent capacity has been reached of the destination STS-1 attached to port 1 of the destination EC-1 card in slot 17.



**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

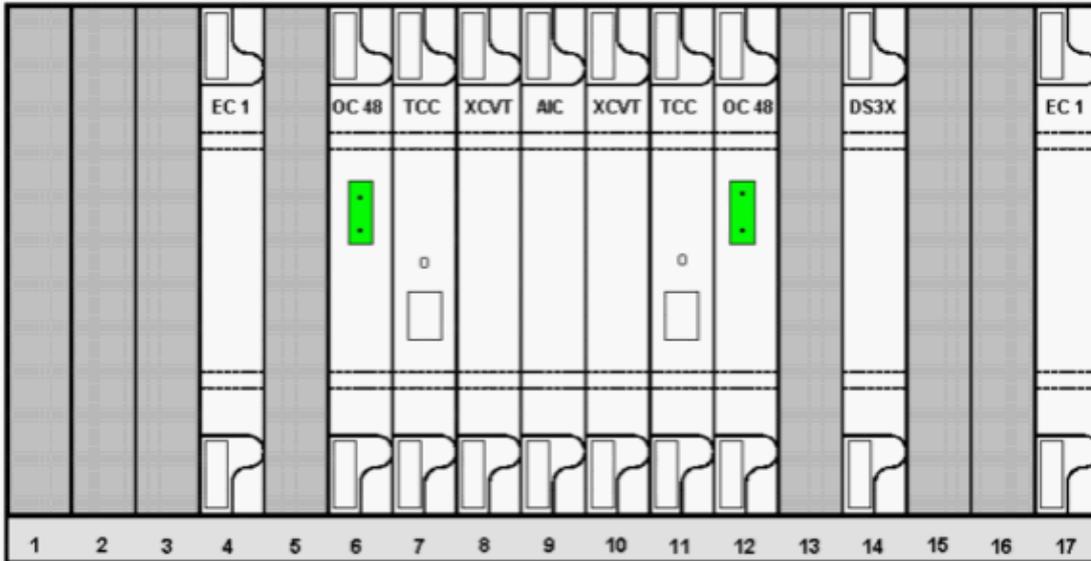
The **Circuit Creation > Circuit Destination** window shown below is for the last circuit destination panel that is being provisioned. All 28 VT1.5 circuits are mapped onto the single destination STS-1 attached to port 1 of the EC-1 card in physical slot 4. By correctly grooming these 28 VT1.5 circuits, 100 percent capacity has been reached of the destination STS-1 attached to port 1 of the destination EC-1 card in slot 17.



**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

## Incorrect Provisioning: Exceeding the VTX Bandwidth With VT1.5 Connections Over Multiple STS-1 Circuits

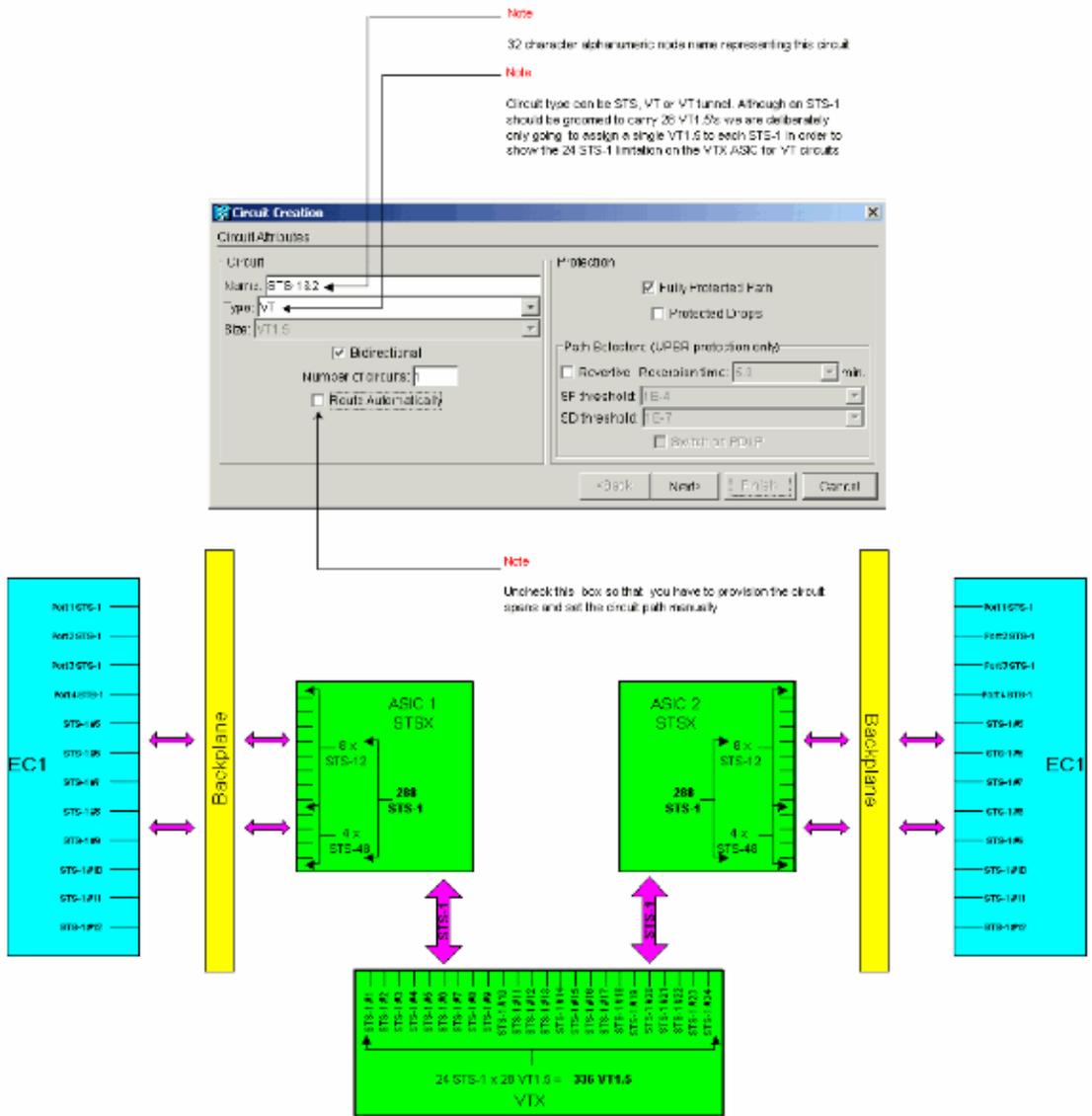
In this example, two EC-1 cards have been installed in physical slots 4 and 17, and a DS-3 card has been installed in physical slot 14. Each EC-1 card provides 12 STS-1 ports, and the ports on each card can be connected to each other by provisioning an STS-1 circuit that carries a single VT1.5. Each STS-1 connection requires two ports on the XC-VTs or XC10Gs VTX ASIC to switch the VT1.5 carried within it. Making these connections uses all 24 STS-1 ports on the VTX ASIC, so attempting to provision an additional STS-1 carrying a single VT1.5 from the DS-3 card exceeds the VTX ASIC limit and displays an error message.



The following steps show how incorrect provisioning can cause errors by exceeding the available bandwidth.

1. To provision the VT1.5 circuits, the Circuit Creation window prompts you for Circuit Attributes.

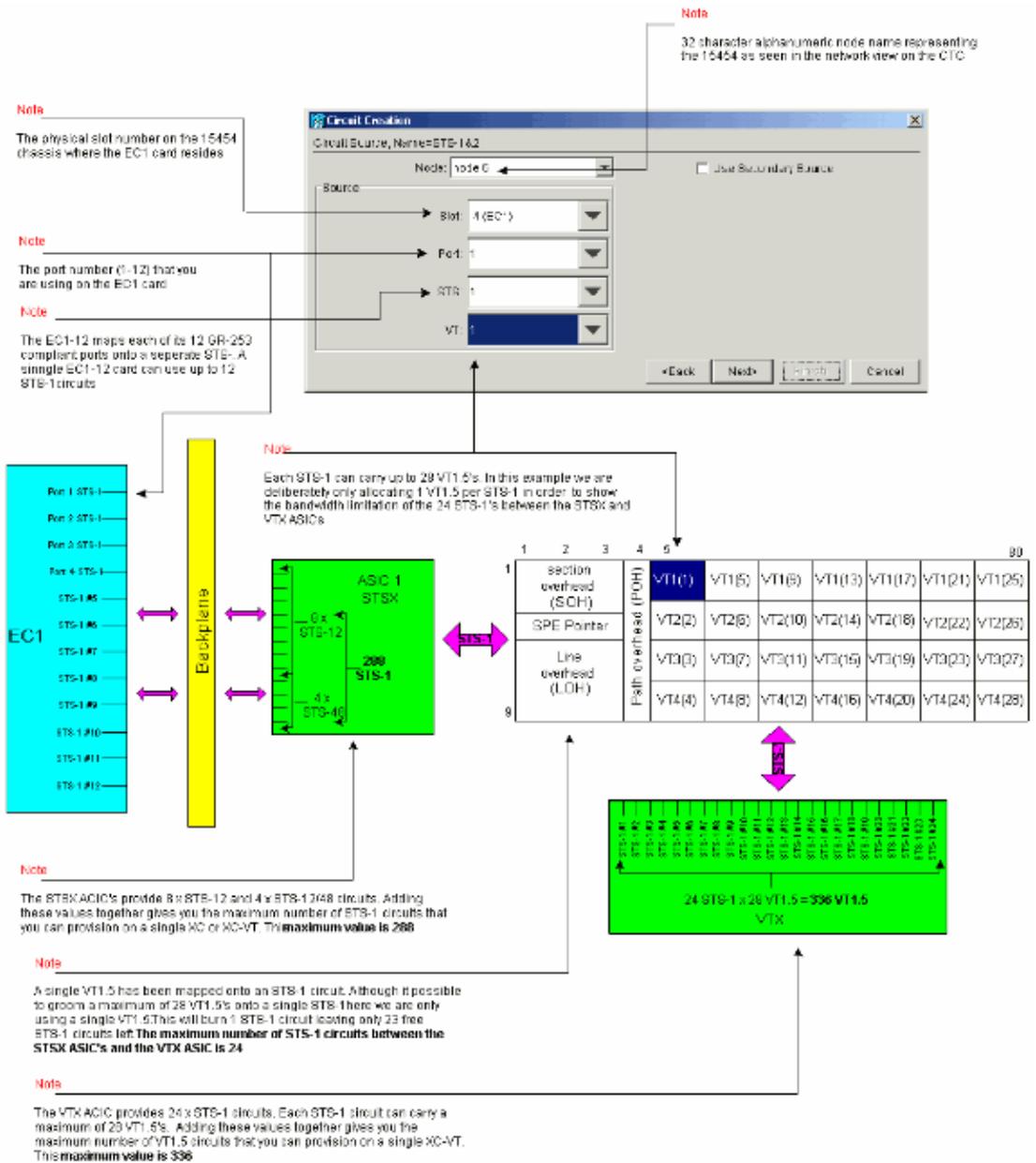
Select **VT** to provision VT1.5 circuits, then uncheck the **Route Automatically** box to manually configure the path the VT1.5 circuits follow. Click **Next**.



**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

2. In the **Circuit Creation > Circuit Source** window, set source information for the VT1.5 circuit being created.

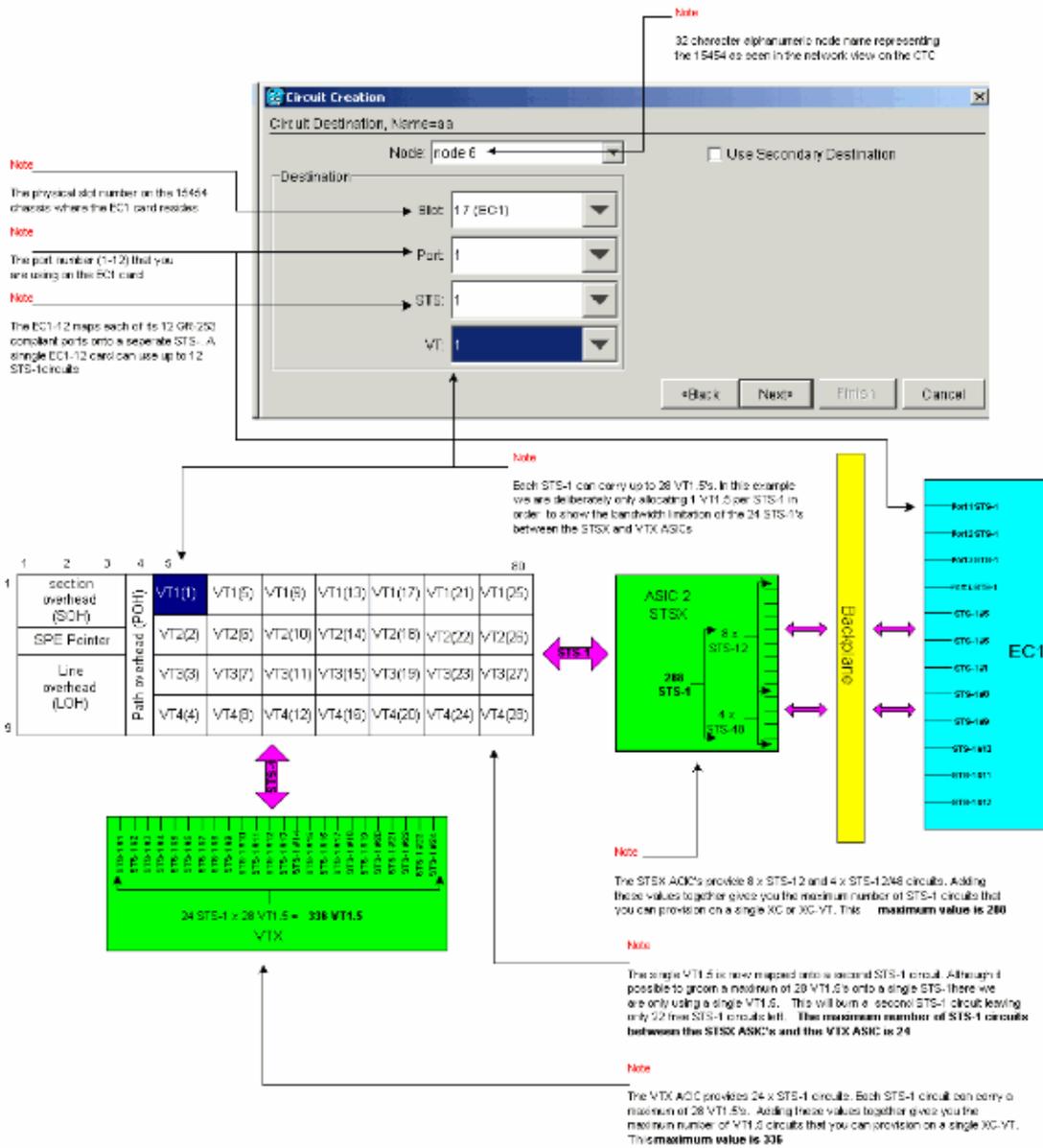
Each of the 12 ports on the source EC-1 cards maps to a single STS-1 circuit. Select the first port on the source EC-1 card in physical slot 4, and select **VT 1** out of the 28 VT1.5 connections available at the source port to be carried within the STS-1 circuit. Click **Next**.



**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

3. In the **Circuit Creation > Circuit Destination** window, set the destination information for the VT1.5 circuit being created.

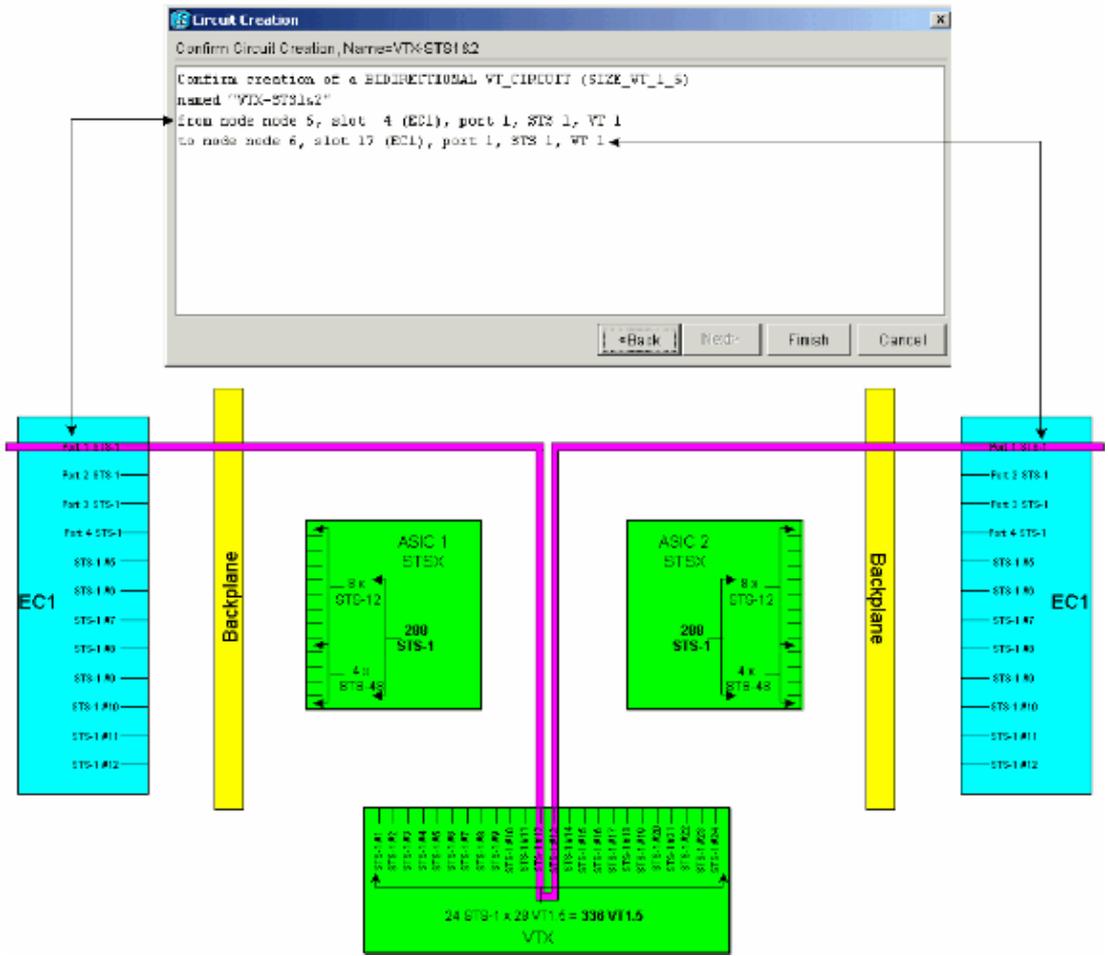
Each of the 12 ports on the destination EC-1 cards maps to a single STS-1 circuit. Select the first port on the destination EC-1 card in physical slot 17, and select **VT 1** out of the 28 VT1.5 connections available at the destination port to be carried within the STS-1 circuit. Click **Next**.



**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

4. In the Circuit Creation confirmation window, verify the settings for the circuit being provisioned.

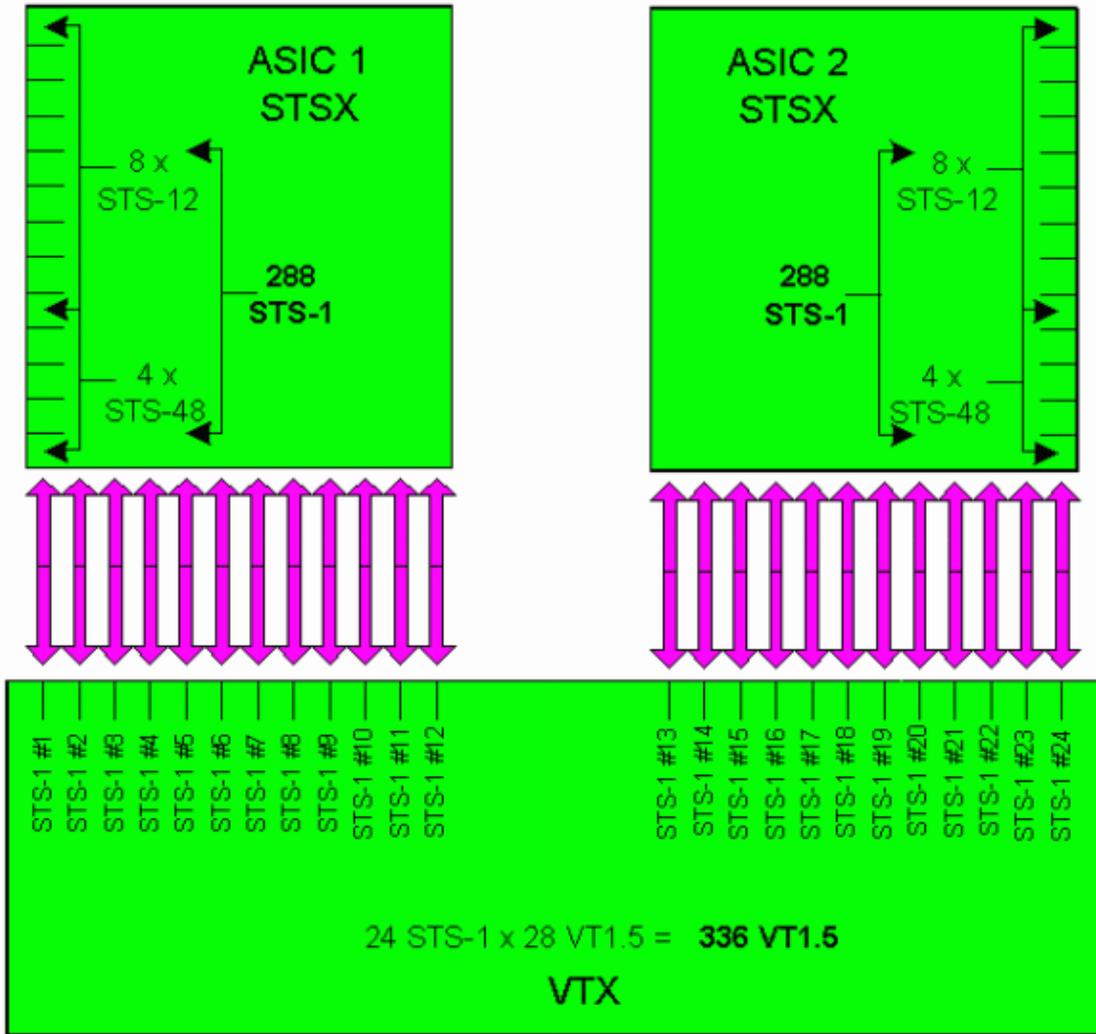
The window below confirms the grooming of the first STS-1 circuit from port 1 of the EC-1 card in slot 4 to port 1 of the EC-1 card in slot 17. Click **Finish** to create the circuit.



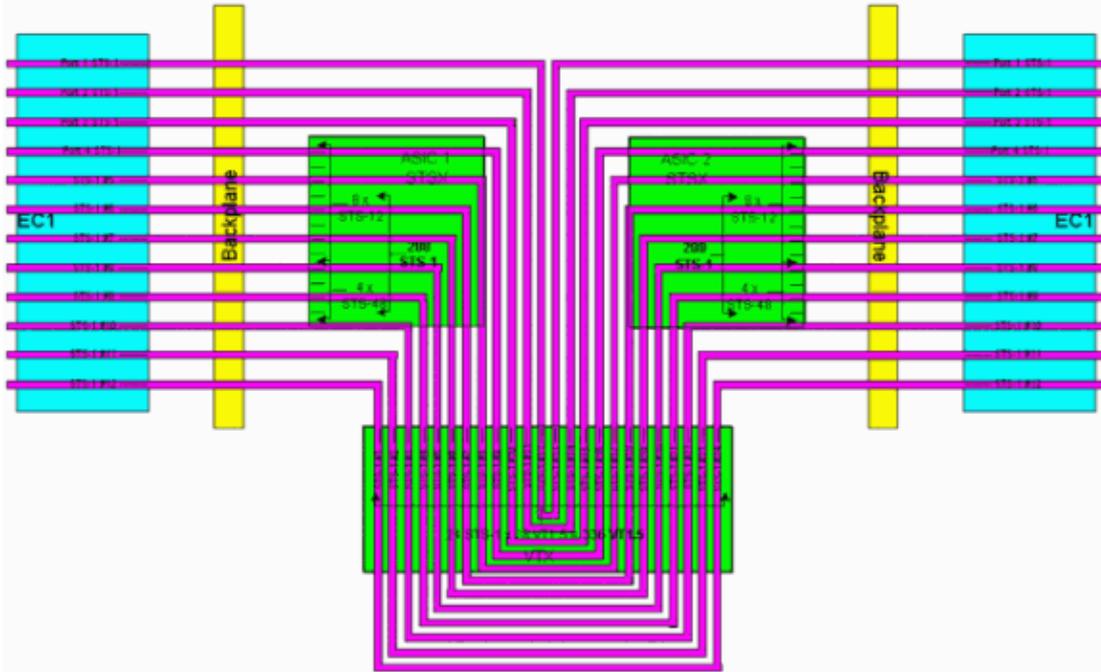
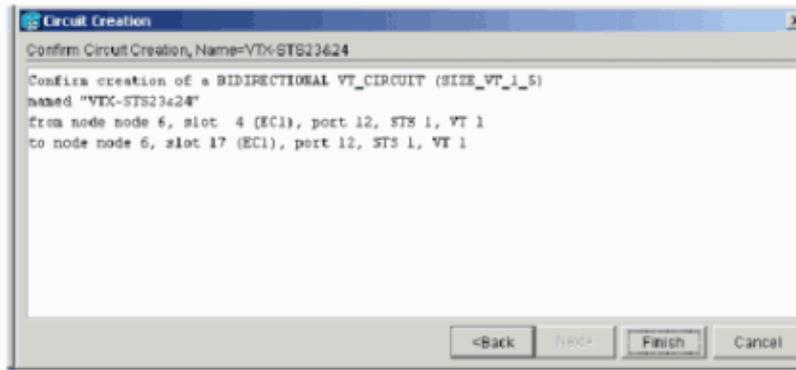
**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

- Repeat Steps 1 through 4 for each of the 12 ports on the source and destination EC-1 cards.

Each provisioned STS-1 circuit burns two of the STS-1 ports on the XC-VTs or XC10Gs VTX ASIC. When all 12 ports are groomed, all of the available 24 STS-1 ports on the VTX ASIC are consumed, and the available STS-1 bandwidth on the VTX ASIC is fully used. However only 12 VT1.5 circuits are built through the VTX ASIC matrix.

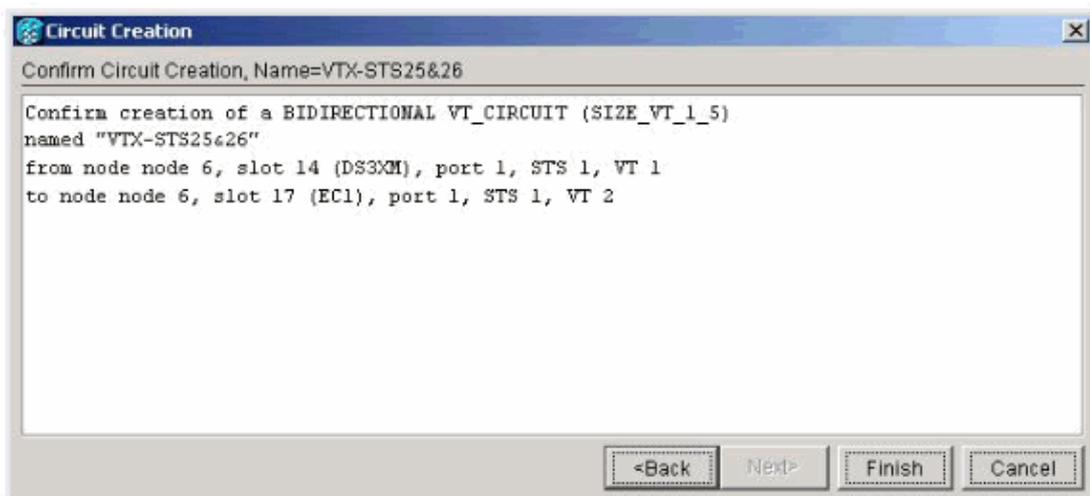


The Circuit Creation confirmation window shown below is displayed immediately before the last STS-1 circuit is groomed from port 12 of the EC-1 card in slot 4 to port 12 of the EC-1 card in slot 17. As shown, all of the 24 STS-1 ports on the VTX ASIC have been used.



**Note:** For a larger version of this diagram, refer to the Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix PDF wallchart.

Now consider what happens when a user tries to provision a 13th VT1.5 circuit from the DS-3 card in physical slot 14 to the second VT1.5 on port 1 of the EC-1 card in physical slot 17. (Remember that the first VT1.5 has already been used.) The confirmation panel shown below appears immediately before the user can attempt to groom the 13th STS-1 circuit.



The Circuit Creation confirmation window shown below indicates that the attempt has failed because there are no available STS-1 ports on the VTX ASIC.



## Cross Connect Wallchart

Use the following PDF wallchart for more information on cross connect:

Understand the XC and XC-VT STS-1 and VT 1.5 Cross Connection Matrix wallchart.

## Related Information

- [Provisioning Cards on the ONS 15454](#)
- [Card References for the ONS 15454](#)
- [Creating and Provisioning Circuits Configuring Networks](#)
- [Optical Technology Support](#)
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