Cisco Silicon One A100 Processor

Revision 2.0

October 2025

Contents

The silicon industry has always been plagued with the trichotomy of switching silicon, routing line card silicon, and routing fabric silicon. Using these three basic building blocks, silicon and system vendors created unique architectures tuned for individual markets and industries. Consequentially, forcing customers to consume and manage these disjointed and dissimilar products caused an explosion in complexity, CapEx, and OpEx for the industry.

The Cisco Silicon One™ architecture ushers in a new era of networking, enabling one silicon architecture to address a broad market space, while simultaneously providing best-of-breed devices.

Product overview

The Cisco Silicon One A100 is a new member in the Cisco Silicon One family of devices, scaling from 200G up to 1.4Tbps and is tailored for the Access markets.

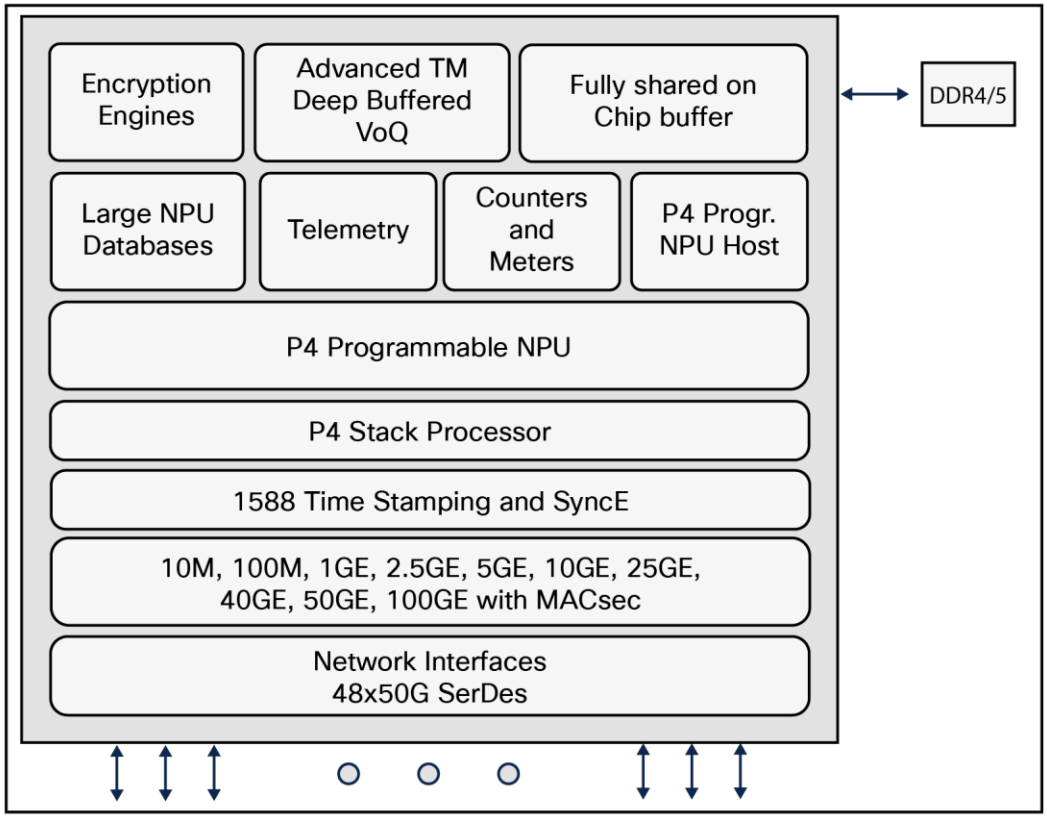

Figure 1.
A100 Block Diagram

Features and benefits

Table 1. Architectural Features and their Benefits

Feature	Benefit
Unified architecture with the rest of the Cisco Silicon One devices	Greatly simplifies customer network infrastructure deployments across multiple market segments and network roles
Unified SDK with the other members of the Cisco Silicon One product line	Provides consistent application programmability across the entire network infrastructure
Cost-effective solution for a wide range of applications	16-nm, 200G up to 1.4Tbps routing and switching
Large and fully unified packet buffer	Provides a fully shared on-die buffer, which has the option to scale up via an external DDR4/5 memory
Run-to-completion network programmable processor	Provides feature flexibility without compromising performance or power efficiency
Encryption support	Line-rate MACsec encryption across all device ports IPsec, Cisco ClearTag, and Cisco Cloudsec encryption support for IP network deployments

Technical details

Features

- 48 56G SerDes supporting NRZ and PAM4 modulation
- Flexible port configuration supporting standard 1M/10M/100M/1G/2.5G/5G/10G/25G/50G and 100G Ethernet interfaces as well as proprietary 200G and 400G high-speed stacking Ethernet interfaces
- Support for multi-MAC USXGMII and USGMII interfaces and Cisco Multigigabit Technology (10G-mGig)
- Resilient high-speed Ethernet stacking interface connecting up to 32 nodes in a ring
- Supports TSN frame preemption for 10G and 25G ports
- Large, fully shared, on-die packet buffer
- IEEE 1588v2 PTP support and SyncE support with class-C accuracy for all port speeds
- On-chip, high-performance, programmable host NPU for high-bandwidth offline packet processing (for example, OAM processing, MAC learning)
- Multiple embedded processors for CPU offloading

Traffic management

- Large pool of configurable queues, supporting DiffServ and hierarchical QoS
- Support for system-level QoS and scheduling for both unicast and multicast traffic
- Support for ingress and egress traffic mirroring
- Support for link-level (IEEE802.3x), PFC priority-level (802.1Qbb) flow control and ECN marking
- Support of port extenders

Network processor

- Run-to-completion programmable network processor
- Large and shared fungible tables
- Line rate even with complex packet processing
- Support for IPv4 fragmentation

Load balancing

- Flow load balancing using ECMP or LAG with support for hierarchical Equal Cost Multipath (ECMP) and Unequal Cost Multipath (UCMP) services

Instrumentation and telemetry

- Programmable meters used for traffic policing and coloring
- Programmable counters used for flow statistics and OAM loss measurements
- Programmable counters used for port utilization, microburst detection, delay measurements, flow tracking, and congestion tracking
- Traffic mirroring: (ER)SPAN on drop
- Support for NetFlow and sFlow
- Comprehensive IP Measurements (IPM) to monitor, analyze, and optimize IP traffic, reliability and efficiency.

Port extender

- Efficient packet processing of packets entering device via a port extender port
- Packet interface channelization for up to four port extender ports
- Support of link-level flow control per port extender port

SDK

- APIs provided in both C++ and Python
- Configurability via high-level networking objects
- Distribution-independent Linux packaging
- Robust simulation environment enables rapid feature development
- CPU packet I/O through native Linux network interfaces

Programmability framework

- Forwarding application development as well as enhancements via a P4-based IDE programming environment
- At compilation, the forwarding application generates low-level register/memory access APIs and higher-level SDK application APIs
- Support for Enterprise, Service Provider Access applications and Data-center management network
- A simulated device can be used for the development of the SDK and applications running over the SDK

A100 SDK

A sample of the features that are currently available and supported by the A100 SDK are listed below. Given that the device is programmable more features are added, as needed.

Table 2. Highlighted Key Features of the A100 SDK

Bridging • L2-Interfaces • Bridge domains • MAC table • MAC learning • Flooding • MC • Storm control • STP • Per protocol L2-interface counters • ECN support for bridged packets	**IP routing** • L3 interfaces • Switched virtual interfaces • IPV4/IPV6 LPM • Extend LPM to HBM • IPv4/IPv6 host routes • VRF • Next hop routers • Router MAC check • Per protocol L3-interface counters • Strict and loose unicast RPF • RX/TX SVI
VLAN services • Per port default VLAN selection • VLAN anywhere (dense mode) • 1 / 2 VLAN tags-based service identification • Programmable Ether-types • Support for QinQ / 802.1ad • Encapsulate 1 / 2 VLAN tag per L2/L3 interface • Private VLAN	**IP multicast** • IPv4/IPv6 multicast • PIM-SM, PIM-SSM, PIM-ASM • IGMP snooping • Multicast RPF • Directly connected sub net • Efficient LAG, vPC pruning
MPLS • LDP, LDP over TE • MPLS-segment routing • BGP LU (over LDP and SR) • TE, RSVP-TE, SR-TE • RSVP TE • MPLS label encapsulation • QoS map/EXP-based ECMP • L2-VPN/L3-VPN service • Point-to-point PWE service • Pseudowire headend (PWHE)	**SRv6** • Base format • uSID (F3216 and F4816) formats • UPD, USD, USP, PSP disposition • H.Encap.red up to 2 SIDs (11 uSIDs) • WLIB support for uSID • SR-TE • L2-VPN services, including EVPN • L3-VPN services

IP tunnels and VxLAN • IP-in-IP, GRE, GUE, VxLAN tunnel encapsulations • IPV4/IPv6 underlay support • Point to point tunnels • P2MP tunnels • EVPN control plane support • Active-active multi-homing • Head-end replication and multicast underlay • L2 and L3 VNI mapping • Extended VxLAN tunnels with recycle • Tunnel split horizon • Tenant routed multicast • Support for ECMP of tunnels • ECN propagation for IP tunnels	**Mirroring** • Rx and Tx mirror sessions with multiple simultaneous mirror copies per packet • ERSPAN v2 encapsulation • sFlow • Generic UDP header encapsulation • Mirroring based of L2 / L3 logical ports • Statistical sampling of mirrored copies • ACL-based mirroring
Crypto • 802.1AE MACsec • IPsec	**Security and QoS ACLs** • CTS/SGT • NAC • FHS • MAC-based ACLs/Time-based, Object-group
Visibility and Telemetry • IPM (Internet protocol measurement) • Streaming telemetry • Microburst detection • Copy on drop/delay • NetFlow • Packet Trace • Built-in packet generator • CFM, BFD • Histograms	

Product sustainability

Information about Cisco's Environmental, Social and Governance (ESG) initiatives and performance is provided in Cisco's CSR and sustainability reporting.

Table 3. Cisco environmental sustainability information

Sustainability topic		Reference
General	Information on product-material-content laws and regulations	Materials
	Information on electronic waste laws and regulations, including our products, batteries and packaging	WEEE Compliance
	Information on product takeback and reuse program	Cisco Takeback and Reuse Program
	Sustainability Inquiries	Contact: csr_inquiries@cisco.com
Material	Product packaging weight and materials	Contact: environment@cisco.com

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For more information

Learn more about the Cisco Silicon One.

Document history

New or revised topic	Described in	Date
Features and benefits and Technical Details	Features and benefits and Technical Details	October 3 2025

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