

Cisco Nexus K3P-S FPGA SmartNIC

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Ultra-low latency network interface card

The fastest network adapter we have built

The Cisco Nexus K3P-S FPGA SmartNIC is specifically optimized for low-latency operation.

Features software trigger-to-response latencies as low as 568ns. This is up to 20 percent faster than previous Cisco Nexus SmartNIC models, making it the fastest NIC we have built. Users will find that this drop-in replacement NIC accelerates tick-to-trade performance to previously unachievable speeds, increasing the efficacy and profitability of software-based trading systems.

Advanced software programmability

The Cisco Nexus K3P-S FPGA SmartNIC provides the most powerful programmable software interface on the market.

Programmability features include:

- **Zero-latency cost hardware flow steering**, allowing users to steer and prefilter important traffic to the right memory and CPU core with no latency penalty.
- **Cut-through receive**, which allows software to process packet fragments as they arrive from the wire, while packet tails are still in flight. This is especially effective for slow line speeds (for example, 1GbE). The Cisco Nexus K3P-S FPGA SmartNIC software API puts users well ahead of traditional store-and-forward NIC designs to make decisions faster.
- **ExaSOCK TCP/IP acceleration**: Unmodified socket applications can benefit from the speed and power of the Cisco Nexus K3P-S FPGA SmartNIC using ExaSOCK. ExaSOCK is an in-place TCP/IP socket acceleration system. ExaSOCK's Extension API allows it to seamlessly interoperate with the Cisco Nexus K3P-S FPGA SmartNIC transmit preloading feature.
- **Pre-loaded packet transmit**: The Cisco Nexus K3P-S FPGA SmartNIC allows users to preload transmit frames, saving 60ns from the transmit path. The Cisco Nexus K3P-S FPGA SmartNIC features enlarged packet transmit buffers allowing many more frames to be preloaded, leading to more versatile transmission choices.
- **High-resolution timestamps**: 4ns timestamps are applied to every received packet and the most recently transmitted packet. The Cisco Nexus K3P-S FPGA SmartNIC also features out of the box support for IEEE1588 (PTP) and high-speed capture to disk using free and open-source exact-capture software.

25GbE support

The Cisco Nexus K3P-S FPGA SmartNIC is a pure FPGA-based network adapter that also supports 25G.

Field-programmable gate array (FPGA) network adapters extend the useful life of the device by allowing new features and speed enhancements to be downloaded into a device after deployment. For example, the Cisco Nexus K3P-S FPGA SmartNIC supports 25G Ethernet speeds through a firmware update. This reduces capital expenditure on difficult infrastructure upgrades.

All FPGA design

The Cisco Nexus K3P-S FPGA SmartNIC is built using the latest generation Xilinx Ultrascale+ FPGA.

It optionally ships with 4GB of DDR4 memory for custom use. It is a compact adapter in a low-profile form-factor. Users can benefit from the pure FPGA design by offloading critical network processing functions directly into the NIC using our fast and powerful Firmware Development Kit (FDK), while maintaining the ease of use and administration of a production-grade network adapter.



Figure 1.
Cisco Nexus K3P-S FPGA SmartNIC

Performance

Typical latency, raw frames:¹

- 64 bytes: 696 ns
- 256 bytes: 897 ns

Typical latency, raw frames with preloaded TX buffer:¹

- 64 bytes: 629 ns
- 256 bytes: 665 ns

Typical latency, UDP:²

- 14 bytes: 810 ns
- 256 bytes: 1.1 μ s

Typical Latency, TCP:²

- 14 bytes: 850 ns
- 256 bytes: 1.1 μ s

Timestamping

Timestamp resolution:

- 4ns

Timestamp availability:

- All received frames, most recent transmitted frame

Time synchronization:

- Host, hardware assisted PTP, optional PPS

PPS input/output:

- 3.3V CMOS, selectable 50ohm termination

Other features

Capture:

- Line-rate capture to disk

Flow steering:

- 128 IP rules per port
- 64 MAC rules per port

Firmware Development Kit (FDK):

- Add custom user logic to the FPGA
- Fully integrated with drivers and utilities
- Xilinx Ultrascale+ XCKU3P-2
- 4GB DDR4 (optional)

General

Form factor:

- Low-profile PCI Express Card
- 117x68mm (4.65x2.67in)

Environmental:

- Operating temperature: 0 °C to 55 °C
- Storage temperature: -40 °C to 70 °C
- Operating Relative Humidity: 5% to 90% (non-condensing)
- Storage Relative Humidity: 5% to 95% (non-condensing)

Recovery:

- Manual firmware recovery button

Ports:

- 2x SFP28
- SMA for PPS in/out

Data rates:

- 25GbE, 10GbE, 1GbE, 100M Fast Ethernet

Supported media:

- Fiber (25GBASE-SR, 25GBASE-LR, 25GBASE-CR), SFP(+/28) Direct Attach

Host interface:

- PCIe x8 Gen 3 @ 8.0 GT/s per lane

Operating systems:

- Linux x86_64 (all distributions)

Notes

¹ Latencies are median latencies for raw frames from wire-userspace-wire via the libexanic library, on a 3.5Ghz Intel® Ivy Bridge processor.

² Latencies are median half-roundtrip time latencies for the sockperf benchmark using the exasock socket acceleration library. More information about benchmarking methodology is available on request.

Cisco environmental sustainability

Information about Cisco’s environmental sustainability policies and initiatives for our products, solutions, operations, and extended operations or supply chain is provided in the “Environment Sustainability” section of Cisco’s [Corporate Social Responsibility](#) (CSR) Report.

Reference links to information about key environmental sustainability topics (mentioned in the “Environment Sustainability” section of the CSR Report) are provided in the following table:

Sustainability topic	Reference
Information on product material content laws and regulations	Materials
Information on electronic waste laws and regulations, including products, batteries, and packaging	WEEE compliance

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