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Contents

1.1 extsprintf 1.3.0
   1.1.1 Available under license

1.2 lodash 4.17.21
   1.2.1 Available under license

1.3 noop-logger 0.1.1

1.4 has-unicode 2.0.1
   1.4.1 Available under license

1.5 libvorbis 1.3.7
   1.5.1 Available under license

1.6 angular-sanitize 1.4.14
   1.6.1 Available under license

1.7 depd 1.1.2
   1.7.1 Available under license

1.8 rimraf 2.7.1
   1.8.1 Available under license

1.9 opus 1.3.1
   1.9.1 Available under license

1.10 ip-address 7.1.0
   1.10.1 Available under license

1.11 semver 4.3.6
   1.11.1 Available under license

1.12 number-is-nan 1.0.1
   1.12.1 Available under license

1.13 universalify 2.0.0
   1.13.1 Available under license

1.14 fast-levenshtein 2.0.6
1.14.1 Available under license

1.15 **minimist** 1.2.5
   1.15.1 Available under license

1.16 **winston** 3.3.3
   1.16.1 Available under license

1.17 **ssh2-streams** 0.4.10
   1.17.1 Available under license

1.18 **has-cors** 1.1.0

1.19 **requirejs** 2.1.22
   1.19.1 Available under license

1.20 **types-cors** 2.8.10
   1.20.1 Available under license

1.21 **socks** 2.6.1
   1.21.1 Available under license

1.22 **http-errors** 1.7.3
   1.22.1 Available under license

1.23 **one-time** 1.0.0
   1.23.1 Available under license

1.24 **angle** ed5f62c36dc056c96e0ceb4d101c0f167903b900
   1.24.1 Available under license

1.25 **bootstrap** 4.3.1
   1.25.1 Available under license

1.26 **logform** 2.2.0
   1.26.1 Available under license

1.27 **verror** 1.10.0
   1.27.1 Available under license

1.28 **backo2** 1.0.2

1.29 **fs-minipass** 2.1.0
   1.29.1 Available under license

1.30 **type-check** 0.3.2
   1.30.1 Available under license

1.31 **string_decoder** 0.10.31
   1.31.1 Available under license

1.32 **libtiff** 4.3.0
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1.33 **request-debug** 0.2.0
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1.34 **uri-js** 4.4.1
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  1.35.1 Available under license
1.36 color-convert 1.9.3
  1.36.1 Available under license
1.37 ajv 6.12.6
  1.37.1 Available under license
1.38 http-proxy-agent 4.0.1
  1.38.1 Available under license
1.39 xmlbuilder 11.0.1
  1.39.1 Available under license
1.40 libwebp 1.2.0
  1.40.1 Available under license
1.41 nuget-commandline 2.8.60318.667
  1.41.1 Available under license
1.42 simple-swizzle 0.2.2
  1.42.1 Available under license
1.43 is-path-cwd 1.0.0
1.44 checksum 0.1.1
  1.44.1 Available under license
1.45 xz 5.0.0
  1.45.1 Available under license
1.46 minipass 3.1.3
  1.46.1 Available under license
1.47 stringify-clone 1.1.1
  1.47.1 Available under license
1.48 aws-sign2 0.7.0
  1.48.1 Available under license
1.49 serialport 9.0.7
  1.49.1 Available under license
1.50 msys2-runtime 3.2.0-3
  1.50.1 Available under license
1.51 moment 2.29.1
  1.51.1 Available under license
1.52 ansi-regex 2.1.1
  1.52.1 Available under license
1.53 ast-types 0.13.4
  1.53.1 Available under license
1.54 libcxxabi 11
  1.54.1 Available under license
1.55 tar 6.1.0
   1.55.1 Available under license
1.56 extend 3.0.2
   1.56.1 Available under license
1.57 lodash 4.17.21
   1.57.1 Available under license
1.58 tslib 2.2.0
   1.58.1 Available under license
1.59 later 1.2.0
   1.59.1 Available under license
1.60 at-least-node 1.0.0
   1.60.1 Available under license
1.61 base64-js 1.5.1
   1.61.1 Available under license
1.62 sqlite 3.34.0
   1.62.1 Available under license
1.63 estraverse 4.3.0
   1.63.1 Available under license
1.64 core-util-is 1.0.2
   1.64.1 Available under license
1.65 angular-animate 1.4.14
   1.65.1 Available under license
1.66 esprima 4.0.1
   1.66.1 Available under license
1.67 simple-concat 1.0.1
   1.67.1 Available under license
1.68 angular-xeditable 0.1.12
   1.68.1 Available under license
1.69 proxy-from-env 1.1.0
   1.69.1 Available under license
1.70 fecha 4.2.1
   1.70.1 Available under license
1.71 ini 1.3.8
   1.71.1 Available under license
1.72 punycode 2.1.1
   1.72.1 Available under license
1.73 signal-exit 3.0.3
   1.73.1 Available under license
1.74 mkdirp-classic 0.5.3
1.74.1 Available under license
1.75 safe-buffer 5.2.1
   1.75.1 Available under license
1.76 @serialport/binding-abstract 9.0.7
   1.76.1 Available under license
1.77 balanced-match 1.0.2
   1.77.1 Available under license
1.78 data-uri-to-buffer 3.0.1
   1.78.1 Available under license
1.79 serialport-parser-cctalk 9.0.7
   1.79.1 Available under license
1.80 libsrt 2.3.0
   1.80.1 Available under license
1.81 angular-recaptcha 4.1.5
   1.81.1 Available under license
1.82 json-stringify-safe 5.0.1
   1.82.1 Available under license
1.83 util-deprecate 1.0.2
   1.83.1 Available under license
1.84 socket.io-adapter 2.1.0
   1.84.1 Available under license
1.85 visual-studio-runtime 11.0.610330.1
   1.85.1 Available under license
1.86 set-blocking 2.0.0
   1.86.1 Available under license
1.87 object-hash 2.1.1
   1.87.1 Available under license
1.88 ip 1.1.5
1.89 esutils 2.0.3
   1.89.1 Available under license
1.90 del 3.0.0
   1.90.1 Available under license
1.91 @serialport/stream 9.0.7
   1.91.1 Available under license
1.92 globby 6.1.0
   1.92.1 Available under license
1.93 pac-resolver 4.2.0
   1.93.1 Available under license
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1.94.1 Available under license

1.95 **flutter 2.0.5**
1.95.1 Available under license

1.96 **delegates 1.0.0**
1.96.1 Available under license

1.97 **readable-stream 1.1.14**
1.97.1 Available under license

1.98 **cygwin 3.2.0**
1.98.1 Available under license

1.99 **har-schema 2.0.0**
1.99.1 Available under license

1.100 **colorscape 1.1.2**
1.100.1 Available under license

1.101 **c-ares 1.17.1**
1.101.1 Available under license

1.102 **https-proxy-agent 5.0.0**
1.102.1 Available under license

1.103 **engine.io-client 4.1.4**
1.103.1 Available under license

1.104 **file-stream-rotator 0.5.7**
1.104.1 Available under license

1.105 **requirejs-domready 2.0.1**
1.105.1 Available under license

1.106 **deep-extend 0.6.0**
1.106.1 Available under license

1.107 **winston-daily-rotate-file 4.5.4**
1.107.1 Available under license

1.108 **nan 2.14.2**
1.108.1 Available under license

1.109 **cookie 0.4.1**
1.109.1 Available under license

1.110 **is-path-in-cwd 1.0.1**
1.110.1 Available under license

1.111 **json-cpp 1.9.4**
1.111.1 Available under license

1.112 **xregexp 2.0.0**
1.112.1 Available under license

1.113 **cryptojslib 3.1.2**
1.113.1 Available under license
1.114 types-cookie 0.4.0
  1.114.1 Available under license
1.115 p-map 1.2.0
  1.115.1 Available under license
1.116 har-validator 5.1.5
  1.116.1 Available under license
1.117 jquery-gritter 1.7.4
  1.117.1 Available under license
1.118 assert-plus 1.0.0
1.119 forever-agent 0.6.1
  1.119.1 Available under license
1.120 strip-json-comments 2.0.1
  1.120.1 Available under license
1.121 npmlog 4.1.2
  1.121.1 Available under license
1.122 llvm 11.0.0
  1.122.1 Available under license
1.123 socket.io-client 3.1.3
  1.123.1 Available under license
1.124 zlib 1.2.11
  1.124.1 Available under license
1.125 is-typedarray 1.0.0
  1.125.1 Available under license
1.126 @dabh/diagnostics 2.0.2
  1.126.1 Available under license
1.127 tar-fs 2.1.1
  1.127.1 Available under license
1.128 color-string 1.5.5
  1.128.1 Available under license
1.129 csv-parse 4.15.4
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1.130 http-signature 1.2.0
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1.131 pity 3.0.0
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1.132 jsbn 0.1.1
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  1.133.1 Available under license
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   1.134.1 Available under license
1.135 minizlib 2.1.2
   1.135.1 Available under license
1.136 sax 1.2.4
   1.136.1 Available under license
1.137 vis 4.15.1
   1.137.1 Available under license
1.138 fast-safe-stringify 2.0.7
   1.138.1 Available under license
1.139 chardet 1.3.0
   1.139.1 Available under license
1.140 aws-sdk-js 2.901.0
   1.140.1 Available under license
1.141 @serialport/parser-inter-byte-timeout 9.0.7
   1.141.1 Available under license
1.142 socket.io 3.1.2
   1.142.1 Available under license
1.143 pubsub-js 1.5.8
   1.143.1 Available under license
1.144 bcrypt-pbkdf 1.0.2
   1.144.1 Available under license
1.145 smart-buffer 4.1.0
   1.145.1 Available under license
1.146 serialport-parser-ready 9.0.7
   1.146.1 Available under license
1.147 code-point-at 1.1.0
   1.147.1 Available under license
1.148 safer-buffer 2.1.2
   1.148.1 Available under license
1.149 escodegen 1.14.3
   1.149.1 Available under license
1.150 streamsearch 0.1.2
   1.150.1 Available under license
1.151 wordwrap 0.0.3
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   1.174.1 Available under license
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   1.175.1 Available under license
1.176 serialport-parser-byte-length 9.0.7
   1.176.1 Available under license
1.177 fast-json-stable-stringify 2.1.0
   1.177.1 Available under license
1.178 brotli 1.0.9
   1.178.1 Available under license
1.179 form-data 2.3.3
   1.179.1 Available under license
1.180 isarray 0.0.1
   1.180.1 Available under license
1.181 angular-route 1.4.14
   1.181.1 Available under license
1.182 agent-base 6.0.2
   1.182.1 Available under license
1.183 simple-get 3.1.0
   1.183.1 Available under license
1.184 libvpx 1.9.0-147-g61edec1ef
   1.184.1 Available under license
1.185 stack-trace 0.0.10
   1.185.1 Available under license
1.186 performance-now 2.1.0
   1.186.1 Available under license
1.187 statuses 1.5.0
   1.187.1 Available under license
1.188 delayed-stream 1.0.0
   1.188.1 Available under license
1.189 cors 2.8.5
   1.189.1 Available under license
1.190 object-assign 4.1.1
   1.190.1 Available under license
1.191 glob 7.1.6
   1.191.1 Available under license
1.192 negotiator 0.6.2
1.193 color 3.0.0
  1.193.1 Available under license
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  1.194.1 Available under license
1.195 socket.io-parser 4.0.4
  1.195.1 Available under license
1.196 moment 2.29.1
  1.196.1 Available under license
1.197 file-uri-to-path 2.0.0
  1.197.1 Available under license
1.198 setprototypeof 1.1.1
1.199 xmlhttprequest 1.8.0
  1.199.1 Available under license
1.200 getpass 0.1.7
  1.200.1 Available under license
1.201 ots 8.1.3
  1.201.1 Available under license
1.202 prelude-ls 1.1.2
  1.202.1 Available under license
1.203 is-stream 2.0.0
  1.203.1 Available under license
1.204 libcxx 11
  1.204.1 Available under license
1.205 buffer 5.7.1
  1.205.1 Available under license
1.206 is-fullwidth-code-point 1.0.0
  1.206.1 Available under license
1.207 minimatch 3.0.4
  1.207.1 Available under license
1.208 @serialport/binding-mock 9.0.7
  1.208.1 Available under license
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  1.209.1 Available under license
1.210 jsonschema 0.2.3
  1.210.1 Available under license
1.211 mime-db 1.47.0
  1.211.1 Available under license
1.212 dashdash 1.14.1
  1.212.1 Available under license
1.213 pump 3.0.0
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  1.215.1 Available under license
1.216 @types/component-emitter 1.2.10
  1.216.1 Available under license
1.217 nghttp2 2.1.3
  1.217.1 Available under license
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  1.219.1 Available under license
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1.221 paralleljs 1.1.0
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  1.222.1 Available under license
1.223 iconv-lite 0.6.2
  1.223.1 Available under license
1.224 base64id 2.0.0
  1.224.1 Available under license
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1.226 async 2.6.3
  1.226.1 Available under license
1.227 ieee754 1.2.1
  1.227.1 Available under license
1.228 expand-template 2.0.3
  1.228.1 Available under license
1.229 jsprim 1.4.1
  1.229.1 Available under license
1.230 concat-map 0.0.1
  1.230.1 Available under license
1.231 ms 2.1.2
  1.231.1 Available under license
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1.232.1 Available under license
1.233 word-wrap 1.2.3
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1.234 node-abi 2.26.0
1.234.1 Available under license
1.235 deep-is 0.1.3
1.235.1 Available under license
1.236 socks-proxy-agent 5.0.0
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1.237 pac-proxy-agent 4.1.0
1.237.1 Available under license
1.238 fs-extra 9.1.0
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1.242 tar-stream 2.2.0
1.242.1 Available under license
1.243 combined-stream 1.0.8
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1.244 angular-resource 1.4.14
1.244.1 Available under license
1.245 libusb 1.0.17
1.245.1 Available under license
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1.246.1 Available under license
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1.248 proxy-agent 4.0.1
1.248.1 Available under license
1.249 toidentifier 1.0.0
1.250 decompress-response 4.2.1
1.250.1 Available under license
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1.251.1 Available under license
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1.252.1 Available under license
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1.257 string-width 1.0.2
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   1.259.1 Available under license
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   1.267.1 Available under license
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1.275 vary 1.1.2
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1.28 backo2 1.0.2

1.29 fs-minipass 2.1.0

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1.31 string_decoder 0.10.31

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1.34 uri-js 4.4.1

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1.36 color-convert 1.9.3
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1.37 ajv 6.12.6
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1.38 http-proxy-agent 4.0.1

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http-proxy-agent

============

### An HTTP(s) proxy `http.Agent` implementation for HTTP

[![Build Status](https://github.com/TooTallNate/node-http-proxy-agent/workflows/Node%20CI/badge.svg)](https://github.com/TooTallNate/node-http-proxy-agent/actions?workflow=Node+CI)

This module provides an `http.Agent` implementation that connects to a specified HTTP or HTTPS proxy server, and can be used with the built-in `http` module.

__Note:__ For HTTP proxy usage with the `https` module, check out [node-https-proxy-agent](https://github.com/TooTallNate/node-https-proxy-agent).

Installation

----------

Install with `npm`:

```bash
$ npm install http-proxy-agent
```

Example
```js
var url = require('url');
var http = require('http');
var HttpProxyAgent = require('http-proxy-agent');

// HTTP/HTTPS proxy to connect to
var proxy = process.env.http_proxy || 'http://168.63.76.32:3128';
console.log('using proxy server %j', proxy);

// HTTP endpoint for the proxy to connect to
console.log('attempting to GET %j', endpoint);
var opts = url.parse(endpoint);

// create an instance of the `HttpProxyAgent` class with the proxy server information
var agent = new HttpProxyAgent(proxy);
opts.agent = agent;

http.get(opts, function (res) {
    console.log('"response" event!', res.headers);
    res.pipe(process.stdout);
});
```

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Found in path(s):
* /opt/cola/permits/1103324354_1604083584.71/0/http-proxy-agent-4-0-1-1-tgz/package/README.md

1.39 xmlbuilder 11.0.1
1.39.1 Available under license:

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1.41 nuget-commandline 2.8.60318.667

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1.47 stringify-clone 1.1.1

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1.48 aws-sign2 0.7.0

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1.50 msys2-runtime 3.2.0-3

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1.78 data-uri-to-buffer 3.0.1

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data-uri-to-buffer

==================

### Generate a Buffer instance from a [Data URI][rfc] string

This module accepts a ["data" URI][rfc] String of data, and returns a node.js `Buffer` instance with the decoded data.

Installation

-------------

Install with `npm`:

```
```bash
$ npm install data-uri-to-buffer
```

Example

-------

```js
var dataUriToBuffer = require('data-uri-to-buffer');

// plain-text data is supported
var uri = 'data:,Hello%2C%20World!';
var decoded = dataUriToBuffer(uri);
console.log(decoded.toString());
// 'Hello, World!'

// base64-encoded data is supported
uri = 'data:text/plain;base64,SGVsbG8sIFdvcmxkIQ%3D%3D';
decoded = dataUriToBuffer(uri);
console.log(decoded.toString());
// 'Hello, World!'
```
### dataUriToBuffer(String uri) → Buffer

The `type` property on the Buffer instance gets set to the main type portion of the "mediatype" portion of the "data" URI, or defaults to "text/plain" if not specified.

The `typeFull` property on the Buffer instance gets set to the entire "mediatype" portion of the "data" URI (including all parameters), or defaults to "text/plain;charset=UTF-8" if not specified.

The `charset` property on the Buffer instance gets set to the Charset portion of the "mediatype" portion of the "data" URI, or defaults to "US-ASCII" if the entire type is not specified, or defaults to "" otherwise.

*Note*: If the only the main type is specified but not the charset, e.g. "data:text/plain,abc", the charset is set to the empty string. The spec only defaults to US-ASCII as charset if the entire type is not specified.

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Found in path(s):
* /opt/cola/permits/1160410767_1620316452.69/0/pac-resolver-4-2-0-tgz/package/README.md

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* /opt/cola/permits/1161428728_1620664037.68/0/libphonenumber-8-10-18-sources-jar/com/google/phonenumbers/PhoneNumberMatch.java
* /opt/cola/permits/1161428728_1620664037.68/0/libphonenumber-8-10-18-sources-jar/com/google/phonenumbers/PhoneNumberMatcher.java
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* /opt/cola/permits/1161428728_1620664037.68/0/libphonenumber-8-10-18-sources-jar/com/google/phonenumbers/Phonemetadata.java
* /opt/cola/permits/1161428728_1620664037.68/0/libphonenumber-8-10-18-sources-jar/com/google/phonenumbers/CountryCodeToRegionCodeMap.java
* /opt/cola/permits/1161428728_1620664037.68/0/libphonenumber-8-10-18-sources-jar/com/google/phonenumbers/Phonenumber.java
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jar/com/google/i18n/phonenumbers/MetadataManager.java
* /opt/cola/permits/1161428728_1620664037.68/0/libphonenumber-8-10-18-sources-
jar/com/google/i18n/phonenumbers/AlternateFormatsCountryCodeSet.java
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jar/com/google/i18n/phonenumbers/ShortNumberInfo.java
* /opt/cola/permits/1161428728_1620664037.68/0/libphonenumber-8-10-18-sources-
jar/com/google/i18n/phonenumbers/ShortNumbersRegionCodeSet.java
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* /opt/cola/permits/1161428728_1620664037.68/0/libphonenumber-8-10-18-sources-jar/com/google/i18n/phonenumbers/NumberParseException.java
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* /opt/cola/permits/1161428728_1620664037.68/0/libphonenumber-8-10-18-sources-jar/com/google/i18n/phonenumbers/SingleFileMetadataSourceImpl.java
* /opt/cola/permits/1161428728_1620664037.68/0/libphonenumber-8-10-18-sources-jar/com/google/i18n/phonenumbers/MetadataSource.java
* /opt/cola/permits/1161428728_1620664037.68/0/libphonenumber-8-10-18-sources-jar/com/google/i18n/phonenumbers/MultiFileMetadataSourceImpl.java

1.95 flutter 2.0.5

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import 'package:flutter_tools/src/base/file_system.dart';
import 'package:flutter_tools/src/convert.dart';
import 'package:flutter_tools/src/license_collector.dart';
import 'package:package_config/package_config.dart';
import 'package:package_config/package_config_types.dart';

import '../src/common.dart';

const String _kMitLicense = r""
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```
void main() {
  FileSystem fileSystem;
  LicenseCollector licenseCollector;

  setUp() {
    fileSystem = MemoryFileSystem.test();
    licenseCollector = LicenseCollector(fileSystem: fileSystem);
  };

  testWithoutContext('processes dependent licenses according to instructions', () async {
    fileSystem.file('foo/NOTICES')
      ..createSync(recursive: true)
      ..writeAsStringSync(_kMitLicense);
```
fileSystem.file('bar/NOTICES')
..createSync(recursive: true)
..writeAsStringSync(_kApacheLicense);
// NOTICES is preferred over LICENSE

fileSystem.file('bar/LICENSE')
..createSync(recursive: true)
..writeAsStringSync('SHOULD NOT BE INCLUDED');

fileSystem.file('fizz/LICENSE')
..createSync(recursive: true)
..writeAsStringSync(_kMitLicense); // intentionally a duplicate

definal File packageConfigFile = fileSystem.file('package_config.json')
..writeAsStringSync(json.encode(<String, Object>{
    'configVersion': 2,
    'packages': <Object>[{
        'name': 'foo',
        'rootUri': 'file:///foo/",
        'packageUri': 'lib/",
        'languageVersion': '2.2'
    },
    <String, Object>{
        'name': 'bar',
        'rootUri': 'file:///bar/",
        'packageUri': 'lib/",
        'languageVersion': '2.2'
    },
    <String, Object>{
        'name': 'fizz',
        'rootUri': 'file:///fizz/",
        'packageUri': 'lib/",
        'languageVersion': '2.2'
    }
}],
});
definal PackageConfig packageConfig = await loadPackageConfig(packageConfigFile.absolute);
definal LicenseResult result = licenseCollector.obtainLicenses(packageConfig, <String, List<File>>{ });

    // All included licenses are combined in the result.
expect(result.combinedLicenses, contains(_kApacheLicense));
expect(result.combinedLicenses, contains(_kMitLicense));

    // String from LICENSE file was not included when NOTICES exists.
expect(result.combinedLicenses, isNot(contains('SHOULD NOT BE INCLUDED')));

    // Licenses are de-duplicated correctly.

result.combinedLicenses.split(LicenseCollector.licenseSeparator).hasLength(2));

// All input licenses included in result.
final Iterable<String> filePaths = result.dependencies.map((File file) => file.path);
expect(filePaths, unorderedEquals(<String>[ '/foo/NOTICES', '/bar/NOTICES', '/fizz/LICENSE' ]));
});

}));

testWithoutContext('includes additional LICENSE files as specified by pubspec.yaml', () async {
  fileSystem.file('foo/NOTICES')
    ..createSync(recursive: true)
    ..writeAsStringSync(_kMitLicense);
  fileSystem.file('bar/NOTICES')
    ..createSync(recursive: true)
    ..writeAsStringSync(_kApacheLicense);
  fileSystem.file('foo.txt').writeAsStringSync('foo.txt');
  fileSystem.file('bar.txt').writeAsStringSync('bar.txt');

  final File packageConfigFile = fileSystem.file('package_config.json')
    ..writeAsStringSync(json.encode(<String, Object>{
      'configVersion': 2,
      'packages': <Object>{
        'name': 'foo',
        'rootUri': 'file:///foo/',
        'packageUri': 'lib/',
        'languageVersion': '2.2'
      },
      <String, Object>{
        'name': 'bar',
        'rootUri': 'file:///bar/',
        'packageUri': 'lib/',
        'languageVersion': '2.2'
      }
    },
    ]
  )
  );
  final PackageConfig packageConfig = await loadPackageConfig(packageConfigFile.absolute);
  final LicenseResult result = licenseCollector.obtainLicenses(packageConfig, <String, List<File>>{
    'foo': <File>[fileSystem.file('foo.txt').absolute],
    'bar': <File>[fileSystem.file('bar.txt').absolute],
  });

  // Additional license files are included in the result.
expect(result.combinedLicenses, contains(_kApacheLicense));
expect(result.combinedLicenses, contains(_kMitLicense));
expect(result.combinedLicenses, contains('foo.txt'));
expect(result.combinedLicenses, contains('bar.txt'));

// All input licenses included in result.
final Iterable<String> filePaths = result.dependencies.map((File file) => file.path);
expect(filePaths, unorderedEquals(<String>[
  '/foo/NOTICES',
  '/bar/NOTICES',
  '/foo.txt',
  '/bar.txt',
]));
}
);

testWithoutContext('Returns a LicenseResult with an error message if an additional LICENSE file does not exist', () async {
  fileSystem.file('foo/NOTICES')
    ..createSync(recursive: true)
    ..writeAsStringSync(_kMitLicense);
  final File packageConfigFile = fileSystem.file('package_config.json')
    ..writeAsStringSync(json.encode(<String, Object>{
      'configVersion': 2,
      'packages': <Object>[<String, Object>{
        'name': 'foo',
        'rootUri': 'file:///foo/',
        'packageUri': 'lib/',
        'languageVersion': '2.2'
      }],
    }));
  final PackageConfig packageConfig = await loadPackageConfig(packageConfigFile.absolute);

  final LicenseResult licenseResult = licenseCollector.obtainLicenses(packageConfig, <String, List<File>>{
    'foo': <File>[fileSystem.file('foo.txt').absolute, fileSystem.file('foo_2.txt').absolute], // Files do not exist.
  });

  expect(licenseResult.combinedLicenses, '');
  expect(licenseResult.dependencies, isEmpty);
  expect(licenseResult.errorMessages, <String>[
    'package foo specified an additional license at /foo.txt, but this file does not exist.',
    'package foo specified an additional license at /foo_2.txt, but this file does not exist.'
  ]);}
);
testWithoutContext('Returns a LicenseResult with an error message if an additional license file is not valid utf8', () async {
    fileSystem.file('foo/NOTICES')
        ..createSync(recursive: true)
        ..writeAsStringSync(_kMitLicense);
    fileSystem.file('foo.txt')
        ..createSync(recursive: true)
        ..writeAsBytesSync(<int>[0xFFFE]);

    final File packageConfigFile = fileSystem.file('package_config.json')
        ..writeAsStringSync(json.encode(
            <String, Object>[
                'configVersion': 2,
                'packages': <Object>[
                    <String, Object>[
                        'name': 'foo',
                        'rootUri': 'file:///foo/',
                        'packageUri': 'lib/',
                        'languageVersion': '2.2'
                    ],
                ],
            ],
        ));
    final PackageConfig packageConfig = await loadPackageConfig(packageConfigFile.absolute);

    final LicenseResult licenseResult = licenseCollector.obtainLicenses(packageConfig, <String, List<File>>{
        'foo': <File>[fileSystem.file('foo.txt').absolute],
    });

    expect(licenseResult.combinedLicenses, '');
    expect(licenseResult.dependencies, isEmpty);
    expect(licenseResult.errorMessages.single,
        'package foo specified an additional license at /foo.txt, but this file could not be read:

       FormatException: Invalid UTF-8 byte (at offset 0)',
    );
});

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abseil-cpp

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DOCUMENTATION ROADMAP

This file contains the following sections:

OVERVIEW General description of JPEG and the IJK software.
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REFERENCES Where to learn more about JPEG.
ARCHIVE LOCATIONS Where to find newer versions of this software.
FILE FORMAT WARS Software *not* to get.
TO DO Plans for future IJG releases.

Other documentation files in the distribution are:

User documentation:
usage.txt Usage instructions for cjpeg, djpeg, jpegtran, rdjpgcom, and wrjpgcom.
*.1 Unix-style man pages for programs (same info as usage.txt).
wizard.txt Advanced usage instructions for JPEG wizards only.
change.log Version-to-version change highlights.

Programmer and internal documentation:
libjpeg.txt How to use the JPEG library in your own programs.
extample.c Sample code for calling the JPEG library.
structure.txt Overview of the JPEG library's internal structure.
coderules.txt Coding style rules --- please read if you contribute code.

Please read at least usage.txt. Some information can also be found in the JPEG FAQ (Frequently Asked Questions) article. See ARCHIVE LOCATIONS below to find out where to obtain the FAQ article.

If you want to understand how the JPEG code works, we suggest reading one or more of the REFERENCES, then looking at the documentation files (in roughly the order listed) before diving into the code.

OVERVIEW
========

This package contains C software to implement JPEG image encoding, decoding, and transcoding. JPEG (pronounced "jay-peg") is a standardized compression method for full-color and grayscale images. JPEG's strong suit is compressing photographic images or other types of images that have smooth color and brightness transitions between neighboring pixels. Images with sharp lines or other abrupt features may not compress well with JPEG, and a higher JPEG quality may have to be used to avoid visible compression artifacts with such images.

JPEG is lossy, meaning that the output pixels are not necessarily identical to the input pixels. However, on photographic content and other "smooth" images, very good compression ratios can be obtained with no visible compression artifacts, and extremely high compression ratios are possible if you are willing to sacrifice image quality (by reducing the "quality" setting in the compressor.)

This software implements JPEG baseline, extended-sequential, and progressive compression processes. Provision is made for supporting all variants of these
processes, although some uncommon parameter settings aren't implemented yet. We have made no provision for supporting the hierarchical or lossless processes defined in the standard.

We provide a set of library routines for reading and writing JPEG image files, plus two sample applications "cjpeg" and "djpeg", which use the library to perform conversion between JPEG and some other popular image file formats. The library is intended to be reused in other applications.

In order to support file conversion and viewing software, we have included considerable functionality beyond the bare JPEG coding/decoding capability; for example, the color quantization modules are not strictly part of JPEG decoding, but they are essential for output to colormapped file formats or colormapped displays. These extra functions can be compiled out of the library if not required for a particular application.

We have also included "jpegtran", a utility for lossless transcoding between different JPEG processes, and "rdjpgcom" and "wrjpgcom", two simple applications for inserting and extracting textual comments in JFIF files.

The emphasis in designing this software has been on achieving portability and flexibility, while also making it fast enough to be useful. In particular, the software is not intended to be read as a tutorial on JPEG. (See the REFERENCES section for introductory material.) Rather, it is intended to be reliable, portable, industrial-strength code. We do not claim to have achieved that goal in every aspect of the software, but we strive for it.

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The Unix configuration script "configure" was produced with GNU Autoconf. It is copyright by the Free Software Foundation but is freely distributable. The same holds for its supporting scripts (config.guess, config.sub, ltmain.sh). Another support script, install-sh, is copyright by X Consortium but is also freely distributable.

The IJG distribution formerly included code to read and write GIF files. To avoid entanglement with the Unisys LZW patent (now expired), GIF reading support has been removed altogether, and the GIF writer has been simplified to produce "uncompressed GIFs". This technique does not use the LZW algorithm; the resulting GIF files are larger than usual, but are readable by all standard GIF decoders.

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We recommend reading one or more of these references before trying to understand the innards of the JPEG software.

The best short technical introduction to the JPEG compression algorithm is Wallace, Gregory K. "The JPEG Still Picture Compression Standard", Communications of the ACM, April 1991 (vol. 34 no. 4), pp. 30–44. (Adjacent articles in that issue discuss MPEG motion picture compression, applications of JPEG, and related topics.) If you don't have the CACM issue handy, a PDF file containing a revised version of Wallace's article is available at http://www.ijg.org/files/Wallace.JPEG.pdf. The file (actually a preprint for an article that appeared in IEEE Trans. Consumer Electronics) omits the sample images that appeared in CACM, but it includes corrections and some added material. Note: the Wallace article is copyright ACM and IEEE, and it may not be used for commercial purposes.

A somewhat less technical, more leisurely introduction to JPEG can be found in "The Data Compression Book" by Mark Nelson and Jean-loup Gailly, published by M&T Books (New York), 2nd ed. 1996, ISBN 1-55851-434-1. This book provides good explanations and example C code for a multitude of compression methods including JPEG. It is an excellent source if you are comfortable reading C code but don't know much about data compression in general. The book's JPEG sample code is far from industrial-strength, but when you are ready to look at a full implementation, you've got one here...


The JPEG standard does not specify all details of an interchangeable file format. For the omitted details we follow the "JFIF" conventions, revision 1.02. JFIF 1.02 has been adopted as an Ecma International Technical Report and thus received a formal publication status. It is available as a free download in PDF format from

The TIFF 6.0 file format specification can be obtained by FTP from ftp://ftp.sgi.com/graphics/tiff/TIFF6.ps.gz. The JPEG incorporation scheme found in the TIFF 6.0 spec of 3-June-92 has a number of serious problems. IJG does not recommend use of the TIFF 6.0 design (TIFF Compression tag 6). Instead, we recommend the JPEG design proposed by TIFF Technical Note #2 (Compression tag 7). Copies of this Note can be obtained from http://www.iijg.org/files/. It is expected that the next revision of the TIFF spec will replace the 6.0 JPEG design with the Note's design. Although IJG's own code does not support TIFF/JPEG, the free libtiff library uses our library to implement TIFF/JPEG per the Note.

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(In any case, our decoder will remain capable of reading existing JPEG image files indefinitely.)

TO DO
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Please send bug reports, offers of help, etc. to jpeg-info@jpegclub.org.

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tcmalloc

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vulkanmemoryallocator

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import 'package:meta/meta.dart';
import 'package:package_config/package_config.dart';

import 'base/file_system.dart';

/// Processes dependencies into a string representing the NOTICES file.
///
/// Reads the NOTICES or LICENSE file from each package in the .packages file, splitting each one into each component license so that it can be de-duped if possible. If the NOTICES file exists, it is preferred over the LICENSE file.
///
/// Individual licenses inside each LICENSE file should be separated by 80 hyphens on their own on a line.
///
/// If a LICENSE or NOTICES file contains more than one component license, then each component license must start with the names of the packages to which the component license applies, with each package name on its own line and the list of package names separated from the actual license text by a blank line. The packages need not match the names of the pub package. For example, a package might itself contain code from multiple third-party sources, and might need to include a license for each one.

class LicenseCollector {
  LicenseCollector({
    @required FileSystem fileSystem
  }) : _fileSystem = fileSystem;

  final FileSystem _fileSystem;

  /// The expected separator for multiple licenses.
  static final String licenseSeparator = '
' + ('-' * 80) + '
';

  /// Obtain licenses from the `packageMap` into a single result.
  ///
  /// [additionalLicenses] should contain aggregated license files from all
  /// of the current applications dependencies.
  LicenseResult obtainLicenses(}
for (final Package package in packageConfig.packages) {
  final Uri packageUri = package.packageUriRoot;
  if (packageUri == null || packageUri.scheme != 'file') {
    continue;
  }
  // First check for NOTICES, then fallback to LICENSE
  File file = _fileSystem.file(packageUri.resolve('../NOTICES'));
  if (!file.existsSync()) {
    file = _fileSystem.file(packageUri.resolve('../LICENSE'));
  }
  if (!file.existsSync()) {
    continue;
  }
  dependencies.add(file);
}

final List<String> rawLicenses = file
  .readAsStringSync()
  .split(licenseSeparator);
for (final String rawLicense in rawLicenses) {
  List<String> packageNames;
  String licenseText;
  if (rawLicenses.length > 1) {
    final int split = rawLicense.indexOf('

');
    if (split >= 0) {
      packageNames = rawLicense.substring(0, split).split('
');
      licenseText = rawLicense.substring(split + 2);
    } else {
      packageNames = [package.name];
      licenseText = rawLicense;
    }
  } else {
    packageNames = [package.name];
    licenseText = rawLicense;
  }
  packageLicenses.putIfAbsent(licenseText, () => [String]()).addAll(packageNames);
  allPackages.addAll(packageNames);
}

final List<String> combinedLicensesList = packageLicenses.keys
  .map<String>((String license) {
    final List<String> packageNames = packageLicenses[license].toList()
      .sort();
return `packageNames.join("\n") + \\
"\n\n + license;
}).toList();
combinedLicensesList.sort();

/// Append additional LICENSE files as specified in the pubspec.yaml.
final List<String> additionalLicenseText = <String>[];
final List<String> errorMessages = <String>[
for (final String package in additionalLicenses.keys) {
  for (final File license in additionalLicenses[package]) {
    if (!license.existsSync()) {
      errorMessages.add(
        'package $package specified an additional license at ${license.path}, but this file ' 
        'does not exist.'
      );
      continue;
    }
    dependencies.add(license);
    try {
      additionalLicenseText.add(license.readAsStringSync());
    } on FormatException catch (err) {
      // File has an invalid encoding.
      errorMessages.add(
        'package $package specified an additional license at ${license.path}, but this file ' 
        'could not be read:\n$err'
      );
    } on FileSystemException catch (err) {
      // File cannot be parsed.
      errorMessages.add(
        'package $package specified an additional license at ${license.path}, but this file ' 
        'could not be read:\n$err'
      );
    }
  }
}
if (errorMessages.isNotEmpty) {
  return LicenseResult(
    combinedLicenses: '',
    dependencies: <File>[],
    errorMessages: errorMessages,
  );
}

final String combinedLicenses = combinedLicensesList
  .followedBy(additionalLicenseText)
  .join(licenseSeparator);

return LicenseResult(
  combinedLicenses: combinedLicenses,
class LicenseResult {
  const LicenseResult({
    @required this.combinedLicenses,
    @required this.dependencies,
    @required this.errorMessages,
  });
}

/// The result of processing licenses with a [LicenseCollector].
class LicenseResult {
  const LicenseResult({
    @required this.combinedLicenses,
    @required this.dependencies,
    @required this.errorMessages,
  });
}

/// The raw text of the consumed licenses.
final String combinedLicenses;

/// Each license file that was consumed as input.
final List<File> dependencies;

/// If non-empty, license collection failed and this messages should
/// be displayed by the asset parser.
final List<String> errorMessages;

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import 'package:flutter/foundation.dart';
import 'package:flutter/material.dart';
import 'package:flutter_driver/driver_extension.dart';

/// This application does nothing but show a screen with the flutter package license in it.

void main() {
  enableFlutterDriverExtension();
  runApp(ShowLicenses());
}

class ShowLicenses extends StatelessWidget {
  Widget _buildTestResultWidget(
   BuildContext context,
    AsyncSnapshot<List<LicenseEntry>> snapshot,
  ) {
    final List<LicenseEntry> entries = snapshot.data;
    String flutterPackage = "";
    final List<String> flutterParagraphs = <String>[
    ];
    String enginePackage = "";
    final List<String> engineParagraphs = <String>[
    ];
    for (final LicenseEntry entry in entries) {
      if (entry.packages.contains('flutter')) {
        flutterPackage = 'flutter';
        flutterParagraphs.addAll(
          entry.paragraphs.map<String>((LicenseParagraph para) => para.text),
        );
      }
      if (entry.packages.contains('engine')) {
        enginePackage = 'engine';
        engineParagraphs.addAll(
          entry.paragraphs.map<String>((LicenseParagraph para) => para.text),
        );
      }
    }
  }
}
final List<Widget> result = <Widget>[];
if (entries.isNotEmpty) {
    result.addAll(<Widget>[
        const Text('License Check Test', key: ValueKey<String>('Header')),
        Text(flutterPackage, key: const ValueKey<String>('FlutterPackage')),
        Text(flutterParagraphs.join(' '), key: const ValueKey<String>('FlutterLicense')),
        Text('${flutterParagraphs.length}', key: const ValueKey<String>('FlutterCount')),
        Text(enginePackage, key: const ValueKey<String>('EnginePackage')),
        Text(engineParagraphs.join(' '), key: const ValueKey<String>('EngineLicense')),
        Text('${engineParagraphs.length}', key: const ValueKey<String>('EngineCount')),
    ]);}
}

return ListView(
    children: result,
);}

@override
Widget build(BuildContext context) {
    return MaterialApp(
        home: Scaffold(
            body: FutureBuilder<List<LicenseEntry>>(
                initialData: const <LicenseEntry>[],
                builder: _buildTestResultWidget,
                future: LicenseRegistry.licenses.toList(),
            ),
        ),
    );
}

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OWNER OR CONTRIBUTORS BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL,
import 'package:meta/meta.dart' show visibleForTesting;

typedef LicenseEntryCollector = Stream<LicenseEntry> Function();

class LicenseParagraph {
  const LicenseParagraph(this.text, this.indent);

  final String text;
  final int indent;
  final int centeredIndent = -1;

  /// Creates a string for a license entry paragraph.
  const LicenseParagraph(this.text, this.indent);

  /// The text of the paragraph. Should not have any leading or trailing whitespace.
  final String text;

  /// How many steps of indentation the paragraph has.
  ///
  /// * 0 means the paragraph is not indented.
  /// * 1 means the paragraph is indented one unit of indentation.
  /// * 2 means the paragraph is indented two units of indentation.
  ///
  /// ...and so forth.
  ///
  /// In addition, the special value [centeredIndent] can be used to indicate
  /// that rather than being indented, the paragraph is centered.
  final int indent; // can be set to centeredIndent

  /// A constant that represents "centered" alignment for [indent].
  static const int centeredIndent = -1;
}

abstract class LicenseEntry {
/// Abstract const constructor. This constructor enables subclasses to provide
/// const constructors so that they can be used in const expressions.
const LicenseEntry();

/// The names of the packages that this license entry applies to.
Iterable<String> get packages;

/// The paragraphs of the license, each as a [LicenseParagraph] consisting of
/// a string and some formatting information. Paragraphs can include newline
/// characters, but this is discouraged as it results in ugliness.
Iterable<LicenseParagraph> get paragraphs;

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```;
```
```

/// This would result in a license with six [paragraphs], the third, fourth, and
/// fifth being indented one level.
```
```
```

## Performance considerations

/// Computing the paragraphs is relatively expensive. Doing the work for one
/// license per frame is reasonable; doing more at the same time is ill-advised.
/// Consider doing all the work at once using [compute] to move the work to
/// another thread, or spreading the work across multiple frames using
/// [SchedulerBinding.scheduleTask].

class LicenseEntryWithLineBreaks extends LicenseEntry {
  /// Create a license entry for a license whose text is hard-wrapped within
  /// paragraphs and has paragraph breaks denoted by blank lines or with
  /// indented text.
  const LicenseEntryWithLineBreaks(this.packages, this.text);

  @override
  final List<String> packages;

  /// The text of the license.
  ///
  /// The text will be split into paragraphs according to the following
  /// conventions:
  ///
  /// * Lines starting with a different number of space characters than the
  ///   previous line start a new paragraph, with those spaces removed.
  /// * Blank lines start a new paragraph.
  /// * Other line breaks are replaced by a single space character.
  /// * Leading spaces on a line are removed.
  ///
  /// For each paragraph, the algorithm attempts (using some rough heuristics)
  /// to identify how indented the paragraph is, or whether it is centered.
final String text;

@override
Iterable<LicenseParagraph> get paragraphs sync* {
  int lineStart = 0;
  int currentPosition = 0;
  int lastLineIndent = 0;
  int currentLineIndent = 0;
  int? currentParagraphIndentation;
  _LicenseEntryWithLineBreaksParserState state = _LicenseEntryWithLineBreaksParserState.beforeParagraph;
  final List<String> lines = <String>[
  void addLine() {
    assert(lineStart < currentPosition);
    lines.add(text.substring(lineStart, currentPosition));
  }
  LicenseParagraph getParagraph() {
    assert(lines.isNotEmpty);
    assert(currentParagraphIndentation != null);
    final LicenseParagraph result = LicenseParagraph(lines.join(' '), currentParagraphIndentation!);
    assert(result.text.trimLeft() == result.text);
    assert(result.text.isNotEmpty);
    lines.clear();
    return result;
  }
  while (currentPosition < text.length) {
    switch (state) {
      case _LicenseEntryWithLineBreaksParserState.beforeParagraph:
        assert(lineStart == currentPosition);
        switch (text[currentPosition]) {
          case ' ':  
            lineStart = currentPosition + 1;
            currentLineIndent += 1;
            state = _LicenseEntryWithLineBreaksParserState.beforeParagraph;
            break;
          case '	':
            lineStart = currentPosition + 1;
            currentLineIndent += 8;
            state = _LicenseEntryWithLineBreaksParserState.beforeParagraph;
            break;
          case '':
          case '
':
          case '':
            if (lines.isNotEmpty) {
              yield getParagraph();
            }
if (text[currentPosition] == '\r' && currentPosition < text.length - 1 && text[currentPosition + 1] == '\n') {
    currentPosition += 1;
}

lastLineIndent = 0;
currentLineIndent = 0;
currentParagraphIndentation = null;
lineStart = currentPosition + 1;
state = _LicenseEntryWithLineBreaksParserState.beforeParagraph;
break;

case 'T':
    // This is a bit of a hack for the LGPL 2.1, which does something like this:
    //
    // [this is a
    //  single paragraph]
    //
    // ...near the top.
    currentLineIndent += 1;
    continue startParagraph;

startParagraph:
    default:
        if (lines.isNotEmpty && currentLineIndent > lastLineIndent) {
            yield getParagraph();
            currentParagraphIndentation = null;
        }
        // The following is a wild heuristic for guessing the indentation level.
        // It happens to work for common variants of the BSD and LGPL licenses.
        if (currentParagraphIndentation == null) {
            if (currentLineIndent > 10)
                currentParagraphIndentation = LicenseParagraph.centeredIndent;
            else
                currentParagraphIndentation = currentLineIndent ~/ 3;
        }
        state = _LicenseEntryWithLineBreaksParserState.inParagraph;
        break;

    case _LicenseEntryWithLineBreaksParserState.inParagraph:
        switch (text[currentPosition]) {
            case '\n':
                addLine();
                lastLineIndent = currentLineIndent;
                currentLineIndent = 0;
                lineStart = currentPosition + 1;
                state = _LicenseEntryWithLineBreaksParserState.beforeParagraph;
                break;
            case '\r':
                addLine();
                yield getParagraph();
```dart
lastLineIndent = 0;
currentLineIndent = 0;
currentParagraphIndentation = null;
lineStart = currentPosition + 1;
state = _LicenseEntryWithLineBreaksParserState.beforeParagraph;
break;
default:
state = _LicenseEntryWithLineBreaksParserState.inParagraph;
}
break;
}
currentPosition += 1;
}
switch (state) {
    case _LicenseEntryWithLineBreaksParserState.beforeParagraph:
        if (lines.isNotEmpty) {
            yield getParagraph();
        }
        break;
    case _LicenseEntryWithLineBreaksParserState.inParagraph:
        addLine();
        yield getParagraph();
        break;
    }
}
}

/// A registry for packages to add licenses to, so that they can be displayed
/// together in an interface such as the [LicensePage].
///
/// Packages can register their licenses using [addLicense]. User interfaces
/// that wish to show all the licenses can obtain them by calling [licenses].
///
/// The flutter tool will automatically collect the contents of all the LICENSE
/// files found at the root of each package into a single LICENSE file in the
/// default asset bundle. Each license in that file is separated from the next
/// by a line of eighty hyphens (`-`), and begins with a list of package names
/// that the license applies to, one to a line, separated from the next by a
/// blank line. The `services` package registers a license collector that splits
/// that file and adds each entry to the registry.
///
/// The LICENSE files in each package can either consist of a single license, or
/// can be in the format described above. In the latter case, each component
/// license and list of package names is merged independently.
///
/// See also:
///
```
/// * [showAboutDialog], which shows a Material-style dialog with information
/// about the application, including a button that shows a [LicensePage] that
/// uses this API to select licenses to show.
/// * [AboutListTile], which is a widget that can be added to a [Drawer]. When
/// tapped it calls [showAboutDialog].

class LicenseRegistry {

  // This class is not meant to be instantiated or extended; this constructor
  // prevents instantiation and extension.
  // ignore: unused_element
  LicenseRegistry._();

  static List<LicenseEntryCollector>? _collectors;

  /// Adds licenses to the registry.
  ///
  /// To avoid actually manipulating the licenses unless strictly necessary,
  /// licenses are added by adding a closure that returns a list of
  /// [LicenseEntry] objects. The closure is only called if [licenses] is itself
  /// called; in normal operation, if the user does not request to see the
  /// licenses, the closure will not be called.
  static void addLicense(LicenseEntryCollector collector) {
    _collectors ??= <LicenseEntryCollector>[];
    _collectors!.add(collector);
  }

  /// Returns the licenses that have been registered.
  ///
  /// Generating the list of licenses is expensive.
  static Stream<LicenseEntry> get licenses async* {
    if (_collectors == null)
      return;
    for (final LicenseEntryCollector collector in _collectors!)
      yield* collector();
  }

  /// Resets the internal state of [LicenseRegistry]. Intended for use in
  /// testing.
  @visibleForTesting
  static void reset() {
    _collectors = null;
  }
}

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1.102 https-proxy-agent 5.0.0

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https-proxy-agent

=================

### An HTTP(s) proxy `http.Agent` implementation for HTTPS

[![Build Status](https://github.com/TooTallNate/node-https-proxy-agent/actions?workflow=Node+CI)](https://github.com/TooTallNate/node-https-proxy-agent/workflows/Node%20CI/badge.svg)

This module provides an `http.Agent` implementation that connects to a specified
HTTP or HTTPS proxy server, and can be used with the built-in `https` module.

Specifically, this `Agent` implementation connects to an intermediary "proxy"
server and issues the [CONNECT HTTP method][CONNECT], which tells the proxy to
open a direct TCP connection to the destination server.

Since this agent implements the CONNECT HTTP method, it also works with other
protocols that use this method when connecting over proxies (i.e. WebSockets).
See the "Examples" section below for more.
Installation
------------

Install with `npm`:

```bash
$ npm install https-proxy-agent
```

Examples
--------

#### `https` module example

```js
var url = require('url');
var https = require('https');
var HttpsProxyAgent = require('https-proxy-agent');

// HTTP/HTTPS proxy to connect to
var proxy = process.env.http_proxy || 'http://168.63.76.32:3128';
console.log('using proxy server %j', proxy);

// HTTPS endpoint for the proxy to connect to
console.log('attempting to GET %j', endpoint);
var options = url.parse(endpoint);

// create an instance of the `HttpsProxyAgent` class with the proxy server information
var agent = new HttpsProxyAgent(proxy);
options.agent = agent;

https.get(options, function (res) {
    console.log("response" event!, res.headers);
    res.pipe(process.stdout);
});
```

#### `ws` WebSocket connection example

```js
var url = require('url');
var WebSocket = require('ws');
var HttpsProxyAgent = require('https-proxy-agent');

// HTTP/HTTPS proxy to connect to
var proxy = process.env.http_proxy || 'http://168.63.76.32:3128';
```
console.log('using proxy server %j', proxy);

// WebSocket endpoint for the proxy to connect to
var endpoint = process.argv[2] || 'ws://echo.websocket.org';
var parsed = url.parse(endpoint);
console.log('attempting to connect to WebSocket %j', endpoint);

// create an instance of the `HttpsProxyAgent` class with the proxy server information
var options = url.parse(proxy);

var agent = new HttpsProxyAgent(options);

// finally, initiate the WebSocket connection
var socket = new WebSocket(endpoint, { agent: agent });

socket.on('open', function () {
  console.log("open" event!);
  socket.send('hello world');
});

socket.on('message', function (data, flags) {
  console.log("message" event! %j %j", data, flags);
  socket.close();
});
```
```

API
---

### `new HttpsProxyAgent(Object options)`

The `HttpsProxyAgent` class implements an `http.Agent` subclass that connects to the specified "HTTP(s) proxy server" in order to proxy HTTPS and/or WebSocket requests. This is achieved by using the [HTTP `CONNECT` method][CONNECT].

The `options` argument may either be a string URI of the proxy server to use, or an `options` object with more specific properties:

* `host` - String - Proxy host to connect to (may use `hostname` as well). Required.
* `port` - Number - Proxy port to connect to. Required.
* `protocol` - String - If `https:`, then use TLS to connect to the proxy.
* `headers` - Object - Additional HTTP headers to be sent on the HTTP CONNECT method.
* Any other options given are passed to the `net.connect()`/`tls.connect()` functions.

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[CONNECT]: http://en.wikipedia.org/wiki/HTTP_tunnel#HTTP_CONNECT_Tunneling

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1.103 engine.io-client 4.1.4

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1.115 p-map 1.2.0

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1.116 har-validator 5.1.5
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1.117 jquery-gritter 1.7.4
1.117.1 Available under license:
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/*
 * Gritter for jQuery
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 *
 * Copyright (c) 2012 Jordan Boesch
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 *
 * Date: February 24, 2012
 * Version: 1.7.4
 */

Found in path(s):
* /opt/ws_local/PERMITS_SQL/1070907640_1594782178.63/0/gritter-7f0c27823f8862ad22860420d26eca933e60169d-1.zip/Gritter-7f0c27823f8862ad22860420d26eca933e60169d/js/jquery.gritter.js
1.118 assert-plus 1.0.0

1.119 forever-agent 0.6.1
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1.120 strip-json-comments 2.0.1

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1.121 npmlog 4.1.2

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1.122 llvm 11.0.0

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=aarch64-- | FileCheck %s

; A shuffle mask with all undef elements is always legal.

define <4 x i32> @PR41535(<2 x i32> %p1, <2 x i32> %p2) {
 ; CHECK-LABEL: PR41535:
 ; CHECK:       // %bb.0:
 ; CHECK-NEXT:  ext v0.8b, v0.8b, v1.8b, #4
 ; CHECK-NEXT:  mov v0.d[1], v0.d[0]
 ; CHECK-NEXT:  ret
 %cat1 = shufflevector <2 x i32> %p1, <2 x i32> undef, <4 x i32> <i32 undef, i32 1, i32 undef, i32 undef>
 %cat2 = shufflevector <2 x i32> %p2, <2 x i32> undef, <4 x i32> <i32 0, i32 undef, i32 undef, i32 undef>
 %r = shufflevector <4 x i32> %cat1, <4 x i32> %cat2, <4 x i32> <i32 undef, i32 undef, i32 1, i32 4>
 ret <4 x i32> %r
}
; RUN: llc < %s -mtriple=s390x-linux-gnu -mcpu=zEC12 -verify-machineinstrs | FileCheck %s
;
; Test that early if conversion produces LOCR with operands of the right
; register classes.

define void @autogen_SD4739(i8*) {
; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
BB:
  %L34 = load i8, i8* %0
  %Cmp56 = icmp sgt i8 undef, %L34
  br label %CF246

CF246: ; preds = %CF246, %BB
  %Sl163 = select i1 %Cmp56, i8 %L34, i8 undef
  br i1 undef, label %CF246, label %CF248

CF248: ; preds = %CF246, %CF246
  store i8 %Sl163, i8* %0
  br label %CF248
}

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; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s

define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
  ; CHECK-LABEL: test_sitofp_fixed:

  ; First, extend each i32 to i64
  ; CHECK-DAG: sshll2.2d [[BLOCK0_HI:v[0-9]+]], v0, #0
  ; CHECK-DAG: sshll2.2d [[BLOCK1_HI:v[0-9]+]], v1, #0
  ; CHECK-DAG: sshll2.2d [[BLOCK2_HI:v[0-9]+]], v2, #0
  ; CHECK-DAG: sshll2.2d [[BLOCK3_HI:v[0-9]+]], v3, #0
  ; CHECK-DAG: sshll.2d [[BLOCK0_LO:v[0-9]+]], v0, #0
  ; CHECK-DAG: sshll.2d [[BLOCK1_LO:v[0-9]+]], v1, #0
  ; CHECK-DAG: sshll.2d [[BLOCK2_LO:v[0-9]+]], v2, #0
  ; CHECK-DAG: sshll.2d [[BLOCK3_LO:v[0-9]+]], v3, #0
; Next, convert each to double.
; CHECK-DAG: scvtf.2d v0, [[BLOCK0_LO]]
; CHECK-DAG: scvtf.2d v1, [[BLOCK0_HI]]
; CHECK-DAG: scvtf.2d v2, [[BLOCK1_LO]]
; CHECK-DAG: scvtf.2d v3, [[BLOCK1_HI]]
; CHECK-DAG: scvtf.2d v4, [[BLOCK2_LO]]
; CHECK-DAG: scvtf.2d v5, [[BLOCK2_HI]]
; CHECK-DAG: scvtf.2d v6, [[BLOCK3_LO]]
; CHECK-DAG: scvtf.2d v7, [[BLOCK3_HI]]

; CHECK: ret
%flt = sitofp <16 x i32> %in to <16 x double>
%res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0>
ret <16 x double> %res
}

; This one is small enough to satisfy isSimple, but still illegally large.
define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
; CHECK-LABEL: test_sitofp_fixed_shortish:

; CHECK-DAG: scvtf.2d v0, v0
; CHECK-DAG: scvtf.2d v1, v1

; CHECK: ret
%flt = sitofp <4 x i64> %in to <4 x double>
%res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
ret <4 x double> %res
}

; NOTE: Assertions have been autogenerated by util/update_llvm_test_checks.py
; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s
;
; D31946
; Check that we dont end up with the ""LLVM ERROR: Cannot select"" error.
; Additionally ensure that the output code actually put fp128 values in SSE registers.

declare fp128 @llvm.fabs.f128(fp128)
declare fp128 @llvm.copysign.f128(fp128, fp128)

define fp128 @TestSelect(fp128 %a, fp128 %b) {
; CHECK-LABEL: TestSelect:
; CHECK: # %bb.0:
; CHECK-NEXT: pushq %rbx
; CHECK-NEXT: .cfi_def_cfa_offset 16
; CHECK-NEXT: subq $32, %rsp
; CHECK-NEXT: .cfi_offset %rbx, -16
; CHECK-NEXT:    movaps %xmm1, [%rip+*] # 16-byte Spill
; CHECK-NEXT:    movaps %xmm0, (%rsp) # 16-byte Spill
; CHECK-NEXT:    callq __gttf2
; CHECK-NEXT:    movl %eax, %ebx
; CHECK-NEXT:    movaps (%rsp), %xmm0 # 16-byte Reload
; CHECK-NEXT:    movaps [%rip+*], %xmm1 # 16-byte Reload
; CHECK-NEXT:    callq __subtf3
; CHECK-NEXT:    testl %ebx, %ebx
; CHECK-NEXT:    jg .LBB0_2
; CHECK-NEXT:    # %bb.1:
; CHECK-NEXT:    xorps %xmm0, %xmm0
; CHECK-NEXT:    .LBB0_2:
; CHECK-NEXT:    addq $32, %rsp
; CHECK-NEXT:    .cfi_def_cfa_offset 16
; CHECK-NEXT:    popq %rbx
; CHECK-NEXT:    .cfi_def_cfa_offset 8
; CHECK-NEXT:    retq
;
%cmp = fcmp ogt fp128 %a, %b
%sub = fsub fp128 %a, %b
%res = select i1 %cmp, fp128 %sub, fp128 0xL00000000000000000000000000000000
ret fp128 %res
}
}
}
}
}
}
; CHECK-NEXT: movaps %xmm0, %xmm1
; CHECK-NEXT: callq __multf3
; CHECK-NEXT: xorps [%rip], %xmm0
; CHECK-NEXT: popq %rax
; CHECK-NEXT: .cfi_def_cfa_offset 8
; CHECK-NEXT: retq
%mul = fmul fp128 %a, %a
%res = fsub fp128 0xL00000000000000008000000000000000, %mul
ret fp128 %res
}
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; RUN: opt %s -inline -S | FileCheck %s

define internal void @innerSmall() "min-legal-vector-width"="128" {
  ret void
}

define internal void @innerLarge() "min-legal-vector-width"="512" {
  ret void
}

define internal void @innerNoAttribute() {
  ret void
}

; We should not add an attribute during inlining. No attribute means unknown.
; Inlining doesn't change the fact that we don't know anything about this
; function.
define void @outerNoAttribute() {
  call void @innerLarge()
  ret void
}

define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
  call void @innerLarge()
  ret void
}
define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
call void @innerSmall()
ret void
}

; We should remove the attribute after inlining since the callee's
; vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
call void @innerNoAttribute()
ret void
}

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }

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; RUN: opt -consthoist -S -o - %s | FileCheck %s
target triple = "thumbv6m-none--musleabi"
; Check that for i8 type, the maximum legal offset is 31.
; Also check that an constant used as value to be stored rather than
; pointer in a store instruction is hoisted.
; CHECK: foo_i8
; CHECK-DAG: %[[C1:const[0-9]??]] = bitcast i32 805874720 to i32
; CHECK-DAG: %[[C2:const[0-9]??]] = bitcast i32 805874688 to i32
; CHECK-DAG: %[[C3:const[0-9]??]] = bitcast i32 805873720 to i32
; CHECK-DAG: %[[C4:const[0-9]??]] = bitcast i32 805873688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i8*
; CHECK-NEXT: %1 = load volatile i8, i8* %0
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i8*
; CHECK-NEXT: %3 = load volatile i8, i8* %2
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i8*
; CHECK-NEXT: %5 = load volatile i8, i8* %4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i8*
; CHECK-NEXT: %7 = load volatile i8, i8* %6
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i8*
; CHECK-NEXT: %9 = load volatile i8, i8* %8
; CHECK-NEXT: %10 = inttoptr i32 %[[C4]] to i8*
; CHECK-NEXT: store i8 %9, i8* %10
; CHECK-NEXT: %11 = inttoptr i32 %[[M4]] to i8*
; CHECK-NEXT: store i8 %7, i8* %11
; CHECK-NEXT: %12 = inttoptr i32 %[[C3]] to i8*
; CHECK-NEXT: store i8 %5, i8* %12
; CHECK-NEXT: %13 = inttoptr i32 %[[M5]] to i8*
; CHECK-NEXT: store i8 %3, i8* %13
; CHECK-NEXT: %14 = inttoptr i32 %[[M6]] to i8*
; CHECK-NEXT: store i8 %14, i8** @goo

@goo = global i8* undef
define void @foo_i8() {
  entry:
  %0 = load volatile i8, i8* inttoptr (i32 805874688 to i8*)
  %1 = load volatile i8, i8* inttoptr (i32 805874692 to i8*)
  %2 = load volatile i8, i8* inttoptr (i32 805874719 to i8*)
  %3 = load volatile i8, i8* inttoptr (i32 805874720 to i8*)
  %4 = load volatile i8, i8* inttoptr (i32 805874727 to i8*)
  store i8 %4, i8* inttoptr(i32 805873688 to i8*)
  store i8 %3, i8* inttoptr(i32 805873719 to i8*)
  store i8 %2, i8* inttoptr(i32 805873720 to i8*)
}
store i8 %1, i8* inttoptr(i32 805873727 to i8*)
store i8* inttoptr(i32 805874800 to i8*), i8** @goo
ret void
}

; Check that for i16 type, the maximum legal offset is 62.
; CHECK: foo_i16
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874752 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i16*
; CHECK-NEXT: %1 = load volatile i16, i16* %0, align 2
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i16*
; CHECK-NEXT: %3 = load volatile i16, i16* %2, align 2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 32
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i16*
; CHECK-NEXT: %5 = load volatile i16, i16* %4, align 2
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C2]], 62
; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to i16*
; CHECK-NEXT: %7 = load volatile i16, i16* %6, align 2
; CHECK-NEXT: %8 = inttoptr i32 %[[C1]] to i16*
; CHECK-NEXT: %9 = load volatile i16, i16* %8, align 2
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 22
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i16*
; CHECK-NEXT: %11 = load volatile i16, i16* %10, align 2

define void @foo_i16() {
entry:
%0 = load volatile i16, i16* inttoptr (i32 805874688 to i16*), align 2
%1 = load volatile i16, i16* inttoptr (i32 805874692 to i16*), align 2
%2 = load volatile i16, i16* inttoptr (i32 805874720 to i16*), align 2
%3 = load volatile i16, i16* inttoptr (i32 805874750 to i16*), align 2
%4 = load volatile i16, i16* inttoptr (i32 805874752 to i16*), align 2
%5 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
ret void
}

; Check that for i32 type, the maximum legal offset is 124.
; CHECK: foo_i32
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i32*
; CHECK-NEXT: %1 = load volatile i32, i32* %0, align 4
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i32*
; CHECK-NEXT: %3 = load volatile i32, i32* %2, align 4
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 124
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i32*
define void @foo_i32() {
  entry:
  %0 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 4
  %1 = load volatile i32, i32* inttoptr (i32 805874692 to i32*), align 4
  %2 = load volatile i32, i32* inttoptr (i32 805874812 to i32*), align 4
  %3 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
  %4 = load volatile i32, i32* inttoptr (i32 805874824 to i32*), align 4
  %5 = load volatile i32, i32* inttoptr (i32 805874828 to i32*), align 4
  ret void
}

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------------------------------------------------------------------------------
clang-tidy CERT Files
------------------------------------------------------------------------------

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; NOTE: Assertions have been autogenerated by utils/update_test_checks.py
; UTC_ARGS: --function-signature --scrub-attributes
; RUN: opt -S -argpromotion < %s | FileCheck %s
; RUN: opt -S -passes=argpromotion < %s | FileCheck %s
; Test that we only promote arguments when the caller/callee have compatible function attributes.

target triple = "x86_64-unknown-linux-gnu"

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
; CHECK-LABEL: define {[[^*]+]}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; CHECK-SAME: (\<8 x i64>\* [\[ARG:.*\]], \<8 x i64\> [\[ARG1_VAL:.*\]][\[ARG\]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [\[ARG1_VAL\]], <8 x i64> [\[ARG\]]
; CHECK-NEXT: ret void

bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
; CHECK-LABEL: define @avx512_legal512_prefer512_call_avx512_legal512_prefer512
; CHECK-SAME: <8 x i64>* [[ARG:%.*]]
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloc <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloc <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void

bb:
%tmp = alloc <8 x i64>, align 32
%tmp2 = alloc <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: <8 x i64>* [[ARG:%.*]], <8 x i64>* [[ARG1:]]
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void

bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(%arg) #1 {
    ; CHECK-LABEL: define [[^@]+] @avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: ([8 x i64]* [[ARG:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: [[TMP:%.*]] = alloca [8 x i64], align 32
    ; CHECK-NEXT: [[TMP2:%.*]] = alloca [8 x i64], align 32
    ; CHECK-NEXT: [[TMP3:%.*]] = bitcast [8 x i64]* [[TMP]] to i8*
    ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
    ; CHECK-NEXT: [[TMP_VAL:%.*]] = load [8 x i64], [8 x i64]* [[TMP]]
    ; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256([8 x i64]* [[TMP2]], [8 x i64] [[TMP_VAL]])
    ; CHECK-NEXT: [[TMP4:%.*]] = load [8 x i64], [8 x i64]* [[TMP2]], align 32
    ; CHECK-NEXT: store [8 x i64] [[TMP4]], [8 x i64]* [[ARG]], align 2
    ; CHECK-NEXT: ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(%arg, %arg1) #1 {
    ; CHECK-LABEL: define [[^@]+] @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
    ; CHECK-SAME: ([8 x i64]* [[ARG:%.*]], [8 x i64] [[ARG1_VAL:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: store [8 x i64] [[ARG1_VAL]], [8 x i64] [[ARG]]
    ; CHECK-NEXT: ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(%arg) #0 {
    ; CHECK-LABEL: define [[^@]+] @avx512_legal512_prefer512_call_avx512_legal512_prefer256
    ; CHECK-SAME: ([8 x i64]* [[ARG:%.*]])
    ; CHECK-NEXT: bb:
}

; Open Source Used In CLI Analyzer 3.6.8 744
; CHECK-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:  call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT:  [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT:  call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP_VAL]])
; CHECK-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:  ret void
;
bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
  ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* [[ARG1_VAL:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
  ; CHECK-NEXT: ret void
  ;
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
  ; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]])

define void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
  ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* [[ARG1_VAL:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
  ; CHECK-NEXT: ret void
  ;
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}
i64* [[TMP2]], <8 x i64>* [[TMP_VAL]]
; CHECK-NEXT:  [[TMP4:..*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:  ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG]]
; CHECK-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
; CHECK-NEXT:  ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:  call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT:  call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]])
; CHECK-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:  ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

: This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 {
  CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
  CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
  CHECK-NEXT: bb:
  CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
  CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
  CHECK-NEXT: ret void

bb:
%tmp = load <8 x i64>, <8 x i64>* %arg
store <8 x i64> %tmp, <8 x i64>* %arg
ret void

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
  CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
  CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
  CHECK-NEXT: bb:
  CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
  CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]])
  CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  CHECK-NEXT: ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote

define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #3 {
; CHECK-LABEL: define ([^@]+) @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
; CHECK-LABEL: define ([^@]+) @avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #4 {
    ; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* [[ARG1_VAL:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
    ; CHECK-NEXT: ret void
    
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
    ; CHECK-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: alloca <8 x i64>, align 32
    ; CHECK-NEXT: alloca <8 x i64>, align 32
    ; CHECK-NEXT: bitcast <8 x i64>* [[TMP]] to i8*
    ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP]], i8 0, i64 32, i1 false)
    ; CHECK-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP_VAL]])
    ; CHECK-NEXT: load <8 x i64>, <8 x i64>* [[TMP2]], align 32
    ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
    ; CHECK-NEXT: ret void
    
    bb:
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
    call void @llvm.memset.p0i8.i64(i8* %tmp3, i8 0, i64 32, i1 false)
    call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ret void
}

; If the arguments are scalar, its ok to promote.
define internal i32 @scalar_callee_avx512_legal256_call_avx512_legal512_prefer256(i32* %X, i32* %Y) #2 {
    ; CHECK-LABEL: define {{[^@]+}}@scalar_callee_avx512_legal256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (i32 [[X_VAL:%.*]], i32 [[Y_VAL:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: = add i32 [[X_VAL]], [[Y_VAL]]

define i32 @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    %A = alloca i32
    store i32 1, i32* %A
    %C = call i32 @scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32 %A, i32 %B)
    ret i32 %C
}

define internal i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %X, i32* %Y) #2 {
    %A = load i32, i32* %X
    %B = load i32, i32* %Y
    %C = add i32 %A, %B
    ret i32 %C
}

define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    %A = alloca i32
    store i32 1, i32* %A
    %C = call i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32 %A, i32 %B)
    ret i32 %C
}
@scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32 \([\text{A\_VAL}]\), i32 \([\text{B\_VAL}]\))

; CHECK-NEXT: ret i32 \([\text{C}]\)

; %A = allocat i32
store i32 1, i32* %A

%C = call i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %A, i32* %B)
ret i32 %C

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit,avx512vbmi | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; Make sure CPUs default to prefer-256-bit. avx512vnni isn't interesting as it just adds an isel peephole for vpmaddwd+vpaddd
This file primarily contains tests for specific places in X86ISelLowering.cpp that needed to be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

define void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="256" {
  CHECK-LABEL: add256:
  CHECK:
    # %bb.0:
    CHECK-NEXT: vmovdqa (%rdi), %ymm0
    CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
    CHECK-NEXT: vpaddd 32(%rsi), %ymm0, %ymm1
    CHECK-NEXT: vpaddd (%rsi), %ymm0, %ymm0
    CHECK-NEXT: vmovdqa %ymm0, (%rdx)
    CHECK-NEXT: vzeroupper
    CHECK-NEXT: retq
    %d = load <16 x i32>, <16 x i32>* %a
    %e = load <16 x i32>, <16 x i32>* %b
    %f = add <16 x i32> %d, %e
    store <16 x i32> %f, <16 x i32>* %c
    ret void
}

define void @add512(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="512" {
  CHECK-LABEL: add512:
  CHECK:
    # %bb.0:
    CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
    CHECK-NEXT: vpadd 32(%rsi), %zmm0, %zmm0
    CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
    CHECK-NEXT: vzeroupper
    CHECK-NEXT: retq
    %d = load <16 x i32>, <16 x i32>* %a
    %e = load <16 x i32>, <16 x i32>* %b
    %f = add <16 x i32> %d, %e
    store <16 x i32> %f, <16 x i32>* %c
ret void
}
define void @avg_v64i8_256(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="256" {
; CHECK-LABEL: avg_v64i8_256:
; CHECK:
# %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT: vpavgb (%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpavgb 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT: vmovdqu %ymm1, (%rax)
; CHECK-NEXT: vmovdqu %ymm0, (%rax)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%1 = load <64 x i8>, <64 x i8>* %a
%2 = load <64 x i8>, <64 x i8>* %b
%3 = zext <64 x i8> %1 to <64 x i32>
%4 = zext <64 x i8> %2 to <64 x i32>
%5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
%6 = add nuw nsw <64 x i32> %5, %4
%7 = lshr <64 x i32> %6, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
%8 = trunc <64 x i32> %7 to <64 x i8>
store <64 x i8> %8, <64 x i8>* undef, align 4
ret void
}

define void @avg_v64i8_512(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="512" {
; CHECK-LABEL: avg_v64i8_512:
; CHECK:
# %bb.0:
; CHECK-NEXT: vmovdqa64 (%rsi), %zmm0
; CHECK-NEXT: vpavgb (%rdi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqu64 %zmm0, (%rax)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%1 = load <64 x i8>, <64 x i8>* %a
%2 = load <64 x i8>, <64 x i8>* %b
%3 = zext <64 x i8> %1 to <64 x i32>
%4 = zext <64 x i8> %2 to <64 x i32>
%5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,

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define void @pmaddwd_32_256(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: pmaddwd_32_256:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
    ; CHECK-NEXT:  vpmaddwd 32(%rsi), %ymm1, %ymm1
    ; CHECK-NEXT:  vpmaddwd (%rsi), %ymm0, %ymm0
    ; CHECK-NEXT:  vmovdqa %ymm0, 32(%rdx)
    ; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
    ; CHECK-NEXT:  vzeroupper
    ; CHECK-NEXT:  retq
    %A = load <32 x i16>, <32 x i16>* %APtr
    %B = load <32 x i16>, <32 x i16>* %BPtr
    %a = sext <32 x i16> %A to <32 x i32>
    %b = sext <32 x i16> %B to <32 x i32>
    %m = mulf nsw <32 x i32> %a, %b
    %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
    %even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
    %ret = add <16 x i32> %odd, %even
    store <16 x i32> %ret, <16 x i32>* %CPtr
    ret void
}

define void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: pmaddwd_32_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
    ; CHECK-NEXT:  vpmaddwd64 (%rsi), %zmm0, %zmm0
    ; CHECK-NEXT:  vpmaddwd64 (%rsi), %zmm0, %zmm0
    ; CHECK-NEXT:  vzeroupper
    ; CHECK-NEXT:  retq
    %A = load <32 x i16>, <32 x i16>* %APtr
    %B = load <32 x i16>, <32 x i16>* %BPtr
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%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> %i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> %i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

define void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="256" {  
; CHECK-LABEL: psubus_64i8_max_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpsubusb 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:  vpsubusb (%rsi), %ymm0, %ymm0
; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

define void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="512" {  
; CHECK-LABEL: psubus_64i8_max_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:  vpsubusb (%rsi), %zmm0, %zmm0
; CHECK-NEXT:  vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
void ret

define i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {

; CHECK-LABEL: _Z9test_charPcS_i_256:
; CHECK:     # %bb.0: # %entry
; CHECK-NEXT: movl %edx, %eax
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: xorl %ecx, %ecx
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT: vpxor %xmm2, %xmm2, %xmm2
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT:  .LBB8_1: # %vector.body
; CHECK-NEXT:     # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:     vpmovsxbw 16(%rdi,%rcx), %ymm3
; CHECK-NEXT:     vpmovsxbw (%rdi,%rcx), %ymm4
; CHECK-NEXT:     vpmovsxbw 16(%rsi,%rcx), %ymm5
; CHECK-NEXT:     vpmaddwd %ymm3, %ymm5, %ymm3
; CHECK-NEXT:     vpaddd %ymm2, %ymm3, %ymm2
; CHECK-NEXT:     vpmovsxbw (%rsi,%rcx), %ymm3
; CHECK-NEXT:     vpmaddwd %ymm4, %ymm3, %ymm3
; CHECK-NEXT:     vpaddd %ymm1, %ymm3, %ymm1
; CHECK-NEXT:     addq $32, %rcx
; CHECK-NEXT:     cmpq %rcx, %rax
; CHECK-NEXT:     jne .LBB8_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:     vpaddd %ymm0, %ymm1, %ymm1
; CHECK-NEXT:     vpaddd %ymm0, %ymm2, %ymm0
; CHECK-NEXT:     vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT:     vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:     vpaddd %ymm1, %xmm0, %xmm0
; CHECK-NEXT:     vpaddd %ymm1, %xmm0, %xmm0
; CHECK-NEXT:     vextracti128 {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:     vpaddd %ymm1, %xmm0, %xmm0
; CHECK-NEXT:     vpaddd %ymm1, %xmm0, %xmm0
; CHECK-NEXT:     vpaddd %ymm1, %xmm0, %xmm0
; CHECK-NEXT:     vpaddd %ymm1, %xmm0, %xmm0
; CHECK-NEXT:     vpaddd %ymm1, %xmm0, %xmm0
; CHECK-NEXT:     vpaddd %ymm1, %xmm0, %xmm0
; CHECK-NEXT:     vpaddd %ymm1, %xmm0, %xmm0
; CHECK-NEXT:     vzeroupper
; CHECK-NEXT:  ; entry:
entry:
%3 = zext i32 %2 to i64
br label %vector.body

vector.body:

vector.body:

}
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body

middle.block:
%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 unde
; CHECK-NEXT:  xorl %ecx, %ecx
; CHECK-NEXT:  vpxor %xmm1, %xmm1, %xmm1  
; CHECK-NEXT:  .p2align 4, 0x90
; CHECK-NEXT:  .LBB9_1: # %vector.body
; CHECK-NEXT:  # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:  vpmovsxbw (%rdi,%rcx), %zmm2
; CHECK-NEXT:  vpmovsxbw (%rsi,%rcx), %zmm3
; CHECK-NEXT:  vpmaddwd %zmm2, %zmm3, %zmm2
; CHECK-NEXT:  vpaddd %zmm1, %zmm2, %zmm1
; CHECK-NEXT:  addq $32, %rcx
; CHECK-NEXT:  cmpq %rcx, %rax
; CHECK-NEXT:  jne .LBB9_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:  vpaddd %zmm0, %zmm1, %zmm0
; CHECK-NEXT:  vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT:  vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:  vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vpshufd [%.#+] xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vpshufd [%.#+] xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vmovd %xmm0, %eax
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq

entry:
%3 = zext i32 %2 to i64  
br label %vector.body

vector.body:
%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body

middle.block:
%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,
define i32 @sad_16i8_256() "min-legal-vector-width"="256" { 
; CHECK-LABEL: sad_16i8_256:
; CHECK:       # %bb.0: # %entry
; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:    movq $-1024, %rax # imm = 0xFC00
; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT:    .p2align 4, 0x90
; CHECK-NEXT:  .LBB10_1: # %vector.body
; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:    vmovdqu a+1024(%rax), %xmm2
; CHECK-NEXT:    vpsadbw b+1024(%rax), %xmm2, %xmm2
; CHECK-NEXT:    vpaddd %ymm1, %ymm2, %ymm1
; CHECK-NEXT:    addq $4, %rax
; CHECK-NEXT:    jne .LBB10_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:    ret
}

@a = global [1024 x i8] zeroinitializer, align 16
@b = global [1024 x i8] zeroinitializer, align 16
entry:
  br label %vector.body

vector.body:
  %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
  %vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
  %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
  %1 = bitcast i8* %0 to <16 x i8>*
  %wide.load = load <16 x i8>, <16 x i8>* %1, align 4
  %2 = zext <16 x i8> %wide.load to <16 x i32>
  %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
  %4 = bitcast i8* %3 to <16 x i8>*
  %wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
  %5 = zext <16 x i8> %wide.load1 to <16 x i32>
  %6 = sub nsw <16 x i32> %2, %5
  %7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
  %8 = sub nsw <16 x i32> zeroinitializer, %6
  %9 = select <16 x i1> %7, %16 x i32> %6, <16 x i32> %8
  %10 = add nsw <16 x i32> %9, %vec.phi
  %index.next = add i64 %index, 1024
  br i1 %11, label %middle.block, label %vector.body

middle.block:
  %rdx.shuf = shufflevector <16 x i32> %10, %16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx = add <16 x i32> %10, %rdx.shuf
  %rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
  %rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
  %rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

define i32 @sad_16i8_512() "min-legal-vector-width"="512" {
  ; CHECK-LABEL: sad_16i8_512:
  ; CHECK:       # %bb.0: # %entry
  ; CHECK-NEXT:  vpxor %xmm0, %xmm0, %xmm0
  ; CHECK-NEXT:  movq $-1024, %rax # imm = 0xF00
  ; CHECK-NEXT:  .p2align 4, 0x90
  ; CHECK-NEXT:  .LBB11_1: # %vector.body
  ; CHECK-NEXT:  # =>This Inner Loop Header: Depth=1
  ; CHECK-NEXT:  vmovdqu a+1024(%rax), %xmm1
  ; CHECK-NEXT:  vpsadbw b+1024(%rax), %xmm1, %xmm1
  ; CHECK-NEXT:  vpaddd %zmm0, %zmm1, %zmm0
  ; CHECK-NEXT:  addq $4, %rax
  ; CHECK-NEXT:  jne .LBB11_1
  ; CHECK-NEXT:  # %bb.2: # %middle.block
  ; CHECK-NEXT:  vextracti64x4 $1, %zmm0, %ymm1
  ; CHECK-NEXT:  vpaddd %zmm1, %zmm0, %zmm0
  ; CHECK-NEXT:  vextracti128 $1, %ymm0, %xmm1
  ; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
  ; CHECK-NEXT:  vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
  ; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
  ; CHECK-NEXT:  vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
  ; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
  ; CHECK-NEXT:  vmovd %xmm0, %eax
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
entry:
br label %vector.body

vector.body:

  %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
  %vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
  %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
  %1 = bitcast i8* %0 to <16 x i8>*
  %2 = zext <16 x i8> %1 to <16 x i32>
  %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
  %4 = bitcast i8* %3 to <16 x i8>*
  %5 = zext <16 x i8> %4 to <16 x i32>
  %6 = sub nsw <16 x i32> %2, %5
  %7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
  %8 = sub nsw <16 x i32> zeroinitializer, %6
  %9 = select <16 x i1> %7, %6, %16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

middle.block:
%rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %10, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

define void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f32_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vcvtq2ps %ymm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm1
; CHECK-NEXT: vcvtq2ps %ymm1, %ymm1
; CHECK-NEXT: vmovaps %ymm1, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vcvtq2ps %ymm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm1
; CHECK-NEXT: vcvtq2ps %ymm1, %ymm1
; CHECK-NEXT: vmovaps %ymm1, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}
define void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="256" {  
  ; CHECK-LABEL: sbto16f64_256:  
  ; CHECK:       # %bb.0:  
  ; CHECK-NEXT:    vpmovw2m %ymm0, %k0  
  ; CHECK-NEXT:    kshiftrw $8, %k0, %k1  
  ; CHECK-NEXT:    vpmovm2d %k1, %ymm0  
  ; CHECK-NEXT:    vcvtq2pd %xmm0, %ymm1  
  ; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm0  
  ; CHECK-NEXT:    vcvtq2pd %xmm0, %ymm0  
  ; CHECK-NEXT:    vpmovm2d %k0, %ymm2  
  ; CHECK-NEXT:    vcvtq2pd %xmm2, %ymm3  
  ; CHECK-NEXT:    vextracti128 $1, %ymm2, %xmm2  
  ; CHECK-NEXT:    vcvtq2pd %xmm2, %ymm2  
  ; CHECK-NEXT:    vmovaps %ymm2, 32(%rdi)  
  ; CHECK-NEXT:    vmovaps %ymm1, (%rdi)  
  ; CHECK-NEXT:    vmovaps %ymm0, 64(%rdi)  
  ; CHECK-NEXT:    vzeroupper  
  ; CHECK-NEXT:    retq  
  %mask = icmp slt <16 x i16> %a, zeroinitializer  
  %1 = sitofp <16 x i1> %mask to <16 x float>  
  store <16 x float> %1, <16 x float>* %res  
  ret void  
}

define void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="512" {  
  ; CHECK-LABEL: sbto16f64_512:  
  ; CHECK:       # %bb.0:  
  ; CHECK-NEXT:    vpmovw2m %ymm0, %k0  
  ; CHECK-NEXT:    vpmovm2d %k0, %ymm0  
  ; CHECK-NEXT:    vcvtq2pd %xmm0, %ymm0  
  ; CHECK-NEXT:    vextracti64x4 $1, %ymm0, %xmm0  
  ; CHECK-NEXT:    vcvtq2pd %ymm0, %xmm0  
  ; CHECK-NEXT:    vmovaps %ymm0, 64(%rdi)  
  ; CHECK-NEXT:    vmovaps %ymm1, (%rdi)  
  ; CHECK-NEXT:    vzeroupper  
  ; CHECK-NEXT:    retq  
  %mask = icmp slt <16 x i16> %a, zeroinitializer  
  %1 = sitofp <16 x i1> %mask to <16 x double>  
  store <16 x double> %1, <16 x double>* %res  
  ret void  
}

define void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="512" {  
  ; CHECK-LABEL: sbto16f64_512:  
  ; CHECK:       # %bb.0:  
  ; CHECK-NEXT:    vpmovw2m %ymm0, %k0  
  ; CHECK-NEXT:    vpmovm2d %k0, %ymm0  
  ; CHECK-NEXT:    vcvtq2pd %xmm0, %ymm0  
  ; CHECK-NEXT:    vextracti64x4 $1, %ymm0, %xmm0  
  ; CHECK-NEXT:    vcvtq2pd %ymm0, %xmm0  
  ; CHECK-NEXT:    vmovaps %ymm0, 64(%rdi)  
  ; CHECK-NEXT:    vmovaps %ymm1, (%rdi)  
  ; CHECK-NEXT:    vzeroupper  
  ; CHECK-NEXT:    retq  

define void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: ubto16f32_256:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:    kshiftrw $8, %k0, %k1
    ; CHECK-NEXT:    vpmovm2d %k1, %ymm0
    ; CHECK-NEXT:    vpsrld $31, %ymm0, %ymm0
    ; CHECK-NEXT:    vcvtqd2ps %ymm0, %ymm0
    ; CHECK-NEXT:    vpmovm2d %k0, %ymm1
    ; CHECK-NEXT:    vpsrld $31, %ymm1, %ymm1
    ; CHECK-NEXT:    vcvtqd2ps %ymm1, %ymm1
    ; CHECK-NEXT:    vmovaps %ymm1, (%rdi)
    ; CHECK-NEXT:    vmovaps %ymm0, 32(%rdi)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %mask = icmp slt <16 x i16> %a, zeroinitializer
    %1 = uitofp <16 x i1> %mask to <16 x float>
    store <16 x float> %1, <16 x float>* %res
    ret void
}

define void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: ubto16f32_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:    vpmovm2d %k0, %zmm0
    ; CHECK-NEXT:    vpsrld $31, %zmm0, %zmm0
    ; CHECK-NEXT:    vcvtqd2ps %zmm0, %zmm0
    ; CHECK-NEXT:    vmovaps %zmm1, (%rdi)
    ; CHECK-NEXT:    vmovaps %zmm0, 32(%rdi)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %mask = icmp slt <16 x i16> %a, zeroinitializer
    %1 = uitofp <16 x i1> %mask to <16 x float>
    store <16 x float> %1, <16 x float>* %res
    ret void
}

define void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: ubto16f64_256:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:    kshiftrw $8, %k0, %k1

define void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f64_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:   vpmovw2m %ymm0, %k0
; CHECK-NEXT:   vpmovm2d %k0, %zmm0
; CHECK-NEXT:   vpsrlq $31, %zmm0, %zmm0
; CHECK-NEXT:   vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT:   vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT:   vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT:   vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:   vmovaps %zmm1, (%rdi)
; CHECK-NEXT:   vzeroupper
; CHECK-NEXT:   retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {
; CHECK-LABEL: test_16f32toub_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:   vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:   vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:   vcvtdq2pd %ymm0, %ymm1
; CHECK-NEXT:   vextracti128 $1, %ymm0, %ymm0
; CHECK-NEXT:   vpmovm2d %k1, %ymm0
; CHECK-NEXT:   vpsrlq $31, %ymm0, %ymm0
; CHECK-NEXT:   vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT:   vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT:   vpmovm2d %k0, %ymm2
; CHECK-NEXT:   vpsrlq $31, %ymm2, %ymm2
; CHECK-NEXT:   vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT:   vextracti64x4 $1, %ymm2, %ymm3
; CHECK-NEXT:   vpmovm2d %k0, %ymm2
; CHECK-NEXT:   vpsrlq $31, %ymm2, %ymm3
; CHECK-NEXT:   vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT:   vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT:   vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT:   vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT:   vzeroupper
; CHECK-NEXT:   retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {
; CHECK-LABEL: test_16f32toub_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:   vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:   vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:   vpmovd2m %ymm1, %k0
; CHECK-NEXT:  vcvtps2dq 32(%rdi), %ymm1
; CHECK-NEXT:  vpslld S31, %ymm1, %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k1
; CHECK-NEXT:  kunpckbw %k0, %k1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 [%k1] [z]
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}
define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {
; CHECK-LABEL: test_16f32toub_512:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vcvtps2dq (%rdi), %zmm1
; CHECK-NEXT:  vpslld S31, %zmm1, %zmm1
; CHECK-NEXT:  vpmovd2m %zmm1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 [%k1] [z]
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}
define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {
; CHECK-LABEL: test_16f32tosb_256:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vcvtps2dq (%rdi), %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k0
; CHECK-NEXT:  vcvtps2dq 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k1
; CHECK-NEXT:  kunpckbw %k0, %k1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 [%k1] [z]
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}
define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {
; CHECK-LABEL: test_16f32tosb_512:
; CHECK:    # %bb.0:
define void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {  
; CHECK-AVX512-LABEL: mul256:  
; CHECK-AVX512: # %bb.0:  
; CHECK-AVX512-NEXT: vmovdqa (%rdi), %ymm0  
; CHECK-AVX512-NEXT: vmovdqa 32(%rdi), %ymm1  
; CHECK-AVX512-NEXT: vmovdqa (%rsi), %ymm2  
; CHECK-AVX512-NEXT: vmovdqa 32(%rsi), %ymm3  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#*+}} ymm4 = ymm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#*+}} ymm5 = ymm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]  
; CHECK-AVX512-NEXT: vpmullw %ymm4, %ymm5, %ymm4  
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm4, %ymm4  
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#*+}} ymm1 = ymm3[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#*+}} ymm3 = ymm2[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]  
; CHECK-AVX512-NEXT: vpackuswb %ymm4, %ymm3, %ymm3  
; CHECK-AVX512-NEXT: vpackuswb {{.*#*+}} ymm3 = ymm2[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vzeroupper  
}
define void @mul512(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="512" {
    ; CHECK-AVX512-LABEL: mul512:
    ; CHECK-AVX512: # %bb.0:
    ; CHECK-AVX512-NEXT: vpmovdqa (%rdi), %zmm0
    ; CHECK-AVX512-NEXT: vpmovdqa 32(%rdi), %zmm1
    ; CHECK-AVX512-NEXT: vpmovdqa (%rsi), %zmm2
    ; CHECK-AVX512-NEXT: vpmovdqa 32(%rsi), %zmm3
    ; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} %zmm4 =
        ymm3[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
    ; CHECK-AVX512-NEXT: vpmullw %zmm3, %zmm1, %zmm1
    ; CHECK-AVX512-NEXT: vpmullw %zmm2, %zmm0, %zmm0
    ; CHECK-AVX512-NEXT: vzeroupper
    ; CHECK-AVX512-NEXT: retq
    %d = load <64 x i8>, <64 x i8>* %a
    %e = load <64 x i8>, <64 x i8>* %b
    %f = mul <64 x i8> %d, %e
    store <64 x i8> %f, <64 x i8>* %c
    ret void
}
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} zmm2 =
  zmm1[8,9,9,10,10,11,11,12,12,13,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
  2,42,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} zmm3 =
  zmm0[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
  2,42,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-AVX512-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-AVX512-NEXT:  vmovdqa64 {{.*#+}} zmm3 =
  55,255,255,255,255,255]
; CHECK-AVX512-NEXT:  vpandq %zmm3, %zmm2, %zmm2
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} zmm1 =
  zmm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
  2,42,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} zmm0 =
  zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
  2,42,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT:  vpmullw %zmm1, %zmm0, %zmm0
; CHECK-AVX512-NEXT:  vpmullw %zmm1, %zmm0, %zmm0
; CHECK-AVX512-NEXT:  vpmullw %zmm1, %zmm0, %zmm0
; CHECK-AVX512-NEXT:  vpackuswb %zmm2, %zmm0, %zmm0
; CHECK-AVX512-NEXT:  vmovdqa64 %zmm0, (%rdx)
; CHECK-AVX512-NEXT:  vzeroupper
; CHECK-AVX512-NEXT:  retq

; CHECK-VBMI-LABEL: mul512:
; CHECK-VBMI:       # %bb.0:
; CHECK-VBMI-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-VBMI-NEXT:  vmovdqa64 (%rsi), %zmm1
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} zmm2 =
  zmm1[8,9,9,10,10,11,11,12,12,13,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
  2,42,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} zmm3 =
  zmm0[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
  2,42,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-VBMI-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-VBMI-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-VBMI-NEXT:  vpermi2b %zmm2, %zmm0, %zmm1
; CHECK-VBMI-NEXT:  vmovdqa64 %zmm1, (%rdx)
; CHECK-VBMI-NEXT:  vzeroupper
%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void

; This threw an assertion at one point.
define <4 x i32> @mload_v4i32(<4 x i32> %trigger, <4 x i32>* %addr, <4 x i32> %dst) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: mload_v4i32:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vptestnmd %xmm0, %xmm0, %k1
    ; CHECK-NEXT:    vpblendmd (%rdi), %xmm1, %xmm0 {%k1}
    ; CHECK-NEXT:    retq
    %mask = icmp eq <4 x i32> %trigger, zeroinitializer
    %res = call <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* %addr, i32 4, <4 x i1> %mask, <4 x i32> %dst)
    ret <4 x i32> %res
}
declare <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>*, i32, <4 x i1>, <4 x i32>)

define <16 x i32> @trunc_v16i64_v16i32(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v16i64_v16i32:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
    ; CHECK-NEXT:    vmovdqa 64(%rdi), %ymm2
    ; CHECK-NEXT:    vmovdqa 96(%rdi), %ymm3
    ; CHECK-NEXT:    vpmovqd %ymm0, %xmm0
    ; CHECK-NEXT:    vpmovqd %ymm1, %xmm1
    ; CHECK-NEXT:    vpmovqd %ymm2, %xmm2
    ; CHECK-NEXT:    vpmovqd %ymm3, %xmm3
    ; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
    ; CHECK-NEXT:    vmovdqa 64(%rdi), %ymm2
    ; CHECK-NEXT:    vmovdqa 96(%rdi), %ymm3
    ; CHECK-NEXT:    vpmovqd %ymm0, %xmm0
    ; CHECK-NEXT:    vpmovqd %ymm1, %xmm1
    ; CHECK-NEXT:    vpmovqd %ymm2, %xmm2
    ; CHECK-NEXT:    vpmovqd %ymm3, %xmm3
    ; CHECK-NEXT:    vinserti128 $1, %xmm1, %ymm0, %ymm0
    ; CHECK-NEXT:    vpmovqd %ymm2, %xmm1
    ; CHECK-NEXT:    vpmovqd %ymm3, %xmm2
    ; CHECK-NEXT:    vinserti128 $1, %xmm2, %ymm1, %ymm1
    ; CHECK-NEXT:    retq
    %a = load <16 x i64>, <16 x i64>* %x
    %b = trunc <16 x i64> %a to <16 x i32>
    ret <16 x i32> %b
}
declare <16 x i32> @trunc_v16i64_v16i32(<16 x i64>* %x)
declare <16 x i8> @trunc_v16i64_v16i8(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
define <16 x i8> @trunc_v16i32_v16i8(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i8:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmovdb %ymm1, %xmm1
; CHECK-NEXT: vpmovdb %ymm0, %xmm0
; CHECK-NEXT: vpmovqldq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <16 x i32>, <16 x i32>* %x
%b = trunc <16 x i32> %a to <16 x i8>
ret <16 x i8> %b
}

define <8 x i8> @trunc_v8i64_v8i8(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i8:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmovdb %ymm1, %xmm1
; CHECK-NEXT: vpmovdb %ymm0, %xmm0
; CHECK-NEXT: vpmovqldq {{.*#+}} xmm0 = xmm0[0],xmm1[0]
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <8 x i32>, <8 x i32>* %x
%b = trunc <8 x i32> %a to <8 x i8>
ret <8 x i8> %b
}

define <8 x i16> @trunc_v8i64_v8i16(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i16:
; CHECK: # %bb.0:
define <8 x i32> @trunc_v8i64_v8i32_zeroes(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v8i64_v8i32_zeroes:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vpsrlq $48, 32(%rdi), %ymm1
    ; CHECK-NEXT:  vpsrlq $48, (%rdi), %ymm2
    ; CHECK-NEXT:  vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]
    ; CHECK-NEXT:  vpermi2w %ymm1, %ymm2, %ymm0
    ; CHECK-NEXT:  retq
    %a = load <8 x i64>, <8 x i64>* %x
    %b = lshr <8 x i64> %a, <i64 16, i64 16, i64 16, i64 16, i64 16, i64 16, i64 16, i64 16>
    %c = trunc <8 x i64> %b to <8 x i32>
    ret <8 x i32> %c
}

define <16 x i16> @trunc_v16i32_v16i16_zeroes(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v16i32_v16i16_zeroes:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vpsrlw $8, 32(%rdi), %ymm0
    ; CHECK-NEXT:  vpackuswb %ymm0, %ymm1, %ymm0
    ; CHECK-NEXT:  vpermi2w {{.*#+}} ymm0 = ymm0[0,2,1,3]
    ; CHECK-NEXT:  retq
    %a = load <16 x i32>, <16 x i32>* %x
    %b = lshr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16>
    %c = trunc <16 x i32> %b to <16 x i16>
    ret <16 x i16> %c
}

define <32 x i8> @trunc_v32i16_v32i8_zeroes(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_zeroes:
    ; CHECK-AVX512:       # %bb.0:
    ; CHECK-AVX512-NEXT:  vpsrlw S8, 32(%rdi), %ymm0
    ; CHECK-AVX512-NEXT:  vpsrlw S8, (%rdi), %ymm1
    ; CHECK-AVX512-NEXT:  vpackuswb %ymm0, %ymm1, %ymm0
    ; CHECK-AVX512-NEXT:  vpermi2w {{.*#+}} ymm0 = ymm0[0,2,1,3]
    ; CHECK-AVX512-NEXT:  retq

define <8 x i32> @trunc_v8i64_v8i32_sign(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {    
    ; CHECK-LABEL: trunc_v8i64_v8i32_sign:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpsraq $48, 32(%rdi), %ymm0
    ; CHECK-NEXT:    vpsraq $48, (%rdi), %ymm1
    ; CHECK-NEXT:    vpmovqd %ymm1, %xmm1
    ; CHECK-NEXT:    vpmovqd %ymm0, %xmm0
    ; CHECK-NEXT:    vinserti128 $1, %xmm0, %ymm1, %ymm0
    ; CHECK-NEXT:    retq
    %a = load <8 x i64>, <8 x i64>* %x
    %b = ashr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>
    %c = trunc <8 x i64> %b to <8 x i32>
    ret <8 x i32> %c
}

define <16 x i16> @trunc_v16i32_v16i16_sign(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {    
    ; CHECK-LABEL: trunc_v16i32_v16i16_sign:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vmovdqa (%rdi), %ymm1
    ; CHECK-NEXT:    vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]
    ; CHECK-NEXT:    vpermi2w 32(%rdi), %ymm1, %ymm0
    ; CHECK-NEXT:    retq
    %a = load <16 x i32>, <16 x i32>* %x
    %b = ashr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16>
    %c = trunc <16 x i32> %b to <16 x i16>
    ret <16 x i16> %c
}

define <32 x i8> @trunc_v32i16_v32i8_sign(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {    
    ; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_sign:
    ; CHECK-AVX512:       # %bb.0:
    ; CHECK-AVX512-NEXT:    vpsraw $8, 32(%rdi), %ymm0

define void @zext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: zext_v16i8_v16i64:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovzxwb {{.*#+}} ymm1 = xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero
; CHECK-NEXT: vpshufd {{.*#+}} xmm2 = xmm1[2,3,0,1]
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm2 = xmm2[0],zero,zero,xmm2[1],zero,zero,xmm2[2],zero,zero,xmm2[3],zero,zero,zero
; CHECK-NEXT: vextracti128 $1, %ymm1, %x
; CHECK-NEXT: vpshufd {{.*#+}} xmm3 = xmm1[2,3,0,1]
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm3 = xmm3[0],zero,zero,xmm3[1],zero,zero,xmm3[2],zero,zero,xmm3[3],zero,zero,zero
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm1 = xmm1[0],zero,zero,xmm1[1],zero,zero,xmm1[2],zero,zero,xmm1[3],zero,zero,zero
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm0 = xmm0[0],zero,zero,zero,xmm0[1],zero,zero,zero,xmm0[2],zero,zero,zero,zero
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm0 = xmm0[0],zero,zero,zero,xmm0[1],zero,zero,zero,xmm0[2],zero,zero,zero,zero
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = zext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}
define void @sext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" { 
; CHECK-LABEL: sext_v16i8_v16i64: 
; CHECK: # %bb.0: 
; CHECK-NEXT: vpmovsxbw %xmm0, %ymm0 
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1] 
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm2 
; CHECK-NEXT: vpshufd {{.*#+}} xmm3 = xmm2[2,3,0,1] 
; CHECK-NEXT: vpmovsxdw %xmm3, %ymm3 
; CHECK-NEXT: vmovdqa %ymm2, 64(%rdi) 
; CHECK-NEXT: vmovdqa %ymm0, (%rdi) 
; CHECK-NEXT: vmovdqa %ymm3, 96(%rdi) 
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdi) 
; CHECK-NEXT: vzeroupper 
; CHECK-NEXT: retq %a = sext <16 x i8> %x to <16 x i64> 
store <16 x i64> %a, <16 x i64>* %y 
ret void 
}

define void @vselect_split_v8i16_setcc(<8 x i16> %s, <8 x i16> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" { 
; CHECK-LABEL: vselect_split_v8i16_setcc: 
; CHECK: # %bb.0: 
; CHECK-NEXT: vpmovsxbw (%rsi), %ymm2 
; CHECK-NEXT: vpmovsxbw 32(%rsi), %ymm3 
; CHECK-NEXT: vpcmpeqw %xmm1, %xmm0, %k1 
; CHECK-NEXT: kshiftrb $4, %k1, %k2 
; CHECK-NEXT: vpmovdqa64 32(%rdi), %ymm3 {%k2} 
; CHECK-NEXT: vpmovdqa64 (%rdi), %ymm2 {%k1} 
; CHECK-NEXT: vpmovdqa %ymm2, (%rdx) 
; CHECK-NEXT: vpmovdqa %ymm3, 32(%rdx) 
; CHECK-NEXT: vzeroupper 
; CHECK-NEXT: retq %x = load <8 x i64>, <8 x i64>* %p 
%y = load <8 x i64>, <8 x i64>* %q 
%a = icmp eq <8 x i16> %s, %t 
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y 
store <8 x i64> %b, <8 x i64>* %r 
ret void 
}

define void @vselect_split_v8i32_setcc(<8 x i32> %s, <8 x i32> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" { 
; CHECK-LABEL: vselect_split_v8i32_setcc: 

; CHECK:       # %bb.0:
; CHECK-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:  vpcmpeqd %ymm1, %ymm0, %k1
; CHECK-NEXT:  kshiftrb $4, %k1, %k2
; CHECK-NEXT:  vmovdqa64 32(%rdi), %ymm3 [%k2]
; CHECK-NEXT:  vmovdqa64 (%rdi), %ymm2 [%k1]
; CHECK-NEXT:  vmovdqa %ymm2, (%rdx)
; CHECK-NEXT:  vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
%a = icmp eq <8 x i32> %s, %t
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}
define void @vselect_split_v16i8_setcc(<16 x i8> %s, <16 x i8> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i8_setcc:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:  vpcmpeqb %xmm1, %xmm0, %k1
; CHECK-NEXT:  kshiftrw $8, %k1, %k2
; CHECK-NEXT:  vmovdqa32 32(%rdi), %ymm3 [%k2]
; CHECK-NEXT:  vmovdqa32 (%rdi), %ymm2 [%k1]
; CHECK-NEXT:  vmovdqa %ymm2, (%rdx)
; CHECK-NEXT:  vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%x = load <16 x i32>, <16 x i32>* %p
%y = load <16 x i32>, <16 x i32>* %q
%a = icmp eq <16 x i8> %s, %t
%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
store <16 x i32> %b, <16 x i32>* %r
ret void
}
define void @vselect_split_v16i16_setcc(<16 x i16> %s, <16 x i16> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i16_setcc:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:  vpcmpeqw %ymm1, %ymm0, %k1
; CHECK-NEXT:  kshiftrb $4, %k1, %k2
; CHECK-NEXT:  vmovdqa64 32(%rdi), %ymm3 [%k2]
; CHECK-NEXT:  vmovdqa64 (%rdi), %ymm2 [%k1]
; CHECK-NEXT:  vmovdqa %ymm2, (%rdx)
; CHECK-NEXT:  vmovdqa %ymm3, 32(%rdx)

; CHECK-NEXT:  kshiftrw $8, %k1, %k2
; CHECK-NEXT:  vmovdqa32 32(%rdi), %ymm3 { %k2 }
; CHECK-NEXT:  vmovdqa32 (%rdi), %ymm2 { %k1 }
; CHECK-NEXT:  vmovdqa %ymm2, (%rdx)
; CHECK-NEXT:  vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <16 x i32>, <16 x i32>* %p
%b = icmp eq <16 x i16> %s, %t
%c = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
store <16 x i32> %b, <16 x i32>* %r
ret void
}
define <16 x i8> @trunc_packus_v16i32_v16i8(<16 x i32>* %p) "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_packus_v16i32_v16i8:
; CHECK:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vpackusdw 32(%rdi), %ymm0, %ymm0
; CHECK-NEXT:  vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT:  vpmovuswb %ymm0, %xmm0
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <16 x i32>, <16 x i32>* %p
%b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> %x, <16 x i32> %y
ret <16 x i8> %f
}
define void @trunc_packus_v16i32_v16i8_store(<16 x i32>* %p, <16 x i8>* %q) "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_packus_v16i32_v16i8_store:
; CHECK:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vpackusdw 32(%rdi), %ymm0, %ymm0
; CHECK-NEXT:  vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT:  vpmovuswb %ymm0, %rsi
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <16 x i32>, <16 x i32>* %p
%b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> %c, <16 x i32> %i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255
%d = icmp sgt <16 x i32> %c, zerosinitializer
%e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zerosinitializer
%f = movi <16 x i32> 0 to <16 x i8>
store <16 x i8> %f, <16 x i8>* %q
ret void
}

define <64 x i1> @v64i1_argument_return(<64 x i1> %x) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: v64i1_argument_return:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    retq
    ret <64 x i1> %x
}

define void @v64i1_shuffle(<64 x i8>* %x, <64 x i8>* %y) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: v64i1_shuffle:
    ; CHECK:       # %bb.0: # %entry
    ; CHECK-NEXT:    vmovdqa (%rdi), %ymm1
    ; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm0
    ; CHECK-NEXT:    vptestnmb %ymm1, %ymm1, %k0
    ; CHECK-NEXT:    kshiftrd $1, %k0, %k1
    ; CHECK-NEXT:    movq $-3, %rax
    ; CHECK-NEXT:    kmovq %rax, %k2
    ; CHECK-NEXT:    kandq %k2, %k1, %k1
    ; CHECK-NEXT:    kshiftlq $63, %k2, %k2
    ; CHECK-NEXT:    kshiftrq $62, %k2, %k2
    ; CHECK-NEXT:    korq %k2, %k1, %k1
    ; CHECK-NEXT:    movq $-5, %rax
    ; CHECK-NEXT:    kmovq %rax, %k2
    ; CHECK-NEXT:    kandq %k2, %k1, %k1
    ; CHECK-NEXT:    kshiftlq $63, %k2, %k2
    ; CHECK-NEXT:    kshiftrq $61, %k2, %k2
    ; CHECK-NEXT:    korq %k2, %k1, %k1
    ; CHECK-NEXT:    movq $-9, %rax
    ; CHECK-NEXT:    kmovq %rax, %k2
    ; CHECK-NEXT:    kandq %k2, %k1, %k1
    ; CHECK-NEXT:    kshiftlq $63, %k2, %k2
    ; CHECK-NEXT:    kshiftrq $60, %k2, %k2
    ; CHECK-NEXT:    korq %k2, %k1, %k1
    ; CHECK-NEXT:    movq $-17, %rax
    ; CHECK-NEXT:    kmovq %rax, %k2
    ; CHECK-NEXT:    kandq %k2, %k1, %k1
    ; CHECK-NEXT:    kshiftlq $5, %k0, %k2
    ; CHECK-NEXT:    kshiftrq $63, %k2, %k2
; CHECK-NEXT:   kshiftrq $59, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-33, %rax
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftrd $4, %k0, %k2
; CHECK-NEXT:   kshiftlq $63, %k2, %k2
; CHECK-NEXT:   kshiftrq $58, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-65, %rax
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftrd $7, %k0, %k2
; CHECK-NEXT:   kshiftlq $63, %k2, %k2
; CHECK-NEXT:   kshiftrq $57, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-129, %rax
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftrd $6, %k0, %k2
; CHECK-NEXT:   kshiftlq $63, %k2, %k2
; CHECK-NEXT:   kshiftrq $56, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-257, %rax # imm = 0xFEFF
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftrd $9, %k0, %k2
; CHECK-NEXT:   kshiftlq $63, %k2, %k2
; CHECK-NEXT:   kshiftrq $55, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-513, %rax # imm = 0xFDFF
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftrd $8, %k0, %k2
; CHECK-NEXT:   kshiftlq $63, %k2, %k2
; CHECK-NEXT:   kshiftrq $54, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-1025, %rax # imm = 0xFBFF
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftrd $11, %k0, %k2
; CHECK-NEXT:   kshiftlq $63, %k2, %k2
; CHECK-NEXT:   kshiftrq $53, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-2049, %rax # imm = 0xF7FF
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftrd $10, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $52, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-4097, %rax # imm = 0xEFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $51, %k2, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  movq $-8193, %rax # imm = 0xDFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftlq $13, %k0, %k2
; CHECK-NEXT:  kshiftrq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $50, %k2, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  movq $-16385, %rax # imm = 0xBFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftlq $12, %k0, %k2
; CHECK-NEXT:  kshiftrq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $49, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-32769, %rax # imm = 0xFFFF7FFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $15, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $48, %k2, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  movq $-65537, %rax # imm = 0xFFFEFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $14, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $47, %k2, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  movq $-131073, %rax # imm = 0xFFFEEEEF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $17, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $46, %k2, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  movq $-262145, %rax # imm = 0xFFFBBBBF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1

Open Source Used in CLI Analyzer 3.6.8 799
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $24, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $38, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-67108865, %rax # imm = 0xFBFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $27, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $37, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-134217729, %rax # imm = 0xF7FFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $26, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $36, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-268435457, %rax # imm = 0xEFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $29, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $35, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-536870913, %rax # imm = 0xDFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $28, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $34, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-1073741825, %rax # imm = 0xBFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $31, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $33, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movabsq $-2147483649, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $30, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $32, %k2, %k2
; CHECK-NEXT:  korq %k0, %k2, %k0

Open Source Used In CLI Analyzer 3.6.8 801
; CHECK-NEXT: movabsq $-4294967297, %rax # imm = 0xFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $1, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $31, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-8589934593, %rax # imm = 0xFFFFFFFFDFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrlq $63, %k1, %k2
; CHECK-NEXT: kshiftlq $30, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-17179869185, %rax # imm = 0xFFFFFFFFBFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $3, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $29, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-34359738369, %rax # imm = 0xFFFFFFFF7FFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $2, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $28, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-68719476737, %rax # imm = 0xFFFFFFFFDFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $4, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $27, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-137438953473, %rax # imm = 0xFFFFFFFFDFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $5, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $26, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-274877906945, %rax # imm = 0xFFFFFFFFBFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $7, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $25, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-549755813889, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $6, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $24, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-1099511627777, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $9, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $23, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-2199023255553, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $8, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $22, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-4398046511105, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $11, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $21, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-8796093022209, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $10, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $20, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-1759218604417, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $13, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $19, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-35184372088833, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $12, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $18, %k2, %k2
entry:
%a = load <64 x i8>, <64 x i8>* %x
%b = icmp eq <64 x i8> %a, zeroinitializer
%shuf = shufflevector <64 x i1> %b, undef, <64 x i1> <i32 1, i32 0, i32 3, i32 2, i32 5, i32 4, i32 7, i32 6, i32 9, i32 8, i32 11, i32 10, i32 13, i32 12, i32 15, i32 14, i32 17, i32 16, i32 19, i32 18, i32 21, i32 20, i32 23, i32 22, i32 25, i32 24, i32 27, i32 26, i32 29, i32 28, i32 31, i32 30, i32 33, i32 32, i32 35, i32 34, i32 37, i32 36, i32 39, i32 38, i32 41, i32 40, i32 43, i32 42, i32 45, i32 44, i32 47, i32 46, i32 49, i32 48, i32 51, i32 50, i32 53, i32 52, i32 55, i32 54, i32 57, i32 56, i32 59, i32 58, i32 61, i32 60, i32 63, i32 62>
call void @llvm.masked.store.v64i8.p0v64i8(<64 x i8> %a, <64 x i8>* %y, %i32 1, <64 x i1> %shuf)
ret void
}
declare void @llvm.masked.store.v64i8.p0v64i8(<64 x i8>, <64 x i8>* , %i32, <64 x i1>)

@mem64_dst = global i64 0, align 8
@mem64_src = global i64 0, align 8
define i32 @v64i1_inline_asm() "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_inline_asm:
; CHECK:
# %bb.0:
; CHECK-NEXT: kmovq {{.*}}(%rip), %k0
; CHECK-NEXT: #APP
; CHECK-NEXT: #NO_APP
; CHECK-NEXT: kmovq %k0, {{.*}}(%rip)
; CHECK-NEXT: movl -{{[0-9]+}}(%rsp), %eax
; CHECK-NEXT: retq
%1 = alloca i32, align 4
%2 = load i64, i64* @mem64_src, align 8
%3 = call i64 asm "", "=k,k,~{dirflag},~{fpsr},~{flags}"(i64 %2)
store i64 %3, i64* @mem64_dst, align 8
%4 = load i32, i32* %1, align 4
ret i32 %4
}
define void @cmp_v8i64_sext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-vectorwidth"="256" {
; CHECK-LABEL: cmp_v8i64_sext:
; CHECK:
# %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT: vpcmpgtq 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT: vpcmpgtq (%rdi), %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %xptr
%y = load <8 x i64>, <8 x i64>* %yptr
%cmp = icmp slt <8 x i64> %x, %y
%ext = sext <8 x i1> %cmp to <8 x i64>
store <8 x i64> %ext, <8 x i64>* %zptr
ret void
}
define void @cmp_v8i64_zext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-vectorwidth"="256" {
; CHECK-LABEL: cmp_v8i64_zext:
; CHECK:
# %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT: vpcmpgtq 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT: vpcmpgtq (%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpsrlq $63, %ymm1, %ymm1
; CHECK-NEXT: vpsrlq $63, %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)

Open Source Used In CLI Analyzer 3.6.8 807


define <16 x i8> @var_rotate_v16i8(<16 x i8> %a, <16 x i8> %b) nounwind "min-legal-vector-width"="256" {
  ; CHECK-LABEL: var_rotate_v16i8:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:    vmovdqa {{.*#+}} xmm2 = [8,8,8,8,8,8,8,8,8,8,8,8,8,8,8,8]
  ; CHECK-NEXT:    vpsubb %xmm1, %xmm2, %xmm2
  ; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm1 =
     xmm1[0],zero,xmm1[1],zero,xmm1[2],zero,xmm1[3],zero,xmm1[4],zero,xmm1[5],zero,xmm1[6],zero,xmm1[7],zero,
     xmm1[8],zero,xmm1[9],zero,xmm1[10],zero,xmm1[11],zero,xmm1[12],zero,xmm1[13],zero,xmm1[14],zero,xmm1[15],zero
  ; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm0 =
     xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,
     xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero
  ; CHECK-NEXT:    vpsllvw %ymm1, %ymm0, %ymm1
  ; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm2 =
     xmm2[0],zero,xmm2[1],zero,xmm2[2],zero,xmm2[3],zero,xmm2[4],zero,xmm2[5],zero,xmm2[6],zero,xmm2[7],zero,
     xmm2[8],zero,xmm2[9],zero,xmm2[10],zero,xmm2[11],zero,xmm2[12],zero,xmm2[13],zero,xmm2[14],zero,xmm2[15],zero
  ; CHECK-NEXT:    vpsrlvw %ymm2, %ymm0, %ymm0
  ; CHECK-NEXT:    vpor %ymm0, %ymm1, %ymm0
  ; CHECK-NEXT:    vpmovwb %ymm0, %xmm0
  ; CHECK-NEXT:    vzeroupper
  ; CHECK-NEXT:    retq
%
  %b8 = sub <16 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %b
  %shl = shl <16 x i8> %a, %b
  %lshr = lshr <16 x i8> %a, %b
  %or = or <16 x i8> %shl, %lshr
  ret <16 x i8> %or
%
}

define <32 x i8> @var_rotate_v32i8(<32 x i8> %a, <32 x i8> %b) nounwind "min-legal-vector-width"="256" {
  ; CHECK-LABEL: var_rotate_v32i8:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:    vpsllw $4, %ymm0, %ymm2
  ; CHECK-NEXT:    vpsrlw $4, %ymm0, %ymm3
  ; CHECK-NEXT:    vpternlogq $216, {{.*}}(%rip), %ymm2, %ymm3
  ; CHECK-NEXT:    vpsllw $5, %ymm1, %ymm1
define <32 x i8> @splatvar_rotate_v32i8(<32 x i8> %a, <32 x i8> %b) nounwind "min-legal-vector-width"="256" {
  ; CHECK-LABEL: splatvar_rotate_v32i8:
  ; CHECK:   # %bb.0:
  %b8 = sub <32 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %b
  %shl = shl <32 x i8> %a, %b8
  %lshr = lshr <32 x i8> %a, %b8
  %or = or <32 x i8> %shl, %lshr
  ret <32 x i8> %or
}
{% or = or <32 x i8> %shl, %lshr
ret <32 x i8> %or
%
define <32 x i8> @constant_rotate_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" { 
    ; CHECK-AVX512-LABEL: constant_rotate_v32i8:
    ; CHECK-AVX512: # %bb.0:
    ; CHECK-AVX512-NEXT: vpshldw $4, %ymm0, %ymm1
    ; CHECK-AVX512-NEXT: vpand {{.*}}(%rip), %ymm1, %ymm1
    ; CHECK-AVX512-NEXT: vbroadcasti128 {{.*#+}} %ymm2 =
      [8192,24640,41088,57356,57344,41152,24704,8256,8192,24640,41088,57356,57344,41152,24704,8256]
    ; CHECK-AVX512-NEXT: # %ymm2 = mem[0,1,0,1]
    ; CHECK-AVX512-NEXT: vpblendvb %ymm2, %ymm1, %ymm0, %ymm1
    ; CHECK-AVX512-NEXT: vpshldw $2, %ymm1, %ymm3
    ; CHECK-AVX512-NEXT: vpand {{.*}}(%rip), %ymm3, %ymm3
    ; CHECK-AVX512-NEXT: vpaddb %ymm2, %ymm2, %ymm2
    ; CHECK-AVX512-NEXT: vpblendvb %ymm2, %ymm3, %ymm1, %ymm1
    ; CHECK-AVX512-NEXT: vpaddb %ymm1, %ymm1, %ymm3
    ; CHECK-AVX512-NEXT: vpaddb %ymm2, %ymm2, %ymm2
    ; CHECK-AVX512-NEXT: vpblendvb %ymm2, %ymm3, %ymm1, %ymm1
    ; CHECK-AVX512-NEXT: vpshldw {{.*#+}} %ymm3 =
      ymm0[8],ymm2[8],ymm0[9],ymm2[9],ymm0[10],ymm2[10],ymm0[11],ymm2[11],ymm0[12],ymm2[12],ymm0[13],ymm2[13],ymm0[14],ymm2[14],ymm0[15],ymm2[15],ymm0[16],ymm2[16],ymm0[17],ymm2[17],ymm0[18],ymm2[18],ymm0[19],ymm2[19],ymm0[20],ymm2[20],ymm0[21],ymm2[21],ymm0[22],ymm2[22],ymm0[23],ymm2[23]
    ; CHECK-AVX512-NEXT: vpshldw {{.*}}(%rip), %ymm3, %ymm3
    ; CHECK-AVX512-NEXT: vpshldw $8, %ymm3, %ymm3
    ; CHECK-AVX512-NEXT: vpunpcklbhw {{.*#+}} %ymm0 =
      ymm0[0],ymm2[0],ymm0[1],ymm2[1],ymm0[2],ymm2[2],ymm0[3],ymm2[3],ymm0[4],ymm2[4],ymm0[5],ymm2[5],ymm0[6],ymm2[6],ymm0[7],ymm2[7],ymm0[8],ymm2[8],ymm0[9],ymm2[9],ymm0[10],ymm2[10],ymm0[11],ymm2[11],ymm0[12],ymm2[12],ymm0[13],ymm2[13],ymm0[14],ymm2[14],ymm0[15],ymm2[15],ymm0[16],ymm2[16],ymm0[17],ymm2[17],ymm0[18],ymm2[18],ymm0[19],ymm2[19],ymm0[20],ymm2[20],ymm0[21],ymm2[21],ymm0[22],ymm2[22],ymm0[23],ymm2[23]
    ; CHECK-AVX512-NEXT: vpshldw {{.*}}(%rip), %ymm0, %ymm0
    ; CHECK-AVX512-NEXT: vpshldw $8, %ymm0, %ymm0
    ; CHECK-AVX512-NEXT: vpackuswb %ymm3, %ymm0, %ymm0
    ; CHECK-AVX512-NEXT: vpshldw %ymm0, %ymm1, %ymm1
    ; CHECK-AVX512-NEXT: vpshldw %ymm0, %ymm0
    ; CHECK-VMBMI-LABEL: constant_rotate_v32i8:
    ; CHECK-VMBMI: # %bb.0:
    ; CHECK-VMBMI-NEXT: vpshldw $4, %ymm0, %ymm1
    ; CHECK-VMBMI-NEXT: vpand {{.*}}(%rip), %ymm1, %ymm1
    ; CHECK-VMBMI-NEXT: vbroadcasti128 {{.*#+}} %ymm2 =
      [8192,24640,41088,57356,57344,41152,24704,8256,8192,24640,41088,57356,57344,41152,24704,8256]
    ; CHECK-VMBMI-NEXT: # %ymm2 = mem[0,1,0,1]
    ; CHECK-VMBMI-NEXT: vpblendvb %ymm2, %ymm1, %ymm0, %ymm1
    ; CHECK-VMBMI-NEXT: vpshldw $2, %ymm1, %ymm3
    ; CHECK-VMBMI-NEXT: vpand {{.*}}(%rip), %ymm3, %ymm3

Open Source Used In CLI Analyzer 3.6.8 810
define <32 x i8> @splatconstant_rotate_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: splatconstant_rotate_v32i8:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vpsllw $4, %ymm0, %ymm1
; CHECK-NEXT:  vpsrlw $4, %ymm0, %ymm0
; CHECK-NEXT:  vpternlogq $216, [[*]](%rip), %ymm1, %ymm0
; CHECK-NEXT:  retq
%shl = shl <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 9, i8 10, i8 11, i8 12>
%lshr = lshr <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 9, i8 10, i8 11, i8 12>
%or = or <32 x i8> %shl, %lshr
ret <32 x i8> %or
}

define <32 x i8> @splatconstant_rotate_mask_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: splatconstant_rotate_mask_v32i8:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vpsllw $4, %ymm0, %ymm1
; CHECK-NEXT:  vpsrlw $4, %ymm0, %ymm0
; CHECK-NEXT:  vpternlogq $216, [[*]](%rip), %ymm1, %ymm0
; CHECK-NEXT:  retq
%shl = shl <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 9, i8 10, i8 11, i8 12>
%lshr = lshr <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 9, i8 10, i8 11, i8 12>
%or = or <32 x i8> %shl, %lshr
ret <32 x i8> %or
}
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add_lldb_library(lldbPluginObjectContainerBSDArchive PLUGIN
ObjectContainerBSDArchive.cpp

LINK_LIBS
  lldbCore
  lldbHost
  lldbSymbol

LINK_COMPONENTS
  Support
)

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target triple = "hexagon"

%struct.0 = type { i8*, i8, %union.anon.0 }
%union.anon.0 = type { i8* }

define hidden fastcc void @fred() unnamed_addr #0 {
  entry:
    br i1 undef, label %while.end, label %while.body.lr.ph
while.body.lr.ph: ; preds = %entry
br label %while.body

while.body: ; preds = %exit.2, %while.body.lr.ph
%lsr.iv = phi %struct.0* [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
switch i32 undef, label %exit [
  i32 1, label %sw.bb.i
  i32 2, label %sw.bb3.i
]

sw.bb.i: ; preds = %while.body
unreachable

sw.bb3.i: ; preds = %while.body
unreachable

exit: ; preds = %while.body
switch i32 undef, label %exit.2 [
  i32 1, label %sw.bb.i17
  i32 2, label %sw.bb3.i20
]

sw.bb.i17: ; preds = %.exit
%0 = bitcast %struct.0* %lsr.iv to i32*
%1 = load i32, i32* %0, align 4
unreachable

sw.bb3.i20: ; preds = %exit
%2 = bitcast %struct.0* %lsr.iv to i8**
%3 = load i8*, i8** %2, align 4
unreachable

exit.2: ; preds = %exit
%cgep22 = getelementptr %struct.0*, %struct.0* %lsr.iv, i32 1
br label %while.body

while.end: ; preds = %entry
ret void
}

attributes #0 = { nounwind optsiz "target-cpu"="hexagonv55" }
; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature --scrub-attributes
; RUN: opt -attributor -attributor-manifest-internal -attributor-max-iterations-verify -attributor-annotate-decl-cs -attributor-max-iterations=4 -S < %s | FileCheck %s --check-prefixes=CHECK,NOT_CGSCC_NPM,NOT_CGSCC_OPM,NOT_TUNIT_NPM,IS__TUNIT____,IS________OMP,M,IS__TUNIT_OPM
; RUN: opt -aa-pipeline=basic-aa -passes=attributor -attributor-manifest-internal -attributor-max-iterations-verify -
attributor-annotate-decl-cs -attributor-max-iterations=3 -S < %s | FileCheck %s --check-prefixes=CHECK,NOT_CGSCC_OPM,NOT_CGSCC_NPM,NOT_TUNIT_OPM,IS__TUNIT____,IS________NP M,IS__TUNIT_NPM
; RUN: opt -attributor-cgscc -attributor-manifest-internal -attributor-annotate-decl-cs -S < %s | FileCheck %s --check-prefixes=CHECK,NOT_TUNIT_NPM,NOT_TUNIT_OPM,NOT_CGSCC_NPM,IS__CGSCC____,IS________OP M,IS__CGSCC_OPM
; RUN: opt -aa-pipeline=basic-aa -passes=attributor-cgscc -attributor-manifest-internal -attributor-annotate-decl-cs -S < %s | FileCheck %s --check-prefixes=CHECK,NOT_TUNIT_NPM,NOT_TUNIT_OPM,NOT_CGSCC_OPM,IS__CGSCC____,IS________NP M,IS__CGSCC_OPM
; Test that we only promote arguments when the caller/callee have compatible attributes.

Test that we only promote arguments when the caller/callee have compatible attributes.

target triple = "x86_64-unknown-linux-gnu"

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* %arg1) #0 {

; NOT_TUNIT_NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; NOT_TUNIT_NPM-NEXT: bb:
; NOT_TUNIT_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; NOT_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: ret void

; IS__TUNIT_NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writable only align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]])
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT: ret void

bb:
%tmp = load <8 x i64>, <8 x i64>* %arg
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {


; IS__TUNIT_OPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__TUNIT_OPM-SAME: (\(<8 \times i64\>* \text{nocapture writeonly } [[\text{ARG}:%.*]])
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__TUNIT_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* \text{nocapture nofree nonnull writeonly align 64 dereferenceable(64) } [[\text{TMP2}]], <8 x i64>* \text{nocapture nofree nonnull readonly align 64 dereferenceable(64) } [[\text{TMP}]]
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__TUNIT_NPM-SAME: (\(<8 \times i64\>* \text{nocapture writeonly } [[\text{ARG}:%.*]])
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* \text{noalias nofree nofree nonnull writeonly align 64 dereferenceable(64) } [[\text{TMP2}]], <8 x i64>* \text{noalias nofree nofree nonnull readonly align 64 dereferenceable(64) } [[\text{TMP}]]
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__CGSCC_OPM-SAME: (\(<8 \times i64\>* \text{nocapture writeonly align 2 dereferenceable(64) } [[\text{ARG}:%.*]])
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__CGSCC_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* \text{noalias nofree nofree nofree nonnull writeonly align 64 dereferenceable(64) } [[\text{TMP2}]], <8 x i64>* \text{noalias nofree nofree nofree nonnull writeonly align 64 dereferenceable(64) } [[\text{TMP}]]
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void
;
; IS__CGSCC_NPM-LABEL: define [{{[^@]+}}] @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [TMP:.%.*] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [TMP2:.%.*] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [TMP3:.%.*] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP2]])
; IS__CGSCC_NPM-NEXT: [TMP4:.%.*] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void

; bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
;
; NOT_TUNIT_NPM-LABEL: define
{{[^@]+}} @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; NOT_TUNIT_NPM-NEXT: bb:
; NOT_TUNIT_NPM-NEXT: [TMP:.%.*] = load <8 x i64>, <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: ret void
;
; IS__TUNIT_NPM-LABEL: define
{{[^@]+}} @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:.%.*]])
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [ARG1_PRIV:.%.*] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

@ callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) {
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

@ callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) {
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}
; IS__CGSCC_OPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP2]] to i8*
; IS__CGSCC_OPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT:  call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nofree nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64
dereferenceable(64) [[TMP3]])
; IS__CGSCC_OPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT:  ret void

; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT:  bb:
; IS__CGSCC_NPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT:  call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly
align 64 dereferenceable(64) [[TMP3]])
; IS__CGSCC_NPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT:  ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {

; NOT_TUNIT_NPM-LABEL: define
{{[^@]+}} @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
  ; NOT_TUNIT_NPM-LABEL: define
  {{[^@]+}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
  ; NOT_TUNIT_NPM-SAME: (8 x i64)* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], (8 x i64)* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
  ; NOT_TUNIT_NPM-NEXT: bb:
  ; NOT_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
  ; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
  ; NOT_TUNIT_NPM-NEXT: ret void
  ;
  ; IS_TUNIT_NPM-LABEL: define
  {{[^@]+}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
  ; NOT_TUNIT_NPM-NEXT: bb:
  ; IS_TUNIT_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
  ; IS_TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
  ; IS_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
  ; IS_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
  ; IS_TUNIT_NPM-NEXT: ret void
  ; bb:
  ;
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
  ;
  ; IS_TUNIT_OPM-LABEL: define {}
  ;@avx512_legal512_prefer256_call_avx512_legal512_prefer512
  ; IS_TUNIT_OPM-SAME: (8 x i64)* nocapture writeonly [[ARG:%.*]])
  ; IS_TUNIT_OPM-NEXT: bb:
  ; IS_TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; IS_TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; IS_TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; IS_TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; IS_TUNIT_OPM-NEXT: call fastcc void
  @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__TUNIT_OPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT:  ret void

; IS__TUNIT_NPM-LABEL: define ([[^@]+]) @avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__TUNIT_NPM-SAME:  (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; IS__TUNIT_NPM-NEXT:  bb:
; IS__TUNIT_NPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__TUNIT_NPM-NEXT:  [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT:  call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(8 x i64)* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]])
; IS__TUNIT_NPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT:  ret void

; IS__CGSCC_OPM-LABEL: define ([[^@]+]) @avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__CGSCC_OPM-SAME:  (<8 x i64>* nocapture writeonly 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_OPM-NEXT:  bb:
; IS__CGSCC_OPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT:  call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(8 x i64)* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_OPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT:  ret void

; IS__CGSCC_NPM-LABEL: define ([[^@]+]) @avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__CGSCC_NPM-SAME:  (<8 x i64>* nocapture writeonly 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT:  bb:
; IS__CGSCC_NPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT:  call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(8 x i64)* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]]
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #1 {

bb:
%tmp = alloc <8 x i64>, align 32
%tmp2 = alloc <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #1 {

bb:
%tmp = alloc <8 x i64>, align 32
%tmp2 = alloc <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #1 {

bb:
%tmp = alloc <8 x i64>, align 32
%tmp2 = alloc <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {

bb:
%tmp = alloc <8 x i64>, align 32
%tmp2 = alloc <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg
ret void
}
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 {
    ; NOT_TUNIT_NPM-LABEL: define
    {{[^@]+}} @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64)
    [[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
    ; NOT_TUNIT_NPM-NEXT: bb:
    ; NOT_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
    ; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
    ; NOT_TUNIT_NPM-NEXT: ret void
    ;
    ; IS__TUNIT_NPM-LABEL: define
    {{[^@]+}} @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nofree nonnull writeonly align 64 dereferenceable(64)
    [[ARG:%.*]], <8 x i64>* noalias nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
    ; IS__TUNIT_NPM-NEXT: bb:
    ; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
    ; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
    ; IS__TUNIT_NPM-NEXT: ret void
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
  ; IS__TUNIT_OPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal256_prefer256
  ; IS__TUNIT_OPM-SAME: (<8 x i64>* noclone writeonly [[ARG:%.*]])
  ; IS__TUNIT_OPM-NEXT: bb:
  ; IS__TUNIT_OPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; IS__TUNIT_OPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; IS__TUNIT_OPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; IS__TUNIT_OPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; IS__TUNIT_OPM-NEXT:  call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* noclone nontempnonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noclone nontempnonnull align 64 dereferenceable(64) [[TMP]])
  ; IS__TUNIT_OPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
  ; IS__TUNIT_OPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; IS__TUNIT_OPM-NEXT:  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
  ; IS__TUNIT_NPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal256_prefer256
  ; IS__TUNIT_NPM-SAME: (<8 x i64>* noclone writeonly [[ARG:%.*]])
  ; IS__TUNIT_NPM-NEXT: bb:
  ; IS__TUNIT_NPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; IS__TUNIT_NPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; IS__TUNIT_NPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; IS__TUNIT_NPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; IS__TUNIT_NPM-NEXT:  call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* noclone nontempnonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noclone nontempnonnull nontempnonnull writeonly align 64 dereferenceable(64) [[TMP]])
  ; IS__TUNIT_NPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
  ; IS__TUNIT_NPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; IS__TUNIT_NPM-NEXT:  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
  ; IS__CGSCC_OPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal256_prefer256
  ; IS__CGSCC_OPM-SAME: (<8 x i64>* noclone writeonly [[ARG:%.*]])
  ; IS__CGSCC_OPM-NEXT: bb:
  ; IS__CGSCC_OPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; IS__CGSCC_OPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; IS__CGSCC_OPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; IS__CGSCC_OPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT:  call fastcc void  
@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_OPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT:  ret void
;
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256( <8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT: bb:
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_NPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT:  ret void
;
; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #3 {
;
; NOT_TUNIT_NPM-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256( <8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; NOT_TUNIT_NPM-NEXT: bb:
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}
define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}
bb:  
%tmp = alloca <8 x i64>, align 32  
%tmp2 = alloca <8 x i64>, align 32  
%tmp3 = bitcast <8 x i64>* %tmp to i8*  
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)  
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %arg)  
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32  
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2  
ret void

}; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #4 {
    ;
    ; NOT_TUNIT_NPM-LABEL: define
    ( {{[@]+}}) @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
    ; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64)
    [[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
    ; NOT_TUNIT_NPM-NEXT: bb:
    ; NOT_TUNIT_NPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
    ; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
    ; NOT_TUNIT_NPM-NEXT: ret void
    ;
    ; IS__TUNIT_NPM-LABEL: define {{[^@]+}} @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
    ; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64)
    [[ARG:%.*]], <8 x i64> [[TMP0:%.*]])
    ; IS__TUNIT_NPM-NEXT: bb:
    ; IS__TUNIT_NPM-NEXT:  [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
    ; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
    ; IS__TUNIT_NPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
    ; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
    ; IS__TUNIT_NPM-NEXT: ret void
    ; bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
    ;
    ; IS__TUNIT_OPM-LABEL: define {{[^@]+}} @avx2_legal512_prefer256_call_avx2_legal256_prefer256
    ; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
    ; IS__TUNIT_OPM-NEXT: bb:
    ; IS__TUNIT_OPM-NEXT:  [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
    ; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
    ; IS__TUNIT_OPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
    ; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
    ; IS__TUNIT_OPM-NEXT: ret void
    ; bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
    ;
    ; IS__TUNIT_NPM-LABEL: define {{[^@]+}} @avx2_legal512_prefer256_call_avx2_legal256_prefer256
    ; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
    ; IS__TUNIT_NPM-NEXT: bb:
    ; IS__TUNIT_NPM-NEXT:  [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
    ; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
    ; IS__TUNIT_NPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
    ; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
    ; IS__TUNIT_NPM-NEXT: ret void
    ; bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}
bb:
%tmp = alloca <8 x i64>, align 32

@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP]], <8 x i64> [[TMP0]])

bb:
%tmp = alloca <8 x i64>, align 32

@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP]], <8 x i64> [[TMP0]])

bb:
%tmp = alloca <8 x i64>, align 32

@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP]], <8 x i64> [[TMP0]])
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }

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; RUN: llc -O3 -mtriple=powerpc-unknown-linux-gnu -mcpu=e500 -mattr=spe < %s | FileCheck %s

; PowerPC SPE is a rare in-tree target that has the FP_TO_SINT node marked
; as Legal.

; Verify that fptosi(42.1) isn't simplified when the rounding mode is
; unknown.
; Verify that no gross errors happen.
; CHECK-LABEL: @f20
; COMMON: cfdecsiz
define i32 @f20(double %a) strictfp {
entry:
%result = call i32 @llvm.experimental.constrained.fptosi.i32.f64(double 42.1,
metadata !"fpexcept.strict")
strictfp
ret i32 %result
}

@llvm.fp.env = thread_local global i8 zeroinitializer, section "llvm.metadata"
declare i32 @llvm.experimental.constrained.fptosi.i32.f64(double, metadata)

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==============================================================================
; NOTE: Assertions have been autogenerated by utils/update_analyze_test_checks.py
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx2 | FileCheck %s --check-prefixes=CHECK,VEC256,AVX
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC256,AVX512VL256
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,-prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC512,AVX512VL512
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC512,AVX512VL512
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,-prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC512,SKX512

Open Source Used In CLI Analyzer 3.6.8 872
define void @zext256() "min-legal-vector-width"="256" {
; VEC256-LABEL: 'zext256'
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'zext256'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'zext256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = zext <8 x i16> undef to <8 x i64>
%B = zext <8 x i32> undef to <8 x i64>
%C = zext <16 x i8> undef to <16 x i32>
%D = zext <16 x i16> undef to <16 x i32>
%E = zext <32 x i8> undef to <32 x i16>
ret void
}

Open Source Used In CLI Analyzer 3.6.8 873
define void @zext512() "min-legal-vector-width"="512" {
  ; AVX-LABEL: 'zext512'
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

  ; AVX512VL256-LABEL: 'zext512'
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <16 x i32>
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <32 x i16>
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

  ; AVX512VL512-LABEL: 'zext512'
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <16 x i32>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <32 x i16>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

  ; SKX256-LABEL: 'zext512'
  ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
  ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
  ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
  ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
  ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
  ; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
define void @sext256() "min-legal-vector-width"="256" {
    ; AVX512VL512-LABEL: 'sext256'
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <16 x i8> undef to <16 x i32>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i16> undef to <16 x i32>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <32 x i8> undef to <32 x i16>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    ;
    %A = sext <8 x i16> undef to <8 x i64>
    %B = sext <8 x i32> undef to <8 x i64>
    %C = sext <16 x i32> undef to <16 x i32>
    %D = sext <16 x i16> undef to <16 x i32>
    %E = sext <32 x i8> undef to <32 x i16>
    ret void
}

define void @sext256() "min-legal-vector-width"="256" {
    ; VEC256-LABEL: 'sext256'
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = sext <16 x i8> undef to <16 x i32>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    ;
    %A = sext <8 x i16> undef to <8 x i64>
    %B = sext <8 x i32> undef to <8 x i64>
    %C = sext <16 x i32> undef to <16 x i32>
    %D = sext <16 x i16> undef to <16 x i32>
    %E = sext <32 x i8> undef to <32 x i16>
    ret void
}
define void @sext512() "min-legal-vector-width"="512" {
  ; AVX-LABEL: 'sext512'
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
  ret void
}

define void @sext512() "min-legal-vector-width"="512" {
  ; AVX-LABEL: 'sext512'
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
  ret void
}

define void @sext512() "min-legal-vector-width"="512" {
  ; AVX-LABEL: 'sext512'
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
  ret void
}
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'sext512'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'sext512'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'sext512'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

define void @trunc256() "min-legal-vector-width"="256" {
    : AVX-LABEL: 'trunc256'
    : AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
    : AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
    : AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
    : AVX-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
    : AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
    : AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
    : AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    :
    : AVX512VL256-LABEL: 'trunc256'
    : AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
    : AVX512VL256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
    : AVX512VL256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
    : AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
    : AVX512VL256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
    : AVX512VL256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
    : AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    :
    : AVX512VL512-LABEL: 'trunc256'
    : AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
    : AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
    : AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
    : AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
    : AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
    : AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
    : AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
define i32 @zext256_vXi1() "min-legal-vector-width"="256" {
    ; AVX-LABEL: 'zext256_vXi1'
    ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; AVX512VL256-LABEL: 'zext256_vXi1'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 12 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V4i8 = zext <4 x i1> undef to <8 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 12 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 25 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; AVX512VL512-LABEL: ‘zext256_vXi1’
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
AVX512VL512-NEXT: Cost Model: Found an estimated cost of 19 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
SKX256-LABEL: 'zext256_vXi1'
SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>

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; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; SKX512-LABEL: 'zext256_vXi1'
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; %V2i64 = zext <2 x i1> undef to <2 x i64>
%V4i64 = zext <4 x i1> undef to <4 x i64>
%V8i64 = zext <8 x i1> undef to <8 x i64>

%V2i32 = zext <2 x i1> undef to <2 x i32>
%V4i32 = zext <4 x i1> undef to <4 x i32>
%V8i32 = zext <8 x i1> undef to <8 x i32>
%V16i32 = zext <16 x i1> undef to <16 x i32>

%V2i16 = zext <2 x i1> undef to <2 x i16>
%V4i16 = zext <4 x i1> undef to <4 x i16>
%V8i16 = zext <8 x i1> undef to <8 x i16>
%V16i16 = zext <16 x i1> undef to <16 x i16>
%V32i16 = zext <32 x i1> undef to <32 x i16>

%V2i8 = zext <2 x i1> undef to <2 x i8>
%V4i8 = zext <4 x i1> undef to <4 x i8>
%V8i8 = zext <8 x i1> undef to <8 x i8>
%V16i8 = zext <16 x i1> undef to <16 x i8>
%V32i8 = zext <32 x i1> undef to <32 x i8>
%V64i8 = zext <64 x i1> undef to <64 x i8>

ret i32 undef
}

define i32 @sext256_vXi1() "min-legal-vector-width"="256" {
  ; AVX-LABEL: 'sext256_vXi1'
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
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AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

AVX512VL256-LABEL: 'sext256_vXi1'
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i64 = sext <16 x i1> undef to <16 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i64 = sext <32 x i1> undef to <32 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V64i64 = sext <64 x i1> undef to <64 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V128i64 = sext <128 x i1> undef to <128 x i64>

AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i64 = sext <16 x i1> undef to <16 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i64 = sext <32 x i1> undef to <32 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V64i64 = sext <64 x i1> undef to <64 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V128i64 = sext <128 x i1> undef to <128 x i64>

AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i32 = sext <32 x i1> undef to <32 x i32>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V64i32 = sext <64 x i1> undef to <64 x i32>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V128i32 = sext <128 x i1> undef to <128 x i32>

AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i16 = sext <64 x i1> undef to <64 x i16>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V128i16 = sext <128 x i1> undef to <128 x i16>

AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V128i8 = sext <128 x i1> undef to <128 x i8>
Open Source Used In CLI Analyzer 3.6.8; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 21 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 42 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
; AVX512VL512-LABEL: 'sext256_vXi1'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 15 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
; SKX256-LABEL: 'sext256_vXi1'
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX512-LABEL: 'sext256_vXi1'
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; SKX512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
%V16i32 = sext <16 x i1> undef to <16 x i32>

%I16 = sext i1 undef to i16
%V2i16 = sext <2 x i1> undef to <2 x i16>
%V4i16 = sext <4 x i1> undef to <4 x i16>
%V8i16 = sext <8 x i1> undef to <8 x i16>
%V16i16 = sext <16 x i1> undef to <16 x i16>
%V32i16 = sext <32 x i1> undef to <32 x i16>

%I8 = sext i1 undef to i8
%V2i8 = sext <2 x i1> undef to <2 x i8>
%V4i8 = sext <4 x i1> undef to <4 x i8>
%V8i8 = sext <8 x i1> undef to <8 x i8>
%V16i8 = sext <16 x i1> undef to <16 x i8>
%V32i8 = sext <32 x i1> undef to <32 x i8>
%V64i8 = sext <64 x i1> undef to <64 x i8>

ret i32 undef
}

define i32 @trunc_vXi1() "min-legal-vector-width"="256" {
  ; AVX-LABEL: 'trunc_vXi1'
  ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 46 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 22 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: \%V4i16 = trunc <4 x i16> undef to <4 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: \%V8i16 = trunc <8 x i16> undef to <8 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: \%V16i16 = trunc <16 x i16> undef to <16 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: \%V32i16 = trunc <32 x i16> undef to <32 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 18 for instruction: \%V64i16 = trunc <64 x i16> undef to <64 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: \%V2i8 = trunc <2 x i8> undef to <2 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: \%V4i8 = trunc <4 x i8> undef to <4 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: \%V8i8 = trunc <8 x i8> undef to <8 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: \%V16i8 = trunc <16 x i8> undef to <16 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: \%V32i8 = trunc <32 x i8> undef to <32 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: \%V64i8 = trunc <64 x i8> undef to <64 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: \%V2i64 = trunc <2 x i64> undef to <2 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: \%V4i64 = trunc <4 x i64> undef to <4 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: \%V8i64 = trunc <8 x i64> undef to <8 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: \%V16i64 = trunc <16 x i64> undef to <16 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 22 for instruction: \%V32i64 = trunc <32 x i64> undef to <32 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 44 for instruction: \%V64i64 = trunc <64 x i64> undef to <64 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: \%V2i32 = trunc <2 x i32> undef to <2 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: \%V4i32 = trunc <4 x i32> undef to <4 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: \%V8i32 = trunc <8 x i32> undef to <8 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: \%V16i32 = trunc <16 x i32> undef to <16 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 10 for instruction: \%V32i32 = trunc <32 x i32> undef to <32 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 20 for instruction: \%V64i32 = trunc <64 x i32> undef to <64 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: \%V2i16 = trunc <2 x i16> undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 32 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 17 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
; AVX512VL512-LABEL: 'trunc_vXi1'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 44 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V64i32 = trunc <64 x i32>
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; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 14 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 15 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; SKX256-LABEL: 'trunc_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 47 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
%V4i64 = trunc <4 x i64> undef to <4 x i1>
%V8i64 = trunc <8 x i64> undef to <8 x i1>
%V16i64 = trunc <16 x i64> undef to <16 x i1>
%V32i64 = trunc <32 x i64> undef to <32 x i1>
%V64i64 = trunc <64 x i64> undef to <64 x i1>
%V2i32 = trunc <2 x i32> undef to <2 x i1>
%V4i32 = trunc <4 x i32> undef to <4 x i1>
%V8i32 = trunc <8 x i32> undef to <8 x i1>
%V16i32 = trunc <16 x i32> undef to <16 x i1>
%V32i32 = trunc <32 x i32> undef to <32 x i1>
%V64i32 = trunc <64 x i32> undef to <64 x i1>
%V2i16 = trunc <2 x i16> undef to <2 x i1>
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1.123 socket.io-client 3.1.3
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1.124 zlib 1.2.11
1.124.1 Available under license :
/* zlib.h -- interface of the 'zlib' general purpose compression library version 1.2.11, January 15th, 2017

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jloup@gzip.org  madler@alumni.caltech.edu

The data format used by the zlib library is described by RFCs (Request for Comments) 1950 to 1952 in the files http://tools.ietf.org/html/rfc1950 (zlib format), rfc1951 (deflate format) and rfc1952 (gzip format).

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1.127 tar-fs 2.1.1

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1.129 csv-parse 4.15.4

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1.130 http-signature 1.2.0

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1.131 pify 3.0.0

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1.134 serialport-parser-readline 9.0.7
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1.142 socket.io 3.1.2

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1.143 pubsub-js 1.5.8

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1.145 smart-buffer 4.1.0

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1.146 serialport-parser-ready 9.0.7

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1.147 code-point-at 1.1.0

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1.148 safer-buffer 2.1.2

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1.149 escodegen 1.14.3

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1.150 streamsearch 0.1.2

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1.155 pinkie 2.0.4

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1.158 ftp 0.3.10

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## Commands to generate dependency files
GEN_DEPS.c=$(CC) -E -MM $(DEFS) $(CPPFLAGS)
GEN_DEPS.cc=$(CXX) -E -MM $(DEFS) $(CPPFLAGS)

## Flags for position independent code
SHAREDLIBCFLAGS = -fPIC
SHAREDLIBCXXFLAGS = -fPIC
SHAREDLIBCPPFLAGS = -DPIC

## Additional flags when building libraries and with threads
THREADSCPPFLAGS = -D_REENTRANT
LIBCPPFLAGS =

## Compiler switch to embed a runtime search path
LD_RPATH=
LD_RPATH_PRE=-Wl,-rpath,

## Compiler switch to embed a library name
LD_SONAME = -Wl,-soname -Wl,$(notdir $(MIDDLE_SO_TARGET))

## Shared library options
LD_SOOPTIONS= -Wl,-Bsymbolic

## Shared object suffix
SO = so
```
## Non-shared intermediate object suffix

STATIC_O = ao

## Compilation rules

%.$(STATIC_O): $(srcdir)/%.c
$(COMPILE.c) $(STATICCPPFLAGS) $(STATICCFLAGS) -o $@ $<
%.o: $(srcdir)/%.c
$(COMPILE.c) $(DYNAMICCPPFLAGS) $(DYNAMICCFLAGS) -o $@ $<

%.$(STATIC_O): $(srcdir)/%.cpp
$(COMPILE.cc) $(STATICCPPFLAGS) $(STATICCXXFLAGS) -o $@ $<
%.o: $(srcdir)/%.cpp
$(COMPILE.cc) $(DYNAMICCPPFLAGS) $(DYNAMICCXXFLAGS) -o $@ $<

## Dependency rules

%.d: $(srcdir)/%.c
@echo "generating dependency information for $<"
@$(SHELL) -ec '$(GEN_DEPS.c) $< \
| sed \"s/([^*])\.*\o\:.*\o @\: /g\" > $@;\ 
[ -s $@ ] || rm -f $@' 

%.d: $(srcdir)/%.cpp
@echo "generating dependency information for $<"
@$(SHELL) -ec '$(GEN_DEPS.cc) $< \
| sed \"s/([^*])\.*\o\:.*\o @\: /g\" > $@;\ 
[ -s $@ ] || rm -f $@' 

## Versioned libraries rules

%.$(SO).$(SO_TARGET_VERSION_MAJOR): %.$(SO).$(SO_TARGET_VERSION)
$(RM) $@ && ln -s ${<F} $@
%.$(SO): %.$(SO).$(SO_TARGET_VERSION_MAJOR)
$(RM) $@ && ln -s ${*F}.$(SO).$(SO_TARGET_VERSION) $@

## Bind internal references

# LDflags that pkgdata will use
BIR_LDFLAGS= -Wl,-Bsymbolic

# Dependencies [i.e. map files] for the final library
BIR_DEPS=

## Remove shared library 's'
STATIC_PREFIX_WHEN_USED =
STATIC_PREFIX =

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1.175 netmask 2.0.2

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Node Netmask

======

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The Netmask class parses and understands IPv4 CIDR blocks so they can be explored. This module is highly inspired by coffeescript module [rs/node-netmask](https://github.com/rs/node-netmask) module.

Synopsis

--------

```javascript
import { Netmask } from '@hg8496/netmask'

const block = new Netmask('10.0.0.0/12');
block.baseIP;                   // 10.0.0.0
block.netmask;                  // 255.240.0.0
block.netmaskBits;              // 12
block.hostmask;                 // 0.15.255.255
block.broadcastIP;              // 10.15.255.255
block.networkSize;              // 1048576
block.firstHostIP;              // 10.0.0.1
block.lastHostIP;               // 10.15.255.254
block.contains('10.0.8.10');    // true
block.contains('10.8.0.10');    // true
block.contains('192.168.1.20'); // false

block.forEach(function(ip, long, index));
```

Constructing

-------------

Netmask objects are created with an IP address and optionally a mask. There are many forms that are recognized:

- `216.240.32.0/24` // The preferred form.
- `216.240.32.0`, `24`
- `216.240.32.0/255.255.255.0`
- `216.240.32.0`, `255.255.255.0`
'216.240.32.4'       // A /32 block.
'216.240.32'         // A /24 block.
'216.240'            // A /16 block.
'140'                // A /8 block.
'216.240.32/24'      
'216.240/16'

API
---

- `.baseIP`: The base address of the network block as a string (eg: 216.240.32.0). Base does not give an indication of the size of the network block.
- `.netmask`: The netmask as a string (eg: 255.255.255.0).
- `.hostmask`: The host mask which is the opposite of the netmask (eg: 0.0.0.255).
- `.netmaskBits`: The netmask as a number of bits in the network portion of the address for this block (eg: 24).
- `.networkSize`: The number of IP addresses in a block (eg: 256).
- `.broadcastIP`: The blocks broadcast address (eg: 192.168.1.0/24 => 192.168.1.255)
- `.firstHostIP`, `.lastHostIP`: First and last useable address
- `.contains(ip)`: Returns a true if the IP number `ip` is part of the network. That is, a true value is returned if `ip` is between `baseIP` and `broadcastIP`.
- `.forEachHost(fn)`: Similar to the Array prototype method. It loops through all the useable addresses, ie between `firstHostIP` and `lastHostIP`.
- `.iterateHosts`: Returns an IterableIterator with the same logic as `forEachHost`
- `.toString()`: The netmask in base/bitmask format (e.g., '216.240.32.0/24')

Installation
------------

$ npm install @hg8496/netmask

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1.176 serialport-parser-byte-length 9.0.7
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1.178 brotli 1.0.9

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1.185 stack-trace 0.0.10
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1.189 cors 2.8.5

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1.191 glob 7.1.6

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1.194 rc 1.2.8

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1.195 socket.io-parser 4.0.4

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1.196 moment 2.29.1

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1.198 setprototypeof 1.1.1

1.199 xmlhttprequest 1.8.0
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1.202 prelude-ls 1.1.2

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========

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1.226 async 2.6.3

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1.231 ms 2.1.2

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* /opt/cola/permits/1103324428_1604083552.87/0/socks-proxy-agent-5-0-0-1-tgz/package/README.md

1.237 pac-proxy-agent 4.1.0
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pac-proxy-agent
===============
### A [PAC file][pac-wikipedia] proxy `http.Agent` implementation for HTTP and HTTPS
[![Build Status](https://github.com/TooTallNate/node-pac-proxy-agent/workflows/Node%20CI/badge.svg)](https://github.com/TooTallNate/node-pac-proxy-agent/actions?workflow=Node+CI)

This module provides an `http.Agent` implementation that retrieves the specified [PAC proxy file][pac-wikipedia] and uses it to resolve which HTTP, HTTPS, or SOCKS proxy, or if a direct connection should be used to connect to the HTTP endpoint.

It is designed to be be used with the built-in `http` and `https` modules.
Installation
------------

Install with `npm`:

```bash
$ npm install pac-proxy-agent
```

Example
-------

```js
var url = require('url');
var http = require('http');
var PacProxyAgent = require('pac-proxy-agent');

// URI to a PAC proxy file to use (the "pac+" prefix is stripped)
var proxy = 'pac+https://cloudup.com/ceGH2yZ0Bjp+';
console.log('using PAC proxy proxy file at %j', proxy);

// HTTP endpoint for the proxy to connect to
var endpoint = 'http://nodejs.org/api/';
console.log('attempting to GET %j', endpoint);
var opts = url.parse(endpoint);

// create an instance of the `PacProxyAgent` class with the PAC file location
var agent = new PacProxyAgent(proxy);
opts.agent = agent;

http.get(opts, function (res) {
    console.log("response" event!", res.headers);
    res.pipe(process.stdout);
});
```

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[pac-wikipedia]: http://wikipedia.org/wiki/Proxy_auto-config

Found in path(s):
* /opt/cola/permits/1103324486_1604083535.38/0/pac-proxy-agent-4-1-0-tgz/package/README.md

1.238 fs-extra 9.1.0

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http-proxy-agent

============

### An HTTP(s) proxy `http.Agent` implementation for HTTP

[![Build Status](https://github.com/TooTallNate/node-http-proxy-agent/workflows/Node%20CI/badge.svg)](https://github.com/TooTallNate/node-http-proxy-agent/actions?workflow=Node+CI)

This module provides an `http.Agent` implementation that connects to a specified HTTP or HTTPS proxy server, and can be used with the built-in `http` module.

__Note:__ For HTTP proxy usage with the `https` module, check out [node-https-proxy-agent](https://github.com/TooTallNate/node-https-proxy-agent).

Installation

----------
Install with `npm`:

```bash
$ npm install http-proxy-agent
```

Example
-------

```js
var url = require('url');
var http = require('http');
var HttpProxyAgent = require('http-proxy-agent');

// HTTP/HTTPS proxy to connect to
var proxy = process.env.http_proxy || 'http://168.63.76.32:3128';
console.log('using proxy server %j', proxy);

// HTTP endpoint for the proxy to connect to
console.log('attempting to GET %j', endpoint);
var opts = url.parse(endpoint);

// create an instance of the `HttpProxyAgent` class with the proxy server information
var agent = new HttpProxyAgent(proxy);
opts.agent = agent;

http.get(opts, function (res) {
    console.log('"response" event!', res.headers);
    res.pipe(process.stdout);
});
```

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Found in path(s):

* /opt/cola/permits/1140279809_1614797817.99/0/http-proxy-agent-4-0-1-2-tgz/package/README.md

1.249 toidentifier 1.0.0

1.250 decompress-response 4.2.1

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1.259 acl 2.3.1

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get-uri
=======

### Returns a `stream.Readable` from a URI string

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This high-level module accepts a URI string and returns a `Readable` stream instance. There is built-in support for a variety of "protocols", and it's easily extensible with more:

<table>
<thead>
<tr>
<th>Protocol</th>
<th>Description</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>data</code></td>
<td>[Data URIs][data]</td>
<td><code>data:text/plain;base64,SGVsbG8sIFdvcmxkIQ%3D%3D</code></td>
</tr>
<tr>
<td><code>file</code></td>
<td>[File URIs][file]</td>
<td><code>file:///c:/windows/example.ini</code></td>
</tr>
<tr>
<td><code>http</code></td>
<td>[HTTP URIs][http]</td>
<td><code>http://www.example.com/path/to/name</code></td>
</tr>
<tr>
<td><code>https</code></td>
<td>[HTTPS URIs][https]</td>
<td><code>https://www.example.com/path/to/name</code></td>
</tr>
</tbody>
</table>

Installation
-------------

Install with `npm`:

```bash
$ npm install get-uri
```

Example
-------

To simply get a `stream.Readable` instance from a `file:` URI, try something like:

```js
var getUri = require('get-uri');

// `file:` maps to a `fs.ReadStream` instance
getUri('file:///Users/nrajlich/wat.json', function (err, rs) {
  if (err) throw err;
  rs.pipe(process.stdout);
});
```

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Missing Endpoints
-------------

When you pass in a URI in which the resource referenced does not exist on the
destination server, then a `NotFoundError` will be returned. The `code` of the
error instance is set to `"ENOTFOUND"`, so you can special-case that in your code
to detect when a bad filename is requested:

```js
getUri('http://example.com/resource.json', function (err, rs) {
    if (err) {
        if ('ENOTFOUND' == err.code) {
            // bad file path requested
        } else {
            // something else bad happened...
            throw err;
    }

    // your app code
});
```

Cacheability
------------

When calling `getUri()` with the same URI multiple times, the `get-uri` module
supports sending an indicator that the remote resource has not been modified
since the last time it has been retrieved from that node process.

To do this, pass in a `cache` option to the "options object" argument
with the value set to the `stream.Readable` instance that was previously
returned. If the remote resource has not been changed since the last call for
that same URI, then a `NotModifiedError` instance will be returned with it's
`code` property set to `"ENOTMODIFIED"`.

When the "ENOTMODIFIED" error occurs, then you can safely re-use the
results from the previous `getUri()` call for that same URI:

```js
// maps to a `fs.ReadStream` instance
getUri('http://example.com/resource.json', function (err, rs) {
    if (err) throw err;

    // some time later, if you need to get this same URI again, pass in the
    // previous `stream.Readable` instance as `cache` option to potentially
    // receive an "ENOTMODIFIED" response:
```
var opts = { cache: rs };  
getUri('http://example.com/resource.json', opts, function (err, rs2) {
    if (err) {
        if ('ENOTFOUND' == err.code) {
            // bad file path requested
        } else if ('ENOTMODIFIED' == err.code) {
            // source file has not been modified since last time it was requested,
            // so `rs2` is undefined and you are expected to re-use results from
            // a previous call to `getUri()`
        } else {
            // something else bad happened...
            throw err;
        }
    }
};

API
---

### getUri(String uri[, Object options,] Function callback)

A `uri` String is required. An optional `options` object may be passed in:

- `cache` - A `stream.Readable` instance from a previous call to `getUri()` with the same URI. If this option is passed in, and the destination endpoint has not been modified, then an `ENOTMODIFIED` error is returned

Any other options passed in to the `options` object will be passed through to the low-level connection creation functions (`http.get()`, `ftp.connect()`, etc).

Invokes the given `callback` function with a `stream.Readable` instance to read the resource at the given `uri`.

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[ftp]: http://www.w3.org/Protocols/rfc959/
[http]: http://www.w3.org/Protocols/rfc2616/rfc2616.html
[https]: http://wikipedia.org/wiki/HTTP_Secure

Found in path(s):
* /opt/cola/permits/1103324573_1604083609.2/0/get-uri-3-0-2-tgz/package/README.md

1.270 console-control-strings 1.1.0

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1.272 angular-bootstrap 1.1.2

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 * http://angular-ui.github.io/bootstrap/
 *
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 */

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* /opt/ws_local/PERMITS_SQL/1068891154_1594751522.06/0/bootstrap-bower-189241b8981b48a353ebc8161a597f1c44e712d12569c69c68bzip/bootstrap-bower-189241b8981b48a353ebc8161a597f1c44e712d12569c69c68bui-bootstrap-tpls.js
* /opt/ws_local/PERMITS_SQL/1068891154_1594751522.06/0/bootstrap-bower-189241b8981b48a353ebc8161a597f1c44e712d12569c69c68bui-bootstrap-tpls.min.js
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1.277 array-union 1.0.2

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1.278 levn 0.3.0

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1.279 xml2js 0.4.23

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1.280 prebuild-install 6.1.2

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1.282 json-schema-traverse 0.4.1
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1.283 ng-grid 2.0.14

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1.284 debug 4.3.1

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1.285 ecc-jsbn 0.1.2
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1.286 ng-idle 1.0.4

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1.287 requirejs-text 2.0.16

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1.288 detect-libc 1.0.3

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1.289 protobuf 3.13.0.1

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1.290 engine.io 4.1.1
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1.292 caseless 0.12.0

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1.293 are-we-there-yet 1.1.5

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1.294 jquery 3.4.1

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Written by: Philip Hazel
Email local part: ph10
Email domain: cam.ac.uk

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1.302 angular-ui-select 0.0.5
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- Layout tests, located in test/mjsunit/third_party/object-keys. These are based on layout tests from webkit.org which are copyrighted by Apple Computer, Inc. and released under a 3-clause BSD license.

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-------------------------------

Written by: Philip Hazel
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Email domain: cam.ac.uk
University of Cambridge Computing Service,

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Python was created in the early 1990s by Guido van Rossum at Stichting Mathematisch Centrum (CWI, see http://www.cwi.nl) in the Netherlands as a successor of a language called ABC. Guido remains Python’s principal author, although it includes many contributions from others.

In 1995, Guido continued his work on Python at the Corporation for National Research Initiatives (CNRI, see http://www.cnri.reston.va.us) in Reston, Virginia where he released several versions of the software.

In May 2000, Guido and the Python core development team moved to BeOpen.com to form the BeOpen PythonLabs team. In October of the same year, the PythonLabs team moved to Digital Creations, which became Zope Corporation. In 2001, the Python Software Foundation (PSF, see https://www.python.org/psf/) was formed, a non-profit organization created specifically to own Python-related Intellectual Property. Zope Corporation was a sponsoring member of the PSF.

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1.315 skia 90

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C++ Big Integer Library
(see ChangeLog for version)

http://mattmccutchen.net/bigint/

Written and maintained by Matt McCutchen <matt@mattmccutchen.net>

You can use this library in a C++ program to do arithmetic on integers of size limited only by your computer's memory. The library provides BigUnsigned and BigInteger classes that represent nonnegative integers and signed integers, respectively. Most of the C++ arithmetic operators are overloaded for these classes, so big-integer calculations are as easy as:

```
#include "BigIntegerLibrary.hh"

BigInteger a = 65536;
cout << (a * a * a * a * a * a * a * a);
```

(prints 340282366920938463463374607431768211456)

The code in `sample.cc' demonstrates the most important features of the library. To get started quickly, read the code and explanations in that file and run it. If you want more detail or a feature not shown in `sample.cc', consult the consult the actual header and source files, which are thoroughly commented.

This library emphasizes ease of use and clarity of implementation over speed; some users will prefer GMP (http://swox.com/gmp/), which is faster. The code is intended to be reasonably portable across computers and modern C++ compilers; in particular, it uses whatever word size the computer provides (32-bit, 64-bit, or otherwise).

Compiling programs that use the library
---------------------------------------
The library consists of a folder full of C++ header files (`.hh') and source files (`.cc'). Your own programs should `#include' the necessary header files and link with the source files. A makefile that builds the sample program (`sample.cc') is included; you can adapt it to replace the sample with your own program.

Alternatively, you can use your own build system or IDE. In that case, you must put the library header files where the compiler will find them and arrange to have your program linked with the library source files; otherwise, you will get errors about missing header files or "undefined references". To learn how to do
this, consult the documentation for the build system or IDE; don't bother asking me. Adding all the library files to your project will work in many IDEs but may not be the most desirable approach.

Resources
---------
The library's Web site (above) provides links to released versions, the current development version, and a mailing list for release announcements, questions, bug reports, and other discussion of the library. I would be delighted to hear from you if you like this library and/or find a good use for it.

Bugs and enhancements
---------------------
The library has been tested by me and others but is by no means bug-free. If you find a bug, please report it, whether it comes in the form of compiling trouble, a mathematically inaccurate result, or a memory-management bloop (since I use Java, these are altogether too common in my C++). I generally fix all reported bugs. You are also welcome to request enhancements, but I am unlikely to do substantial amounts of work on enhancements at this point.

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1.325 degenerator 2.2.0

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degenerator

============

### Compiles sync functions into async functions

[![Build Status](https://github.com/TooTallNate/node-degenerator/workflows/Node%20CI/badge.svg)](https://github.com/TooTallNate/node-degenerator/actions?workflow=Node+CI)

Sometimes you need to write sync looking code that's really async under the hood. This module takes a String to one or more synchronous JavaScript functions, and returns a new String that with those JS functions transpiled into `async` functions.
So this:

```js
function foo() {
  return a('bar') || b();
}
```

Gets compiled into:

```js
async function foo() {
  return await a('bar') || await b();
}
```

With the compiled output code, you can evaluate the code using the `vm` module in Node.js, or save the code to a file and require it, or whatever.

Installation
-------------

Install with `npm`:

```bash
$ npm install degenerator
```

Example
-------

You must explicitly specify the names of the functions that should be "asyncified". So say we wanted to expose a `get(url)` function that did an HTTP request and returned the response body.

The user has provided us with this implementation:

```js
function myFn() {
  const one = get('https://google.com');
  const two = get('http://nodejs.org');
  const three = JSON.parse(get('http://jsonip.org'));
  return [one, two, three];
}
```
Now we can compile this into an asynchronous function, implement the async `get()` function, and finally evaluate it into a real JavaScript function instance with the `vm` module:

```typescript
import vm from 'vm';
import degenerator from 'degenerator';

// The `get()` function is Promise-based (error handling omitted for brevity)
function get(endpoint: string) {
  return new Promise((resolve, reject) => {
    var mod = 0 == endpoint.indexOf('https:') ? require('https') : require('http');
    var req = mod.get(endpoint);
    req.on('response', function (res) {
      var data = '';
      res.setEncoding('utf8');
      res.on('data', function (b) { data += b; });
      res.on('end', function () {
        resolve(data);
      });
    });
  });
}

// Convert the JavaScript string provided from the user (assumed to be `str` var)
str = degenerator(str, ['get']);

// Turn the JS String into a real async function instance
const asyncFn = vm.runInNewContext(`(${str})`, { get });

// Now we can invoke the function asynchronously
asyncFn().then((res) => {
  // Do something with `res`...
  ...
});

---

### degenerator(code: string, names: Array<string|RegExp>, options?: DegeneratorOptions): String

Returns a "degeneratorified" JavaScript string, with `async`/`await` transplanted.

#### DegeneratorOptions

An options object _may_ be passed in as the third parameter, with the following
values:

* `output` - string - May be `'async'` or `'generator'`, defaults to `'async'`.

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Found in path(s):
* /opt/cola/permits/1103324621_1604083557.66/0/degenerator-2-2-0-tgz/package/README.md

1.326 Iru-cache 5.1.1

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1.327 mime-types 2.1.30

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1.328 angular-datatables 0.5.6

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* /opt/ws_local/PERMITS_SQL/1068891073_1594751600.84/0/bootstrap-bower-189241b8981b48a353ebc8161a597ffcc144e712d-zip/bootstrap-bower-189241b8981b48a353ebc8161a597ffcc144e712d/ui-bootstrap.min.js
* /opt/ws_local/PERMITS_SQL/1068891073_1594751600.84/0/bootstrap-bower-189241b8981b48a353ebc8161a597ffcc144e712d-zip/bootstrap-bower-189241b8981b48a353ebc8161a597ffcc144e712d/ui-bootstrap-tpls.min.js
* /opt/ws_local/PERMITS_SQL/1068891073_1594751600.84/0/bootstrap-bower-189241b8981b48a353ebc8161a597ffcc144e712d-zip/bootstrap-bower-189241b8981b48a353ebc8161a597ffcc144e712d/ui-bootstrap-tpls.js
* /opt/ws_local/PERMITS_SQL/1068891073_1594751600.84/0/bootstrap-bower-189241b8981b48a353ebc8161a597ffcc144e712d-zip/bootstrap-bower-189241b8981b48a353ebc8161a597ffcc144e712d/ui-bootstrap-tpls.js

1.349 yallist 3.1.1
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1.350 end-of-stream 1.4.4

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1.351 blink 90.0.4430.93
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