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; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature --scrub-attributes
; RUN: opt -attributor -attributor-manifest-internal -attributor-max-iterations=verify -attributor-annotate-decl-cs -attributor-max-iterations=4 -S %s | FileCheck %s --check-prefixes=CHECK,NOT_CGSCC_NPM,NOT_CGSCC_OPM,NOT_TUNIT_NPM,IS__TUNIT__,IS______OPM,IS__TUNIT_OPM
; RUN: opt -aa-pipeline=basic-aa -passes=attributor -attributor-manifest-internal -attributor-max-iterations=verify -attributor-annotate-decl-cs -attributor-max-iterations=3 -S %s | FileCheck %s --check-prefixes=CHECK,NOT_CGSCC_OPM,NOT_CGSCC_NPM,NOT_TUNIT_OPM,IS__TUNIT__,IS______NPM,IS__TUNIT_NPM
; RUN: opt -attributor-cgscc -attributor-manifest-internal -attributor-annotate-decl-cs -S %s | FileCheck %s --check-prefixes=CHECK,NOT_TUNIT_NPM,NOT_TUNIT_OPM,NOT_CGSCC_NPM,IS__CGSCC____,IS______OPM,IS__CGSCC_OPM
; RUN: opt -aa-pipeline=basic-aa -passes=attributor-cgsc -attributor-manifest-internal -attributor-annotate-decl-cs -S < %s | FileCheck %s --check-prefixes=CHECK,NOT_TUNIT_NPM,NOT_TUNIT_OPM,NOT_CGSCC_OPM,IS__CGSCC____,IS________NPM,IS__CGSCC_NPM
; Test that we only promote arguments when the caller/callee have compatible function attributes.

target triple = "x86_64-unknown-linux-gnu"

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT: call fastcc void
@calleee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly
align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @calleee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should promote
define internal fastcc void @calleee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
;
; NOT_TUNIT_NPM-LABEL: define
{([^@]+)}@calleee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; NOT_TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* noalias nocapture nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; NOT_TUNIT_NPM-NEXT: bb:
; NOT_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: ret void
;
; IS__TUNIT_NPM-LABEL: define
{([^@]+)}@calleee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64> [[TMP0:%.*]])
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32 %arg) #1 {
  ; IS__TUNIT_OPM-LABEL: define {{[^@]+}} %0 @avx512_legal512_prefer256_call_avx512_legal512_prefer256
  ; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
  ; IS__TUNIT_OPM-NEXT: bb:
    ; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloc <8 x i64>, align 32
    ; IS__TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloc <8 x i64>, align 32
    ; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; IS__TUNIT_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32 %arg)
  ; IS__TUNIT_NPM-LABEL: define {{[^@]+}} %0 @avx512_legal512_prefer256_call_avx512_legal512_prefer256
  ; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
  ; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 i64>, <8 x i64>* [[TMP]], align 64
  ; IS__TUNIT_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32 %arg)
  ; IS__CGSCC_OPM-LABEL: define {{[^@]+}} %0 @avx512_legal512_prefer256_call_avx512_legal512_prefer256
  ; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
  ; IS__CGSCC_OPM-NEXT: bb:
    ; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloc <8 x i64>, align 32
    ; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloc <8 x i64>, align 32
    ; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; IS__CGSCC_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32 %arg)
dereferenceable(64) [[TMP]])

; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void

; IS__CGSCC_NPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT: bb:

; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly
align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {

; NOT_TUNIT_NPM-LABEL: define
([[@]+]) @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; NOT_TUNIT_NPM-NEXT: bb:
; NOT_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: ret void

; IS/__TUNIT_NPM-LABEL: define
([[@]+]) @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG1%.%]], <8 x i64>* [[TMP0%.%]])
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[ARG1_PRIV%.%]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: [[TMP%.%]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT: ret void

; bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
; IS__TUNIT_OPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG%.%]])
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP%.%]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP2%.%]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP3%.%]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__TUNIT_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__TUNIT_OPM-NEXT: [[TMP4%.%]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void

; IS__TUNIT_NPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture writeonly [[ARG%.%]])
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP%.%]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2%.%]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3%.%]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__TUNIT_NPM-NEXT: [[TMP0%.%]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP0]], <8 x i64>* [[TMP0]])
; IS__TUNIT_NPM-NEXT: [[TMP4%.%]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
; IS__CGSCC_OPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_OPM-NEXT: bb:
  ; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; IS__CGSCC_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void

; IS__CGSCC_NPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT: bb:
  ; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; IS__CGSCC_NPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void

bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
    bb:
      %tmp = load <8 x i64>, <8 x i64>* %arg
      store <8 x i64> %tmp, <8 x i64>* %arg
      ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
    bb:
      %tmp = load <8 x i64>, <8 x i64>* %arg
      store <8 x i64> %tmp, <8 x i64>* %arg
      ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
    bb:
      %tmp = load <8 x i64>, <8 x i64>* %arg
      store <8 x i64> %tmp, <8 x i64>* %arg
      ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
    bb:
      %tmp = load <8 x i64>, <8 x i64>* %arg
      store <8 x i64> %tmp, <8 x i64>* %arg
      ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
    bb:
      %tmp = load <8 x i64>, <8 x i64>* %arg
      store <8 x i64> %tmp, <8 x i64>* %arg
      ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
    bb:
      %tmp = load <8 x i64>, <8 x i64>* %arg
      store <8 x i64> %tmp, <8 x i64>* %arg
      ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
    bb:
      %tmp = load <8 x i64>, <8 x i64>* %arg
      store <8 x i64> %tmp, <8 x i64>* %arg
      ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
    bb:
      %tmp = load <8 x i64>, <8 x i64>* %arg
      store <8 x i64> %tmp, <8 x i64>* %arg
      ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
    bb:
      %tmp = load <8 x i64>, <8 x i64>* %arg
      store <8 x i64> %tmp, <8 x i64>* %arg
      ret void
}
; IS__TUNIT_NPM-NEXT: [[TMP;%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2;%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3;%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nullwriteonly align 32
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__TUNIT_NPM-NEXT: [[TMP0;%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]])
; IS__TUNIT_NPM-NEXT: [[TMP4;%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void

; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocaption nullwriteonly align 2 dereferenceable(64) [[ARG;%.*]])
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP;%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2;%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3;%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nullwriteonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nullwriteonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_OPM-NEXT: [[TMP4;%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void

; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocaption nullwriteonly align 2 dereferenceable(64) [[ARG;%.*]])
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP;%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2;%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3;%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nullwriteonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nullwriteonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_NPM-NEXT: [[TMP4;%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {

;
; NOT_TUNIT_NPM-LABEL: define
{ {{[^@]+}} } @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; NOT_TUNIT_NPM-NEXT: bb:
; NOT_TUNIT_NPM-NEXT:   [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: ret void
;
; IS__TUNIT_NPM-LABEL: define
{ {{[^@]+}} } @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* noalias nocapture nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT:   [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}
define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {

;
; IS__TUNIT_OPM-LABEL: define { {{[^@]+}} } @avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT:   [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:   [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:   [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT:   call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__TUNIT_OPM-NEXT:   call fastcc void
@callee_avx512_legal256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__UNIT_OPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__UNIT_OPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__UNIT_OPM-NEXT:    ret void

; IS__UNIT_NPM-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture writeonly [[ARG:%.*]])
; IS__UNIT_NPM-NEXT:    bb:
; IS__UNIT_NPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__UNIT_NPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__UNIT_NPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__UNIT_NPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__UNIT_NPM-NEXT:    call fastcc void

@callee_avx512_legal256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__UNIT_NPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__UNIT_NPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__UNIT_NPM-NEXT:    ret void

; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_OPM-NEXT:    bb:
; IS__CGSCC_OPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT:    call fastcc void

@callee_avx512_legal256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_OPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT:    ret void

; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT:    bb:
; IS__CGSCC_NPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT:    call fastcc void
define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {

    ; This should not promote
    define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 {

        ; NOT_TUNIT_NPM-LABEL: define
        {{[^@]+}} @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256

        ; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
        ; NOT_TUNIT_NPM-NEXT: bb:

        ; NOT_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
        ; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
        ; NOT_TUNIT_NPM-NEXT: ret void

        ; IS__TUNIT_NPM-LABEL: define
        {{[^@]+}} @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256

        ; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
        ; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
        ; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
        ; IS__CGSCC_NPM-NEXT: ret void

        bb:

        %tmp = alloca <8 x i64>, align 32
    
    %tmp2 = alloca <8 x i64>, align 32
    
    %tmp3 = bitcast <8 x i64>* %tmp to i8*

    call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)

    call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)

    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32

    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2

    ret void

    }
; IS__TUNIT_OPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT:  [[TMP:.%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:  [[TMP2:.%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:  [[TMP3:.%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__TUNIT_OPM-NEXT:  call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nfree nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nfree nnull readonly align 64
dereferenceable(64) [[TMP]])
; IS__TUNIT_OPM-NEXT:  [[TMP4:.%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT:  ret void
;
; IS__TUNIT_NPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT:  [[TMP:.%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT:  [[TMP2:.%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT:  [[TMP3:.%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__TUNIT_NPM-NEXT:  call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nfree
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nfree nnull readonly
align 64 dereferenceable(64) [[TMP]])
; IS__TUNIT_NPM-NEXT:  [[TMP4:.%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT:  ret void
;
; IS__CGSCC_OPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT:  [[TMP:.%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:  [[TMP2:.%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:  [[TMP3:.%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT:  call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nfree nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nfree nnull readonly align 64
dereferenceable(64) [[TMP]])
; IS__CGSCC_OPM-NEXT:  [[TMP4:.%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT:  ret void
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; IS__CGSCC_NPM-LABEL: define ( {{[^@]+}} ) @avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS__CGSCC_NPM-SAME: ( <8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [ [ARG:%.*]] )
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP2]] to i8*
; IS__CGSCC_NPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [ [TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT:  call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256( <8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [ [TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [ [TMP3]] )
; IS__CGSCC_NPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [ [ARG] ], align 2
; IS__CGSCC_NPM-NEXT:  ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256( <8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256( <8 x i64>* %arg, <8 x i64>* readonly %arg1) #3 {

; NOT_TUNIT_NPM-LABEL: define
{ {{[^@]+}} } @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; NOT_TUNIT_NPM-SAME: ( <8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [ [ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [ [ARG1:%.*]] )
; NOT_TUNIT_NPM-NEXT: bb:
; NOT_TUNIT_NPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [ [ARG1] ], align 64
; NOT_TUNIT_NPM-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [ [ARG] ], align 64
; NOT_TUNIT_NPM-NEXT:  ret void

; IS__TUNIT_NPM-LABEL: define
{ {{[^@]+}} } @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS__TUNIT_NPM-SAME: ( <8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [ [ARG:%.*]], <8 x i64> [ [TMP0] ] )
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT:  [ [ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT:  store <8 x i64> [ [TMP0] ], <8 x i64>* [ [ARG1_PRIV] ], align 64
define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
    ;
    ; IS__TUNIT_OPM-LABEL: define {[^@]+} @avx2_legal256_prefer256_call_avx2_legal512_prefer256
    ; IS__TUNIT_OPM-SAME: ( <8 x i64>* nocapture writeonly [[ARG:%.*]])
    ; IS__TUNIT_OPM-NEXT: bb:
    ; IS__TUNIT_OPM-NEXT:   [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; IS__TUNIT_OPM-NEXT:   [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; IS__TUNIT_OPM-NEXT:   [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; IS__TUNIT_OPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
    ; IS__TUNIT_OPM-NEXT:    call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* noalias nocapture nonnull readonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nonnull readonly align 64 dereferenceable(64) [[TMP]])
    ; IS__TUNIT_OPM-NEXT:   [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
    ; IS__TUNIT_OPM-NEXT:   store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
    ; IS__TUNIT_OPM-NEXT:   ret void
    ;
    ; IS__TUNIT_NPM-LABEL: define {[^@]+} @avx2_legal256_prefer256_call_avx2_legal512_prefer256
    ; IS__TUNIT_NPM-SAME: ( <8 x i64>* nocapture writeonly [[ARG:%.*]])
    ; IS__TUNIT_NPM-NEXT: bb:
    ; IS__TUNIT_NPM-NEXT:   [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; IS__TUNIT_NPM-NEXT:   [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; IS__TUNIT_NPM-NEXT:   [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; IS__TUNIT_NPM-NEXT:    [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
    ; IS__TUNIT_NPM-NEXT:    call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* noalias nocapture nonnull readonly align 64 dereferenceable(64) [[TMP0]], <8 x i64>* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP0]])
    ; IS__TUNIT_NPM-NEXT:   [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
    ; IS__TUNIT_NPM-NEXT:   store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
    ; IS__TUNIT_NPM-NEXT:   ret void
    ;
    ; IS__CGSCC_OPM-LABEL: define {[^@]+} @avx2_legal256_prefer256_call_avx2_legal512_prefer256
    ; IS__CGSCC_OPM-SAME: ( <8 x i64>* nocapture writeonly [[ARG:%.*]])
    ; IS__CGSCC_OPM-NEXT: bb:
    ; IS__CGSCC_OPM-NEXT:   [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; IS__CGSCC_OPM-NEXT:   [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; IS__CGSCC_OPM-NEXT:   [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; IS__CGSCC_OPM-NEXT:    [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
    ; IS__CGSCC_OPM-NEXT:    call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* noalias nocapture nonnull nonnull align 64 dereferenceable(64) [[TMP0]], <8 x i64>* nocapture nonnull readonly align 64 dereferenceable(64) [[TMP0]])
    ; IS__CGSCC_OPM-NEXT:   [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
    ; IS__CGSCC_OPM-NEXT:   store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
    ; IS__CGSCC_OPM-NEXT:   ret void
    ;
    ; IS__CGSCC_NPM-LABEL: define {[^@]+} @avx2_legal256_prefer256_call_avx2_legal512_prefer256
    ; IS__CGSCC_NPM-SAME: ( <8 x i64>* nocapture writeonly [[ARG:%.*]])
    ; IS__CGSCC_NPM-NEXT: bb:
    ; IS__CGSCC_NPM-NEXT:   [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; IS__CGSCC_NPM-NEXT:   [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; IS__CGSCC_NPM-NEXT:   [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; IS__CGSCC_NPM-NEXT:    [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
    ; IS__CGSCC_NPM-NEXT:    call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* noalias nocapture nonnull readonly align 64 dereferenceable(64) [[ARG]], align 2
    ; IS__CGSCC_NPM-NEXT:   ret void
    ;
    ; IS__CGSCC_OPM-LABEL: define {[^@]+} @avx2_legal256_prefer256_call_avx2_legal512_prefer256
    ; IS__CGSCC_OPM-SAME: ( <8 x i64>* nocapture writeonly [[ARG:%.*]])
    ; IS__CGSCC_OPM-NEXT: bb:
    ; IS__CGSCC_OPM-NEXT:   [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; IS__CGSCC_OPM-NEXT:   [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; IS__CGSCC_OPM-NEXT:   [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; IS__CGSCC_OPM-NEXT:    [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
    ; IS__CGSCC_OPM-NEXT:    call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* noalias nocapture nonnull align 64 dereferenceable(64) [[ARG]], align 2
    ; IS__CGSCC_OPM-NEXT:   ret void
    ;
; IS__CGSCC_OPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP2]] to i8*
; IS__CGSCC_OPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT:  call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* nocapture noref nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture noref nonnull readonly align 64 dereferenceable(64) [[TMP3]])
; IS__CGSCC_OPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT:  ret void
;
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT:  bb:

%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
;

This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #4 {
;
; NOT_TUNIT_NPM-LABEL: define
{{[^@]+}} @callee_avx2_legal512_prefer256_call_avx2_legal512_prefer256
; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; IS__TUNIT_NPM-NEXT:    call fastcc void
@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nofree nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]])
; IS__TUNIT_NPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT:    ret void

; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT:    call fastcc void
@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nofree nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_OPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT:    ret void

; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT:    call fastcc void
@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nofree nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_NPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT:    ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; Function Attrs: argnemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #5 = { argnemonly nounwind }
; RUN: opt %s -inline -S | FileCheck %s

define internal void @innerSmall() "min-legal-vector-width"="128" {
  ret void
}

define internal void @innerLarge() "min-legal-vector-width"="512" {
  ret void
}

define internal void @innerNoAttribute() {
  ret void
}

; We should not add an attribute during inlining. No attribute means unknown.
; Inlining doesn't change the fact that we don't know anything about this
; function.
define void @outerNoAttribute() {
  call void @innerLarge()
  ret void
}

define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
  call void @innerLarge()
  ret void
}

define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
  call void @innerSmall()
  ret void
}
We should remove the attribute after inlining since the callee's vector width requirements are unknown.

```c
define void @outerAttribute() "min-legal-vector-width"="128" {
  call void @innerNoAttribute()
  ret void
}

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }

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HIC++ Coding Standard as created by PRQA.

Please see http://www.codingstandard.com/section/conditions-of-use/ for more information.

```c
; RUN: llc < %s -mtriple=s390x-linux-gnu -mcpu=zEC12 -verify-machineinstrs | FileCheck %s
;
; Test that early if conversion produces LOCR with operands of the right register classes.

define void @autogen_SD4739(i8*) {
    ; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
    BB:
    %L34 = load i8, i8* %0
    %Cmp56 = icmp sgt i8 undef, %L34
    br label %CF246

    CF246:                                            ; preds = %CF246, %BB
    %SI163 = select i1 %Cmp56, i8 %L34, i8 undef
    br i1 undef, label %CF246, label %CF248

    CF248:                                            ; preds = %CF248, %CF246
    store i8 %SI163, i8* %0
    br label %CF248
}
```

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; NOTE: Assertions have been autogenerated by utils/update_analyze_test_checks.py
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx2 | FileCheck %s --check-prefixes=CHECK,VEC256,AVX
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC256,AVX512VL256
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,-prefer-256-bit |
FileCheck %s --check-prefixes=CHECK,VEC512,AVX512VL512
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC256,SKX256
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,-prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC512,SKX512

define void @zext256() "min-legal-vector-width"="256" {
; VEC256-LABEL: 'zext256'
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'zext256'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'zext256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
define void @zext512() "min-legal-vector-width"="512" {
    ; AVX-LABEL: 'zext512'
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    
    ; AVX512VL256-LABEL: 'zext512'
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    
    ; AVX512VL512-LABEL: 'zext512'
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    
    ; SKX256-LABEL: 'zext512'
    ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
}
define void @sext256() "min-legal-vector-width"="256" {  
  ; VEC256-LABEL: 'sext256'
  ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
  ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
  ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <16 x i8> undef to <16 x i32>
  ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i16> undef to <16 x i32>
  ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <32 x i8> undef to <32 x i16>
  ; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
  ;
  ; AVX512VL512-LABEL: 'sext256'
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
define void @sext512() "min-legal-vector-width"="512" { 
  ; AVX-LABEL: 'sext512'
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = sext <16 x i8> undef to <16 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

  ; SKX512-LABEL: 'sext256'
  ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
  ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
  ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
  ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
  ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
  ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
  ; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

  ; AVX512VL256-LABEL: 'sext256'
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>

#define void @sext512() "min-legal-vector-width"="512" {
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>

 ret void }
define void @trunc256() "min-legal-vector-width"="256" {
    %A = sext <8 x i8> undef to <8 x i64>
    %B = sext <8 x i16> undef to <8 x i64>
    %C = sext <8 x i32> undef to <8 x i64>
    %D = sext <8 x i64> undef to <8 x i8>
    %E = sext <16 x i8> undef to <16 x i16>
    %F = sext <16 x i16> undef to <16 x i8>
    %G = sext <32 x i8> undef to <32 x i16>
    ret void
}

define void @trunc256() "min-legal-vector-width"="256" {
    %A = trunc <8 x i64> undef to <8 x i32>
    %B = trunc <8 x i64> undef to <8 x i16>
    %C = trunc <8 x i64> undef to <8 x i8>
    %D = trunc <8 x i32> undef to <8 x i16>
    %E = trunc <8 x i32> undef to <8 x i8>
    %F = trunc <8 x i16> undef to <8 x i8>
    ret void
}

define void @trunc256() "min-legal-vector-width"="256" {
    %A = trunc <8 x i64> undef to <8 x i32>
    %B = trunc <8 x i64> undef to <8 x i16>
    %C = trunc <8 x i64> undef to <8 x i8>
    %D = trunc <8 x i32> undef to <8 x i16>
    %E = trunc <8 x i32> undef to <8 x i8>
    %F = trunc <8 x i16> undef to <8 x i8>
    ret void
}
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'trunc256'
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'trunc256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

%A = trunc <8 x i64> undef to <8 x i32>
%B = trunc <8 x i64> undef to <8 x i16>
%C = trunc <8 x i64> undef to <8 x i8>
%D = trunc <16 x i32> undef to <16 x i16>
%E = trunc <16 x i32> undef to <16 x i8>
%F = trunc <32 x i16> undef to <32 x i8>
ret void
define i32 @zext256_vXi1() "min-legal-vector-width"="256" {  
    ; AVX-LABEL: 'zext256_vXi1'
    ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef  
    
    ; AVX512VL256-LABEL: 'zext256_vXi1'
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
}
to <8 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 19 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX256-LABEL: 'zext256_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; SKX512-LABEL: 'zext256_vXi1'
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
; %V2i64 = zext <2 x i1> undef to <2 x i64>
%V4i64 = zext <4 x i1> undef to <4 x i64>
%V8i64 = zext <8 x i1> undef to <8 x i64>

%V2i32 = zext <2 x i1> undef to <2 x i32>
%V4i32 = zext <4 x i1> undef to <4 x i32>
%V8i32 = zext <8 x i1> undef to <8 x i32>
%V16i32 = zext <16 x i1> undef to <16 x i32>

%V2i16 = zext <2 x i1> undef to <2 x i16>
%V4i16 = zext <4 x i1> undef to <4 x i16>
%V8i16 = zext <8 x i1> undef to <8 x i16>
%V16i16 = zext <16 x i1> undef to <16 x i16>
%V32i16 = zext <32 x i1> undef to <32 x i16>

%V2i8 = zext <2 x i1> undef to <2 x i8>
%V4i8 = zext <4 x i1> undef to <4 x i8>
%V8i8 = zext <8 x i1> undef to <8 x i8>
%V16i8 = zext <16 x i1> undef to <16 x i8>
%V32i8 = zext <32 x i1> undef to <32 x i8>
%V64i8 = zext <64 x i1> undef to <64 x i8>

ret i32 undef
}

define i32 @sext256_vXi1() "min-legal-vector-width"="256"
 { ; AVX-LABEL: 'sext256_vXi1'
 ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
 ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
 ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
 ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = sext <4 x i1> undef to <4 x
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; AVX512VL256-LABEL: `sext256_vXi1'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 20 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
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; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 21 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 42 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL512-LABEL: 'sext256_vXi1'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i64 = sext <16 x i1> undef to <16 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i64 = sext <32 x i1> undef to <32 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
<8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 15 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; SKX256-LABEL: 'sext256_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX512-LABEL: 'sext256_vXii'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
%I64 = sext i1 undef to i64
define i32 @trunc_vXi1() "min-legal-vector-width"="256" {
  ; AVX-LABEL: 'trunc_vXi1'
  ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 46 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 16 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 32 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 64 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 128 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 256 for instruction: %V128i16 = trunc <128 x i16> undef to <128 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 16 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 32 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 64 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 128 for instruction: %V128i8 = trunc <128 x i8> undef to <128 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i1 = trunc <2 x i1> undef to <2 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i1 = trunc <4 x i1> undef to <4 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i1 = trunc <8 x i1> undef to <8 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 16 for instruction: %V16i1 = trunc <16 x i1> undef to <16 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 32 for instruction: %V32i1 = trunc <32 x i1> undef to <32 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 64 for instruction: %V64i1 = trunc <64 x i1> undef to <64 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 128 for instruction: %V128i1 = trunc <128 x i1> undef to <128 x i1>
  ret i32 undef
}
<table>
<thead>
<tr>
<th>Instruction</th>
<th>Cost Model</th>
<th>Estimated Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>V16i32 = trunc &lt;16 x i32&gt; undef to &lt;16 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 5 for instruction:</td>
<td>5</td>
</tr>
<tr>
<td>V32i32 = trunc &lt;32 x i32&gt; undef to &lt;32 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 10 for instruction:</td>
<td>10</td>
</tr>
<tr>
<td>V64i32 = trunc &lt;64 x i32&gt; undef to &lt;64 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 20 for instruction:</td>
<td>20</td>
</tr>
<tr>
<td>V2i16 = trunc &lt;2 x i16&gt; undef to &lt;2 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 3 for instruction:</td>
<td>3</td>
</tr>
<tr>
<td>V4i16 = trunc &lt;4 x i16&gt; undef to &lt;4 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 3 for instruction:</td>
<td>3</td>
</tr>
<tr>
<td>V8i16 = trunc &lt;8 x i16&gt; undef to &lt;8 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 3 for instruction:</td>
<td>3</td>
</tr>
<tr>
<td>V16i16 = trunc &lt;16 x i16&gt; undef to &lt;16 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 8 for instruction:</td>
<td>8</td>
</tr>
<tr>
<td>V32i16 = trunc &lt;32 x i16&gt; undef to &lt;32 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 17 for instruction:</td>
<td>17</td>
</tr>
<tr>
<td>V64i16 = trunc &lt;64 x i16&gt; undef to &lt;64 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 34 for instruction:</td>
<td>34</td>
</tr>
<tr>
<td>V2i8 = trunc &lt;2 x i8&gt; undef to &lt;2 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 0 for instruction:</td>
<td>0</td>
</tr>
<tr>
<td>V4i8 = trunc &lt;4 x i8&gt; undef to &lt;4 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 8 for instruction:</td>
<td>8</td>
</tr>
<tr>
<td>V8i8 = trunc &lt;8 x i8&gt; undef to &lt;8 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 11 for instruction:</td>
<td>11</td>
</tr>
<tr>
<td>V16i8 = trunc &lt;16 x i8&gt; undef to &lt;16 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 17 for instruction:</td>
<td>17</td>
</tr>
<tr>
<td>V32i8 = trunc &lt;32 x i8&gt; undef to &lt;32 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 34 for instruction:</td>
<td>34</td>
</tr>
<tr>
<td>V64i8 = trunc &lt;64 x i8&gt; undef to &lt;64 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 11 for instruction:</td>
<td>11</td>
</tr>
<tr>
<td>V2i32 = trunc &lt;2 x i32&gt; undef to &lt;2 x i1&gt;</td>
<td>Cost Model: Found an estimated cost of 2 for instruction:</td>
<td>2</td>
</tr>
<tr>
<td>V4i32 = trunc &lt;4 x i32&gt;</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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undef to <4 x i1>

AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>

AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>

AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>

AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>

AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>

AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>

AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>

SKX256-LABEL: 'trunc_vXi1'

SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>

SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>

SKX256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>

SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>

SKX256-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>

SKX256-NEXT: Cost Model: Found an estimated cost of 47 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; SKX512-LABEL: 'trunc_vXi1'
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
%V2i32 = trunc <2 x i32> undef to <2 x i1>
%V4i32 = trunc <4 x i32> undef to <4 x i1>
%V8i32 = trunc <8 x i32> undef to <8 x i1>
%V16i32 = trunc <16 x i32> undef to <16 x i1>
%V32i32 = trunc <32 x i32> undef to <32 x i1>
%V64i32 = trunc <64 x i32> undef to <64 x i1>

%V2i16 = trunc <2 x i16> undef to <2 x i1>
%V4i16 = trunc <4 x i16> undef to <4 x i1>
%V8i16 = trunc <8 x i16> undef to <8 x i1>
%V16i16 = trunc <16 x i16> undef to <16 x i1>
%V32i16 = trunc <32 x i16> undef to <32 x i1>
%V64i16 = trunc <64 x i16> undef to <64 x i1>

%V2i8 = trunc <2 x i8> undef to <2 x i1>
%V4i8 = trunc <4 x i8> undef to <4 x i1>
%V8i8 = trunc <8 x i8> undef to <8 x i1>
%V16i8 = trunc <16 x i8> undef to <16 x i1>
%V32i8 = trunc <32 x i8> undef to <32 x i1>
%V64i8 = trunc <64 x i8> undef to <64 x i1>

ret i32 undef
}
add_lldb_library(lldbPluginObjectContainerBSDArchive PLUGIN
ObjectContainerBSDArchive.cpp

LINK_LIBS
  lldbCore
  lldbHost
  lldbSymbol
LINK_COMPONENTS
  Support
)}
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit,avx512vbmi | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; Make sure CPUs default to prefer-256-bit. avx512vnni isn't interesting as it just adds an isel peephole for
vpmaddwd+vpadd
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cascadelake | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cooperlake | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=cannonlake | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=avx512vnni -mcpu=icelake-client | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=avx512vnni -mcpu=icelake-server | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=avx512vnni -mcpu=tigerlake | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI

; This file primarily contains tests for specific places in X86ISelLowering.cpp that needed be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

define void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: add256:
  ; CHECK: # %bb.0:
  ; CHECK-NEXT: vmovdqa (%rdi), %ymm0
  ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
  ; CHECK-NEXT: vpaddd 32(%rsi), %ymm1, %ymm1
  ; CHECK-NEXT: vpaddd (%rsi), %ymm0, %ymm0
  ; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
  ; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
  ; CHECK-NEXT: vzeroupper
  ; CHECK-NEXT: retq
  %d = load <16 x i32>, <16 x i32>* %a
  %e = load <16 x i32>, <16 x i32>* %b
  %f = add <16 x i32> %d, %e
  store <16 x i32> %f, <16 x i32>* %c
  ret void
}

define void @add512(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="512" {
  ; CHECK-LABEL: add512:
  ; CHECK: # %bb.0:
  ; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
  ; CHECK-NEXT: vmovdqa (%rsi), %zmm1
  ; CHECK-NEXT: vpadd 32(%rsi), %zmm0, %zmm0
  ; CHECK-NEXT: vpadd (%rsi), %zmm0, %zmm1
  ; CHECK-NEXT: vmovdqa %zmm0, (%rdx)
  ; CHECK-NEXT: vmovdqa %zmm1, 32(%rdx)
  ; CHECK-NEXT: vzeroupper
  ; CHECK-NEXT: retq
  %d = load <16 x i32>, <16 x i32>* %a
  %e = load <16 x i32>, <16 x i32>* %b
  %f = add <16 x i32> %d, %e
  store <16 x i32> %f, <16 x i32>* %c
  ret void
}

define void @avg_v64i8_256(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: avg_v64i8_256:
  ; CHECK: # %bb.0:
  ; CHECK-NEXT: vmovdqa (%rsi), %zmm0
  ; CHECK-NEXT: vmovdqa32 (%rsi), %zmm1
  ; CHECK-NEXT: vpaddd (%rsi), %zmm1, %zmm1
  ; CHECK-NEXT: vpaddd 32(%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT: vmovdqa %zmm0, (%rdx)
  ; CHECK-NEXT: vmovdqa %zmm1, 32(%rdx)
  ; CHECK-NEXT: vpaddd 32(%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT: vmovdqa %zmm0, (%rdx)
  ; CHECK-NEXT: vmovdqa %zmm1, 32(%rdx)
  ; CHECK-NEXT: vpaddd (%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT: vmovdqa %zmm0, (%rdx)
  ; CHECK-NEXT: vmovdqa %zmm1, 32(%rdx)
  ; CHECK-NEXT: vpaddd 32(%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT: vmovdqa %zmm0, (%rdx)
  ; CHECK-NEXT: vmovdqa %zmm1, 32(%rdx)
  ; CHECK-NEXT: vpaddd (%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT: vmovdqa %zmm0, (%rdx)
  ; CHECK-NEXT: vmovdqa %zmm1, 32(%rdx)
  ; CHECK-NEXT: vpaddd 32(%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT: vmovdqa %zmm0, (%rdx)
  ; CHECK-NEXT: vmovdqa %zmm1, 32(%rdx)
  ; CHECK-NEXT: vpaddd 32(%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT: vmovdqa %zmm0, (%rdx)
  ; CHECK-NEXT: vmovdqa %zmm1, 32(%rdx)
  ; CHECK-NEXT: vpaddd 32(%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT: vmovdqa %zmm0, (%rdx)
  ; CHECK-NEXT: vmovdqa %zmm1, 32(%rdx)
  ; CHECK-NEXT: vpaddd 32(%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT: vmovdqa %zmm0, (%rdx)
  ; CHECK-NEXT: vmovdqa %zmm1, 32(%rdx)
  ; CHECK-NEXT: vpaddd 32(%rsi), %zmm1, %zmm0
  ; CHECK-NEXT: vpaddd (%rsi), %zmm1, %zmm0
  ; CHECK-NEX...
define void @avg_v64i8_512(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: avg_v64i8_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vmovdqa64 (%rsi), %zmm0
    ; CHECK-NEXT:    vpavgb (%rdi), %zmm0, %zmm0
    ; CHECK-NEXT:    vmovdqu64 %zmm0, (%rax)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq

    %1 = load <64 x i8>, <64 x i8>* %a
    %2 = load <64 x i8>, <64 x i8>* %b
    %3 = zext <64 x i8> %1 to <64 x i32>
    %4 = zext <64 x i8> %2 to <64 x i32>
    %5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
    %6 = add nuw nsw <64 x i32> %5, %4
    %7 = lshr <64 x i32> %6, %4
    %8 = zext <64 x i8> %7 to <64 x i32>
    %9 = trunc <64 x i32> %8 to <64 x i8>
    store <64 x i8> %9, <64 x i8>* undef, align 4
    ret void
}
define void @pmaddwd_32_256(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: pmaddwd_32_256:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
    ; CHECK-NEXT:  vpmaddwd 32(%rsi), %ymm1, %ymm1
    ; CHECK-NEXT:  vpmaddwd (%rsi), %ymm0, %ymm0
    ; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
    ; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
    ; CHECK-NEXT:  vzeroupper
    ; CHECK-NEXT:  retq
    %A = load <32 x i16>, <32 x i16>* %APtr
    %B = load <32 x i16>, <32 x i16>* %BPtr
    %a = sext <32 x i16> %A to <32 x i32>
    %b = sext <32 x i16> %B to <32 x i32>
    %m = mul nsw <32 x i32> %a, %b
    %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
    %even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
    %ret = add <16 x i32> %odd, %even
    store <16 x i32> %ret, <16 x i32>* %CPtr
    ret void
}

define void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: pmaddwd_32_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
    ; CHECK-NEXT:  vpmaddwd (%rsi), %zmm0, %zmm0
    ; CHECK-NEXT:  vmovdqa64 %zmm0, (%rdx)
    ; CHECK-NEXT:  vzeroupper
    ; CHECK-NEXT:  retq
    %A = load <32 x i16>, <32 x i16>* %APtr
    %B = load <32 x i16>, <32 x i16>* %BPtr
    %a = sext <32 x i16> %A to <32 x i32>
    %b = sext <32 x i16> %B to <32 x i32>
    %m = mul nsw <32 x i32> %a, %b
    %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
    %even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
    %ret = add <16 x i32> %odd, %even
ret void
}
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

define void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %y.ptr, <64 x i8>* %z.ptr) "min-legal-vector-width"="256" {
 ; CHECK-LABEL: psubus_64i8_max_256:
 ; CHECK: # %bb.0:
 ; CHECK-NEXT: vmovdqa (%rdi), %ymm0
 ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
 ; CHECK-NEXT: vpsubusb 32(%rsi), %ymm1, %ymm1
 ; CHECK-NEXT: vpsubusb (%rsi), %ymm0, %ymm0
 ; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
 ; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
 ; CHECK-NEXT: vzeroupper
 ; CHECK-NEXT: retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %y.ptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %z.ptr
ret void
}

define void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %y.ptr, <64 x i8>* %z.ptr) "min-legal-vector-width"="512" {
 ; CHECK-LABEL: psubus_64i8_max_512:
 ; CHECK: # %bb.0:
 ; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
 ; CHECK-NEXT: vpsubusb (%rsi), %zmm0, %zmm0
 ; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
 ; CHECK-NEXT: vzeroupper
 ; CHECK-NEXT: retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %y.ptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %z.ptr
ret void
}

define i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {
 ; CHECK-LABEL: _Z9test_charPcS_i_256:
 ; CHECK: # %bb.0: # %entry
 ; CHECK-NEXT: movl %edx, %eax

; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:    xorl %ecx, %ecx
; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT:    vpxor %xmm2, %xmm2, %xmm2
; CHECK-NEXT:    .p2align 4, 0x90
; CHECK-NEXT:  .LBB8_1: # %vector.body
; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:    vpmovsxbw 16(%rdi,%rcx), %ymm3
; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %ymm4
; CHECK-NEXT:    vpmovsxbw 16(%rsi,%rcx), %ymm5
; CHECK-NEXT:    vpmaddwd %ymm3, %ymm5, %ymm3
; CHECK-NEXT:    vpaddd %ymm1, %ymm3, %ymm2
; CHECK-NEXT:    addq $32, %rcx
; CHECK-NEXT:    cmpq %rcx, %rax
; CHECK-NEXT:    jne .LBB8_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm1
; CHECK-NEXT:    vpaddd %ymm0, %ymm2, %ymm0
; CHECK-NEXT:    vpmaddwd %ymm0, %ymm0, %ymm1
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vmovd %xmm0, %eax
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
entry:
%3 = zext i32 %2 to i64
br label %vector.body

vector.body:
%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %21, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %21, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body

middle.block:
%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx1 = add <32 x i32> %12, %rdx.shuf1
%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <32 x i32> %rdx.shuf, %bin.rdx1
%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx18 = add <32 x i32> %bin.rdx17, %rdx.shuf17
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx20 = add <32 x i32> %bin.rdx19, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13

define i32 @_Z9test_charPcS_i_512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="512" {
  ; CHECK-LABEL: @_Z9test_charPcS_i_512:
  ; CHECK:  # %bb.0: # %entry
  ; CHECK-NEXT:  movl %edx, %eax
  ; CHECK-NEXT:  vpxor %xmm0, %xmm0, %xmm0
  ; CHECK-NEXT:  xorl %ecx, %ecx
  ; CHECK-NEXT:  vpxor %xmm1, %xmm1, %xmm1
  ; CHECK-NEXT:  .p2align 4, 0x90
  ; CHECK-NEXT:  .LBB9_1: # %vector.body
  ; CHECK-NEXT:  # =>This Inner Loop Header: Depth=1
  ; CHECK-NEXT:  vpmovsxbw (%rdi, %rcx), %zmm2
  ; CHECK-NEXT:  vpmovsxbw (%rsi, %rcx), %zmm3
  ; CHECK-NEXT:  vpmaddwd %zmm2, %zmm3, %zmm2
; CHECK-NEXT:  vpaddd %zmm1, %zmm2, %zmm1
; CHECK-NEXT:  addq $32, %rcx
; CHECK-NEXT:  cmpq %rcx, %rax
; CHECK-NEXT:  jne .LBB9_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:  vpaddd %zmm0, %zmm1, %zmm0
; CHECK-NEXT:  vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT:  vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:  vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vmovd %xmm0, %eax
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
entry:
  %3 = zext i32 %2 to i64
br label %vector.body
vector.body:
  %index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
  %vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
  %4 = getelementptr inbounds i8, i8* %0, i64 %index
  %5 = bitcast i8* %4 to <32 x i8>*
  %wide.load = load <32 x i8>, <32 x i8>* %5, align 1
  %6 = sext <32 x i8> %wide.load to <32 x i32>
  %7 = getelementptr inbounds i8, i8* %1, i64 %index
  %8 = bitcast i8* %7 to <32 x i8>*
  %wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
  %9 = sext <32 x i8> %wide.load14 to <32 x i32>
  %10 = mul nsw <32 x i32> %9, %6
  %11 = add nsw <32 x i32> %10, %vec.phi
  %index.next = add i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body
middle.block:
  %rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 unde
%bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13
}

@a = global [1024 x i8] zeroinitializer, align 16
@b = global [1024 x i8] zeroinitializer, align 16

define i32 @sad_16i8_256() "min-legal-vector-width"="256" {
; CHECK-LABEL: sad_16i8_256:
; CHECK: # %bb.0: # %entry
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: movq -1024, %rax # imm = 0xFC00
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB10_1: # %vector.body
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-NEXT: vmovdqu a+1024(%rax), %ymm2
; CHECK-NEXT: vpsadbw b+1024(%rax), %ymm2, %ymm2
; CHECK-NEXT: vpadd %ymm1, %ymm2, %ymm1
; CHECK-NEXT: addq $4, %rax
; CHECK-NEXT: jne .LBB10_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT: vpadd %ymm0, %ymm1, %ymm0
; CHECK-NEXT: vextracti128 %ymm0[1], %ymm0, %ymm1
; CHECK-NEXT: vpadd %ymm1, %ymm0, %xmm0
; CHECK-NEXT: vpxor %ymm1, %ymm1, %xmm0
; CHECK-NEXT: vpsadbw {{.*,+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpsadbw {{.*,+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vmovd %xmm0, %eax
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
entry:
  br label %vector.body

vector.body:
  %index = phi i64 [ 0, entry ], [ %index.next, %vector.body ]
  %vec.phi = phi <16 x i32> [ zeroinitializer, entry ], [ %10, %vector.body ]
  %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
  %1 = bitcast i8* %0 to <16 x i8>*
  %wide.load = load <16 x i8>, <16 x i8>* %1, align 4
  %2 = zext <16 x i8> %wide.load to <16 x i32>
  %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
  %4 = bitcast i8* %3 to <16 x i8>*
  %wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
  %5 = zext <16 x i8> %wide.load1 to <16 x i32>
  %6 = sub nsw <16 x i32> %2, %5
  %7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
  %8 = sub nsw <16 x i32> zeroinitializer, %6
  %9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
  %10 = add nsw <16 x i32> %9, %vec.phi
  %index.next = add i64 %index, 4
  %11 = icmp eq i64 %index.next, 1024
  br i1 %11, label %middle.block, label %vector.body

middle.block:
  %rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx = add <16 x i32> %10, %rdx.shuf
  %rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
  %rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
  %rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
  %12 = extractelement <16 x i32> %bin.rdx4, i32 0
  ret i32 %12
}

define i32 @sad_16i8_512() "min-legal-vector-width"="512" {
  ; CHECK-LABEL: sad_16i8_512:
  ; CHECK:     # %bb.0: # %entry
  ; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
}
entry:
  br label %vector.body

vector.body:
  %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
  %vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
  %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
  %1 = bitcast i8* %0 to <16 x i8>*
  %wide.load = load <16 x i8>, <16 x i8>* %1, align 4
  %2 = zext <16 x i8> %wide.load to <16 x i32>
  %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
  %4 = bitcast i8* %3 to <16 x i8>*
  %wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
  %5 = zext <16 x i8> %wide.load1 to <16 x i32>
  %6 = sub nsw <16 x i32> %2, %5
  %7 = icmp sgt <16 x i32> %6, %<i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
  %8 = sub nsw <16 x i32> zeroinitializer, %6
  %9 = select <16 x i1> %7, %<16 x i32> %6, %<16 x i32> %8
  %10 = add nsw <16 x i32> %9, %vec.phi
  %index.next = add i64 %index, 4
  %11 = icmp eq i64 %index.next, 1024
  br i1 %11, label %middle.block, label %vector.body

middle.block:
  %rdx.shuf = shufflevector <16 x i32> %10, %<16 x i32> undef, %<16 x i32> %<i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %10, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

define void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f32_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k0, %ymm0
; CHECK-NEXT: vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm1
; CHECK-NEXT: vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT: vmovaps %ymm1, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}
define void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: sbto16f64_256:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:    kshiftrw $8, %k0, %k1
    ; CHECK-NEXT:    vpmovm2d %k1, %ymm0
    ; CHECK-NEXT:    vcvtqd2pd %xmm0, %ymm1
    ; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm0
    ; CHECK-NEXT:    vcvtqd2pd %xmm0, %ymm0
    ; CHECK-NEXT:    vpmovm2d %k0, %ymm2
    ; CHECK-NEXT:    vcvtqd2pd %xmm2, %ymm3
    ; CHECK-NEXT:    vextracti128 $1, %ymm2, %xmm2
    ; CHECK-NEXT:    vcvtqd2pd %xmm2, %ymm2
    ; CHECK-NEXT:    vmovaps %ymm2, 32(%rdi)
    ; CHECK-NEXT:    vmovaps %ymm3, (%rdi)
    ; CHECK-NEXT:    vmovaps %ymm0, 96(%rdi)
    ; CHECK-NEXT:    vmovaps %ymm1, 64(%rdi)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %mask = icmp slt <16 x i16> %a, zeroinitializer
    %1 = sitofp <16 x i1> %mask to <16 x double>
    store <16 x double> %1, <16 x double>* %res
    ret void
}

define void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: sbto16f64_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:    vpmovm2d %k0, %zmm0
    ; CHECK-NEXT:    vcvtqd2pd %ymm0, %zmm1
    ; CHECK-NEXT:    vextracti64x4 $1, %zmm0, %ymm0
    ; CHECK-NEXT:    vcvtqd2pd %ymm0, %zmm0
    ; CHECK-NEXT:    vmovaps %zmm0, 64(%rdi)
    ; CHECK-NEXT:    vmovaps %zmm1, (%rdi)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %mask = icmp slt <16 x i16> %a, zeroinitializer
    %1 = sitofp <16 x i1> %mask to <16 x double>
    store <16 x double> %1, <16 x double>* %res
    ret void
}

define void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: ubto16f32_256:

define void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
  ; CHECK-LABEL: ubto16f32_512:
  ; CHECK:      # %bb.0:
  ; CHECK-NEXT:  vpmovw2m %ymm0, %k0
  ; CHECK-NEXT:  kshiftrw $8, %k0, %k1
  ; CHECK-NEXT:  vpmovm2d %k1, %ymm0
  ; CHECK-NEXT:  vpsrld $31, %ymm0, %ymm0
  ; CHECK-NEXT:  vcvtfd2ps %ymm0, %ymm0
  ; CHECK-NEXT:  vpmovm2d %k0, %ymm1
  ; CHECK-NEXT:  vpsrld $31, %ymm1, %ymm1
  ; CHECK-NEXT:  vcvtfd2ps %ymm1, %ymm1
  ; CHECK-NEXT:  vmovaps %ymm1, (%rdi)
  ; CHECK-NEXT:  vmovaps %ymm0, 32(%rdi)
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = uitofp <16 x i1> %mask to <16 x float>
  store <16 x float> %1, <16 x float>* %res
  ret void
}

define void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: ubto16f64_256:
  ; CHECK:      # %bb.0:
  ; CHECK-NEXT:  vpmovw2m %ymm0, %k0
  ; CHECK-NEXT:  vpmovm2d %k0, %zmm0
  ; CHECK-NEXT:  vpsrld $31, %zmm0, %zmm0
  ; CHECK-NEXT:  vcvtfd2ps %zmm0, %zmm0
  ; CHECK-NEXT:  vmovaps %zmm0, (%rdi)
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = uitofp <16 x i1> %mask to <16 x float>
  store <16 x float> %1, <16 x float>* %res
  ret void
}

; CHECK-NEXT:  vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT:  vcvtqd2pd %xmm2, %ymm2
; CHECK-NEXT:  vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT:  vmovaps %ymm3, (%rdi)
; CHECK-NEXT:  vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT:  vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}
define void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f64_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vpmovw2m %ymm0, %k0
; CHECK-NEXT:  vpmovm2d %k0, %zmm0
; CHECK-NEXT:  vpsrlq $31, %zmm0, %zmm0
; CHECK-NEXT:  vcvtqd2pd %ymm0, %zmm0
; CHECK-NEXT:  vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT:  vcvtqd2pd %ymm0, %zmm0
; CHECK-NEXT:  vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:  vmovaps %zmm1, (%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}
define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {
; CHECK-LABEL: test_16f32toub_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vcvtpps2dq (%rdi), %ymm1
; CHECK-NEXT:  vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k0
; CHECK-NEXT:  vcvtpps2dq 32(%rdi), %ymm1
; CHECK-NEXT:  vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k1
; CHECK-NEXT:  kunpckbw %k0, %k1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer  
ret <16 x i16> %select  
}

define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {  
; CHECK-LABEL: test_16f32toub_512:  
; CHECK:  
; CHECK-NEXT: vcvttps2dq (%rdi), %zmm1  
; CHECK-NEXT: vpssld $31, %zmm1, %zmm1  
; CHECK-NEXT: vpmovd2m %zmm1, %k1  
; CHECK-NEXT: vmovdqu16 %ymm0, %ymm0 [%k1] {z}  
; CHECK-NEXT: retq  
%a = load <16 x float>, <16 x float>* %ptr  
%mask = fptoui <16 x float> %a to <16 x i1>  
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroiniti
define void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {
  ; CHECK-AVX512-LABEL: mul256:
  ; CHECK-AVX512: # %bb.0:
  ; CHECK-AVX512-NEXT: vmovdqa (%rdi), %ymm0
  ; CHECK-AVX512-NEXT: vmovdqa 32(%rdi), %ymm1
  ; CHECK-AVX512-NEXT: vmovdqa (%rsi), %ymm2
  ; CHECK-AVX512-NEXT: vmovdqa 32(%rsi), %ymm3
  ; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm4 =
    ymm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
  ; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm5 =
    ymm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
  ; CHECK-AVX512-NEXT: vpmullw %ymm4, %ymm5, %ymm4
  ; CHECK-AVX512-NEXT: vmovdqa {{.*#+}} ymm5 =
  ; CHECK-AVX512-NEXT: vpand %ymm5, %ymm4, %ymm4
  ; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm4 =
    ymm3[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
  ; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm1 =
    ymm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
  ; CHECK-AVX512-NEXT: vpmullw %ymm3, %ymm1, %ymm1
  ; CHECK-AVX512-NEXT: vpand %ymm5, %ymm1, %ymm1
  ; CHECK-AVX512-NEXT: vpackuswb %ymm4, %ymm3, %ymm1
  ; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm3 =
    ymm2[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
  ; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm4 =
    ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
  ; CHECK-AVX512-NEXT: vpmullw %ymm3, %ymm4, %ymm3
  ; CHECK-AVX512-NEXT: vpand %ymm5, %ymm3, %ymm3
  ; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm2 =
    ymm2[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
  ; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm0 =
    ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
  ; CHECK-AVX512-NEXT: vpmullw %ymm2, %ymm0, %ymm0
  ; CHECK-AVX512-NEXT: vpand %ymm5, %ymm0, %ymm0
  ; CHECK-AVX512-NEXT: vpackuswb %ymm3, %ymm0, %ymm0
  ; CHECK-AVX512-NEXT: vmovdqa %ymm0, (%rdx)
  ; CHECK-AVX512-NEXT: vmovdqa %ymm1, 32(%rdx)
  ; CHECK-AVX512-NEXT: vzeroupper
  ; CHECK-AVX512-NEXT: retq
  ;}
  ; CHECK-VBMI-LABEL: mul256:
  ; CHECK-VBMI: # %bb.0:
  ; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm0
  ; CHECK-VBMI-NEXT: vmovdqa 32(%rdi), %ymm1
  ; CHECK-VBMI-NEXT: vmovdqa (%rsi), %ymm2
  ; CHECK-VBMI-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-VBMI-NEXT:    vpunpckhbw {{.*#+}} ymm4 =
    ymm3[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT:    vpunpckhbw {{.*#+}} ymm5 =
    ymm1[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT:    vpmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT:    vpmullw %ymm3, %ymm1, %ymm1
; CHECK-VBMI-NEXT:    vmovdqa {{.*#+}} ymm3 =
    [0,2,4,6,8,10,12,14,32,34,36,38,40,42,44,46,16,18,20,22,24,26,28,30,48,50,52,54,56,58,60,62]
; CHECK-VBMI-NEXT:    vpermt2b %ymm4, %ymm3, %ymm1
; CHECK-VBMI-NEXT:    vpunpckhbw {{.*#+}} ymm4 =
    ymm2[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT:    vpmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT:    vpmullw %ymm2, %ymm0, %ymm0
; CHECK-VBMI-NEXT:    vzeroupper
; CHECK-VBMI-NEXT:    retq

%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void

}
; CHECK-AVX512-NEXT:  vpandq %zmm3, %zmm2, %zmm2
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} zmm1 =
   zmm1[0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,36,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} zmm0 =
   zmm0[0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,36,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT:  vpmullw %zmm1, %zmm0, %zmm0
; CHECK-AVX512-NEXT:  vpackuswb %zmm2, %zmm0, %zmm0
; CHECK-AVX512-NEXT:  vmovdqa64 %zmm0, (%rdx)
; CHECK-AVX512-NEXT:  vzeroupper
; CHECK-AVX512-NEXT:  retq

; CHECK-VBMI-LABEL: mul512:
; CHECK-VBMI:       # %bb.0:
; CHECK-VBMI-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-VBMI-NEXT:  vmovdqa64 (%rsi), %zmm1
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} zmm2 =
   zmm2[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,42,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} zmm3 =
   zmm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,42,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-VBMI-NEXT:  vpermi2b %zmm2, %zmm0, %zmm1
; CHECK-VBMI-NEXT:  vmovdqa64 %zmm1, (%rdx)
; CHECK-VBMI-NEXT:  vzeroupper
; CHECK-VBMI-NEXT:  retq

%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void
; This threw an assertion at one point.
define <4 x i32> @mload_v4i32(<4 x i32> %trigger, <4 x i32>* %addr, <4 x i32> %dst) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: mload_v4i32:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:   vptestmd %xmm0, %xmm0, %k1
  ; CHECK-NEXT:   vpblendmd (%rdi), %xmm1, %xmm0 {%k1}
  ; CHECK-NEXT:   retq
  %mask = icmp eq <4 x i32> %trigger, zeroinitializer
  %res = call <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* %addr, i32 4, <4 x i1> %mask, <4 x i32> %dst)
  ret <4 x i32> %res
} declare <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>*, i32, <4 x i1>, <4 x i32>)

define <16 x i32> @trunc_v16i64_v16i32(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
  ; CHECK-LABEL: trunc_v16i64_v16i32:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:   vmovdqa (%rdi), %ymm0
  ; CHECK-NEXT:   vmovdqa 32(%rdi), %ymm1
  ; CHECK-NEXT:   vmovdqa 64(%rdi), %ymm2
  ; CHECK-NEXT:   vmovdqa 96(%rdi), %ymm3
  ; CHECK-NEXT:   vpmovqd %ymm0, %xmm0
  ; CHECK-NEXT:   vpmovqd %ymm1, %xmm1
  ; CHECK-NEXT:   vpmovqd %ymm2, %xmm2
  ; CHECK-NEXT:   vpmovqd %ymm3, %xmm3
  ; CHECK-NEXT:   vinserti128 $1, %xmm1, %ymm0, %ymm0
  ; CHECK-NEXT:   vpmovq %xmm2, %ymm1
  ; CHECK-NEXT:   vpmovq %ymm2, %ymm1
  ; CHECK-NEXT:   vpmovq %ymm3, %ymm1
  ; CHECK-NEXT:   retq
  %a = load <16 x i64>, <16 x i64>* %x
  %b = trunc <16 x i64> %a to <16 x i32>
  ret <16 x i32> %b
} define <16 x i8> @trunc_v16i64_v16i8(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
  ; CHECK-LABEL: trunc_v16i64_v16i8:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:   vmovdqa (%rdi), %ymm0
  ; CHECK-NEXT:   vmovdqa 32(%rdi), %ymm1
  ; CHECK-NEXT:   vmovdqa 64(%rdi), %ymm2
  ; CHECK-NEXT:   vmovdqa 96(%rdi), %ymm3
  ; CHECK-NEXT:   vpmovqb %ymm3, %xmm3
  ; CHECK-NEXT:   vpmovq %ymm2, %xmm2
  ; CHECK-NEXT:   vpunpckldq {{.*#+}} xmm2 = xmm2[0],xmm3[0],xmm2[1],xmm3[1]
  ; CHECK-NEXT:   vpmovq %ymm1, %xmm1
  ; CHECK-NEXT:   vpmovq %ymm0, %xmm0
  ; CHECK-NEXT:   vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
  ; CHECK-NEXT:   vpmovq %ymm2, %xmm2
  ; CHECK-NEXT:   vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm2[0]
define <16 x i8> @trunc_v16i32_v16i8(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v16i32_v16i8:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT: vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
    ; CHECK-NEXT: vpmovdb %ymm1, %xmm1
    ; CHECK-NEXT: vpmovdb %ymm0, %xmm0
    ; CHECK-NEXT: vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm1[0]
    ; CHECK-NEXT: vzeroupper
    ; CHECK-NEXT: retq
    %a = load <16 x i32>, <16 x i32>* %x
    %b = trunc <16 x i32> %a to <16 x i8>
    ret <16 x i8> %b
}

define <8 x i8> @trunc_v8i64_v8i8(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v8i64_v8i8:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT: vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
    ; CHECK-NEXT: vpmovqb %ymm1, %xmm1
    ; CHECK-NEXT: vpmovqb %ymm0, %xmm0
    ; CHECK-NEXT: vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
    ; CHECK-NEXT: vzeroupper
    ; CHECK-NEXT: retq
    %a = load <8 x i64>, <8 x i64>* %x
    %b = trunc <8 x i64> %a to <8 x i8>
    ret <8 x i8> %b
}

define <8 x i16> @trunc_v8i64_v8i16(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v8i64_v8i16:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT: vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
    ; CHECK-NEXT: vpmovqw %ymm1, %xmm1
    ; CHECK-NEXT: vpmovqw %ymm0, %xmm0
    ; CHECK-NEXT: vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
    ; CHECK-NEXT: vzeroupper
    ; CHECK-NEXT: retq
    %a = load <8 x i64>, <8 x i64>* %x
    %b = trunc <8 x i64> %a to <8 x i16>
    ret <8 x i16> %b
}
%b = trunc <8 x i64> %a to <8 x i16>
ret <8 x i16> %b
}

define <8 x i32> @trunc_v8i64_v8i32_zeroes(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i32_zeroes:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vpsrlq $48, 32(%rdi), %ymm1
; CHECK-NEXT:  vpsrlq $48, (%rdi), %ymm2
; CHECK-NEXT:  vmovdqa {%.+} ymm0 = [0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30]
; CHECK-NEXT:  vpermi2w %ymm1, %ymm2, %ymm0
; CHECK-NEXT:  retq
%a = load <8 x i64>, <8 x i64>* %x
%b = lshr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>
%c = trunc <8 x i64> %b to <8 x i32>
ret <8 x i32> %c
}

define <16 x i16> @trunc_v16i32_v16i16_zeroes(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i16_zeroes:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm1
; CHECK-NEXT:  vmovdqa {%.+} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]
; CHECK-NEXT:  vpermi2w 32(%rdi), %ymm1, %ymm0
; CHECK-NEXT:  retq
%a = load <16 x i32>, <16 x i32>* %x
%b = lshr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16>
%c = trunc <16 x i32> %b to <16 x i16>
ret <16 x i16> %c
}

define <32 x i8> @trunc_v32i16_v32i8_zeroes(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_zeroes:
; CHECK-AVX512:       # %bb.0:
; CHECK-AVX512-NEXT: vpsrlw $8, 32(%rdi), %ymm0
; CHECK-AVX512-NEXT: vpsrlw $8, (%rdi), %ymm1
; CHECK-AVX512-NEXT:vpackuswb %ymm0, %ymm1, %ymm0
; CHECK-AVX512-NEXT: vpermq {%.+} ymm0 = ymm0[0,2,1,3]
; CHECK-AVX512-NEXT: retq
; CHECK-VBMI-LABEL: trunc_v32i16_v32i8_zeroes:
; CHECK-VBMI:       # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-VBMI-NEXT: vmovdqa {%.+} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63]
; CHECK-VBMI-NEXT: vpermi2b 32(%rdi), %ymm1, %ymm0
; CHECK-VBMI-NEXT: retq
%a = load <32 x i16>, <32 x i16>* %x
%b = lshr <32 x i16> %a, <i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8>  
%c = trunc <32 x i16> %b to <32 x i8>  
ret <32 x i8> %c

define <8 x i32> @trunc_v8i64_v8i32_sign(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {  
; CHECK-LABEL: trunc_v8i64_v8i32_sign:  
; CHECK:  
; CHECK-NEXT: vpsraq $48, 32(%rdi), %ymm0  
; CHECK-NEXT: vpsraq $48, (%rdi), %ymm1  
; CHECK-NEXT: vpmovqd %ymm1, %xmm1  
; CHECK-NEXT: vpmovqd %ymm0, %xmm0  
; CHECK-NEXT: vinserti128 $1, %xmm0, %ymm1, %ymm0  
; CHECK-NEXT: retq  
%a = load <8 x i64>, <8 x i64>* %x  
%b = ashr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>  
%c = trunc <8 x i64> %b to <8 x i32>  
ret <8 x i32> %c

define <16 x i16> @trunc_v16i32_v16i16_sign(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {  
; CHECK-LABEL: trunc_v16i32_v16i16_sign:  
; CHECK:  
; CHECK-NEXT: vmovdqa (%rdi), %ymm1  
; CHECK-NEXT: vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]  
; CHECK-NEXT: vpermi2w 32(%rdi), %ymm1, %ymm0  
; CHECK-NEXT: retq  
%a = load <16 x i32>, <16 x i32>* %x  
%b = ashr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16>  
%c = trunc <16 x i32> %b to <16 x i16>  
ret <16 x i16> %c

define <32 x i8> @trunc_v32i16_v32i8_sign(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {  
; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_sign:  
; CHECK-AVX512:  
; CHECK-AVX512-NEXT: vpsraw $8, 32(%rdi), %ymm0  
; CHECK-AVX512-NEXT: vpsraw $8, (%rdi), %ymm1  
; CHECK-AVX512-NEXT: vpacksswb %ymm0, %ymm1, %ymm0  
; CHECK-AVX512-NEXT: vpermq {{.*#}} ymm0 = ymm0[0,2,1,3]  
; CHECK-AVX512-NEXT: retq  
; CHECK-VBMI-LABEL: trunc_v32i16_v32i8_sign:  
; CHECK-VBMI:  
; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-VBMI-NEXT:    vpmovzxbw {{.*#+}} ymm1 = xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero
; CHECK-NEXT:    vpmovsxwq {{.*#+}} ymm2 = xmm2[0],zero,zero,xmm2[1],zero,zero,zero,xmm2[2],zero,zero,zero,xmm2[3],zero,zero,zero
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm2
; CHECK-NEXT:    vpshufd {{.*#+}} xmm3 = xmm1[2,3,0,1]
; CHECK-NEXT:    vpmovzxbw %xmm0, %ymm0
; CHECK-NEXT:    vpshufd {{.*#+}} ymm3 = ymm1[2,3,0,1]
; CHECK-NEXT:    vpmovsxwq {{.*#+}} ymm3 = xmm3[0],zero,zero,xmm3[1],zero,zero,zero,xmm3[2],zero,zero,zero,xmm3[3],zero,zero,zero
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm0 = xmm0[0],zero,zero,zero,xmm0[1],zero,zero,zero,xmm0[2],zero,zero,zero,xmm0[3],zero,zero,zero,xmm0[4],zero,zero,zero,xmm0[5],zero,zero,zero,xmm0[6],zero,zero,zero,xmm0[7],zero,zero,zero,xmm0[8],zero,zero,zero,xmm0[9],zero,zero,zero,xmm0[10],zero,zero,zero,xmm0[11],zero,zero,zero,xmm0[12],zero,zero,zero,xmm0[13],zero,zero,zero,xmm0[14],zero,zero,zero,xmm0[15],zero
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm1 = xmm1[0],zero,zero,zero,xmm1[1],zero,zero,zero,xmm1[2],zero,zero,zero,xmm1[3],zero,zero,zero
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
; CHECK-NEXT:    vpmovzxbw %xmm0, %ymm0
; CHECK-NEXT:    vpmovzxbw %xmm0, %ymm0
; CHECK-NEXT:    vpmovzxbw %xmm0, %ymm0
; CHECK-NEXT:    vpmovzxbw %xmm0, %ymm0
; CHECK-NEXT:    vpmovzxbw %xmm0, %ymm0
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
%a = zext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}

define void @zext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: zext_v16i8_v16i64:
; CHECK:    # %bb.0:
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm1 = xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm2 = xmm2[0],zero,zero,xmm2[1],zero,zero,zero,xmm2[2],zero,zero,zero,xmm2[3],zero,zero,zero
; CHECK-NEXT:    vextracti128 $1, %ymm1, %xmm2
; CHECK-NEXT:    vpshufd {{.*#+}} xmm3 = xmm1[2,3,0,1]
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm3 = xmm3[0],zero,zero,xmm3[1],zero,zero,zero,xmm3[2],zero,zero,zero,xmm3[3],zero,zero,zero
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm0 = xmm0[0],zero,zero,zero,xmm0[1],zero,zero,zero,xmm0[2],zero,zero,zero,xmm0[3],zero,zero,zero,xmm0[4],zero,zero,zero,xmm0[5],zero,zero,zero,xmm0[6],zero,zero,zero,xmm0[7],zero,zero,zero,xmm0[8],zero,zero,zero,xmm0[9],zero,zero,zero,xmm0[10],zero,zero,zero,xmm0[11],zero,zero,zero,xmm0[12],zero,zero,zero,xmm0[13],zero,zero,zero,xmm0[14],zero,zero,zero,xmm0[15],zero
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm1 = xmm1[0],zero,zero,zero,xmm1[1],zero,zero,zero,xmm1[2],zero,zero,zero,xmm1[3],zero,zero,zero
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
%a = zext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}

define void @sext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: sext_v16i8_v16i64:
; CHECK:    # %bb.0:
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm1 = xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm2 = xmm2[0],zero,zero,xmm2[1],zero,zero,zero,xmm2[2],zero,zero,zero,xmm2[3],zero,zero,zero
; CHECK-NEXT:    vextracti128 $1, %ymm1, %xmm2
; CHECK-NEXT:    vpshufd {{.*#+}} xmm3 = xmm1[2,3,0,1]
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm3 = xmm3[0],zero,zero,xmm3[1],zero,zero,zero,xmm3[2],zero,zero,zero,xmm3[3],zero,zero,zero
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm0 = xmm0[0],zero,zero,zero,xmm0[1],zero,zero,zero,xmm0[2],zero,zero,zero,xmm0[3],zero,zero,zero,xmm0[4],zero,zero,zero,xmm0[5],zero,zero,zero,xmm0[6],zero,zero,zero,xmm0[7],zero,zero,zero,xmm0[8],zero,zero,zero,xmm0[9],zero,zero,zero,xmm0[10],zero,zero,zero,xmm0[11],zero,zero,zero,xmm0[12],zero,zero,zero,xmm0[13],zero,zero,zero,xmm0[14],zero,zero,zero,xmm0[15],zero
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm1 = xmm1[0],zero,zero,zero,xmm1[1],zero,zero,zero,xmm1[2],zero,zero,zero,xmm1[3],zero,zero,zero
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
%a = zext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}
define void @vselect_split_v8i16_setcc(<8 x i16> %s, <8 x i16> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: vselect_split_v8i16_setcc:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vmovdqa (%rsi), %ymm2
    ; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm3
    ; CHECK-NEXT:    vpcmpeqw %xmm1, %xmm0, %k1
    ; CHECK-NEXT:    kshiftrb $4, %k1, %k2
    ; CHECK-NEXT:    vmovdqa64 32(%rdi), %ymm3 {%k2}
    ; CHECK-NEXT:    vmovdqa64 (%rdi), %ymm2 {%k1}
    ; CHECK-NEXT:    vmovdqa %ymm2, (%rdx)
    ; CHECK-NEXT:    vmovdqa %ymm3, 32(%rdx)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %a = load <8 x i64>, <8 x i64>* %p
    %y = load <8 x i64>, <8 x i64>* %q
    %a = icmp eq <8 x i16> %s, %t
    %b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
    store <8 x i64> %b, <8 x i64>* %r
    ret void
}

define void @vselect_split_v8i32_setcc(<8 x i32> %s, <8 x i32> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: vselect_split_v8i32_setcc:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vmovdqa (%rsi), %ymm2
    ; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm3
    ; CHECK-NEXT:    vpcmpeqd %ymm1, %ymm0, %k1
    ; CHECK-NEXT:    kshiftrb $4, %k1, %k2
    ; CHECK-NEXT:    vmovdqa64 32(%rdi), %ymm3 {%k2}
    ; CHECK-NEXT:    vmovdqa64 (%rdi), %ymm2 {%k1}
    ; CHECK-NEXT:    vmovdqa %ymm2, (%rdx)
    ; CHECK-NEXT:    vmovdqa %ymm3, 32(%rdx)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %x = load <8 x i64>, <8 x i64>* %p
    %y = load <8 x i64>, <8 x i64>* %q
    %a = icmp eq <8 x i32> %s, %t
    store <8 x i64> %b, <8 x i64>* %r
    ret void
}
; CHECK-NEXT:    vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
%a = icmp eq <8 x i32> %s, %t
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}

define void @vselect_split_v16i8_setcc(<16 x i8> %s, <16 x i8> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i8_setcc:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rsi), %ymm2
; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:    vpcmpeqb %xmm1, %xmm0, %k1
; CHECK-NEXT:    kshiftrw $8, %k1, %k2
; CHECK-NEXT:    vmovdqa32 32(%rdi), %ymm3 [%k2]
; CHECK-NEXT:    vmovdqa32 (%rdi), %ymm2 [%k1]
; CHECK-NEXT:    vmovdqa %ymm2, (%rdx)
; CHECK-NEXT:    vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
%x = load <16 x i32>, <16 x i32>* %p
%y = load <16 x i32>, <16 x i32>* %q
%a = icmp eq <16 x i8> %s, %t
%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
store <16 x i32> %b, <16 x i32>* %r
ret void
}

define void @vselect_split_v16i16_setcc(<16 x i16> %s, <16 x i16> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i16_setcc:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rsi), %ymm2
; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:    vpcmpeqw %ymm1, %ymm0, %k1
; CHECK-NEXT:    kshiftrw $8, %k1, %k2
; CHECK-NEXT:    vmovdqa32 32(%rdi), %ymm3 [%k2]
; CHECK-NEXT:    vmovdqa32 (%rdi), %ymm2 [%k1]
; CHECK-NEXT:    vmovdqa %ymm2, (%rdx)
; CHECK-NEXT:    vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
%x = load <16 x i32>, <16 x i32>* %p
%y = load <16 x i32>, <16 x i32>* %q
%a = icmp eq <16 x i16> %s, %t
%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
store <16 x i32> %b, <16 x i32>* %r
ret void
}

define <16 x i8> @trunc_packus_v16i32_v16i8(<16 x i32>* %p) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_packus_v16i32_v16i8:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:   vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT:   vpckusdw 32(%rdi), %ymm0, %ymm0
    ; CHECK-NEXT:   vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
    ; CHECK-NEXT:   vpmovuswb %ymm0, %xmm0
    ; CHECK-NEXT:   vzeroupper
    ; CHECK-NEXT:   retq
%a = load <16 x i32>, <16 x i32>* %p
%b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> %c, <16 x i32> czeroinitializer
%d = icmp sgt <16 x i32> %c, czeroinitializer
%e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> czeroinitializer
%f = trunc <16 x i32> %e to <16 x i8>
ret <16 x i8> %f
}

define void @trunc_packus_v16i32_v16i8_store(<16 x i32>* %p, <16 x i8>* %q) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_packus_v16i32_v16i8_store:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:   vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT:   vpckusdw 32(%rdi), %ymm0, %ymm0
    ; CHECK-NEXT:   vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
    ; CHECK-NEXT:   vpmovuswb %ymm0, (%rsi)
    ; CHECK-NEXT:   vzeroupper
    ; CHECK-NEXT:   retq
%a = load <16 x i32>, <16 x i32>* %p
%b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> %c, <16 x i32> czeroinitializer
%d = icmp sgt <16 x i32> %c, czeroinitializer
%e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> czeroinitializer
%f = trunc <16 x i32> %e to <16 x i8>
store <16 x i8> %f, <16 x i8>* %q
ret void
}
define <64 x i1> @v64i1_argument_return(<64 x i1> %x) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: v64i1_argument_return:
  ; CHECK:      # %bb.0: # %entry
  ; CHECK-NEXT: retq
  ret <64 x i1> %x
}

define void @v64i1_shuffle(<64 x i8>* %x, <64 x i8>* %y) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: v64i1_shuffle:
  ; CHECK:      # %bb.0: # %entry
  ; CHECK-NEXT: vmovdqa (%rdi), %ymm1
  ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm0
  ; CHECK-NEXT: vptestnmb %ymm1, %ymm1, %k0
  ; CHECK-NEXT: kshiftrd $1, %k0, %k1
  ; CHECK-NEXT: movq $-3, %rax
  ; CHECK-NEXT: kmovq %rax, %k2
  ; CHECK-NEXT: kandq %k2, %k1, %k1
  ; CHECK-NEXT: kshiflq $63, %k0, %k2
  ; CHECK-NEXT: kshifr $62, %k2, %k2
  ; CHECK-NEXT: korr %k2, %k1, %k1
  ; CHECK-NEXT: movq $-5, %rax
  ; CHECK-NEXT: kmovq %rax, %k2
  ; CHECK-NEXT: kandq %k2, %k1, %k1
  ; CHECK-NEXT: kshiftrd $3, %k0, %k2
  ; CHECK-NEXT: kshiftlq $63, %k2, %k2
  ; CHECK-NEXT: kshifrq $61, %k2, %k2
  ; CHECK-NEXT: korr %k2, %k1, %k1
  ; CHECK-NEXT: movq $-9, %rax
  ; CHECK-NEXT: kmovq %rax, %k2
  ; CHECK-NEXT: kandq %k2, %k1, %k1
  ; CHECK-NEXT: kshiftrd $2, %k0, %k2
  ; CHECK-NEXT: kshiftlq $63, %k2, %k2
  ; CHECK-NEXT: kshifrq $60, %k2, %k2
  ; CHECK-NEXT: korr %k2, %k1, %k1
  ; CHECK-NEXT: movq $-17, %rax
  ; CHECK-NEXT: kmovq %rax, %k2
  ; CHECK-NEXT: kandq %k2, %k1, %k1
  ; CHECK-NEXT: kshiftrd $5, %k0, %k2
  ; CHECK-NEXT: kshiftlq $63, %k2, %k2
  ; CHECK-NEXT: kshifrq $59, %k2, %k2
  ; CHECK-NEXT: korr %k2, %k1, %k1
  ; CHECK-NEXT: movq $-33, %rax
  ; CHECK-NEXT: kmovq %rax, %k2
  ; CHECK-NEXT: kandq %k2, %k1, %k1
  ; CHECK-NEXT: kshiftrd $4, %k0, %k2
  ; CHECK-NEXT: kshiftlq $63, %k2, %k2
  ; CHECK-NEXT: kshifrq $58, %k2, %k2

; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-65, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $7, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $57, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-129, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $6, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $56, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-257, %rax # imm = 0xFEFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $9, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $55, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-513, %rax # imm = 0xFDFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $8, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $54, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-1025, %rax # imm = 0xFBFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $11, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $53, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-2049, %rax # imm = 0xF7FF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $10, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $52, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-4097, %rax # imm = 0xEFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $13, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $51, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-8193, %rax # imm = 0xDFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $12, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq %k2, %k1, %k1
; CHECK-NEXT:  movq $-16385, %rax # imm = 0xBFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd %15, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq %k2, %k1, %k1
; CHECK-NEXT:  movq $-32769, %rax # imm = 0xFFFF7FFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $14, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $49, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-65537, %rax # imm = 0xFFFEFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $17, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $47, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-131073, %rax # imm = 0xFFFFDFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $16, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $46, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-262145, %rax # imm = 0xFFFBBBBF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $19, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $45, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-524289, %rax # imm = 0xFFFF7FFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $18, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $44, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-1048577, %rax # imm = 0xFFEFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $21, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $43, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-2097153, %rax # imm = 0xFFDFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $20, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $42, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-4194305, %rax # imm = 0xFFFBBBBF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $23, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $41, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-8388609, %rax # imm = 0xFF7FFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $22, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $40, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-16777217, %rax # imm = 0xFEFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $25, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $39, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-33554433, %rax # imm = 0xFDFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $24, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $38, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-67108865, %rax # imm = 0xFBFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1

; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrq %63, %k1, %k2
; CHECK-NEXT:  kshiftrq $30, %k2, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-1719869185, %rax # imm = 0xFFFFFFFFF8FFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $3, %k1, %k2
; CHECK-NEXT:  kshiftrq $63, %k2, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-34359738369, %rax # imm = 0xFFFFFFFFF7FFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $2, %k1, %k2
; CHECK-NEXT:  kshiftrq $63, %k2, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-68719476737, %rax # imm = 0xFFFFFFFFF6FFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $5, %k1, %k2
; CHECK-NEXT:  kshiftrq $63, %k2, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-137438953473, %rax # imm = 0xFFFFFFFFF5FFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $4, %k1, %k2
; CHECK-NEXT:  kshiftrq $63, %k2, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-274877906945, %rax # imm = 0xFFFFFFFFF4FFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $7, %k1, %k2
; CHECK-NEXT:  kshiftrq $63, %k2, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-549755813889, %rax # imm = 0xFFFFFFFFF3FFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $6, %k1, %k2
; CHECK-NEXT:  kshiftrq $63, %k2, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-1099511627777, %rax # imm = 0xFFFFFFFFF2FFFFFFF

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entry:
  %a = load <64 x i8>, <64 x i8>* %x
  %b = icmp eq <64 x i8> %a, zeroinitializer
  %shuf = shufflevector <64 x i1> %b, <64 x i1> undef, <64 x i32> <i32 1, i32 0, i32 2, i32 3, i32 2, i32 5, i32 4, i32 7, i32 6, i32 9, i32 8, i32 11, i32 10, i32 13, i32 12, i32 15, i32 14, i32 17, i32 16, i32 19, i32 18, i32 21, i32 20, i32 23, i32 22, i32 25, i32 24, i32 27, i32 26, i32 29, i32 28, i32 31, i32 30, i32 33, i32 32, i32 35, i32 34, i32 37, i32 36, i32 39, i32 38, i32 41, i32 40, i32 43, i32 42, i32 45, i32 44, i32 47, i32 46, i32 49, i32 48, i32 51, i32 50, i32 53, i32 52, i32 55, i32 54, i32 57, i32 56, i32 59, i32 58, i32 61, i32 60, i32 63, i32 62>
call void @llvm.masked.store.v64i8.p0v64i8(<64 x i8> %a, <64 x i8>* %y, i32 1, <64 x i1> %shuf)
ret void
}
declare void @llvm.masked.store.v64i8.p0v64i8(<64 x i8>, <64 x i8>*, i32, <64 x i1>)

@mem64_dst = global i64 0, align 8
@mem64_src = global i64 0, align 8
define i32 @v64i1_inline_asm() "min-legal-vector-width"="256" {
    ; CHECK-LABEL: v64i1_inline_asm:
    ; CHECK:      # %bb.0:
    ; CHECK-NEXT: kmovq [{.}](%rip), %k0
    ; CHECK-NEXT: #APP
    ; CHECK-NEXT: #NO_APP
    ; CHECK-NEXT: kmovq %k0, [{.}](%rip)
    ; CHECK-NEXT: movl -{[0-9]+}(%rsp), %eax

define void @cmp_v8i64_sext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: cmp_v8i64_sext:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa (%rsi), %ymm0
  ; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm1
  ; CHECK-NEXT:  vpcmpgtq 32(%rdi), %ymm1, %ymm1
  ; CHECK-NEXT:  vpcmpgtq (%rdi), %ymm0, %ymm0
  ; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
  ; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  %x = load <8 x i64>, <8 x i64>* %xptr
  %y = load <8 x i64>, <8 x i64>* %yptr
  %cmp = icmp slt <8 x i64> %x, %y
  %ext = sext <8 x i1> %cmp to <8 x i64>
  store <8 x i64> %ext, <8 x i64>* %zptr
  ret void
}

define void @cmp_v8i64_zext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: cmp_v8i64_zext:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa (%rsi), %ymm0
  ; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm1
  ; CHECK-NEXT:  vpcmpgtq 32(%rdi), %ymm1, %ymm1
  ; CHECK-NEXT:  vpcmpgtq (%rdi), %ymm0, %ymm0
  ; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
  ; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  %x = load <8 x i64>, <8 x i64>* %xptr
  %y = load <8 x i64>, <8 x i64>* %yptr
  %cmp = icmp slt <8 x i64> %x, %y
  %ext = zext <8 x i1> %cmp to <8 x i64>
  store <8 x i64> %ext, <8 x i64>* %zptr
  ret void
}
ret void
}

define <16 x i8> @var_rotate_v16i8(<16 x i8> %a, <16 x i8> %b) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: var_rotate_v16i8:
; CHECK:     # %bb.0:
; CHECK-NEXT: vmovdqa {{.*#+}} xmm2 = [8,8,8,8,8,8,8,8,8,8,8,8,8,8,8,8]
; CHECK-NEXT: vpsubb %xmm1, %xmm2, %xmm2
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm1 =
                xmm1[0],zero,xmm1[1],zero,xmm1[2],zero,xmm1[3],zero,xmm1[4],zero,xmm1[5],zero,xmm1[6],zero,xmm1[7],zero,
                xmm1[8],zero,xmm1[9],zero,xmm1[10],zero,xmm1[11],zero,xmm1[12],zero,xmm1[13],zero,xmm1[14],zero,xmm1[15],zero
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm0 =
                xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,
                xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero
; CHECK-NEXT: vpsllvw %ymm1, %ymm0, %ymm1
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm2 =
                xmm2[0],zero,xmm2[1],zero,xmm2[2],zero,xmm2[3],zero,xmm2[4],zero,xmm2[5],zero,xmm2[6],zero,xmm2[7],zero,
                xmm2[8],zero,xmm2[9],zero,xmm2[10],zero,xmm2[11],zero,xmm2[12],zero,xmm2[13],zero,xmm2[14],zero,xmm2[15],zero
; CHECK-NEXT: vpsrlw %ymm2, %ymm0, %ymm0
; CHECK-NEXT: vpor %ymm0, %ymm1, %ymm0
; CHECK-NEXT: vpmovw %ymm0, %xmm0
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
  %b8 = sub <16 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %b
  %shl = shl <16 x i8> %a, %b
  %lshr = lshr <16 x i8> %a, %b8
  %or = or <16 x i8> %shl, %lshr
ret <16 x i8> %or
}

define <32 x i8> @var_rotate_v32i8(<32 x i8> %a, <32 x i8> %b) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: var_rotate_v32i8:
; CHECK:     # %bb.0:
; CHECK-NEXT: vpsllw $4, %ymm0, %ymm2
; CHECK-NEXT: vpsrlw $4, %ymm0, %ymm3
; CHECK-NEXT: vpternlogq $216, {{.*}}(%rip), %ymm2, %ymm3
; CHECK-NEXT: vpsllw $5, %ymm1, %ymm1
; CHECK-NEXT: vpsllw $2, %ymm0, %ymm2
; CHECK-NEXT: vpsrlw $6, %ymm0, %ymm3
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm0 =
                xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,
                xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm2 =
                xmm2[0],zero,xmm2[1],zero,xmm2[2],zero,xmm2[3],zero,xmm2[4],zero,xmm2[5],zero,xmm2[6],zero,xmm2[7],zero,
                xmm2[8],zero,xmm2[9],zero,xmm2[10],zero,xmm2[11],zero,xmm2[12],zero,xmm2[13],zero,xmm2[14],zero,xmm2[15],zero
; CHECK-NEXT: vpsllw $4, %ymm2, %ymm0, %ymm2
; CHECK-NEXT: vpsllw $4, %ymm0, %ymm3
; CHECK-NEXT: vpsrlw $4, %ymm0, %ymm3
; CHECK-NEXT: vpsllw $5, %ymm1, %ymm1
; CHECK-NEXT: vpsllw $2, %ymm0, %ymm2
; CHECK-NEXT: vpsrlw $6, %ymm0, %ymm3
; CHECK-NEXT: vpternlogq $216, {{.*}}(%rip), %ymm2, %ymm3
; CHECK-NEXT: vpsrlw $7, %ymm0, %ymm2
; CHECK-NEXT: vpaddd %ymm1, %ymm0, %ymm2

; CHECK-NEXT:  vpternlogq $248, {{.*}}(%rip), %ymm2, %ymm3
; CHECK-NEXT:  vpaddb %ymm1, %ymm1, %ymm1
; CHECK-NEXT:  vblendvb %ymm1, %ymm3, %ymm0, %ymm0
; CHECK-NEXT:  retq
%b8 = sub <32 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %b
%shl = shl <32 x i8> %a, %b
%lsr = lshr <32 x i8> %a, %b8
%or = or <32 x i8> %shl, %lsr
ret <32 x i8> %or
}
define <32 x i8> @splatvar_rotate_v32i8(<32 x i8> %a, <32 x i8> %b) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: splatvar_rotate_v32i8:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vbroadcastb %xmm1, %xmm1
; CHECK-NEXT:  vpand {{.*}}(%rip), %xmm1, %xmm1
; CHECK-NEXT:  vmovzxbq {{.*#+}} xmm2 =
        xmm1[0],zero,zero,zero,zero,zero,zero,zero,xmm1[1],zero,zero,zero,zero,zero,zero,zero
; CHECK-NEXT:  vpsllw %xmm2, %ymm0, %ymm3
; CHECK-NEXT:  vmovdqa {{.*#+}} xmm4 = [8,8,8,8,8,8,8,8,8,8,8,8,8,8,8,8]
; CHECK-NEXT:  vpsubb %xmm1, %xmm4, %xmm1
; CHECK-NEXT:  vcmppeqd %xmm4, %xmm4, %xmm4
; CHECK-NEXT:  vpsllw %xmm2, %xmm4, %xmm2
; CHECK-NEXT:  vbroadcastb %xmm2, %ymm2
; CHECK-NEXT:  vmovzxbq {{.*#+}} xmm1 =
        xmm1[0],zero,zero,zero,zero,zero,zero,zero,xmm1[1],zero,zero,zero,zero,zero,zero,zero
; CHECK-NEXT:  vpsrlw %ymm1, %ymm0, %ymm5
; CHECK-NEXT:  vpand %ymm2, %ymm3, %ymm2
; CHECK-NEXT:  vpsrlw %ymm1, %xmm4, %xmm0
; CHECK-NEXT:  vpsrlw $8, %xmm0, %xmm0
; CHECK-NEXT:  vbroadcastb %ymm0, %ymm0
; CHECK-NEXT:  vpternlogq $236, %ymm5, %ymm2, %ymm0
; CHECK-NEXT:  retq
%ssplat = shufflevector <32 x i8> %b, <32 x i8> undef, <32 x i32> zeroinitializer
%ssplat8 = sub <32 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %ssplat
%shl = shl <32 x i8> %a, %ssplat
%lsr = lshr <32 x i8> %a, %ssplat8
%or = or <32 x i8> %shl, %lsr
ret <32 x i8> %or
}
define <32 x i8> @constant_rotate_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: constant_rotate_v32i8:
; CHECK-AVX512:  # %bb.0:
; CHECK-AVX512-NEXT:  vpsllw $4, %ymm0, %ymm1

%rmask = and <32 x i8> %lshr, <i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55>

%lmask = and <32 x i8> %shl, <i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33>

%or = or <32 x i8> %lmask, %rmask

ret <32 x i8> %or

; RUN: llvm -O3 -mtriple=powerpc-unknown-linux-gnu -mcpu=e500 -mattr=spec | FileCheck %s

; PowerPC SPE is a rare in-tree target that has the FP_TO_SINT node marked
; as Legal.

; Verify that fptosi(42.1) isn't simplified when the rounding mode is
; unknown.
; Verify that no gross errors happen.
; CHECK-LABEL: @f20
; COMMON: cfdsctsiz
define i32 @f20(double %a) strictfp {
entry:
%result = call i32 @llvm.experimental.constrained.fptosi.i32.f64(double 42.1,
    metadata !"fpexcept.strict")
strictfp
ret i32 %result
}

@llvm.fp.env = thread_local global i8 zeroinitializer, section "llvm.metadata"
declare i32 @llvm.experimental.constrained.fptosi.i32.f64(double, metadata)

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s
; D31946
; Check that we dont end up with the "LLVM ERROR: Cannot select" error.
; Additionally ensure that the output code actually put fp128 values in SSE registers.

declare fp128 @llvm.fabs.f128(fp128)
declare fp128 @llvm.copysign.f128(fp128)

define fp128 @TestSelect(fp128 %a, fp128 %b) {
; CHECK-LABEL: TestSelect:
; CHECK:    # %bb.0:
; CHECK-NEXT:    pushq %rbx
; CHECK-NEXT:    .cfi_def_cfa offset 16
; CHECK-NEXT:    subq $32, %rsp
; CHECK-NEXT:    .cfi_def_cfa_offset 48
; CHECK-NEXT:    .cfi_offset %rbx, -16
; CHECK-NEXT:    movaps %xmm1, [{-[0-9]+}][%r{[sb]}]p) # 16-byte Spill
; CHECK-NEXT:    movaps %xmm0, (%rsp) # 16-byte Spill
; CHECK-NEXT:    callq __gttf2
; CHECK-NEXT:    movl %eax, %ebx
; CHECK-NEXT:    movaps (%rsp), %xmm0 # 16-byte Reload
; CHECK-NEXT:    movaps [{-[0-9]+}][%r{[sb]}]p, %xmm1 # 16-byte Reload
; CHECK-NEXT:    callq __subtf3
; CHECK-NEXT:    testl %ebx, %ebx
; CHECK-NEXT:    jg .LBB0_2
; CHECK-NEXT:  # %bb.1:

; CHECK-NEXT:  ; CHECK-NEXT:  ...
define fp128 @TestFabs(fp128 %a) {
  ; CHECK-LABEL: TestFabs:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:   andps {{.*}}(%rip), %xmm0
  ; CHECK-NEXT:   retq
  %res = call fp128 @llvm.fabs.f128(fp128 %a)
  ret fp128 %res
}

define fp128 @TestCopysign(fp128 %a, fp128 %b) {
  ; CHECK-LABEL: TestCopysign:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:   andps {{.*}}(%rip), %xmm1
  ; CHECK-NEXT:   andps {{.*}}(%rip), %xmm0
  ; CHECK-NEXT:   orps %xmm1, %xmm0
  ; CHECK-NEXT:   retq
  %res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
  ret fp128 %res
}

define fp128 @TestFneg(fp128 %a) {
  ; CHECK-LABEL: TestFneg:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:   pushq %rax
  ; CHECK-NEXT:   .cfi_def_cfa_offset 16
  ; CHECK-NEXT:   movaps %xmm0, %xmm1
  ; CHECK-NEXT:   callq __multf3
  ; CHECK-NEXT:   xorps {{.*}}(%rip), %xmm0
  ; CHECK-NEXT:   popq %rax
  ; CHECK-NEXT:   .cfi_def_cfa_offset 8
  ; CHECK-NEXT:   retq
  %mul = fmul fp128 %a, %a
  %res = fsub fp128 0xL00000000000000000000000000000000, %mul
  ret fp128 %res
}
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A shuffle mask with all undef elements is always legal.

```assembly
define <4 x i32> @PR41535(<2 x i32> %p1, <2 x i32> %p2) {
; CHECK-LABEL: PR41535:
; CHECK:    // %bb.0:
; CHECK-NEXT:  ext v0.8b, v0.8b, v1.8b, #4
; CHECK-NEXT:  mov v0.d[1], v0.d[0]
; CHECK-NEXT:  ret
%cat1 = shufflevector <2 x i32> %p1, <2 x i32> undef, <4 x i32> undef, i32 undef, i32 1, i32 undef, i32 undef
%cat2 = shufflevector <2 x i32> %p2, <2 x i32> undef, <4 x i32> <i32 0, i32 undef, i32 undef, i32 undef>
%r = shufflevector <4 x i32> %cat1, <4 x i32> %cat2, <4 x i32> <i32 undef, i32 undef, i32 1, i32 4>
ret <4 x i32> %r
}
```

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 */

; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s

define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
; CHECK-LABEL: test_sitofp_fixed:

; First, extend each i32 to i64
; CHECK-DAG: sshll2.2d [[BLOCK0_HI:v[0-9]+]], v0, #0
; CHECK-DAG: sshll2.2d [[BLOCK1_HI:v[0-9]+]], v1, #0
; CHECK-DAG: sshll2.2d [[BLOCK2_HI:v[0-9]+]], v2, #0
; CHECK-DAG: sshll.2d [[BLOCK0_LO:v[0-9]+]], v0, #0
; CHECK-DAG: sshll.2d [[BLOCK1_LO:v[0-9]+]], v1, #0
; CHECK-DAG: sshll.2d [[BLOCK2_LO:v[0-9]+]], v2, #0
; CHECK-DAG: sshll.2d [[BLOCK3_LO:v[0-9]+]], v3, #0

; Next, convert each to double.
; CHECK-DAG: scvtf.2d v0, [[BLOCK0_LO]]
; CHECK-DAG: scvtf.2d v1, [[BLOCK0_HI]]
; CHECK-DAG: scvtf.2d v2, [[BLOCK1_LO]]
; CHECK-DAG: scvtf.2d v3, [[BLOCK1_HI]]
; CHECK-DAG: scvtf.2d v4, [[BLOCK2_LO]]
; CHECK-DAG: scvtf.2d v5, [[BLOCK2_HI]]
; CHECK-DAG: scvtf.2d v6, [[BLOCK3_LO]]
; CHECK-DAG: scvtf.2d v7, [[BLOCK3_HI]]

; CHECK: ret
%flt = sitofp <16 x i32> %in to <16 x double>
%res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0>
ret <16 x double> %res
}

; This one is small enough to satisfy isSimple, but still illegally large.
define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
; CHECK-LABEL: test_sitofp_fixed_shortish:

; CHECK-DAG: scvtf.2d v0, v0
; CHECK-DAG: scvtf.2d v1, v1

; CHECK: ret
%flt = sitofp <4 x i64> %in to <4 x double>
%res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
ret <4 x double> %res
}

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NOTE: Assertions have been autogenerate by utils/update_test_checks.py UTC_ARGS: --function-signature --scrub-attributes

RUN: opt -S -argpromotion < %s | FileCheck %s
RUN: opt -S - passes=argpromotion < %s | FileCheck %s

Test that we only promote arguments when the caller/callee have compatible function attributes.

target triple = "x86_64-unknown-linux-gnu"

define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
    ; CHECK-LABEL: define {{[^\^]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
    CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
    CHECK-NEXT: bb:
    CHECK-NEXT: store <8 x i64>, <8 x i64>* %arg1
    CHECK-NEXT: ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
    ; CHECK-LABEL: define {{[^\^]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
    CHECK-SAME: (<8 x i64>* [[ARG1:%.*]], <8 x i64> [[ARG]])
    CHECK-NEXT: bb:
    CHECK-NEXT: %tmp = load <8 x i64>, <8 x i64>* %arg
    CHECK-NEXT: store <8 x i64> %tmp, <8 x i64>* %arg
    CHECK-NEXT: ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
    ; CHECK-LABEL: define {{[^\^]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
    CHECK-SAME: (<8 x i64>* [[ARG1:%.*]], <8 x i64> [[ARG]])
    CHECK-NEXT: bb:
    CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
    CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
    CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
    CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
    CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
    ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: store <8 x i64> %tmp, <8 x i64>* %arg
    ; CHECK-NEXT: ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
    ; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
    ; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
    ; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    ; CHECK-NEXT: %tmp4 = load <8 x i64>, <8 x i64>* %tmp4, align 32
    ; CHECK-NEXT: store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ; CHECK-NEXT: ret void
};

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp4, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
    ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512/legal512_prefer512
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: store <8 x i64> %tmp, <8 x i64>* %arg
    ; CHECK-NEXT: ret void
};

bb:
%tmp = load <8 x i64>, <8 x i64>* %arg
store <8 x i64> %tmp, <8 x i64>* %arg
ret void

; This should promote
define void @avx512/legal512_prefer256_call_avx512/legal512_prefer256(<8 x i64>* %arg) #1 {
    ; CHECK-LABEL: define {{[^@]+}}@avx512/legal512_prefer256_call_avx512/legal512_prefer256
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
    ; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
    ; CHECK-NEXT: call fastcc void @callee_avx512/legal512_prefer256_call_avx512/legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    ; CHECK-NEXT: %tmp4 = load <8 x i64>, <8 x i64>* %tmp4, align 32
    ; CHECK-NEXT: store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ; CHECK-NEXT: ret void
};

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
    ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
    ; CHECK-NEXT: ret void
    ;
    bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
    ; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
    ; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
    ; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
    ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
    ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
    ; CHECK-NEXT: ret void
    ;
    bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #0 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
}

bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
}

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256 
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]]) 
; CHECK-NEXT: bb: 
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]] 
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]] 
; CHECK-NEXT: ret void 
; 
bb: 
%tmp = load <8 x i64>, <8 x i64>* %arg 
store <8 x i64> %tmp, <8 x i64>* %arg 
ret void 
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 
; CHECK-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256 
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]]) 
; CHECK-NEXT: bb: 
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32 
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32 
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8* 
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false) 
; CHECK-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]]) 
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32 
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2 
; CHECK-NEXT: ret void 
; 
bb: 
%tmp = alloca <8 x i64>, align 32 
%tmp2 = alloca <8 x i64>, align 32 
%tmp3 = bitcast <8 x i64>* %tmp to i8* 
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false) 
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp) 
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32 
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2 
ret void 
}

; This should not promote 
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256 
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]]) 
; CHECK-NEXT: bb: 
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]] 
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
  bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #3 {
  bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}
define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(8 x i64)* %arg) #4 {
  ; CHECK-LABEL: define (\^[@\+\{\}\+\}]+) @avx2_legal256_prefer256_call_avx2_legal512_prefer256
  ; CHECK-SAME: (8 x i64)* [[ARG:.*]]
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP2:.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP3:.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, 64 32, i1 false)
  ; CHECK-NEXT: [[TMP_VAL:.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
  ; CHECK-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP_VAL]])
  ; CHECK-NEXT: [[TMP4:.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; CHECK-NEXT: ret void
}

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, 64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal512_prefer256(8 x i64)* %arg, <8 x i64>* readonly %arg1) #4 {
  ; CHECK-LABEL: define (\^[@\+\{\}\+\}]+) @callee_avx2_legal512_prefer256_call_avx2_legal512_prefer256
  ; CHECK-SAME: (8 x i64)* [[ARG:.*]], <8 x i64>* [[ARG1.VAL:.*]]
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: store <8 x i64> [[ARG1.VAL]], <8 x i64>* [[ARG]]
  ; CHECK-NEXT: ret void
  ;
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal512_prefer256(8 x i64)* %arg) #3 {
  ; CHECK-LABEL: define (\^[@\+\{\}\+\}]+) @avx2_legal512_prefer256_call_avx2_legal512_prefer256
  ; CHECK-SAME: (8 x i64)* [[ARG:.*]]
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:.*]] = alloca <8 x i64>, align 32
define i32 @scalar_call_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %X, i32* %Y) #2 {
    %A = load i32, i32* %X
    %B = load i32, i32* %Y
    %C = add i32 %A, %B
    ret i32 %C
}

define i32 @scalar_avx512_legal256_prefer256(i32* %B) #2 {
    %A = alloca i32
    %A = store i32 1, i32* %A
    %A = load i32, i32* %A
    ret i32 %A
}

; If the arguments are scalar, it's ok to promote.
define internal i32 @scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %X, i32* %Y) #2 {
    %A = load i32, i32* %X
    %B = load i32, i32* %Y
    %C = add i32 %A, %B
    ret i32 %C
}
%A = alloca i32
store i32 1, i32* %A
%C = call i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32* %A, i32* %B)
ret i32 %C
}

; If the arguments are scalar, its ok to promote.
define internal i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %X, i32* %Y) #2 {
    %A = load i32, i32* %X
    %B = load i32, i32* %Y
    %C = add i32 %A, %B
    ret i32 %C
}
define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %B) #2 {
    %A = alloca i32
    store i32 1, i32* %A
    %C = call i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32* %A, i32* %B)
    ret i32 %C
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = [ inlinehint norecourse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" ]
attributes #1 = [ inlinehint norecourse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" ]
attributes #2 = [ inlinehint norecourse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" ]
attributes #3 = [ inlinehint norecourse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" ]
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; RUN: llc -march=hexagon < %s
; REQUIRES: asserts

; The two loads based on %struct.0, loading two different data types
; cause LSR to assume type "void" for the memory type. This would then
; cause an assert in isLegalAddressingMode. Make sure we no longer crash.

target triple = "hexagon"

%struct.0 = type { i8*, i8, %union.anon.0 }
%union.anon.0 = type { i8* }

define hidden fastcc void @fred() unnamed_addr #0 {
  entry:
     br i1 undef, label %while.end, label %while.body.lr.ph

while.body.lr.ph:
  ; preds = %entry
  br label %while.body

while.body:
  ; preds = %exit.2, %while.body.lr.ph
  %lsr.iv = phi %struct.0* [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
  switch i32 undef, label %exit [ i32 1, label %sw.bb.i
  i32 2, label %sw.bb3.i
  ]

sw.bb.i:
  ; preds = %while.body
  unreachable

sw.bb3.i:
  ; preds = %while.body
  unreachable

exit:
  ; preds = %while.body
  switch i32 undef, label %exit.2 [ i32 1, label %sw.bb.i17
  i32 2, label %sw.bb3.i20
  ]

sw.bb.i17:
  ; preds = %exit
  %0 = bitcast %struct.0* %lsr.iv to i32*
  %1 = load i32, i32* %0, align 4
  unreachable

sw.bb3.i20:
  ; preds = %exit
  %2 = bitcast %struct.0* %lsr.iv to i8**
  %3 = load i8*, i8** %2, align 4
  unreachable
exit.2:                        ; preds = %exit
%cgep22 = getelementptr %struct.0, %struct.0* %lsr.iv, i32 1
br label %while.body

while.end:                     ; preds = %entry
  ret void
}

attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }

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define void @foo_i8() {
  entry:
  %0 = load volatile i8, i8* inttoptr (i32 805874688 to i8*)
  %1 = load volatile i8, i8* inttoptr (i32 805874692 to i8*)
  %2 = load volatile i8, i8* inttoptr (i32 805874719 to i8*)
  %3 = load volatile i8, i8* inttoptr (i32 805874720 to i8*)
  %4 = load volatile i8, i8* inttoptr (i32 805874727 to i8*)
  store i8 %4, i8* inttoptr(i32 805873688 to i8*)
  store i8 %3, i8* inttoptr(i32 805873719 to i8*)
  store i8 %2, i8* inttoptr(i32 805873720 to i8*)
  store i8 %1, i8* inttoptr(i32 805873727 to i8*)
  store i8* inttoptr(i32 805874800 to i8*), i8** @goo
  ret void
}

define void @foo_i16() {
  entry:
  %1 = load volatile i8, i8* inttoptr (i32 805874688 to i8*)
  %2 = load volatile i8, i8* inttoptr (i32 805874692 to i8*)
  %3 = load volatile i8, i8* inttoptr (i32 805874719 to i8*)
  %4 = load volatile i8, i8* inttoptr (i32 805874720 to i8*)
  %5 = load volatile i8, i8* inttoptr (i32 805874727 to i8*)
  store i8 %5, i8* inttoptr(i32 805873688 to i8*)
  store i8 %4, i8* inttoptr(i32 805873688 to i8*)
  store i8 %3, i8* inttoptr(i32 805873719 to i8*)
  store i8 %2, i8* inttoptr(i32 805873720 to i8*)
  store i8 %1, i8* inttoptr(i32 805873727 to i8*)
  store i8* inttoptr(i32 805874800 to i8*), i8** @goo
  ret void
}

; Check that for i16 type, the maximum legal offset is 62.
; CHECK: foo_i16
; CHECK-DAG: %[[C1:const[0-9]??]] = bitcast i32 805874752 to i32
; CHECK-DAG: %[[C2:const[0-9]??]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i16*
; CHECK-NEXT: %1 = load volatile i16, i16* %0, align 2
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i16*
; CHECK-NEXT: %3 = load volatile i16, i16* %2, align 2
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i16*
; CHECK-NEXT: %5 = load volatile i16, i16* %4, align 2
; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to i16*
; CHECK-NEXT: %7 = load volatile i16, i16* %6, align 2
; CHECK-NEXT: %8 = inttoptr i32 %[[C1]] to i16*
; CHECK-NEXT: %9 = load volatile i16, i16* %8, align 2
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i16*
; CHECK-NEXT: %11 = load volatile i16, i16* %10, align 2

define void @foo_i16() {
  entry:
  %0 = load volatile i16, i16* inttoptr (i32 805874688 to i16*), align 2
  %1 = load volatile i16, i16* inttoptr (i32 805874692 to i16*), align 2
  %2 = load volatile i16, i16* inttoptr (i32 805874720 to i16*), align 2
  %3 = load volatile i16, i16* inttoptr (i32 805874750 to i16*), align 2
  %4 = load volatile i16, i16* inttoptr (i32 805874752 to i16*), align 2
  %5 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
  ret void
}

; Check that for i32 type, the maximum legal offset is 124.
; CHECK: foo_i32
; CHECK-DAG: %[[C1:const[0-9]??]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]??]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i32*
; CHECK-NEXT: %1 = load volatile i32, i32* %0, align 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i32*
; CHECK-NEXT: %3 = load volatile i32, i32* %2, align 4
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i32*
; CHECK-NEXT: %5 = load volatile i32, i32* %4, align 4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i32*
; CHECK-NEXT: %7 = load volatile i32, i32* %6, align 4
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i32*
; CHECK-NEXT: %9 = load volatile i32, i32* %8, align 4
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i32*
; CHECK-NEXT: %11 = load volatile i32, i32* %10, align 4
define void @foo_i32() {
  entry:
  %0 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 4
  %1 = load volatile i32, i32* inttoptr (i32 805874692 to i32*), align 4
  %2 = load volatile i32, i32* inttoptr (i32 805874812 to i32*), align 4
  %3 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
  %4 = load volatile i32, i32* inttoptr (i32 805874824 to i32*), align 4
  %5 = load volatile i32, i32* inttoptr (i32 805874828 to i32*), align 4
  ret void
}

1.6 find-and-replace-dom-text 0.4.3
1.6.1 Available under license:

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* @projectDescription Advanced and extensible data dumping for Javascript.
* @version 1.0.0
* @author Ariel Flesler
* @link {http://flesler.blogspot.com/2008/05/jsdump-pretty-dump-of-any-javascript.html}
* /
/**

* Javascript Diff Algorithm
* By John Resig (http://ejohn.org/)
* Modified by Chu Alan "sprite"
* 
* Released under the MIT license.
*
* More Info:
* http://ejohn.org/projects/javascript-diff-algorithm/
*
* Usage: QUnit.diff(expected, actual)
*
* QUnit.diff("the quick brown fox jumped over", "the quick fox jumps over") == "the  quick <del>brown </del> fox <del>jumped </del><ins>jumps </ins> over"
* /

Found in path(s):
* /opt/ws_local/PERMITS_SQL/1068888556_1594467755.19/0/findandreplacedomtext-4bc72dfb84c456739495e6e20532bd8d9250315-zip/findAndReplaceDOMText-4bc72dfb84c456739495e6e20532bd8d9250315/test/qunit.js

1.7 readable-stream 1.1.14
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1.8 setprototypeof 1.1.1

1.9 har-validator 5.1.5
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1.10 triple-beam 1.3.0
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1.11 ncp 0.5.1

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1.12 ms 2.1.2

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1.13 opus 1.1.2

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1.28 has-unicode 2.0.1

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1.33 pac-proxy-agent 4.1.0
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pac-proxy-agent

==============
### A [PAC file][pac-wikipedia] proxy `http.Agent` implementation for HTTP and HTTPS
[![Build Status](https://github.com/TooTallNate/node-pac-proxy-agent/workflows/Node%20CI/badge.svg)](https://github.com/TooTallNate/node-pac-proxy-agent/actions?workflow=Node+CI)

This module provides an `http.Agent` implementation that retrieves the specified [PAC proxy file][pac-wikipedia] and uses it to resolve which HTTP, HTTPS, or SOCKS proxy, or if a direct connection should be used to connect to the HTTP endpoint.

It is designed to be be used with the built-in `http` and `https` modules.

Installation
------------

Install with `npm`:
```
$ npm install pac-proxy-agent
```
Example
-------

```js
var url = require('url');
var http = require('http');
var PacProxyAgent = require('pac-proxy-agent');

// URI to a PAC proxy file to use (the "pac+" prefix is stripped)
var proxy = 'pac+https://cloudup.com/ceGH2yZ0Bjp+';
console.log('using PAC proxy proxy file at %j', proxy);

// HTTP endpoint for the proxy to connect to
var endpoint = 'http://nodejs.org/api/';
console.log('attempting to GET %j', endpoint);
var opts = url.parse(endpoint);

// create an instance of the `PacProxyAgent` class with the PAC file location
var agent = new PacProxyAgent(proxy);
opts.agent = agent;

http.get(opts, function (res) {
  console.log('response event!', res.headers);
  res.pipe(process.stdout);
});
```
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[pac-wikipedia]: http://wikipedia.org/wiki/Proxy_auto-config

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* /opt/cola/permits/1103324486_1604083535.38/0/pac-proxy-agent-4-1-0-tgz/package/README.md

1.34 minizlib 2.1.2

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1.35 socket.io-adapter 1.1.2
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1.38 ieee754 1.2.1

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1.41 http-proxy-agent 4.0.1

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http-proxy-agent

================

### An HTTP(s) proxy `http.Agent` implementation for HTTP

[![Build Status](https://github.com/TooTallNate/node-http-proxy-agent/workflows/Node%20CI/badge.svg)](https://github.com/TooTallNate/node-http-proxy-agent/actions?workflow=Node+CI)

This module provides an `http.Agent` implementation that connects to a specified HTTP or HTTPS proxy server, and can be used with the built-in `http` module.

__Note:__ For HTTP proxy usage with the `https` module, check out [node-https-proxy-agent](https://github.com/TooTallNate/node-https-proxy-agent).

Installation

----------
Install with `npm`:

```bash
$ npm install http-proxy-agent
```

Example
-------

```js
var url = require('url');
vary = require('http');
var HttpProxyAgent = require('http-proxy-agent');

// HTTP/HTTPS proxy to connect to
var proxy = process.env.http_proxy || 'http://168.63.76.32:3128';
console.log('using proxy server %j', proxy);

// HTTP endpoint for the proxy to connect to
console.log('attempting to GET %j', endpoint);
var opts = url.parse(endpoint);

// create an instance of the `HttpProxyAgent` class with the proxy server information
var agent = new HttpProxyAgent(proxy);
opts.agent = agent;

http.get(opts, function (res) {
    console.log('"response" event!', res.headers);
    res.pipe(process.stdout);
});
```

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-------

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Found in path(s):
* /opt/cola/permits/1103324354_1604083584.71/0/http-proxy-agent-4-0-1-1-tgz/package/README.md

1.42 async 3.2.0

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1.45 glob 7.1.6

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1.51 after 0.8.2

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/* zlib.h -- interface of the 'zlib' general purpose compression library version 1.2.11, January 15th, 2017

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1.77 angular-recaptcha 4.1.5

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1.79 minimist 1.2.5

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1.80 libxml 2.9.10

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1.81 ip 1.1.5

1.82 xregexp 2.0.0

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1.83 fast-json-stable-stringify 2.1.0

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1.84 tar 6.0.5

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1.85 which-pm-runs 1.0.0

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1.86 http-errors 1.7.3

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1.87 nan 2.14.2

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1.90 concat-map 0.0.1

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1.92 icu 67

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```
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## Commands to generate dependency files
GEN_DEPS.c=$(CC) -E -MM $(DEFS) $(CPPFLAGS)
GEN_DEPS.cc=$(CXX) -E -MM $(DEFS) $(CPPFLAGS)

## Flags for position independent code
SHAREDLIBCFLAGS = -fPIC
SHAREDLIBCXXFLAGS = -fPIC
SHAREDLIBCPPFLAGS = -DPIC

## Additional flags when building libraries and with threads
THREADSCPPFLAGS = -D_REENTRANT
LIBCPPFLAGS =

## Compiler switch to embed a runtime search path
LD_RPATH=
LD_RPATH_PRE=-Wl,-rpath,

## Compiler switch to embed a library name
LD_SONAME = -Wl,-soname -Wl,$(notdir $(MIDDLE_SO_TARGET))

## Shared library options
LD_SOOPTIONS= -Wl,- Bsymblic

## Shared object suffix
SO = so
## Non-shared intermediate object suffix
STATIC_O = ao
```
## Compilation rules

```
%.$(STATIC_O): $(srcdir)/%.c
$(COMPILE.c) $(STATICCPPFLAGS) $(STATICCFLAGS) -o $@ $<

%.$(STATIC_O): $(srcdir)/%.cpp
$(COMPILE.cc) $(STATICCPPFLAGS) $(STATICCXXFLAGS) -o $@ $<
```  

```
%.(O): $(srcdir)/%.c
$(COMPILE.c) $(DYNAMICCPPFLAGS) $(DYNAMICCFLAGS) -o $@ $<

%.(O): $(srcdir)/%.cpp
$(COMPILE.cc) $(DYNAMICCPPFLAGS) $(DYNAMICCXXFLAGS) -o $@ $<
```  

## Dependency rules

```
%.d: $(srcdir)/%.c
@echo "generating dependency information for $<"
@$(SHELL) -ec '$(GEN_DEPS.c) $< \
| sed \"s/(.*)\.o[ :]*/\1.o $@ : /g\" > $@; \
[ -s $@ ] || rm -f $@'

%.d: $(srcdir)/%.cpp
@echo "generating dependency information for $<"
@$(SHELL) -ec '$(GEN_DEPS.cc) $< \n| sed \"s/(.*)\.o[ :]*/\1.o $@ : /g\" > $@; \
[ -s $@ ] || rm -f $@'
```  

## Versioned libraries rules

```
%.$(SO).$(SO_TARGET_VERSION_MAJOR): %.$(SO).$(SO_TARGET_VERSION)
$(RM) $@ && ln -s ${<F} $@

%.$(SO): %.$(SO).$(SO_TARGET_VERSION_MAJOR)
$(RM) $@ && ln -s ${*F}.$(SO).$(SO_TARGET_VERSION) $@
```  

## Bind internal references

```
# LDflags that pkgdata will use
BIR_LDFLAGS= -Wl,-Bsymbolic

# Dependencies [i.e. map files] for the final library
BIR_DEPS=
```  

```
## Remove shared library ‘s’
STATIC_PREFIX_WHEN_USED =
STATIC_PREFIX =
```  

## End BSD-specific setup

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1.94 async 1.5.2

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1.96 fast-safe-stringify 2.0.7

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1.99 wide-align 1.1.3

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1.103 end-of-stream 1.4.4

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C++ Big Integer Library
(see ChangeLog for version)

http://mattmccutchen.net/bigint/

Written and maintained by Matt McCutchen <matt@mattmccutchen.net>

You can use this library in a C++ program to do arithmetic on integers of size limited only by your computer's memory. The library provides BigUnsigned and BigInteger classes that represent nonnegative integers and signed integers, respectively. Most of the C++ arithmetic operators are overloaded for these classes, so big-integer calculations are as easy as:

```
#include "BigIntegerLibrary.hh"

BigInteger a = 65536;
cout << (a * a * a * a * a * a * a);```
The code in `sample.cc' demonstrates the most important features of the library. To get started quickly, read the code and explanations in that file and run it. If you want more detail or a feature not shown in `sample.cc', consult the actual header and source files, which are thoroughly commented.

This library emphasizes ease of use and clarity of implementation over speed; some users will prefer GMP (http://swox.com/gmp/), which is faster. The code is intended to be reasonably portable across computers and modern C++ compilers; in particular, it uses whatever word size the computer provides (32-bit, 64-bit, or otherwise).

Compiling programs that use the library

The library consists of a folder full of C++ header files (`.hh') and source files (`.cc'). Your own programs should `#include' the necessary header files and link with the source files. A makefile that builds the sample program (`sample.cc') is included; you can adapt it to replace the sample with your own program.

Alternatively, you can use your own build system or IDE. In that case, you must put the library header files where the compiler will find them and arrange to have your program linked with the library source files; otherwise, you will get errors about missing header files or "undefined references". To learn how to do this, consult the documentation for the build system or IDE; don't bother asking me. Adding all the library files to your project will work in many IDEs but may not be the most desirable approach.

Resources

The library's Web site (above) provides links to released versions, the current development version, and a mailing list for release announcements, questions, bug reports, and other discussion of the library. I would be delighted to hear from you if you like this library and/or find a good use for it.

Bugs and enhancements

The library has been tested by me and others but is by no means bug-free. If you find a bug, please report it, whether it comes in the form of compiling trouble, a mathematically inaccurate result, or a memory-management bloop (since I use Java, these are altogether too common in my C++). I generally fix all reported bugs. You are also welcome to request enhancements, but I am unlikely to do substantial amounts of work on enhancements at this point.

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1.113 pify 3.0.0

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1.114 **indexOf 0.0.1**

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1.115 **mkdirp-classic 0.5.3**

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1.116 has-cors 1.1.0

1.117 deep-extend 0.6.0

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1.118 fs-constants 1.0.0

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1.119 angular-animate 1.4.14

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1.120 later 1.2.0
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1.121 combined-stream 1.0.8

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1.122 angular-scroll 1.0.2
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1.123 detect-libc 1.0.3
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1.124 streamsearch 0.1.2

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1.125 tunnel-agent 0.6.0

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1.138 http-signature 1.2.0

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1.139 decompress-response 4.2.1

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1.140 sshpk 1.16.1

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1.141 punycode 2.1.1

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1.142 fast-deep-equal 3.1.3

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1.143 v8 8.5.210.26

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Written by: Philip Hazel
THE C++ WRAPPER FUNCTIONS
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Python was created in the early 1990s by Guido van Rossum at Stichting Mathematisch Centrum (CWI, see http://www.cwi.nl) in the Netherlands as a successor of a language called ABC. Guido remains Python’s principal author, although it includes many contributions from others.

In 1995, Guido continued his work on Python at the Corporation for
National Research Initiatives (CNRI, see http://www.cnri.reston.va.us) in Reston, Virginia where he released several versions of the software.

In May 2000, Guido and the Python core development team moved to BeOpen.com to form the BeOpen PythonLabs team. In October of the same year, the PythonLabs team moved to Digital Creations, which became Zope Corporation. In 2001, the Python Software Foundation (PSF, see https://www.python.org/psf/) was formed, a non-profit organization created specifically to own Python-related Intellectual Property. Zope Corporation was a sponsoring member of the PSF.

All Python releases are Open Source (see http://www.opensource.org for the Open Source Definition). Historically, most, but not all, Python releases have also been GPL-compatible; the table below summarizes the various releases.

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1.153 request 2.88.2

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1.155 degenerator 2.2.0
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degenerator

==============
### Compiles sync functions into async functions

Sometimes you need to write sync looking code that's really async under the hood. This module takes a String to one or more synchronous JavaScript functions, and returns a new String that with those JS functions transpiled into `async` functions.

So this:

```js
function foo() {
  return a('bar') || b();
}
```

Gets compiled into:

```js
async function foo() {
  return await a('bar') || await b();
}
```

With the compiled output code, you can evaluate the code using the `vm` module in Node.js, or save the code to a file and require it, or whatever.

**Installation**

----------

Install with `npm`:

```bash
$ npm install degenerator
```

**Example**

-------
You must explicitly specify the names of the functions that should be "asyncified". So say we wanted to expose a `get(url)` function that did and HTTP request and returned the response body.

The user has provided us with this implementation:

```js
function myFn() {
    const one = get('https://google.com');
    const two = get('http://nodejs.org');
    const three = JSON.parse(get('http://jsonip.org'));
    return [one, two, three];
}
```

Now we can compile this into an asynchronous function, implement the async `get()` function, and finally evaluate it into a real JavaScript function instance with the `vm` module:

```typescript
import vm from 'vm';
import degenerator from 'degenerator';

// The `get()` function is Promise-based (error handling omitted for brevity)
function get(endpoint: string) {
    return new Promise((resolve, reject) => {
        var mod = 0 == endpoint.indexOf('https:') ? require('https') : require('http');
        var req = mod.get(endpoint);
        req.on('response', function (res) {
            var data = "";
            res.setEncoding('utf8');
            res.on('data', function (b) { data += b; });
            res.on('end', function () {
                resolve(data);
            });
        });
    });
}

// Convert the JavaScript string provided from the user (assumed to be `str` var)
str = degenerator(str, ['get']);

// Turn the JS String into a real async function instance
const asyncFn = vm.runInNewContext(`(${str})`, { get });

// Now we can invoke the function asynchronously
asyncFn().then((res) => {
```
// Do something with `res`...
});
```
1.156 universalify 1.0.0

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1.157 are-we-there-yet 1.1.5

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1.160 depd 1.1.2

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1.165 tar-fs 2.1.0

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*
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Kai Uwe Rommel (OS/2), John Bush and Paul Kienitz (Amiga), Antoine Verheijen (Macintosh), Hunter Goatley (more VMS), Mike White (Windows DLLs), Christian Spieler (overall logic, optimization, VMS, etc.) and others. See the file CONTRIBUTIONS in the source distribution for a much more complete list of contributors.

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1.172 asn1 0.2.4

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1.173 serialport-parser-byte-length 9.0.1

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1.193 Iodash 4.17.20

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1.201 debug 4.2.0

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1.204 color-name 1.1.3

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Python was created in the early 1990s by Guido van Rossum at Stichting Mathematisch Centrum (CWI, see http://www.cwi.nl) in the Netherlands as a successor of a language called ABC. Guido remains Python’s principal author, although it includes many contributions from others.

In 1995, Guido continued his work on Python at the Corporation for National Research Initiatives (CNRI, see http://www.cnri.reston.va.us) in Reston, Virginia where he released several versions of the software.

In May 2000, Guido and the Python core development team moved to BeOpen.com to form the BeOpen PythonLabs team. In October of the same year, the PythonLabs team moved to Digital Creations, which became Zope Corporation. In 2001, the Python Software Foundation (PSF, see https://www.python.org/psf/) was formed, a non-profit organization created specifically to own Python-related Intellectual Property. Zope Corporation was a sponsoring member of the PSF.

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<td>PSF</td>
<td>yes</td>
</tr>
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<td>2.2 and above</td>
<td>2.1.1</td>
<td>2001-now</td>
<td>PSF</td>
<td>yes</td>
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* /opt/ws_local/PERMITS_SQL/1011812636_1591373973.1/0/libphonenumber-8-10-17-sources-jar/com/google/i18n/phonenumbers/NumberParseException.java
* /opt/ws_local/PERMITS_SQL/1011812636_1591373973.1/0/libphonenumber-8-10-17-sources-jar/com/google/i18n/phonenumbers/AsYouTypeFormatter.java
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* /opt/ws_local/PERMITS_SQL/1011812636_1591373973.1/0/libphonenumber-8-10-17-sources-jar/com/google/i18n/phonenumbers/MetadataLoader.java
* /opt/ws_local/PERMITS_SQL/1011812636_1591373973.1/0/libphonenumber-8-10-17-sources-jar/com/google/i18n/phonenumbers/internal/RegexBasedMatcher.java
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  jar/com/google/i18n/phonenumbers/MetadataManager.java
* /opt/ws_local/PERMITS_SQL/1011812636_1591373973.1/0/libphonenumber-8-10-17-sources-
  jar/com/google/i18n/phonenumbers/AlternateFormatsCountryCodeSet.java
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  jar/com/google/i18n/phonenumbers/PhoneNumberUtil.java
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* /opt/ws_local/PERMITS_SQL/1011812636_1591373973.1/0/libphonenumber-8-10-17-sources-jar/com/google/i18n/phonenumbers/SingleFileMetadataSourceImpl.java
* /opt/ws_local/PERMITS_SQL/1011812636_1591373973.1/0/libphonenumber-8-10-17-sources-jar/com/google/i18n/phonenumbers/MetadataSource.java

1.222 graceful-fs 4.2.4

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1.223 levn 0.3.0

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1.224 xml2js 0.4.23

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1.225 ng-idle 1.3.3

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1.226 string_decoder 0.10.31

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1.227 angular-ui-select 0.0.5

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1.234 text-hex 1.0.0

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1.235 angular-bootstrap 1.1.2

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1.236 deep-is 0.1.3

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https-proxy-agent

===============
### An HTTP(s) proxy `http.Agent` implementation for HTTPS
[![Build Status](https://github.com/TooTallNate/node-https-proxy-agent/workflows/Node%20CI/badge.svg)](https://github.com/TooTallNate/node-https-proxy-agent/workflows/Node%20CI/badge.svg)
This module provides an `http.Agent` implementation that connects to a specified HTTP or HTTPS proxy server, and can be used with the built-in `https` module.

Specifically, this `Agent` implementation connects to an intermediary "proxy" server and issues the [CONNECT HTTP method][CONNECT], which tells the proxy to open a direct TCP connection to the destination server.

Since this agent implements the CONNECT HTTP method, it also works with other protocols that use this method when connecting over proxies (i.e. WebSockets). See the "Examples" section below for more.

Installation
------------

Install with `npm`:

```bash
$ npm install https-proxy-agent
```

Examples
--------

#### `https` module example

```javascript
var url = require('url');
var https = require('https');
var HttpsProxyAgent = require('https-proxy-agent');

// HTTP/HTTPS proxy to connect to
var proxy = process.env.http_proxy || 'http://168.63.76.32:3128';
console.log('using proxy server %j', proxy);

// HTTPS endpoint for the proxy to connect to
console.log('attempting to GET %j', endpoint);
var options = url.parse(endpoint);

// create an instance of the `HttpsProxyAgent` class with the proxy server information
var agent = new HttpsProxyAgent(proxy);
options.agent = agent;

https.get(options, function (res) {
```

[Connect HTTP method]: https://developer.mozilla.org/en-US/docs/Web/HTTP/Methods/CONNECT

```javascript
var url = require('url');
var WebSocket = require('ws');
var HttpsProxyAgent = require('https-proxy-agent');

// HTTP/HTTPS proxy to connect to
var proxy = process.env.http_proxy || 'http://168.63.76.32:3128';
console.log('using proxy server %j', proxy);

// WebSocket endpoint for the proxy to connect to
var endpoint = process.argv[2] || 'ws://echo.websocket.org';
var parsed = url.parse(endpoint);
console.log('attempting to connect to WebSocket %j', endpoint);

// create an instance of the `HttpsProxyAgent` class with the proxy server information
var options = url.parse(proxy);

var agent = new HttpsProxyAgent(options);

// finally, initiate the WebSocket connection
var socket = new WebSocket(endpoint, { agent: agent });

socket.on('open', function () {
  console.log("open" event!);
  socket.send('hello world');
});

socket.on('message', function (data, flags) {
  console.log("message" event! %j %j, data, flags);
  socket.close();
});
```

---

### new HttpsProxyAgent(Object options)

The `HttpsProxyAgent` class implements an `http.Agent` subclass that connects to the specified "HTTP(s) proxy server" in order to proxy HTTPS and/or WebSocket requests. This is achieved by using the [HTTP "CONNECT" method][CONNECT].
The `options` argument may either be a string URI of the proxy server to use, or an "options" object with more specific properties:

* `host` - String - Proxy host to connect to (may use `hostname` as well). Required.
* `port` - Number - Proxy port to connect to. Required.
* `protocol` - String - If `https:`, then use TLS to connect to the proxy.
* `headers` - Object - Additional HTTP headers to be sent on the HTTP CONNECT method.
* Any other options given are passed to the `net.connect()`/`tls.connect()` functions.

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[CONNECT]: http://en.wikipedia.org/wiki/HTTP_tunnel#HTTP_CONNECT_Tunneling

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1.254 proxy-agent 4.0.0

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https-proxy-agent

============

### An HTTP(s) proxy `http.Agent` implementation for HTTPS

[![Build Status](https://github.com/TooTallNate/node-https-proxy-agent/workflows/Node%20CI/badge.svg)](https://github.com/TooTallNate/node-https-proxy-agent/actions?workflow=Node+CI)

This module provides an `http.Agent` implementation that connects to a specified HTTP or HTTPS proxy server, and can be used with the built-in `https` module.

Specifically, this `Agent` implementation connects to an intermediary "proxy" server and issues the [CONNECT HTTP method][CONNECT], which tells the proxy to open a direct TCP connection to the destination server.

Since this agent implements the CONNECT HTTP method, it also works with other protocols that use this method when connecting over proxies (i.e. WebSockets). See the "Examples" section below for more.

Installation

----------
Install with `npm`:

```bash
$ npm install https-proxy-agent
```

Examples
--------

##### `https` module example

```js
var url = require('url');
var https = require('https');
var HttpsProxyAgent = require('https-proxy-agent');

// HTTP/HTTPS proxy to connect to
var proxy = process.env.http_proxy || 'http://168.63.76.32:3128';
console.log('using proxy server %j', proxy);

// HTTPS endpoint for the proxy to connect to
console.log('attempting to GET %j', endpoint);
var options = url.parse(endpoint);

// create an instance of the `HttpsProxyAgent` class with the proxy server information
var agent = new HttpsProxyAgent(proxy);
options.agent = agent;

https.get(options, function (res) {
    console.log("response" event!, res.headers);
    res.pipe(process.stdout);
});
```

##### `ws` WebSocket connection example

```js
var url = require('url');
var WebSocket = require('ws');
var HttpsProxyAgent = require('https-proxy-agent');

// HTTP/HTTPS proxy to connect to
var proxy = process.env.http_proxy || 'http://168.63.76.32:3128';
console.log('using proxy server %j', proxy);
```
// WebSocket endpoint for the proxy to connect to
var endpoint = process.argv[2] || 'ws://echo.websocket.org';
var parsed = url.parse(endpoint);
console.log('attempting to connect to WebSocket %j', endpoint);

// create an instance of the `HttpsProxyAgent` class with the proxy server information
var options = url.parse(proxy);

var agent = new HttpsProxyAgent(options);

// finally, initiate the WebSocket connection
var socket = new WebSocket(endpoint, { agent: agent });

socket.on('open', function () {
    console.log('"open" event!');
    socket.send('hello world');
});

socket.on('message', function (data, flags) {
    console.log('"message" event! %j %j', data, flags);
    socket.close();
    ...
    
    API

    ---

    ### new HttpsProxyAgent(Object options)

    The `HttpProxyAgent` class implements an `http.Agent` subclass that connects
to the specified "HTTP(s) proxy server" in order to proxy HTTPS and/or WebSocket
requests. This is achieved by using the [HTTP `CONNECT` method][CONNECT].

    The `options` argument may either be a string URI of the proxy server to use, or an
"options" object with more specific properties:

* `host` - String - Proxy host to connect to (may use `hostname` as well). Required.
* `port` - Number - Proxy port to connect to. Required.
* `protocol` - String - If `https:`, then use TLS to connect to the proxy.
* `headers` - Object - Additional HTTP headers to be sent on the HTTP CONNECT method.
* Any other options given are passed to the `net.connect()`/`tls.connect()` functions.

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[CONNECT]: http://en.wikipedia.org/wiki/HTTP_tunnel#HTTP_CONNECT_Tunneling

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* /opt/cola/permits/1103324372_1604083539.76/0/https-proxy-agent-4-0-0-4-tgz/package/README.md

1.255 moment-timezone 0.5.31

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1.264 json-stringify-safe 5.0.1

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1.266 data-uri-to-buffer 3.0.1

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data-uri-to-buffer

=============

### Generate a Buffer instance from a [Data URI][rfc] string
[![Build Status](https://travis-ci.org/TooTallNate/node-data-uri-to-buffer.svg?branch=master)](https://travis-ci.org/TooTallNate/node-data-uri-to-buffer)

This module accepts a "data” URI[rfc] String of data, and returns a node.js `Buffer` instance with the decoded data.

Installation

----------

Install with `npm`:
```bash
$ npm install data-uri-to-buffer
```

Example
-------

```js
var dataUriToBuffer = require('data-uri-to-buffer');

// plain-text data is supported
var uri = 'data:,Hello%2C%20World!';
var decoded = dataUriToBuffer(uri);
console.log(decoded.toString());
// 'Hello, World!'

// base64-encoded data is supported
uri = 'data:text/plain;base64,SGVsbG8sIFdvcmxkIQ%3D%3D';
decoded = dataUriToBuffer(uri);
console.log(decoded.toString());
// 'Hello, World!'
```

API
---

```javascript
### dataUriToBuffer(String uri)  Buffer

The `type` property on the Buffer instance gets set to the main type portion of the "mediatetype" portion of the "data" URI, or defaults to "text/plain" if not specified.

The `typeFull` property on the Buffer instance gets set to the entire "mediatetype" portion of the "data" URI (including all parameters), or defaults to "text/plain;charset=US-ASCII" if not specified.

The `charset` property on the Buffer instance gets set to the Charset portion of the "mediatetype" portion of the "data" URI, or defaults to "US-ASCII" if the entire type is not specified, or defaults to "" otherwise.

*Note*: If the only the main type is specified but not the charset, e.g. "data:text/plain,abc"", the charset is set to the empty string. The spec only defaults to US-ASCII as charset if the entire type is not specified.
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Found in path(s):
* /opt/cola/permits/1103324543_1604083603.09/0/data-uri-to-buffer-3-0-1-tgz/package/README.md

1.267 angle 85.0.4183.121

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1.270 console-control-strings 1.1.0
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1.273 angular-sanitize 1.4.14

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1.274 xmlhttprequest 1.8.0

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1.277 toidentifier 1.0.0

1.278 openssl 1.0.2d
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1.297 angular-datatables 0.5.6

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* 
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* 
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- IDEA is no longer included, its use is deprecated  
- DES is now external, in the OpenSSL library  
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1.306 ng-grid 2.0.14

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1.311 wrappy 1.0.2

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1.318 asynckit 0.4.0

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1.319 zlib 1.2.8
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   version 1.2.11, January 15th, 2017

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1.320 socks 2.5.0

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1.321 socket.io-parser 3.4.1

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1.324 highcharts-downsample 8.2.0

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1.325 c-ares 1.41.0

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1.326 Iodash 4.17.20

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1.356 sqlite 3.33.0

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1.357 esprima 4.0.1

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1.358 safe-buffer 5.2.1
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1.359 libvorbis 1.3.7

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1.360 libvpx 1.8.2-202-g769129fb2

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1.361 angular-route 1.4.14

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### Returns a `stream.Readable` from a URI string

This high-level module accepts a URI string and returns a `Readable` stream instance. There is built-in support for a variety of "protocols", and it's easily extensible with more:

<table>
<thead>
<tr>
<th>Protocol</th>
<th>Description</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>data</code></td>
<td>[Data URIs][data]</td>
<td><code>data:text/plain;base64,SGVsbG8sIFdvcmxkIQ%3D%3D</code></td>
</tr>
<tr>
<td><code>file</code></td>
<td>[File URIs][file]</td>
<td><code>file:///c:/windows/example.ini</code></td>
</tr>
<tr>
<td><code>http</code></td>
<td>[HTTP URIs][http]</td>
<td><code>http://www.example.com/path/to/name</code></td>
</tr>
</tbody>
</table>
Installation
------------

Install with `npm`:

```bash
$ npm install get-uri
```

Example
-------

To simply get a `stream.Readable` instance from a `file:` URI, try something like:

```js
var getUri = require('get-uri');

// `file:` maps to a `fs.ReadStream` instance
getUri('file:///Users/nrajlich/wat.json', function (err, rs) {
  if (err) throw err;
  rs.pipe(process.stdout);
});
```

Missing Endpoints
-----------------

When you pass in a URI in which the resource referenced does not exist on the destination server, then a `NotFoundError` will be returned. The `code` of the error instance is set to `"ENOTFOUND"`, so you can special-case that in your code to detect when a bad filename is requested:

```js
getUri('http://example.com/resource.json', function (err, rs) {
  if (err) {
    if ('ENOTFOUND' == err.code) {
      // bad file path requested
    } else {
      // something else bad happened...
      throw err;
    }
  }
}
```
Cacheability
-------------

When calling `getUri()` with the same URI multiple times, the `get-uri` module supports sending an indicator that the remote resource has not been modified since the last time it has been retrieved from that node process.

To do this, pass in a `cache` option to the "options object" argument with the value set to the `stream.Readable` instance that was previously returned. If the remote resource has not been changed since the last call for that same URI, then a `NotModifiedError` instance will be returned with it's `code` property set to "ENOTMODIFIED".

When the "ENOTMODIFIED" error occurs, then you can safely re-use the results from the previous `getUri()` call for that same URI:
```
```
API
---

### getUri(String uri[, Object options,] Function callback)

A `uri` String is required. An optional `options` object may be passed in:

- `cache` - A `stream.Readable` instance from a previous call to `getUri()` with the same URI. If this option is passed in, and the destination endpoint has not been modified, then an `ENOTMODIFIED` error is returned.

Any other options passed in to the `options` object will be passed through to the low-level connection creation functions (`http.get()`, `ftp.connect()`, etc).

Invokes the given `callback` function with a `stream.Readable` instance to read the resource at the given `uri`.

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------

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[ftp]: http://www.w3.org/Protocols/rfc959/
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1.365 better-assert 1.0.2

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1.366 csv-parse 4.12.0

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1.367 har-schema 2.0.0

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1.368 skia 85.0.4183.121

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 *
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 * Author: Oystein Moseng
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 * license: MIT (http://opensource.org/licenses/MIT)
 * author: yFiles for HTML Support Team <yfilesh.html@yworks.com>
 * homepage: https://github.com/yWorks/svg2pdf.js#readme
 * version: 1.0.5
 * 
 * svgpath:
 * license: MIT (http://opensource.org/licenses/MIT)
 * maintainers: vitaly <vitaly@rcdesign.ru>
 * homepage: https://github.com/fontello/svgpath#readme
 * version: 2.2.1
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 * MIT Licensed
 * Gabe Lerner (gabelerner@gmail.com)
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 * author: yFiles for HTML Support Team <yfileshtml@yworks.com>
 * homepage: https://github.com/yWorks/svg2pdf.js#readme
 * version: 1.0.5
 *
 * svgpath:
 * license: MIT (http://opensource.org/licenses/MIT)
 * maintainers: vitaly <vitaly@rcdesign.ru>
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A class to parse color values
@author Stoyan Stefanov <sstoo@gmail.com>
@link http://www.ph Pied.com/rgb-color-parser-in-javascript/
Use it if you like it

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