Open Source Used In CLI Analyzer 3.6.6

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In your requests please include the following reference number 78EE117C99-1068885166

Contents

1.1 repeat-string 1.6.1
   1.1.1 Available under license
1.2 ssh2-streams 0.1.20
   1.2.1 Available under license
1.3 ansi-bgred 0.1.1
   1.3.1 Available under license
1.4 once 1.4.0
   1.4.1 Available under license
1.5 which-pm-runs 1.0.0
   1.5.1 Available under license
1.6 direct3d 10.0.16299.15
   1.6.1 Available under license
1.7 angular-recaptcha 4.1.5
   1.7.1 Available under license
1.8 inherits 2.0.4
   1.8.1 Available under license
1.9 bootstrap 4.3.1
   1.9.1 Available under license
1.10 leveldb 11
   1.10.1 Available under license
1.11 extend-shallow 2.0.1
   1.11.1 Available under license
1.12 assert-plus 1.0.0
1.13 uri-js 4.2.2
   1.13.1 Available under license
1.14 longest 1.0.1
1.14.1 Available under license

1.15 log-utils 0.2.1
1.15.1 Available under license

1.16 is-accessor-descriptor 1.0.0
1.16.1 Available under license

1.17 libxslt 1.1.34
1.17.1 Available under license

1.18 crcradio 670.3396.99
1.18.1 Available under license

1.19 for-in 1.0.2
1.19.1 Available under license

1.20 buffer-fill 1.0.0

1.21 mimic-response 1.0.1
1.21.1 Available under license

1.22 ansi-hidden 0.1.1
1.22.1 Available under license

1.23 color-name 1.1.3
1.23.1 Available under license

1.24 ansi-bghwhite 0.1.1
1.24.1 Available under license

1.25 tar-fs 1.16.3
1.25.1 Available under license

1.26 esutils 2.0.3
1.26.1 Available under license

1.27 mute-stream 0.0.7
1.27.1 Available under license

1.28 data-uri-to-buffer 1.2.0

1.29 backo2 1.0.2

1.30 serialport-parser-readline 1.0.5
1.30.1 Available under license

1.31 private 0.1.8
1.31.1 Available under license

1.32 ng-idle 1.0.4
1.32.1 Available under license

1.33 angular-bootstrap 1.1.2
1.33.1 Available under license

1.34 rimraf 2.7.1
1.34.1 Available under license

1.35 mime-db 1.44.0
1.35.1 Available under license

**1.36 string-width 1.0.2**
1.36.1 Available under license

**1.37 to-array 0.1.4**
1.37.1 Available under license

**1.38 exit 0.1.2**
1.38.1 Available under license

**1.39 has-cors 1.1.0**

**1.40 tar 3.2.1**
1.40.1 Available under license

**1.41 @dabh/diagnostics 2.0.2**
1.41.1 Available under license

**1.42 lru-cache 4.1.5**
1.42.1 Available under license

**1.43 ansi-black 0.1.1**
1.43.1 Available under license

**1.44 radio-symbol 2.0.0**
1.44.1 Available under license

**1.45 ansi-inverse 0.1.1**
1.45.1 Available under license

**1.46 array-union 1.0.2**
1.46.1 Available under license

**1.47 blob 0.0.5**
1.47.1 Available under license

**1.48 icu 65.1**
1.48.1 Available under license

**1.49 minizlib 1.3.3**
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**1.50 skia 20170511-53d6729-1.4**
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**1.51 pac-proxy-agent 3.0.1**
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**1.52 openssl 1.1.0h**
1.52.1 Available under license

**1.53 is-descriptor 1.0.2**
1.53.1 Available under license

**1.54 fs.realpath 1.0.0**
1.54.1 Available under license

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1.55.1 Available under license
1.56 socket.io 2.3.0
  1.56.1 Available under license
1.57 xml2js 0.4.23
  1.57.1 Available under license
1.58 lodash 4.17.19
  1.58.1 Available under license
1.59 ansi-bggreen 0.1.1
  1.59.1 Available under license
1.60 text-hex 1.0.0
  1.60.1 Available under license
1.61 tweetnacl 0.14.5
  1.61.1 Available under license
1.62 color-convert 1.9.3
  1.62.1 Available under license
1.63 window-size 0.1.4
  1.63.1 Available under license
1.64 nghttp2 1.41.0
  1.64.1 Available under license
1.65 end-of-stream 1.4.4
  1.65.1 Available under license
1.66 component-inherit 0.0.3
  1.66.1 Available under license
1.67 is-my-json-valid 2.20.4
  1.67.1 Available under license
1.68 paralleljs 0.2.1
  1.68.1 Available under license
1.69 to-object-path 0.3.0
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  1.70.1 Available under license
1.71 nghttp2 1.41.0
  1.71.1 Available under license
1.72 node-abi 2.18.0
  1.72.1 Available under license
1.73 trix 0.10.2
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1.74 bl 1.1.2
  1.74.1 Available under license
1.75 ansi-white 0.1.1
  1.75.1 Available under license
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  1.76.1 Available under license
1.77 lodash-find 4.6.0
  1.77.1 Available under license
1.78 optimist 0.3.7
  1.78.1 Available under license
1.79 array-uniq 1.0.3
  1.79.1 Available under license
1.80 parseuri 0.0.5
  1.80.1 Available under license
1.81 prompt-question 5.0.2
  1.81.1 Available under license
1.82 bluebird 2.11.0
  1.82.1 Available under license
1.83 arr-flatten 1.1.0
  1.83.1 Available under license
1.84 protobuf 20.2.0
  1.84.1 Available under license
1.85 chalk 1.1.3
  1.85.1 Available under license
1.86 is-windows 1.0.2
  1.86.1 Available under license
1.87 ftp 0.3.10
  1.87.1 Available under license
1.88 util-deprecate 1.0.2
  1.88.1 Available under license
1.89 ncp 0.5.1
  1.89.1 Available under license
1.90 mkdirp 0.5.0
  1.90.1 Available under license
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  1.91.1 Available under license
1.92 fast-json-stable-stringify 2.1.0
  1.92.1 Available under license
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   1.116.1 Available under license
1.117 fast-deep-equal 3.1.3
   1.117.1 Available under license
1.118 zlib 1.2.8
   1.118.1 Available under license
1.119 object-copy 0.1.0
   1.119.1 Available under license
1.120 pointer-symbol 1.0.0
   1.120.1 Available under license
1.121 requirejs-text 2.0.16
   1.121.1 Available under license
1.122 libphonenumber 8.12.7
   1.122.1 Available under license
1.123 isstream 0.1.2
   1.123.1 Available under license
1.124 libsrtp 2.3.0
   1.124.1 Available under license
1.125 libjpeg 6b
   1.125.1 Notifications
   1.125.2 Available under license
1.126 to-buffer 1.1.1
   1.126.1 Available under license
1.127 mixin-object 2.0.1
   1.127.1 Available under license
1.128 tough-cookie 2.5.0
   1.128.1 Available under license
1.129 moment-timezone 0.5.31
   1.129.1 Available under license
1.130 cygwin 2.3.0
   1.130.1 Available under license
1.131 readline-utils 2.2.3
   1.131.1 Available under license
1.132 is-fullwidth-code-point 1.0.0
   1.132.1 Available under license
1.133 indexof 0.0.1
  1.133.1 Available under license
1.134 smart-buffer 4.1.0
  1.134.1 Available under license
1.135 log-ok 0.1.1
  1.135.1 Available under license
1.136 balanced-match 1.0.0
  1.136.1 Available under license
1.137 is-plain-object 2.0.4
  1.137.1 Available under license
1.138 hawk 3.1.3
  1.138.1 Available under license
1.139 combined-stream 1.0.8
  1.139.1 Available under license
1.140 glob 7.1.6
  1.140.1 Available under license
1.141 fast-levenshtein 2.0.6
  1.141.1 Available under license
1.142 accepts 1.3.7
1.143 colorspace 1.1.2
  1.143.1 Available under license
1.144 static-extend 0.1.2
  1.144.1 Available under license
1.145 setprototypeof 1.1.1
1.146 arraybuffer.slice 0.0.7
  1.146.1 Available under license
1.147 async 0.2.10
  1.147.1 Available under license
1.148 chardet 0.1.0
  1.148.1 Available under license
1.149 clone-deep 1.0.0
1.150 expand-template 1.1.1
  1.150.1 Available under license
1.151 unzip 6.0
  1.151.1 Available under license
1.152 cliui 2.1.0
  1.152.1 Available under license
1.153 ws 7.3.1
  1.153.1 Available under license
1.154 performance-now 2.1.0
   1.154.1 Available under license
1.155 free-type 2.10.2
   1.155.1 Available under license
1.156 semver 4.3.6
   1.156.1 Available under license
1.157 serialport-parser-cctalk 1.0.5
   1.157.1 Available under license
1.158 estraverse 4.3.0
   1.158.1 Available under license
1.159 warning-symbol 0.1.0
   1.159.1 Available under license
1.160 wrappy 1.0.2
   1.160.1 Available under license
1.161 sqlite 3.22.0
   1.161.1 Available under license
1.162 eyes 0.1.8
   1.162.1 Available under license
1.163 sprintf-js 1.1.2
   1.163.1 Available under license
1.164 object-assign 4.1.1
   1.164.1 Available under license
1.165 base64-arraybuffer 0.1.5
   1.165.1 Available under license
1.166 npmlog 4.1.2
   1.166.1 Available under license
1.167 angular-route 1.4.14
   1.167.1 Available under license
1.168 libcxx 10.0.0
   1.168.1 Available under license
1.169 stringmap 0.2.2
   1.169.1 Available under license
1.170 koalas 1.0.2
   1.170.1 Available under license
1.171 ansi-gray 0.1.1
   1.171.1 Available under license
1.172 proxy-from-env 1.1.0
   1.172.1 Available under license
1.173 socks 2.3.3
1.173.1 Available under license

1.174 jquery 3.4.1
   1.174.1 Available under license

1.175 delegates 1.0.0
   1.175.1 Available under license

1.176 ansi-bgblack 0.1.1
   1.176.1 Available under license

1.177 angular-datatables 0.5.6
   1.177.1 Available under license

1.178 toidentifier 1.0.0

1.179 base64id 2.0.0
   1.179.1 Available under license

1.180 extend 3.0.2
   1.180.1 Available under license

1.181 deep-extend 0.6.0
   1.181.1 Available under license

1.182 visual-studio-runtime 11.0.610330.1
   1.182.1 Available under license

1.183 yallist 2.1.2
   1.183.1 Available under license

1.184 pac-resolver 3.0.0

1.185 pify 3.0.0
   1.185.1 Available under license

1.186 winston-daily-rotate-file 4.5.0
   1.186.1 Available under license

1.187 yeast 0.1.2
   1.187.1 Available under license

1.188 simple-is 0.2.0
   1.188.1 Available under license

1.189 jsonpointer 4.1.0
   1.189.1 Available under license

1.190 libxml 2.9.10
   1.190.1 Available under license

1.191 align-text 0.1.4
   1.191.1 Available under license

1.192 engine.io-client 3.4.3
   1.192.1 Available under license

1.193 ansi-bgblue 0.1.1
   1.193.1 Available under license
1.194 https-proxy-agent 2.2.4
   1.194.1 Available under license
1.195 ip 1.1.5
1.196 is-extendable 0.1.1
   1.196.1 Available under license
1.197 c-ares 1.21.0
   1.197.1 Available under license
1.198 angular-ui-select 0.0.5
   1.198.1 Available under license
1.199 libvorbis 1.3.7
   1.199.1 Available under license
1.200 collection-visit 1.0.0
   1.200.1 Available under license
1.201 har-validator 5.1.3
   1.201.1 Available under license
1.202 engine.io 3.4.2
   1.202.1 Available under license
1.203 ms 2.1.2
   1.203.1 Available under license
1.204 socket.io-client 2.3.0
   1.204.1 Available under license
1.205 xregexp 2.0.0
   1.205.1 Available under license
1.206 request-debug 0.2.0
   1.206.1 Available under license
1.207 lodash-padstart 4.6.1
   1.207.1 Available under license
1.208 klaw 1.3.1
   1.208.1 Available under license
1.209 angular-xeditable 0.1.12
   1.209.1 Available under license
1.210 pubsub-js 1.5.8
   1.210.1 Available under license
1.211 cookie 0.3.1
   1.211.1 Available under license
1.212 deep-is 0.1.3
   1.212.1 Available under license
1.213 lodash-max 4.0.1
   1.213.1 Available under license
1.214 gauge 2.7.4
    1.214.1 Available under license
1.215 safer-buffer 2.1.2
    1.215.1 Available under license
1.216 is-path-inside 1.0.1
    1.216.1 Available under license
1.217 json-schema-traverse 0.4.1
    1.217.1 Available under license
1.218 minipass 2.9.0
    1.218.1 Available under license
1.219 ecc-jsbn 0.1.2
    1.219.1 Available under license
1.220 prompt-choices 4.1.0
    1.220.1 Available under license
1.221 fecha 4.2.0
    1.221.1 Available under license
1.222 socket.io-parser 3.4.1
    1.222.1 Available under license
1.223 request 2.74.0
    1.223.1 Available under license
1.224 getpass 0.1.7
    1.224.1 Available under license
1.225 alter 0.2.0
    1.225.1 Available under license
1.226 data-tables 1.10.21
    1.226.1 Available under license
1.227 ansi-bgcyan 0.1.1
    1.227.1 Available under license
1.228 dashdash 1.14.1
    1.228.1 Available under license
1.229 checksum 0.1.1
    1.229.1 Available under license
1.230 tryor 0.1.2
    1.230.1 Available under license
1.231 set-value 3.0.2
    1.231.1 Available under license
1.232 async 2.6.3
    1.232.1 Available under license
1.233 strip-json-comments 2.0.1
1.233.1 Available under license

1.234 breakable 1.0.0
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1.235 is-path-in-cwd 1.0.1
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1.236 isobject 3.0.1
   1.236.1 Available under license

1.237 noop-logger 0.1.1

1.238 pinkie-promise 2.0.1
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1.239 bcrypt-pbkdf 1.0.2
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1.240 psl 1.8.0
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1.241 simple-fmt 0.1.0
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1.242 info-symbol 0.1.0
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1.243 ansi-wrap 0.1.0
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1.244 color 3.0.0
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1.245 v8 6.7.288.46
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1.246 stack-trace 0.0.10
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1.247 newlib 2.0.0
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1.248 simple-get 2.8.1
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1.249 stable 0.1.8

1.250 acorn 5.7.4
   1.250.1 Available under license

1.251 arr-swap 1.0.1
   1.251.1 Available under license

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1.5 which-pm-runs 1.0.0

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1.6 direct3d 10.0.16299.15
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1.12 assert-plus 1.0.0

1.13 uri-js 4.2.2

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1.15 log-utils 0.2.1

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1.16 is-accessor-descriptor 1.0.0

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1.21 mimic-response 1.0.1

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1.25 tar-fs 1.16.3

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1.26 esutils 2.0.3

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1.28 data-uri-to-buffer 1.2.0

1.29 backo2 1.0.2

1.30 serialport-parser-readline 1.0.5
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1.31 private 0.1.8

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1.32 ng-idle 1.0.4

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1.33 angular-bootstrap 1.1.2

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 * http://angular-ui.github.io/bootstrap/
 *
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 */

Found in path(s):
* /opt/ws_local/PERMITS_SQL/1068891154_1594751522.06/0/bootstrap-bower-189241b8981b48a353ebc8161a597ffe144e712d-.zip/bootstrap-bower-189241b8981b48a353ebc8161a597ffe144e712d/ui-bootstrap-tpls.js
* /opt/ws_local/PERMITS_SQL/1068891154_1594751522.06/0/bootstrap-bower-189241b8981b48a353ebc8161a597ffe144e712d-.zip/bootstrap-bower-189241b8981b48a353ebc8161a597ffe144e712d/ui-bootstrap-tpls.min.js
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1.34 rimraf 2.7.1

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1.39 has-cors 1.1.0

1.40 tar 3.2.1
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1.45 ansi-inverse 0.1.1

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1.47 blob 0.0.5

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1.54 fs.realpath 1.0.0
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1.56 socket.io 2.3.0
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1.57 xml2js 0.4.23

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1.58 lodash 4.17.19

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1.59 ansi-bggreen 0.1.1

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1.60 text-hex 1.0.0

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1.61 tweetnacl 0.14.5

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1.64 nghttp2 1.41.0

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set yrange [0:]
set terminal pngcairo font 'Sans, 8' lw 1 size 1400,1024
set xtics rotate by -45
set style histogram errorbars gap 2 lw 1
set style fill solid border -1
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1.66 component-inherit 0.0.3

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1.67 is-my-json-valid 2.20.4

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1.68 paralleljs 0.2.1

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1.70 agent-base 4.3.0

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* /opt/ws_local/PERMITS_SQL/1068887942_1594703341.35/0/agent-base-4-3-0-tgz/package/README.md

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1.71 nghttp2 1.41.0

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set yrange [0:]
set terminal pngcairo font 'Sans, 8' lw 1 size 1400,1024
set xtics rotate by -45
set style histogram errorbars gap 2 lw 1
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1.73 trix 0.10.2

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1.74 bl 1.1.2

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1.80 parseuri 0.0.5

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1.81 prompt-question 5.0.2

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1.84 protobuf 20.2.0

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This file contains a list of people who have made large contributions to the public version of Protocol Buffers.

Original Protocol Buffers design and implementation:
Sanjay Ghemawat <sanjay@google.com>
Jeff Dean <jeff@google.com>
Daniel Dulitz <daniel@google.com>
Craig Silverstein
Paul Haahr <haahr@google.com>
Corey Anderson <corin@google.com>
(and many others)

Proto2 C++ and Java primary author:
Kenton Varda <kenton@google.com>

Proto2 Python primary authors:
Will Robinson <robinson@google.com>
Petar Petrov <petar@google.com>

Java Nano primary authors:
Brian Duff <bduff@google.com>
Tom Chao <chaot@google.com>
Max Cai <maxtroy@google.com>
Ulas Kirazci <ulas@google.com>

Large code contributions:
Large quantity of code reviews:
Scott Bruce <sbruce@google.com>
Frank Yellin
Neal Norwitz <nnorwitz@google.com>
Jeffrey Yasskin <jyasskin@google.com>
Ambrose Feinstein <ambrose@google.com>

Documentation:
Lisa Carey <lcarey@google.com>

Maven packaging:
Gregory Kick <gak@google.com>

Patch contributors:
Kevin Ko <kevin.s.ko@gmail.com>
    * Small patch to handle trailing slashes in --proto_path flag.
Johan Euphrosine <proppy@aminche.com>
    * Small patch to fix Python CallMethod().
Ulrich Kunitz <kune@deine-taler.de>
    * Small optimizations to Python serialization.
Leandro Lucarella <llucax@gmail.com>
    * VI syntax highlighting tweaks.
    * Fix compiler to not make output executable.
Dilip Joseph <dilip.antony.joseph@gmail.com>
    * Heuristic detection of sub-messages when printing unknown fields in
text format.
Brian Atkinson <nairb774@gmail.com>
    * Added @Override annotation to generated Java code where appropriate.
Vincent Choinire <Choiniere.Vincent@hydro.qc.ca>
    * Tru64 support.
Monty Taylor <monty.taylor@gmail.com>
    * Solaris 10 + Sun Studio fixes.
Alek Storm <alek.storm@gmail.com>
    * Slicing support for repeated scalar fields for the Python API.
Oleg Smolsky <oleg.smolsky@gmail.com>
    * MS Visual Studio error format option.
    * Detect unordered_map in stl_hash.m4.
Brian Olson <brianolson@google.com>
    * gzip/zlib I/O support.
Michael Poole <mdpoole@troilus.org>
    * Fixed warnings about generated constructors not explicitly initializing
all fields (only present with certain compiler settings).
    * Added generation of field number constants.
Wink Saville <wink@google.com>
* Fixed initialization ordering problem in logging code.
Will Pierce <willp@nuclei.com>

* Small patch improving performance of in Python serialization.
Alexandre Vassalotti <alexandre@peadrop.com>

* Emacs mode for Protocol Buffers (editors/protobuf-mode.el).
Scott Stafford <scott.stafford@gmail.com>

* Added Swap(), SwapElements(), and RemoveLast() to Reflection interface.
Alexander Melnikov <alm@sibmail.ru>

* HPUX support.
Oliver Jowett <oliver.jowett@gmail.com>

* Detect whether zlib is new enough in configure script.
* Fixes for Solaris 10 32/64-bit confusion.
Evan Jones <evanj@mit.edu>

* Optimize Java serialization code when writing a small message to a stream.
  * Optimize Java serialization of strings so that UTF-8 encoding happens only
    once per string per serialization call.
* Clean up some Java warnings.
* Fix bug with permanent callbacks that delete themselves when run.
Michael Kucharski <m.kucharski@gmail.com>

* Added CodedInputStream.getTotalBytesRead().
Kacper Kowalik <xarthisius.kk@gmail.com>

* Fixed m4/acx_pthread.m4 problem for some Linux distributions.
William Orr <will@worrbase.com>

* Fixed detection of sched_yield on Solaris.
* Added atomicops for Solaris
Andrew Paprocki <andrew@ishiboo.com>

* Fixed minor IBM xLC compiler build issues
  * Added atomicops for AIX (POWER)

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* Author: Oystein Moseng
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 *
 * svg2pdf.js:
 * license: MIT (http://opensource.org/licenses/MIT)
 * author: yFiles for HTML Support Team <yfileshtml@yworks.com>
 * homepage: https://github.com/yWorks/svg2pdf.js#readme
 * version: 1.0.5
 *
 * svgpath:
 * license: MIT (http://opensource.org/licenses/MIT)
 * maintainers: vitaly <vitaly@rcdesign.ru>
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* CommitID 38732db74a

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* https://github.com/niklasvh/base64-arraybuffer
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* /opt/ws_local/PERMITS_SQL/1068891109_1594432961.23/0/highcharts-5-0-14-1-tgz/package/themes/avocado.js
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 * author: yFiles for HTML Support Team <yfileshtml@yworks.com>
 * homepage: https://github.com/yWorks/svg2pdf.js#readme
 * version: 1.0.5
 *
 * svgpath:
 * license: MIT (http://opensource.org/licenses/MIT)
 * maintainers: vitaly <vitaly@rcdesign.ru>
 * homepage: https://github.com/fontello/svgpath#readme
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* /opt/ws_local/PERMITS_SQL/10688911109_1594432961.23/0/highcharts-5-0-14-1-tgz/package/js/modules/heatmap.src.js
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* /opt/ws_local/PERMITS_SQL/1068891109_1594432961.23/0/highcharts-5-0-14-1-tgz/package/js/themes/dark-unica.src.js
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* /opt/ws_local/PERMITS_SQL/1068891109_1594432961.23/0/highcharts-5-0-14-1-tgz/package/themes/sand-signika.src.js
* /opt/ws_local/PERMITS_SQL/1068891109_1594432961.23/0/highcharts-5-0-14-1-tgz/package/themes/grid.src.js
* /opt/ws_local/PERMITS_SQL/1068891109_1594432961.23/0/highcharts-5-0-14-1-tgz/package/themes/gray.src.js
* /opt/ws_local/PERMITS_SQL/1068891109_1594432961.23/0/highcharts-5-0-14-1-tgz/package/js/themes/dark-blue.src.js
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tgz/package/js/modules/stock.src.js
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@author Stoyan Stefanov <sstoo@gmail.com>
@link http://www.phpied.com/rgb-color-parser-in-javascript/
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1.106 openjpeg 2.3.1

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1.107 bindings 1.3.0

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node-bindings

=============

### Helper module for loading your native module's .node file

This is a helper module for authors of Node.js native addon modules.
It is basically the "swiss army knife" of `require()`ing your native module's `.node` file.

Throughout the course of Node's native addon history, addons have ended up being compiled in a variety of different places, depending on which build tool and which version of node was used. To make matters worse, now the _gyp_ build tool can produce either a _Release_ or _Debug_ build, each being built into different locations.

This module checks _all_ the possible locations that a native addon would be built at, and returns the first one that loads successfully.

Installation

-----------

Install with `npm`:

```bash
$ npm install bindings
```
Or add it to the "dependencies" section of your _package.json_ file.

Example
-------

`require()`ing the proper bindings file for the current node version, platform and architecture is as simple as:

``` js
var bindings = require('bindings')('binding.node')
// Use your bindings defined in your C files
bindings.your_c_function()
```

Nice Error Output
-----------------

When the `.node` file could not be loaded, `node-bindings` throws an Error with a nice error message telling you exactly what was tried. You can also check the `err.tries` Array property.

```
Error: Could not load the bindings file. Tried:
/Users/nrajlich/ref/build/binding.node
/Users/nrajlich/ref/build/Debug/binding.node
/Users/nrajlich/ref/build/Release/binding.node
/Users/nrajlich/ref/out/Debug/binding.node
/Users/nrajlich/ref/Debug/binding.node
/Users/nrajlich/ref/out/Release/binding.node
/Users/nrajlich/ref/Release/binding.node
/Users/nrajlich/ref/build/default/binding.node
/Users/nrajlich/ref/compiled/0.8.2/darwin/x64/binding.node
    at bindings (/Users/nrajlich/ref/node_modules/bindings/bindings.js:84:13)
    at Object.<anonymous> (/Users/nrajlich/ref/lib/ref.js:5:47)
    at Module._compile (module.js:449:26)
    at Object.Module._extensions..js (module.js:467:10)
    at Module.load (module.js:356:32)
    at Function.Module._load (module.js:312:12)
...```

The searching for the `.node` file will originate from the first directory in which has a `package.json` file is found.
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-------

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1.108 recast 0.10.33

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1.112 requirejs 2.1.22

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 * see: http://github.com/jrburke/requirejs for details
 */

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* /opt/ws_local/PERMITS_SQL/1068891234_1594752192.52/0/requirejs-bower-9cd0b99417eac61e890d11c5119f2e45e752c999-require.js

1.113 lazy-cache 1.0.4

1.113.1 Available under license:
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1.115 har-schema 2.0.0
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1.118 zlib 1.2.8

1.118.1 Available under license :

/* zlib.h -- interface of the 'zlib' general purpose compression library
   version 1.2.11, January 15th, 2017

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# Core team:
#
# These people were responsible for the initial implementations in Java and
# C++, and carry out the bulk of metadata maintenance, bug fixes & feature
# requests, and porting new features to Javascript.

Shaopeng Jia
Lara Rennie
David Yonge-Mallo
David Beaumont

# Additional contributions:
# Javascript
Nikolaos Tronikos  
-- Initial implementation, some subsequent maintenance.

# Java:
Walter Erqunigo  
-- Timezone mapper.
Philippe Liard  
-- Offline geocoder, local Maven expert.
Cecilia Roes  
-- Carrier mapper.
Tom Hofmann  
-- First version of the PhoneNumberMatcher and related classes.
Fabien Allanic
Kushal Pisavadia

# C++:
Patrick Mzard  
-- Geocoding library implementation.
Philippe Liard  
-- Initial open-sourcing of a C++ library, responsible for getting this to work across multiple platforms.
Ben Gertzfield
Fredrik Roubert
George Yakovlev
Nico Weber
Yoshifumi Inoue

# Debian:
Fredrik Roubert

# Metadata:
Alec McTurk
Alexandru Manea
Andrs Eisenberger
Anssi Hannula
Boshi Lian -- Maintains Chinese geocoding data
Bradford Smith
Cecilia Roes
Florian Grisch
Fredrik Roubert
Ian Galpin -- Maintains the data for the UK
Javier Kohen
Jeanine Lilleng
Karen Lees
Khaled Hafez
Lei Zhang
monjiwired@
Philippe Liard  
Sang-il Lee  
Yugui Sonoda  

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Upstream-Contact: Fredrik Roubert <roubert@google.com>
Source: https://github.com/googlei18n/libphonenumber/

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       cpp/src/phonenumbers/base/thread_checker.h
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       cpp/src/phonenumbers/base/memory singleton_posix.h
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DOCUMENTATION ROADMAP
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This file contains the following sections:

OVERVIEW General description of JPEG and the IJG software.
LEGAL ISSUES Copyright, lack of warranty, terms of distribution.
REFERENCES Where to learn more about JPEG.
ARCHIVE LOCATIONS Where to find newer versions of this software.
RELATED SOFTWARE Other stuff you should get.
FILE FORMAT WARS Software *not* to get.
TO DO Plans for future IJG releases.

Other documentation files in the distribution are:

User documentation:
install.doc How to configure and install the IJG software.
usage.doc Usage instructions for cjpeg, djpeg, jpegtran,
rdjpgcom, and wrjpgcom.
*.1 Unix-style man pages for programs (same info as usage.doc).
wizard.doc Advanced usage instructions for JPEG wizards only.
change.log Version-to-version change highlights.

Programmer and internal documentation:
libjpeg.doc How to use the JPEG library in your own programs.
example.c Sample code for calling the JPEG library.
structure.doc Overview of the JPEG library's internal structure.
filelist.doc Road map of IJG files.
coderules.doc Coding style rules --- please read if you contribute code.

Please read at least the files install.doc and usage.doc. Useful information can also be found in the JPEG FAQ (Frequently Asked Questions) article. See ARCHIVE LOCATIONS below to find out where to obtain the FAQ article.

If you want to understand how the JPEG code works, we suggest reading one or more of the REFERENCES, then looking at the documentation files (in roughly
OVERVIEW
========

This package contains C software to implement JPEG image compression and decompression. JPEG (pronounced "jay-peg") is a standardized compression method for full-color and gray-scale images. JPEG is intended for compressing "real-world" scenes; line drawings, cartoons and other non-realistic images are not its strong suit. JPEG is lossy, meaning that the output image is not exactly identical to the input image. Hence you must not use JPEG if you have to have identical output bits. However, on typical photographic images, very good compression levels can be obtained with no visible change, and remarkably high compression levels are possible if you can tolerate a low-quality image. For more details, see the references, or just experiment with various compression settings.

This software implements JPEG baseline, extended-sequential, and progressive compression processes. Provision is made for supporting all variants of these processes, although some uncommon parameter settings aren't implemented yet. For legal reasons, we are not distributing code for the arithmetic-coding variants of JPEG; see LEGAL ISSUES. We have made no provision for supporting the hierarchical or lossless processes defined in the standard.

We provide a set of library routines for reading and writing JPEG image files, plus two sample applications "cjpeg" and "djpeg", which use the library to perform conversion between JPEG and some other popular image file formats. The library is intended to be reused in other applications.

In order to support file conversion and viewing software, we have included considerable functionality beyond the bare JPEG coding/decoding capability; for example, the color quantization modules are not strictly part of JPEG decoding, but they are essential for output to colormapped file formats or colormapped displays. These extra functions can be compiled out of the library if not required for a particular application. We have also included "jpegtran", a utility for lossless transcoding between different JPEG processes, and "rdjpgcom" and "wrjpgcom", two simple applications for inserting and extracting textual comments in JFIF files.

The emphasis in designing this software has been on achieving portability and flexibility, while also making it fast enough to be useful. In particular, the software is not intended to be read as a tutorial on JPEG. (See the REFERENCES section for introductory material.) Rather, it is intended to be reliable, portable, industrial-strength code. We do not claim to have achieved that goal in every aspect of the software, but we strive for it.

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The Unix configuration script "configure" was produced with GNU Autoconf. It is copyright by the Free Software Foundation but is freely distributable. The same holds for its supporting scripts (config.guess, config.sub, ltconfig, ltmain.sh). Another support script, install-sh, is copyright by M.I.T. but is also freely distributable.

It appears that the arithmetic coding option of the JPEG spec is covered by patents owned by IBM, AT&T, and Mitsubishi. Hence arithmetic coding cannot legally be used without obtaining one or more licenses. For this reason, support for arithmetic coding has been removed from the free JPEG software. (Since arithmetic coding provides only a marginal gain over the unpatented Huffman mode, it is unlikely that very many implementations will support it.) So far as we are aware, there are no patent restrictions on the remaining code.

The IJG distribution formerly included code to read and write GIF files. To avoid entanglement with the Unisys LZW patent, GIF reading support has been removed altogether, and the GIF writer has been simplified to produce "uncompressed GIFs". This technique does not use the LZW algorithm; the resulting GIF files are larger than usual, but are readable by all standard GIF decoders.

We are required to state that
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REFERENCES
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We highly recommend reading one or more of these references before trying to understand the innards of the JPEG software.
The best short technical introduction to the JPEG compression algorithm is Wallace, Gregory K. "The JPEG Still Picture Compression Standard", Communications of the ACM, April 1991 (vol. 34 no. 4), pp. 30-44. (Adjacent articles in that issue discuss MPEG motion picture compression, applications of JPEG, and related topics.) If you don't have the CACM issue handy, a PostScript file containing a revised version of Wallace's article is available at ftp://ftp.uu.net/graphics/jpeg/wallace.ps.gz. The file (actually a preprint for an article that appeared in IEEE Trans. Consumer Electronics) omits the sample images that appeared in CACM, but it includes corrections and some added material. Note: the Wallace article is copyright ACM and IEEE, and it may not be used for commercial purposes.

A somewhat less technical, more leisurely introduction to JPEG can be found in "The Data Compression Book" by Mark Nelson and Jean-loup Gailly, published by M&T Books (New York), 2nd ed. 1996, ISBN 1-55851-434-1. This book provides good explanations and example C code for a multitude of compression methods including JPEG. It is an excellent source if you are comfortable reading C code but don't know much about data compression in general. The book's JPEG sample code is far from industrial-strength, but when you are ready to look at a full implementation, you've got one here...


The JPEG standard itself is not available electronically; you must order a paper copy through ISO or ITU. (Unless you feel a need to own a certified official copy, we recommend buying the Pennebaker and Mitchell book instead; it's much cheaper and includes a great deal of useful explanatory material.) In the USA, copies of the standard may be ordered from ANSI Sales at (212) 642-4900, or from Global Engineering Documents at (800) 854-7179. (ANSI doesn't take credit card orders, but Global does.) It's not cheap: as of 1992, ANSI was charging $95 for Part 1 and $47 for Part 2, plus 7% shipping/handling. The standard is divided into two parts, Part 1 being the actual specification, while Part 2 covers compliance testing methods. Part 1 is titled "Digital Compression and Coding of Continuous-tone Still Images, Part 1: Requirements and guidelines" and has document numbers ISO/IEC IS 10918-1, ITU-T T.81. Part 2 is titled "Digital Compression and Coding of Continuous-tone Still Images, Part 2: Compliance testing" and has document numbers ISO/IEC IS 10918-2, ITU-T T.83.

Some extensions to the original JPEG standard are defined in JPEG Part 3, a newer ISO standard numbered ISO/IEC IS 10918-3 and ITU-T T.84. IJG currently does not support any Part 3 extensions.
The JPEG standard does not specify all details of an interchangeable file format. For the omitted details we follow the "JFIF" conventions, revision 1.02. A copy of the JFIF spec is available from:

Literature Department
C-Cube Microsystems, Inc.
1778 McCarthy Blvd.
Milpitas, CA 95035
phone (408) 944-6300, fax (408) 944-6314

A PostScript version of this document is available by FTP at ftp://ftp.uu.net/graphics/jpeg/jfif.ps.gz. There is also a plain text version at ftp://ftp.uu.net/graphics/jpeg/jfif.txt.gz, but it is missing the figures.

The TIFF 6.0 file format specification can be obtained by FTP from ftp://ftp.sgi.com/graphics/tiff/TIFF6.ps.gz. The JPEG incorporation scheme found in the TIFF 6.0 spec of 3-June-92 has a number of serious problems. IJG does not recommend use of the TIFF 6.0 design (TIFF Compression tag 6). Instead, we recommend the JPEG design proposed by TIFF Technical Note #2 (Compression tag 7). Copies of this Note can be obtained from ftp.sgi.com or from ftp://ftp.uu.net/graphics/jpeg/. It is expected that the next revision of the TIFF spec will replace the 6.0 JPEG design with the Note's design. Although IJG's own code does not support TIFF/JPEG, the free libtiff library uses our library to implement TIFF/JPEG per the Note. libtiff is available from ftp://ftp.sgi.com/graphics/tiff/.

ARCHIVE LOCATIONS
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The "official" archive site for this software is ftp.uu.net (Internet address 192.48.96.9). The most recent released version can always be found there in directory graphics/jpeg. This particular version will be archived as ftp://ftp.uu.net/graphics/jpeg/jpegsrc.v6b.tar.gz. If you don't have direct Internet access, UUNET's archives are also available via UUCP; contact help@uunet.uu.net for information on retrieving files that way.

Numerous Internet sites maintain copies of the UUNET files. However, only ftp.uu.net is guaranteed to have the latest official version.

You can also obtain this software in DOS-compatible "zip" archive format from the SimTel archives (ftp://ftp.simtel.net/pub/simtelnet/msdos/graphics/), or on CompuServe in the Graphics Support forum (GO CIS:GRAPHSUP), library 12 "JPEG Tools". Again, these versions may sometimes lag behind the ftp.uu.net release.

The JPEG FAQ (Frequently Asked Questions) article is a useful source of general information about JPEG. It is updated constantly and therefore is
not included in this distribution. The FAQ is posted every two weeks to Usenet newsgroups comp.graphics.misc, news.answers, and other groups. It is available on the World Wide Web at http://www.faqs.org/faqs/jpeg-faq/ and other news.answers archive sites, including the official news.answers archive at rtfm.mit.edu: ftp://rtfm.mit.edu/pub/usenet/news.answers/jpeg-faq/. If you don't have Web or FTP access, send e-mail to mail-server@rtfm.mit.edu with body
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RELATED SOFTWARE
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Numerous viewing and image manipulation programs now support JPEG. (Quite a few of them use this library to do so.) The JPEG FAQ described above lists some of the more popular free and shareware viewers, and tells where to obtain them on Internet.

If you are on a Unix machine, we highly recommend Jef Poskanzer's free PBMPLUS software, which provides many useful operations on PPM-format image files. In particular, it can convert PPM images to and from a wide range of other formats, thus making cjpeg/djpeg considerably more useful. The latest version is distributed by the NetPBM group, and is available from numerous sites, notably ftp://wuarchive.wustl.edu/graphics/graphics/packages/NetPBM/. Unfortunately PBMPLUS/NETPBM is not nearly as portable as the IJG software is; you are likely to have difficulty making it work on any non-Unix machine.

A different free JPEG implementation, written by the PVRG group at Stanford, is available from ftp://havefun.stanford.edu/pub/jpeg/. This program is designed for research and experimentation rather than production use; it is slower, harder to use, and less portable than the IJG code, but it is easier to read and modify. Also, the PVRG code supports lossless JPEG, which we do not. (On the other hand, it doesn't do progressive JPEG.)

FILE FORMAT WARS
================

Some JPEG programs produce files that are not compatible with our library. The root of the problem is that the ISO JPEG committee failed to specify a concrete file format. Some vendors "filled in the blanks" on their own, creating proprietary formats that no one else could read. (For example, none of the early commercial JPEG implementations for the Macintosh were able to exchange compressed files.)

The file format we have adopted is called JFIF (see REFERENCES). This format has been agreed to by a number of major commercial JPEG vendors, and it has
become the de facto standard. JFIF is a minimal or "low end" representation. We recommend the use of TIFF/JPEG (TIFF revision 6.0 as modified by TIFF Technical Note #2) for "high end" applications that need to record a lot of additional data about an image. TIFF/JPEG is fairly new and not yet widely supported, unfortunately.

The upcoming JPEG Part 3 standard defines a file format called SPIFF. SPIFF is interoperable with JFIF, in the sense that most JFIF decoders should be able to read the most common variant of SPIFF. SPIFF has some technical advantages over JFIF, but its major claim to fame is simply that it is an official standard rather than an informal one. At this point it is unclear whether SPIFF will supersede JFIF or whether JFIF will remain the de-facto standard. IJG intends to support SPIFF once the standard is frozen, but we have not decided whether it should become our default output format or not. (In any case, our decoder will remain capable of reading JFIF indefinitely.)

Various proprietary file formats incorporating JPEG compression also exist. We have little or no sympathy for the existence of these formats. Indeed, one of the original reasons for developing this free software was to help force convergence on common, open format standards for JPEG files. Don't use a proprietary file format!

TO DO
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The major thrust for v7 will probably be improvement of visual quality. The current method for scaling the quantization tables is known not to be very good at low Q values. We also intend to investigate block boundary smoothing, "poor man's variable quantization", and other means of improving quality-vs-file-size performance without sacrificing compatibility.

In future versions, we are considering supporting some of the upcoming JPEG Part 3 extensions --- principally, variable quantization and the SPIFF file format.

As always, speeding things up is of great interest.

Please send bug reports, offers of help, etc. to jpeg-info@uunet.uu.net.

1.126 to-buffer 1.1.1

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1.133 indexof 0.0.1

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1.137 is-plain-object 2.0.4

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1.142 accepts 1.3.7

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1.145 setprototypeof 1.1.1

1.146 arraybuffer.slice 0.0.7

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1.149 clone-deep 1.0.0

1.150 expand-template 1.1.1

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1.161 sqlite 3.22.0

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1.162 eyes 0.1.8

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1.163 sprintf-js 1.1.2

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1.164 object-assign 4.1.1

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1.165 base64-arraybuffer 0.1.5
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1.166 npmlog 4.1.2
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1.167 angular-route 1.4.14

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1.168 libcxx 10.0.0

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Albert Pretorius <pretoalb@gmail.com>
Arne Beer <arne@twobeer.de>
Billy Robert O'Neal III <billy.oneal@gmail.com> <bion@microsoft.com>
Chris Kennelly <ckennelly@google.com> <ckennelly@ckennelly.com>
Christopher Seymour <chris.j.seymour@hotmail.com>
Cyrille Faucheux <cyrille.faucheux@gmail.com>
David Coeurjolly <david.coeurjolly@liris.cnrs.fr>
Deniz Evrenci <denizevrenci@gmail.com>
Dominic Hamon <dma@stripysock.com> <dominic@google.com>
Dominik Czarnota <dominik.b.czarnota@gmail.com>
Eric Fiselier <eric@efcs.ca>
Eugene Zhuk <eugene.zhuk@gmail.com>
Evgeny Safronov <division494@gmail.com>
Federico Ficarelli <federico.ficarelli@gmail.com>
Felix Homann <linuxaudio@showlabor.de>
Ismael Jimenez Martinez <ismael.jimenez.martinez@gmail.com>
Jern-Kuan Leong <jernkuan@gmail.com>
JianXiong Zhou <zhoujianxiong2@gmail.com>
Joao Paulo Magalhaes <joaoppmagalhaes@gmail.com>
John Millikin <jmillikin@stripe.com>
Jussi Knuuttila <jussi.knuuttila@gmail.com>
Kai Wolf <kai.wolf@gmail.com>
Kishan Kumar <kumar.kishan@outlook.com>
Kaito Udagawa <umireon@gmail.com>
Lei Xu <eddyxu@gmail.com>
Matt Clarkson <mattyclarkson@gmail.com>
Maxim Vafin <maxvafin@gmail.com>
Nick Hutchinson <nshutchinson@gmail.com>
Oleksandr Sochka <sasha.sochka@gmail.com>
Ori Livneh <ori.livneh@gmail.com>
Pascal Leroy <phl@google.com>
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; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s ;
; D31946
; Check that we dont end up with the "LLVM ERROR: Cannot select" error.
; Additionally ensure that the output code actually put fp128 values in SSE registers.

declare fp128 @llvm.fabs.f128(fp128)
declare fp128 @llvm.copysign.f128(fp128, fp128)

define fp128 @TestSelect(fp128 %a, fp128 %b) {
  %cmp = fcmp ogt fp128 %a, %b
  %sub = fsub fp128 %a, %b
  %res = select i1 %cmp, fp128 %sub, fp128 0xL00000000000000000000000000000000
  ret fp128 %res
}

; CHECK-LABEL: TestSelect:
; CHECK movaps 16(%rsp), %xmm1
; CHECK-NEXT callq __subtf3
; CHECK-NEXT testl %ebx, %ebx
; CHECK-NEXT jg .LBB0_2
; CHECK-NEXT # %bb.1:
; CHECK-NEXT movaps .LCPI0_0(%rip), %xmm0
; CHECK-NEXT .LBB0_2:
; CHECK-NEXT addq $32, %rsp
bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
  bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #1 {
  bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* %arg1) #0 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* noalias noclaim nofree nonnull writeonly align 32 dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define (\[[^@]+\])@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: \[[TMP:%.*\]] = alloca <8 x i64>, align 32
; CHECK-NEXT: \[[TMP2:%.*\]] = alloca <8 x i64>, align 32
; CHECK-NEXT: \[[TMP3:%.*\]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
; CHECK-NEXT: \[[TMP4:%.*\]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
do not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define (\[[^@]+\])@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: \[[TMP:%.*\]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
do not promote
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
; CHECK-LABEL: define (\[[^@]+\])@avx512_legal512_prefer256_call_avx512_legal512_prefer256

define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #2 {
  ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
  ; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: %tmp = load <8 x i64>, <8 x i64>* %arg1
  ; CHECK-NEXT: store <8 x i64> %tmp, <8 x i64>* %arg
  ; CHECK-NEXT: ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
  ; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
  ; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: %tmp = alloca <8 x i64>, align 32
  ; CHECK-NEXT: %tmp2 = alloca <8 x i64>, align 32
  ; CHECK-NEXT: %tmp3 = bitcast <8 x i64>* %tmp to i8*
  ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  ; CHECK-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
  ; CHECK-NEXT: %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  ; CHECK-NEXT: store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ; CHECK-NEXT: ret void
}
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #3 {
  bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1, align 32
    %tmp2 = load <8 x i64>, <8 x i64>* %arg, align 32
    %tmp3 = bitcast <8 x i64>* %tmp2 to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg1, <8 x i64>* %arg)
    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
  bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #3 {
  bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1, align 32
    %tmp2 = load <8 x i64>, <8 x i64>* %arg, align 32
    %tmp3 = bitcast <8 x i64>* %tmp2 to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg1, <8 x i64>* %arg)
    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #4 {
  bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}
open source used in cli analyzer 3.6.6

32, i1 false)
})

; CHECK-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* noalias nocompute nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocompute nofree nonfree nonnull writeonly align 32 dereferenceable(64) [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #4 {
 ; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
 ; CHECK-SAME: (<8 x i64>* noalias nocompute nocompute nonnull writeonly align 32 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* noalias nocompute nocompute nonfree nonnull writeonly align 32 dereferenceable(64) [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
 ; CHECK-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
 ; CHECK-SAME: (<8 x i64>* nocompute writeonly [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP2]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocompute nocompute nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocompute
nofree nonnull readonly align 32 dereferenceable(64) [[TMP]]
; CHECK-NEXT:   [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:   store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:   ret void
;
bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }

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define internal void @innerSmall() "min-legal-vector-width"="128" {
    ret void
}

define internal void @innerLarge() "min-legal-vector-width"="512" {
    ret void
}

define internal void @innerNoAttribute() {
    ret void
}

; We should not add an attribute during inlining. No attribute means unknown.
; Inlining doesn't change the fact that we don't know anything about this
; function.
define void @outerNoAttribute() {
    call void @innerLarge()
    ret void
}

define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
    call void @innerLarge()
    ret void
}

define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
    call void @innerSmall()
    ret void
}

; We should remove the attribute after inlining since the callee's
; vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
    call void @innerNoAttribute()
    ret void
}

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }
; A shuffle mask with all undef elements is always legal.

define <4 x i32> @PR41535(<2 x i32> %p1, <2 x i32> %p2) {
; CHECK-LABEL: PR41535:
; CHECK:       // %bb.0:
; CHECK-NEXT:  ext v0.8b, v0.8b, v1.8b, #4
; CHECK-NEXT:  mov v0.d[1], v0.d[0]
; CHECK-NEXT:  ret
%cat1 = shufflevector <2 x i32> %p1, <2 x i32> undef, <4 x i32> <i32 undef, i32 1, i32 undef, i32 undef>
%cat2 = shufflevector <2 x i32> %p2, <2 x i32> undef, <4 x i32> <i32 0, i32 undef, i32 undef, i32 undef>
%r = shufflevector <4 x i32> %cat1, <4 x i32> %cat2, <4 x i32> <i32 undef, i32 undef, i32 1, i32 4>
ret <4 x i32> %r
}

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Deniz Evrenci <denizevrencai@gmail.com>
Dominic Hamon <dma@stripysock.com> <dominic@google.com>
Dominik Czarnota <dominik.b.czarnota@gmail.com>
Eric Fiselier <eric@efcs.ca>
Eugene Zhuk <eugene.zhuk@gmail.com>
define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
 ; CHECK-LABEL: test_sitofp_fixed:

 ; First, extend each i32 to i64
 ; CHECK-DAG: sshll2.2d [[BLOCK0_HI:v[0-9]+]], v0, #0
 ; CHECK-DAG: sshll2.2d [[BLOCK1_HI:v[0-9]+]], v1, #0
 ; CHECK-DAG: sshll2.2d [[BLOCK2_HI:v[0-9]+]], v2, #0
 ; CHECK-DAG: sshll2.2d [[BLOCK3_HI:v[0-9]+]], v3, #0
 ; CHECK-DAG: sshll.2d [[BLOCK0_LO:v[0-9]+]], v0, #0
 ; CHECK-DAG: sshll.2d [[BLOCK1_LO:v[0-9]+]], v1, #0
 ; CHECK-DAG: sshll.2d [[BLOCK2_LO:v[0-9]+]], v2, #0
 ; CHECK-DAG: sshll.2d [[BLOCK3_LO:v[0-9]+]], v3, #0

 ; Next, convert each to double.
 ; CHECK-DAG: scvtf.2d v0, [[BLOCK0_LO]]
 ; CHECK-DAG: scvtf.2d v1, [[BLOCK0_HI]]
; CHECK-DAG: scvtf.2d v2, [[BLOCK1_LO]]
; CHECK-DAG: scvtf.2d v3, [[BLOCK1_HI]]
; CHECK-DAG: scvtf.2d v4, [[BLOCK2_LO]]
; CHECK-DAG: scvtf.2d v5, [[BLOCK2_HI]]
; CHECK-DAG: scvtf.2d v6, [[BLOCK3_LO]]
; CHECK-DAG: scvtf.2d v7, [[BLOCK3_HI]]

; CHECK: ret
%flt = sitofp <16 x i32> %in to <16 x double>
%res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0>
ret <16 x double> %res
}

; This one is small enough to satisfy isSimple, but still illegally large.
define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
; CHECK-LABEL: test_sitofp_fixed_shortish:

; CHECK-DAG: scvtf.2d v0, v0
; CHECK-DAG: scvtf.2d v1, v1

; CHECK: ret
%flt = sitofp <4 x i64> %in to <4 x double>
%res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
ret <4 x double> %res
}

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add_lldb_library(lldbPluginObjectContainerBSDArchive PLUGIN
ObjectContainerBSDArchive.cpp

LINK_LIBS
   llldbCore
   llldbHost
   llldbSymbol
LINK_COMPONENTS
   Support
)

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; NOTE: Assertions have been autogenerated by utils/update_analyze_test_checks.py
; RUN: opt -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx2 | FileCheck %s --check-prefixes=CHECK,VEC256,AVX
; RUN: opt -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC256,SKX256
define void @zext256() "min-legal-vector-width"="256" {
    ; VEC256-LABEL: 'zext256'
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    
    ; %A = zext <8 x i16> undef to <8 x i64>
    %B = zext <8 x i32> undef to <8 x i64>
    %C = zext <16 x i8> undef to <16 x i32>
    %D = zext <16 x i16> undef to <16 x i32>
    %E = zext <32 x i8> undef to <32 x i16>
    ret void
}

define void @zext512() "min-legal-vector-width"="512" {
    ; AVX-LABEL: 'zext512'
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

define void @sext256() "min-legal-vector-width"="256" {
    %A = sext <8 x i8> undef to <8 x i64>
    %B = sext <8 x i16> undef to <8 x i64>
    %C = sext <16 x i8> undef to <16 x i32>
    %D = sext <16 x i16> undef to <16 x i32>
    %E = sext <32 x i8> undef to <32 x i16>
    ret void
}

define void @sext256() "min-legal-vector-width"="256" {
    %A = sext <8 x i8> undef to <8 x i64>
    %B = sext <8 x i16> undef to <8 x i64>
    %C = sext <16 x i8> undef to <16 x i32>
    %D = sext <16 x i16> undef to <16 x i32>
    %E = sext <32 x i8> undef to <32 x i16>
    ret void
}

define void @sext256() "min-legal-vector-width"="256" {
    %A = sext <8 x i8> undef to <8 x i64>
    %B = sext <8 x i16> undef to <8 x i64>
    %C = sext <16 x i8> undef to <16 x i32>
    %D = sext <16 x i16> undef to <16 x i32>
    %E = sext <32 x i8> undef to <32 x i16>
    ret void
}
;Open Source Used In CLI Analyzer 3.6.6
;
; VEC512-LABEL: 'sext256'
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

define void @sext512() "min-legal-vector-width"="512" { 
; AVX-LABEL: 'sext512'
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'sext512'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;

; VEC512-LABEL: 'sext512'
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

; %A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

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define void @autogen_SD4739(i8*) {
; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
BB:
%L34 = load i8, i8* %0
%Cmp56 = icmp sgt i8 undef, %L34
br label %CF246

CF246: ; preds = %CF246, %BB
%SI163 = select i1 %Cmp56, i8 %L34, i8 undef  
br i1 undef, label %CF246, label %CF248

CF248:  ; preds = %CF248, %CF246
    store i8 %SI163, i8* %0
    br label %CF248
}

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; Verify that fptosi(42.1) isn't simplified when the rounding mode is unknown.
; Verify that no gross errors happen.
; CHECK-LABEL: @f20
; COMMON: cfdctsiz
define i32 @f20(double %a) strictfp {
  entry:
  %result = call i32 @llvm.experimental.constrained.fptosi.i32.f64(double 42.1,
                   metadata !"fpexcept.strict")
  ret i32 %result
}
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; RUN: opt -consthoist -S -o %s | FileCheck %s

target triple = "thumbv6m-none--musleabi"

; Check that for i8 type, the maximum legal offset is 31.
; Also check that an constant used as value to be stored rather than
; pointer in a store instruction is hoisted.
; CHECK: foo_i8
; CHECK-DAG:  %[[C1:const[0-9]??]] = bitcast i32 805874720 to i32
; CHECK-DAG:  %[[C2:const[0-9]??]] = bitcast i32 805874688 to i32
; CHECK-DAG:  %[[C3:const[0-9]??]] = bitcast i32 805873720 to i32
; CHECK-DAG:  %[[C4:const[0-9]??]] = bitcast i32 805873688 to i32
; CHECK:  %0 = inttoptr i32 %[[C2]] to i8*
; CHECK-NEXT:  %1 = load volatile i8, i8* %0
; CHECK-NEXT:  %[[M1:const_mat[0-9]??]] = add i32 %[[C2]], 4
; CHECK-NEXT:  %2 = inttoptr i32 %[[M1]] to i8*
; CHECK-NEXT:  %3 = load volatile i8, i8* %2
; CHECK-NEXT:  %[[M2:const_mat[0-9]??]] = add i32 %[[C2]], 31
; CHECK-NEXT:  %4 = inttoptr i32 %[[M2]] to i8*
; CHECK-NEXT:  %5 = load volatile i8, i8* %4
; CHECK-NEXT:  %6 = inttoptr i32 %[[C1]] to i8*
; CHECK-NEXT:  %7 = load volatile i8, i8* %6
; CHECK-NEXT:  %[[M3:const_mat[0-9]??]] = add i32 %[[C1]], 7
; CHECK-NEXT:  %8 = inttoptr i32 %[[M3]] to i8*
; CHECK-NEXT:  %9 = load volatile i8, i8* %8
; CHECK-NEXT:  %10 = inttoptr i32 %[[C4]] to i8*
; CHECK-NEXT:  store i8 %9, i8* %10
; CHECK-NEXT:  %[[M4:const_mat[0-9]??]] = add i32 %[[C4]], 31
; CHECK-NEXT:  %11 = inttoptr i32 %[[M4]] to i8*
; CHECK-NEXT:  store i8 %7, i8* %11
; CHECK-NEXT:  %12 = inttoptr i32 %[[C3]] to i8*
define void @foo_i8() {
entry:
%0 = load volatile i8, i8* inttoptr (i32 805874688 to i8*)
%1 = load volatile i8, i8* inttoptr (i32 805874692 to i8*)
%2 = load volatile i8, i8* inttoptr (i32 805874719 to i8*)
%3 = load volatile i8, i8* inttoptr (i32 805874720 to i8*)
%4 = load volatile i8, i8* inttoptr (i32 805874727 to i8*)
store i8 %4, i8* inttoptr(i32 805873688 to i8*)
store i8 %3, i8* inttoptr(i32 805873719 to i8*)
store i8 %2, i8* inttoptr(i32 805873720 to i8*)
store i8 %1, i8* inttoptr(i32 805873727 to i8*)
store i8* inttoptr(i32 805874800 to i8*), i8** @goo
ret void
}

define void @foo_i16() {
entry:
%0 = load volatile i16, i16* inttoptr (i32 805874752 to i16*)
%1 = load volatile i16, i16* inttoptr (i32 805874688 to i16*)
%2 = load volatile i16, i16* inttoptr (i32 805874719 to i16*)
%3 = load volatile i16, i16* inttoptr (i32 805874720 to i16*)
%4 = load volatile i16, i16* inttoptr (i32 805874727 to i16*)
store i16 %4, i16* inttoptr(i32 805873688 to i16*)
store i16 %3, i16* inttoptr(i32 805873719 to i16*)
store i16 %2, i16* inttoptr(i32 805873720 to i16*)
store i16 %1, i16* inttoptr(i32 805873727 to i16*)
store i16* inttoptr(i32 805874800 to i16*), i16** @goo
ret void
}
%0 = load volatile i16, i16* inttoptr (i32 805874688 to i16*), align 2
%1 = load volatile i16, i16* inttoptr (i32 805874692 to i16*), align 2
%2 = load volatile i16, i16* inttoptr (i32 805874720 to i16*), align 2
%3 = load volatile i16, i16* inttoptr (i32 805874750 to i16*), align 2
%4 = load volatile i16, i16* inttoptr (i32 805874752 to i16*), align 2
%5 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
ret void

define void @foo_i32() {
entry:
%0 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 4
%1 = load volatile i32, i32* inttoptr (i32 805874692 to i32*), align 4
%2 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
%3 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
%4 = load volatile i32, i32* inttoptr (i32 805874824 to i32*), align 4
%5 = load volatile i32, i32* inttoptr (i32 805874828 to i32*), align 4
ret void
}

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; RUN: llc -march=hexagon < %s
; REQUIRES: asserts

; The two loads based on %struct.0, loading two different data types
; cause LSR to assume type "void" for the memory type. This would then
; cause an assert in isLegalAddressingMode. Make sure we no longer crash.

target triple = "hexagon"

%struct.0 = type { i8*, i8, %union.anon.0 }
%union.anon.0 = type { i8* }

define hidden fastcc void @fred() unnamed_addr #0 {
entry:
  br i1 undef, label %while.end, label %while.body.lr.ph

while.body.lr.ph:                                 ; preds = %entry
  br label %while.body

while.body:                                       ; preds = %exit.2, %while.body.lr.ph
  %lsr.iv = phi %struct.0* [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
  switch i32 undef, label %exit [ i32 1, label %sw.bb.i 
    i32 2, label %sw.bb3.i 
  ]

sw.bb.i:                                          ; preds = %while.body
  unreachable

sw.bb3.i:                                         ; preds = %while.body
  unreachable

exit:                                              ; preds = %while.body
  switch i32 undef, label %exit.2 [ i32 1, label %sw.bb.i17
    i32 2, label %sw.bb3.i20
  ]
sw.bb.i17:          ; preds = %.exit
%0 = bitcast %struct.0* %lsr.iv to i32*
%1 = load i32, i32* %0, align 4
  unreachable

sw.bb3.i20:        ; preds = %exit
%2 = bitcast %struct.0* %lsr.iv to i8**
%3 = load i8*, i8** %2, align 4
  unreachable

exit.2:             ; preds = %exit
%cgep22 = getelementptr %struct.0, %struct.0* %lsr.iv, i32 1
br label %while.body

while.end:          ; preds = %entry
ret void
}

attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }

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; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature --
crubb-attributes
; RUN: opt -S -argpromotion < %s | FileCheck %s
; RUN: opt -S -passes=argpromotion < %s | FileCheck %s
; Test that we only promote arguments when the caller/callee have compatible
; function attributes.

target triple = "x86_64-unknown-linux-gnu"

define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #0 {

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {

bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {

bb:
%tmp = alloc %arg
%tmp2 = alloc %arg
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {

bb:
%tmp = alloc %arg
%tmp2 = alloc %arg
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
  ; CHECK-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
  ; CHECK-NEXT: [[TMPVAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
  ; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64> [[TMPVAL]])
  ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; CHECK-NEXT: ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
  ; CHECK-LABEL: define {{[^@]+}} @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
  ; CHECK-NEXT: ret void
  
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {  
; CHECK-LABEL: define {[^@]+}@avx512_legal512_prefer512_call_avx512_legal512_prefer256  
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])  
; CHECK-NEXT: bb:  
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32  
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32  
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*  
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)  
; CHECK-NEXT: [[TMP_VALUE:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]  
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP_VALUE]])  
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32  
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2  
; CHECK-NEXT: ret void  
}  
bb:  
%tmp = alloca <8 x i64>, align 32  
%tmp2 = alloca <8 x i64>, align 32  
%tmp3 = bitcast <8 x i64>* %tmp to i8*  
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)  
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)  
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32  
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2  
ret void  
}  

; This should promote  
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {  
; CHECK-LABEL: define {[^@]+}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512  
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VALUE:%.*]])  
; CHECK-NEXT: bb:  
; CHECK-NEXT: store <8 x i64> [[ARG1_VALUE]], <8 x i64>* [[ARG]]  
; CHECK-NEXT: ret void  
}  
bb:  
%tmp = load <8 x i64>, <8 x i64>* %arg1  
store <8 x i64> %tmp, <8 x i64>* %arg  
ret void  
}  

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {  
; CHECK-LABEL: define {[^@]+}@avx512_legal512_prefer256_call_avx512_legal512_prefer512  
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])  
; CHECK-NEXT: bb:  
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32  
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32  

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define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg1, <8 x i64>* readonly %arg2) #1 {
    bb:
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
    call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
    call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
    bb:
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
    call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
    call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg1, <8 x i64>* readonly %arg2) #1 {
    bb:
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
    call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
    call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ret void
}
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 {
  ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
  ; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
  ; CHECK-NEXT: ret void
  ;
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
  ; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
  ; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]])
  ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; CHECK-NEXT: ret void
  ;
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg) #3 {
  CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
  CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
  CHECK-NEXT: bb:
  CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
  CHECK-NEXT: ret void

  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}
define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
  CHECK-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
  CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
  CHECK-NEXT: bb:
  CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
  CHECK-NEXT: [[TMP VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
  CHECK-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64> [[TMP VAL]])
  CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  CHECK-NEXT: ret void

  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #4 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [ARG:%.*], <8 x i64> [ARG1_VAL:%.*])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [ARG1_VAL], <8 x i64>* [ARG]
; CHECK-NEXT: ret void

bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
; CHECK-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [ARG:%.*])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]]
; CHECK-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5
attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }

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; NOTE: Assertions have been autogenerated by utils/update_llvm_test_checks.py
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit,avx512vbmi | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; Make sure CPUs default to prefer-256-bit. avx512vnni isn't interesting as it just adds an isel peephole for vpaddwd+vpadd
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cascadelake | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cooperlake | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=cannonlake | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=icelake-client | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=icelake-server | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=tigerlake | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI

; This file primarily contains tests for specific places in X86ISelLowering.cpp that needed be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

define void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="256" {


define void @add512(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="512" {
    %d = load <16 x i32>, <16 x i32>* %a
    %e = load <16 x i32>, <16 x i32>* %b
    %f = add <16 x i32> %d, %e
    store <16 x i32> %f, <16 x i32>* %c
    ret void
}

define void @avg_v64i8_256(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="256" {
    %1 = load <64 x i8>, <64 x i8>* %a
    %2 = load <64 x i8>, <64 x i8>* %b
    %3 = zext <64 x i8> %1 to <64 x i32>
    %4 = zext <64 x i8> %2 to <64 x i32>
    %5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,

define void @avg_v64i8_512(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="512" {  
; CHECK-LABEL: avg_v64i8_512:  
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa64 (%rsi), %zmm0  
; CHECK-NEXT:    vpavgb (%rdi), %zmm0, %zmm0  
; CHECK-NEXT:    vmovdqu64 %zmm0, (%rax)  
; CHECK-NEXT:    vzeroupper  
; CHECK-NEXT:    retq  
%1 = load <64 x i8>, <64 x i8>* %a  
%2 = load <64 x i8>, <64 x i8>* %b  
%3 = zext <64 x i8> %1 to <64 x i32>  
%4 = zext <64 x i8> %2 to <64 x i32>  
%5 = add nuw nsw <64 x i32> %3, %4  
%6 = add nuw nsw <64 x i32> %5, %4  
%7 = lshr <64 x i32> %6, %5, %4  
%8 = trunc <64 x i32> %7 to <64 x i8>  
store <64 x i8> %8, <64 x i8>* undef, align 4  
ret void  
}
; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%A = load <32 x i16>, <32 x i16>* %APtr
%B = load <32 x i16>, <32 x i16>* %BPtr
%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

define void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="512" {
; CHECK-LABEL: pmaddwd_32_512:
; CHECK:  
; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:  vpmaddwd (%rsi), %zmm0, %zmm0
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%A = load <32 x i16>, <32 x i16>* %APtr
%B = load <32 x i16>, <32 x i16>* %BPtr
%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

define void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="256" {
; CHECK-LABEL: psubus_64i8_max_256:
; CHECK:  
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vpmaddwd (%rsi), %ymm0, %ymm0
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%A = load <32 x i16>, <32 x i16>* %APtr
%B = load <32 x i16>, <32 x i16>* %BPtr
%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}
define void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="512" {
; CHECK-LABEL: psubus_64i8_max_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT: vpsubusb (%rsi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %yptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

define void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="512" {
; CHECK-LABEL: psubus_64i8_max_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT: vpsubusb (%rsi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %yptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

define i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {
; CHECK-LABEL: _Z9test_charPcS_i_256:
; CHECK: # %bb.0: # %entry
; CHECK-NEXT: movl %edx, %eax
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: xorl %ecx, %ecx
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT: vpxor %xmm2, %xmm2, %xmm2
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB8_1: # %vector.body
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-NEXT: vpmovsxbw (%rdi,%rcx), %ymm3
; CHECK-NEXT: vpmovsxbw 16(%rdi,%rcx), %ymm4
; CHECK-NEXT: vpmovsxbw (%rsi,%rcx), %ymm5
; CHECK-NEXT: vpmaddwd %ymm3, %ymm5, %ymm3

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; CHECK-NEXT: vpaddd %ymm1, %ymm3, %ymm1
; CHECK-NEXT: vpmovsxrbw 16(%rsi,%rcx), %ymm3
; CHECK-NEXT: vpmaddwd %ymm4, %ymm3, %ymm3
; CHECK-NEXT: vpaddd %ymm2, %ymm3, %ymm2
; CHECK-NEXT: addq $32, %rcx
; CHECK-NEXT: cmpq %rcx, %rax
; CHECK-NEXT: jne .LBB8_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT: vpaddd %ymm0, %ymm1, %ymm1
; CHECK-NEXT: vpaddd %ymm0, %ymm2, %ymm0
; CHECK-NEXT: vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT: vextracti128 s1, %ymm0, %xmm1
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT: vpaddd %ymm0, %xmm0, %xmm0
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT: vpaddd %ymm1, %xmm0, %xmm0
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq

entry:
%3 = zext i32 %2 to i64
br label %vector.body

vector.body:
%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitiializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body

middle.block:
%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undefined
define i32 @_Z9test_charPcS_i_512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: _Z9test_charPcS_i_512:
    ; CHECK:       # %bb.0: # %entry
    ; CHECK-NEXT:    movl %edx, %eax
    ; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
    ; CHECK-NEXT:    xorl %ecx, %ecx
    ; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
    ; CHECK-NEXT:    .p2align 4, 0x90
    ; CHECK-NEXT:  .LBB9_1: # %vector.body
    ; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
    ; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %zmm2
    ; CHECK-NEXT:    vpmovsxbw (%rsi,%rcx), %zmm3
    ; CHECK-NEXT:    vpmaddwd %zmm2, %zmm3, %zmm2
    ; CHECK-NEXT:    vpaddd %zmm1, %zmm2, %zmm1
    ; CHECK-NEXT:    addq $32, %rcx
    ; CHECK-NEXT:    cmpq %rcx, %rax
    ; CHECK-NEXT:    jne .LBB9_1
    ; CHECK-NEXT:  # %bb.2: # %middle.block
    ; CHECK-NEXT:    vpaddd %zmm0, %zmm1, %zmm0
    ; CHECK-NEXT:    vpxor %xmm0, %xmm0, %zmm0
    ; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
    ; CHECK-NEXT:    .p2align 4, 0x90
    ; CHECK-NEXT:  ; LBB9_1: # %vector.body
    ; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
    ; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %zmm2
    ; CHECK-NEXT:    vpmovsxbw (%rsi,%rcx), %zmm3
    ; CHECK-NEXT:    vpmaddwd %zmm2, %zmm3, %zmm2
    ; CHECK-NEXT:    vpaddd %zmm1, %zmm2, %zmm1
    ; CHECK-NEXT:    addq $32, %rcx
    ; CHECK-NEXT:    cmpq %rcx, %rax
    ; CHECK-NEXT:    jne .LBB9_1
    ; CHECK-NEXT:  # %bb.2: # %middle.block
    ; CHECK-NEXT:    vpaddd %zmm0, %zmm1, %zmm0
    ; CHECK-NEXT:    vpxor %xmm0, %xmm0, %zmm0
    ; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
    ; CHECK-NEXT:    .p2align 4, 0x90
    ; CHECK-NEXT:  ; LBB9_1: # %vector.body
    ; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
    ; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %zmm2
    ; CHECK-NEXT:    vpmovsxbw (%rsi,%rcx), %zmm3
    ; CHECK-NEXT:    vpmaddwd %zmm2, %zmm3, %zmm2
    ; CHECK-NEXT:    vpaddd %zmm1, %zmm2, %zmm1
    ; CHECK-NEXT:    addq $32, %rcx
    ; CHECK-NEXT:    cmpq %rcx, %rax
    ; CHECK-NEXT:    jne .LBB9_1
    ; CHECK-NEXT:  # %bb.2: # %middle.block
    ; CHECK-NEXT:    vpaddd %zmm0, %zmm1, %zmm0
    ; CHECK-NEXT:    vpxor %xmm0, %xmm0, %zmm0
    ; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
    ; CHECK-NEXT:    .p2align 4, 0x90
    ; CHECK-NEXT:  ; LBB9_1: # %vector.body
    ; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
    ; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %zmm2
    ; CHECK-NEXT:    vpmovsxbw (%rsi,%rcx), %zmm3
    ; CHECK-NEXT:    vpmaddwd %zmm2, %zmm3, %zmm2
    ; CHECK-NEXT:    vpaddd %zmm1, %zmm2, %zmm1
    ; CHECK-NEXT:    addq $32, %rcx
    ; CHECK-NEXT:    cmpq %rcx, %rax
    ; CHECK-NEXT:    jne .LBB9_1
    ; CHECK-NEXT:  # %bb.2: # %middle.block
    ; CHECK-NEXT:    vpaddd %zmm0, %zmm1, %zmm0
    ; CHECK-NEXT:    vpxor %xmm0, %xmm0, %zmm0
    ; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
    ; CHECK-NEXT:    .p2align 4, 0x90
    ; CHECK-NEXT:  ; LBB9_1: # %vector.body
    ; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
    ; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %zmm2
    ; CHECK-NEXT:    vpmovsxbw (%rsi,%rcx), %zmm3
    ; CHECK-NEXT:    vpmaddwd %zmm2, %zmm3, %zmm2
    ; CHECK-NEXT:    vpaddd %zmm1, %zmm2, %zmm1
    ; CHECK-NEXT:    addq $32, %rcx
    ; CHECK-NEXT:    cmpq %rcx, %rax
    ; CHECK-NEXT:    jne .LBB9_1
}

entry:
\%3 = zext i32 \%2 to i64
br label \%vector.body

vector.body:
\%index = phi i64 [ \%index.next, \%vector.body ], [ 0, \%entry ]
\%vec.phi = phi <32 x i32> [ \%11, \%vector.body ], [ zeroinitialize, \%entry ]
\%4 = getelementptr inbounds i8, i8* \%i, i8* \%0, i64 \%index
\%5 = bitcast i8* \%4 to <32 x i8>*
\%wide.load = load <32 x i8>, <32 x i8>* \%5, align 1
\%6 = sext <32 x i8> to <32 x i32>
\%7 = getelementptr inbounds i8, i8* \%i, i8* \%1, i64 \%index
\%8 = bitcast i8* \%7 to <32 x i8>*
\%wide.load14 = load <32 x i8>, <32 x i8>* \%8, align 1
\%9 = sext <32 x i8> to <32 x i32>
\%10 = mul nsw <32 x i32> \%9, \%6
\%11 = add nsw <32 x i32> \%10, \%vec.phi
\%index.next = add i64 \%index, 32
\%12 = icmp eq i64 \%index.next, \%3
br i1 \%12, label \%middle.block, label \%vector.body

middle.block:
\%rdx.shuf1 = shufflevector <32 x i32> \%11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 unde
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13
}

@a = global [1024 x i8] zeroinitiializer, align 16
@b = global [1024 x i8] zeroinitiializer, align 16

define i32 @sad_16i8_256() "min-legal-vector-width"="256" {
; CHECK-LABEL: sad_16i8_256:
; CHECK:       # %bb.0: # %entry
; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:    movq $-1024, %rax # imm = 0xFC00
; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT:    .p2align 4, 0x90
; CHECK-NEXT:  .LBB10_1: # %vector.body
; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:    vmovdqu a+1024(%rax), %xmm2
; CHECK-NEXT:    vpsadbw b+1024(%rax), %xmm2, %xmm2
; CHECK-NEXT:    vpadd %ymm1, %ymm2, %ymm1
; CHECK-NEXT:    addq $4, %rax
; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vmovd %xmm0, %eax
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
}

entry:
br label %vector.body

vector.body:
%index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
%vec.phi = phi i16 [ <16 x i32> zeroinitializer, %entry ], [ %10, %vector.body ]
%0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
%1 = bitcast i8* %0 to <16 x i8>*
%wide.load = load <16 x i8>, <16 x i8>* %1, align 4
%2 = zext <16 x i8> %wide.load to <16 x i32>
%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
%4 = bitcast i8* %3 to <16 x i8>*
%wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
%5 = zext <16 x i8> %wide.load1 to <16 x i32>
%6 = sub nsw <16 x i32> %2, %5
%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
%8 = sub nsw <16 x i32> zeroinitializer, %6
%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

middle.block:
%.lcssa = phi <16 x i32> [ %10, %vector.body ]
%rdx.shuf = shufflevector <16 x i32> %.lcssa, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %.lcssa, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 8, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12

define i32 @sad_16i8_512() "min-legal-vector-width"="512" {
  ; CHECK-LABEL: sad_16i8_512:
  ; CHECK:    # %bb.0: # %entry
  ; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
  ; CHECK-NEXT: movq $-1024, %rax # imm = 0xFC00
  ; CHECK-NEXT: .p2align 4, 0x90
  ; CHECK-NEXT: .LBB11_1: # %vector.body
  ; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
  ; CHECK-NEXT:      vnmovdq a+1024(%rax), %xmm1
  ; CHECK-NEXT:      vpsadbw b+1024(%rax), %xmm1, %xmm1
  ; CHECK-NEXT:      vpadd %zmm0, %zmm1, %zmm0
  ; CHECK-NEXT:      addq $4, %rax
  ; CHECK-NEXT:      jne .LBB11_1
  ; CHECK-NEXT:    # %bb.2: # %middle.block
define void @ssto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: ssto16f32_256:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:    kshiftrw $8, %k0, %k1
    ; CHECK-NEXT:    vpmovm2d %k1, %ymm0
    ; CHECK-NEXT:    vcvtdq2ps %ymm0, %ymm0
    ; CHECK-NEXT:    vpmovm2d %k0, %ymm1
    ; CHECK-NEXT:    vcvtdq2ps %ymm1, %ymm1
    ; CHECK-NEXT:    vmovaps %ymm1, (%rdi)
    ; CHECK-NEXT:    vmovaps %ymm0, 32(%rdi)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %mask = icmp slt <16 x i16> %a, zeronitializer
    %1 = sitofp <16 x i1> %mask to <16 x float>
    store <16 x float> %1, <16 x float>* %res
    ret void
}

define void @ssto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: ssto16f32_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:    vpmovm2d %k0, %zmm0
    ; CHECK-NEXT:    vcvtdq2ps %zmm0, %zmm0
    ; CHECK-NEXT:    vmovaps %zmm0, (%rdi)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %mask = icmp slt <16 x i16> %a, zeronitializer
    %1 = sitofp <16 x i1> %mask to <16 x float>
    store <16 x float> %1, <16 x float>* %res
    ret void
}

define void @ssto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: ssto16f64_256:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:    kshiftrw $8, %k0, %k1
    ; CHECK-NEXT:    vpmovm2d %k1, %ymm0
    ; CHECK-NEXT:    vcvtdq2ps %ymm0, %ymm0
    ; CHECK-NEXT:    vmovaps %ymm1, (%rdi)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
define void @sbto16f64_512(%a: i16, %res: double*) "min-legal-vector-width"="512" {
    %mask = icmp slt 8 x i16 %a, zeroinitialize
    %lt = sitofp 8 x i1 %mask to 8 x double
    store 8 x double %lt, 8 x double* %res
    ret void
}

define void @ubto16f32_256(%a: i16, %res: float*) "min-legal-vector-width"="256" {
    %mask = icmp slt 8 x i16 %a, zeroinitialize
    %lt = sitofp 8 x i1 %mask to 8 x double
    store 8 x double %lt, 8 x double* %res
    ret void
}
define void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f32_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vpsrld $31, %zmm0, %zmm0
; CHECK-NEXT: vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f64_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm2
; CHECK-NEXT: vpsrld $31, %ymm2, %ymm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT: vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT: vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT: vmovaps %ymm3, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT: vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer

define void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {  
; CHECK-LABEL: ubto16f64_512:  
; CHECK:   # %bb.0:  
; CHECK-NEXT: vpmovw2m %ymm0, %k0  
; CHECK-NEXT: vpmovm2d %k0, %zmm0  
; CHECK-NEXT: vpslld $31, %zmm0, %zmm0  
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm0  
; CHECK-NEXT: vextracti64x4 $1, %zmm0, %ymm0  
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm0  
; CHECK-NEXT: vmovaps %zmm0, 64(%rdi)  
; CHECK-NEXT: vmovaps %zmm1, (%rdi)  
; CHECK-NEXT: vzeroupper  
; CHECK-NEXT: retq  
%mask = icmp slt <16 x i16> %a, zeroinitializer  
%1 = uito fp <16 x i1> %mask to <16 x double>  
store <16 x double> %1, <16 x double>* %res  
ret void  
}
define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: test_16f32tosb_256:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:    vcvttps2dq (%rdi), %ymm1
  ; CHECK-NEXT:    vpmovd2m %ymm1, %k0
  ; CHECK-NEXT:    vcvttps2dq 32(%rdi), %ymm1
  ; CHECK-NEXT:    vpmovd2m %ymm1, %k1
  ; CHECK-NEXT:    kunpckbw %k0, %k1, %k1
  ; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 {%k1} {z}
  ; CHECK-NEXT:    retq
  %a = load <16 x float>, <16 x float>* %ptr
  %mask = fptoui <16 x float> %a to <16 x i1>
  %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitialize
  ret <16 x i16> %select
}

define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {
  ; CHECK-LABEL: test_16f32tosb_512:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:    vcvttps2dq (%rdi), %zmm1
  ; CHECK-NEXT:    vpmovd2m %zmm1, %k1
  ; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 {%k1} {z}
  ; CHECK-NEXT:    retq
  %a = load <16 x float>, <16 x float>* %ptr
  %mask = fptosi <16 x float> %a to <16 x i1>
  %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitialize
  ret <16 x i16> %select
}

define void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {
  ; CHECK-AVX512-LABEL: mul256:
  ; CHECK-AVX512:       # %bb.0:
  ; CHECK-AVX512-NEXT: vmovdqa (%rdi), %ymm0
  ; CHECK-AVX512-NEXT: vmovdqa 32(%rdi), %ymm1
  ; CHECK-AVX512-NEXT: vmovdqa (%rsi), %ymm2
  ; CHECK-AVX512-NEXT: vmovdqa 32(%rsi), %ymm3
}
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} ymm4 =
    ymm3[8], ymm0[8], ymm3[9], ymm0[9], ymm3[10], ymm0[10], ymm3[11], ymm0[11], ymm3[12], ymm0[12], ymm3[13],
    ymm0[13], ymm3[14], ymm0[14], ymm3[15], ymm0[15], ymm3[24], ymm0[24], ymm3[25], ymm0[25], ymm3[26], ymm0[26],
    ymm3[27], ymm0[27], ymm3[28], ymm0[28], ymm3[29], ymm0[29], ymm3[30], ymm0[30], ymm3[31], ymm0[31];
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} ymm5 =
    ymm1[8], ymm0[8], ymm1[9], ymm0[9], ymm1[10], ymm0[10], ymm1[11], ymm0[11], ymm1[12], ymm0[12], ymm1[13],
    ymm0[13], ymm1[14], ymm0[14], ymm1[15], ymm0[15], ymm1[24], ymm0[24], ymm1[25], ymm0[25], ymm1[26], ymm0[26],
    ymm1[27], ymm0[27], ymm1[28], ymm0[28], ymm1[29], ymm0[29], ymm1[30], ymm0[30], ymm1[31], ymm0[31];
; CHECK-AVX512-NEXT:  vpmullw %ymm4, %ymm5, %ymm4
; CHECK-AVX512-NEXT:  vmovdqa {{.*#+}} ymm5 =
; CHECK-AVX512-NEXT:  vpand %ymm5, %ymm4, %ymm4
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} ymm3 =
    ymm3[0], ymm0[0], ymm3[1], ymm0[1], ymm3[2], ymm0[2], ymm3[3], ymm0[3], ymm3[4], ymm0[4], ymm3[5], ymm0[5],
    ymm3[6], ymm0[6], ymm3[7], ymm0[7], ymm3[16], ymm0[16], ymm3[17], ymm0[17], ymm3[18], ymm0[18], ymm3[19],
    ymm0[19], ymm3[20], ymm0[20], ymm3[21], ymm0[21], ymm3[22], ymm0[22], ymm3[23], ymm0[23]
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} ymm1 =
    ymm1[0], ymm0[0], ymm1[1], ymm0[1], ymm1[2], ymm0[2], ymm1[3], ymm0[3], ymm1[4], ymm0[4], ymm1[5], ymm0[5],
    ymm1[6], ymm0[6], ymm1[7], ymm0[7], ymm1[16], ymm0[16], ymm1[17], ymm0[17], ymm1[18], ymm0[18], ymm1[19],
    ymm0[19], ymm1[20], ymm0[20], ymm1[21], ymm0[21], ymm1[22], ymm0[22], ymm1[23], ymm0[23]
; CHECK-AVX512-NEXT:  vpmullw %ymm3, %ymm1, %ymm1
; CHECK-AVX512-NEXT:  vpand %ymm5, %ymm1, %ymm1
; CHECK-AVX512-NEXT:  vpackuswb %ymm4, %ymm1, %ymm1
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} ymm3 =
    ymm2[8], ymm0[8], ymm2[9], ymm0[9], ymm2[10], ymm0[10], ymm2[11], ymm0[11], ymm2[12], ymm0[12], ymm2[13],
    ymm0[13], ymm2[14], ymm0[14], ymm2[15], ymm0[15], ymm2[24], ymm0[24], ymm2[25], ymm0[25], ymm2[26], ymm0[26],
    ymm2[27], ymm0[27], ymm2[28], ymm0[28], ymm2[29], ymm0[29], ymm2[30], ymm0[30], ymm2[31], ymm0[31];
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} ymm4 =
    ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT:  vpmullw %ymm3, %ymm4, %ymm3
; CHECK-AVX512-NEXT:  vpand %ymm5, %ymm3, %ymm3
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} ymm2 =
    ymm2[0], ymm0[0], ymm2[1], ymm0[1], ymm2[2], ymm0[2], ymm2[3], ymm0[3], ymm2[4], ymm0[4], ymm2[5], ymm0[5],
    ymm2[6], ymm0[6], ymm2[7], ymm0[7], ymm2[16], ymm0[16], ymm2[17], ymm0[17], ymm2[18], ymm0[18], ymm2[19],
    ymm0[19], ymm2[20], ymm0[20], ymm2[21], ymm0[21], ymm2[22], ymm0[22], ymm2[23], ymm0[23]
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} ymm0 =
    ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT:  vpmullw %ymm2, %ymm0, %ymm0
; CHECK-AVX512-NEXT:  vpand %ymm5, %ymm0, %ymm0
; CHECK-AVX512-NEXT:  vpackuswb %ymm3, %ymm0, %ymm0
; CHECK-AVX512-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-AVX512-NEXT:  vmovdqa %ymm1, 32(%rdx)
; CHECK-AVX512-NEXT:  vzeroupper
; CHECK-AVX512-NEXT:  retq
;
; CHECK-VBMI-LABEL: mul256:
; CHECK-VBMI: # %bb.0:
; CHECK-VBMI-NEXT: vmovq (%rdi), %ymm0
; CHECK-VBMI-NEXT: vmovq 32(%rdi), %ymm1
; CHECK-VBMI-NEXT: vmovq (%rsi), %ymm2
; CHECK-VBMI-NEXT: vmovq 32(%rsi), %ymm3
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm4 = ymm3[8], ymm0[8], ymm3[9], ymm0[9], ymm3[10], ymm0[10], ymm3[11], ymm0[11], ymm3[12], ymm0[12], ymm3[13], ymm0[13], ymm3[14], ymm0[14], ymm3[15], ymm0[15], ymm3[24], ymm0[24], ymm3[25], ymm0[25], ymm3[26], ymm0[26], ymm3[27], ymm0[27], ymm3[28], ymm0[28], ymm3[29], ymm0[29], ymm3[30], ymm0[30], ymm3[31], ymm0[31]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm5 = ymm1[8], ymm0[8], ymm1[9], ymm0[9], ymm1[10], ymm0[10], ymm1[11], ymm0[11], ymm1[12], ymm0[12], ymm1[13], ymm0[13], ymm1[14], ymm0[14], ymm1[15], ymm0[15], ymm1[24], ymm0[24], ymm1[25], ymm0[25], ymm1[26], ymm0[26], ymm1[27], ymm0[27], ymm1[28], ymm0[28], ymm1[29], ymm0[29], ymm1[30], ymm0[30], ymm1[31], ymm0[31]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm3 = ymm3[0], ymm0[0], ymm3[1], ymm0[1], ymm3[2], ymm0[2], ymm3[3], ymm0[3], ymm3[4], ymm0[4], ymm3[5], ymm0[5], ymm3[6], ymm0[6], ymm3[7], ymm0[7], ymm3[16], ymm0[16], ymm3[17], ymm0[17], ymm3[18], ymm0[18], ymm3[19], ymm0[19], ymm3[20], ymm0[20], ymm3[21], ymm0[21], ymm3[22], ymm0[22], ymm3[23], ymm0[23]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm1 = ymm1[0], ymm0[0], ymm1[1], ymm0[1], ymm1[2], ymm0[2], ymm1[3], ymm0[3], ymm1[4], ymm0[4], ymm1[5], ymm0[5], ymm1[6], ymm0[6], ymm1[7], ymm0[7], ymm1[16], ymm0[16], ymm1[17], ymm0[17], ymm1[18], ymm0[18], ymm1[19], ymm0[19], ymm1[20], ymm0[20], ymm1[21], ymm0[21], ymm1[22], ymm0[22], ymm1[23], ymm0[23]
; CHECK-VBMI-NEXT: vpnullw %ymm3, %ymm1
; CHECK-VBMI-NEXT: vpmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT: vpmullw %ymm3, %ymm1
; CHECK-VBMI-NEXT: vpermt2b %ymm4, %ymm3, %ymm1
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm4 = ymm2[8], ymm0[8], ymm2[9], ymm0[9], ymm2[10], ymm0[10], ymm2[11], ymm0[11], ymm2[12], ymm0[12], ymm2[13], ymm0[13], ymm2[14], ymm0[14], ymm2[15], ymm0[15], ymm2[24], ymm0[24], ymm2[25], ymm0[25], ymm2[26], ymm0[26], ymm2[27], ymm0[27], ymm2[28], ymm0[28], ymm2[29], ymm0[29], ymm2[30], ymm0[30], ymm2[31], ymm0[31]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm5 = ymm0[8], ymm9[8], 10, 10, 11, 11, 12, 12, 13, 13, 14, 14, 15, 15, 16, 24, 24, 25, 25, 26, 26, 27, 27, 28, 28, 29, 29, 30, 30, 31, 31
; CHECK-VBMI-NEXT: vpnullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm2 = ymm2[0], ymm0[0], ymm2[1], ymm0[1], ymm2[2], ymm0[2], ymm2[3], ymm0[3], ymm2[4], ymm0[4], ymm2[5], ymm0[5], ymm2[6], ymm0[6], ymm2[7], ymm0[7], ymm2[16], ymm0[16], ymm2[17], ymm0[17], ymm2[18], ymm0[18], ymm2[19], ymm0[19], ymm2[20], ymm0[20], ymm2[21], ymm0[21], ymm2[22], ymm0[22], ymm2[23], ymm0[23]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm0 = ymm0[0, 0, 1, 1, 2, 2, 3, 3, 4, 4, 5, 5, 6, 6, 7, 7, 16, 16, 17, 17, 18, 18, 19, 19, 20, 20, 21, 21, 22, 22, 23, 23]
; CHECK-VBMI-NEXT: vpnullw %ymm2, %ymm0, %ymm0
; CHECK-VBMI-NEXT: vpmullw %ymm3, %ymm0, %ymm0
; CHECK-VBMI-NEXT: vzeroupper
define void @mul512(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="512" {
; CHECK-AVX512-LABEL: mul512:
; CHECK-AVX525:
; # %bb.0:
; CHECK-AVX525-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-AVX525-NEXT: vmovdqa64 (%rsi), %zmm1
; CHECK-AVX525-NEXT: vpunpckhfwb {{.*#+}} zmm2 =
    zmm1[8],zmm0[8],zmm1[9],zmm0[9],zmm1[10],zmm0[10],zmm1[11],zmm0[11],zmm1[12],zmm0[12],zmm1[13],
    zmm0[13],zmm1[14],zmm0[14],zmm1[15],zmm0[15],zmm1[24],zmm0[24],zmm1[25],zmm0[25],zmm1[26],zmm0
    [26],zmm1[27],zmm0[27],zmm1[28],zmm0[28],zmm1[29],zmm0[29],zmm1[30],zmm0[30],zmm1[31],zmm0[31],
    z
    mm1[40],zmm0[40],zmm1[41],zmm0[41],zmm1[42],zmm0[42],zmm1[43],zmm0[43],zmm1[44],zmm0[44],zmm1[45],
    zmm0[45],zmm1[46],zmm0[46],zmm1[47],zmm0[47],zmm1[56],zmm0[56],zmm1[57],zmm0[57],zmm1[58],z
    mm0[58],zmm1[59],zmm0[59],zmm1[60],zmm0[60],zmm1[61],zmm0[61],zmm1[62],zmm0[62],zmm1[63],zmm0[63]
; CHECK-AVX525-NEXT: vpunpckhfwb {{.*#+}} zmm3 =
    zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
    2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX525-NEXT: vpmullw %zmm2, %zmm3, %zmm2
; CHECK-AVX525-NEXT: vpmullw %zmm1, %zmm0, %zmm0
; CHECK-AVX525-NEXT: vpmullw %zmm1, %zmm0, %zmm0
; CHECK-AVX525-NEXT: vpackuswb %zmm2, %zmm0, %zmm0
; CHECK-AVX525-NEXT: vzeroupper
; CHECK-AVX525-NEXT: retq
; CHECK-VBMI-LABEL: retq
# %bb.0:
}
; CHECK-VBMI-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-VBMI-NEXT:  vmovdqa64 (%rsi), %zmm1
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} zmm2 =
; CHECK-VBMI-NEXT:  zmm1[8],zmm0[8],zmm1[9],zmm0[9],zmm1[10],zmm0[10],zmm1[11],zmm0[11],zmm1[12],zmm0[12],zmm1[13],
zmm0[13],zmm1[14],zmm0[14],zmm1[15],zmm0[15],zmm1[16],zmm0[16],zmm1[17],zmm0[17],zmm1[18],zmm0[18],zmm1[19],
zmm0[19],zmm1[20],zmm0[20],zmm1[21],zmm0[21],zmm1[22],zmm0[22],zmm1[23],zmm0[23],zmm1[24],zmm0[24],
zmm1[25],zmm0[25],zmm1[26],zmm0[26],zmm1[27],zmm0[27],zmm1[28],zmm0[28],zmm1[29],zmm0[29],zmm1[30],zmm0[30],
zmm1[31],zmm0[31],zmm1[32],zmm0[32],zmm1[33],zmm0[33],zmm1[34],zmm0[34],zmm1[35],zmm0[35],zmm1[36],zmm0[36],
zmm1[37],zmm0[37],zmm1[38],zmm0[38],zmm1[39],zmm0[39],zmm1[40],zmm0[40],zmm1[41],zmm0[41],zmm1[42],
zmm0[42],zmm1[43],zmm0[43],zmm1[44],zmm0[44],zmm1[145],zmm0[45],zmm1[46],zmm0[46],zmm1[47],zmm0[47],
zmm1[48],zmm0[48],zmm1[49],zmm0[49],zmm1[50],zmm0[50],zmm1[51],zmm0[51],zmm1[52],zmm0[52],zmm1[53],
zmm0[53],zmm1[54],zmm0[54],zmm1[55],zmm0[55],zmm1[56],zmm0[56],zmm1[57],zmm0[57],zmm1[58],zmm0[58],
zmm1[59],zmm0[59],zmm1[60],zmm0[60],zmm1[61],zmm0[61],zmm1[62],zmm0[62],zmm1[63],zmm0[63]
; CHECK-VBMI-NEXT:  vpunpckhlbw {{.*#+}} zmm3 =
; CHECK-VBMI-NEXT:  zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,42,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} zmm2 =
; CHECK-VBMI-NEXT:  zmm1[8],zmm0[8],zmm1[9],zmm0[9],zmm1[10],zmm0[10],zmm1[11],zmm0[11],zmm1[12],zmm0[12],zmm1[13],
zmm0[13],zmm1[14],zmm0[14],zmm1[15],zmm0[15],zmm1[16],zmm0[16],zmm1[17],zmm0[17],zmm1[18],zmm0[18],zmm1[19],
zmm0[19],zmm1[20],zmm0[20],zmm1[21],zmm0[21],zmm1[22],zmm0[22],zmm1[23],zmm0[23],zmm1[24],zmm0[24],
zmm1[25],zmm0[25],zmm1[26],zmm0[26],zmm1[27],zmm0[27],zmm1[28],zmm0[28],zmm1[29],zmm0[29],zmm1[30],zmm0[30],
zmm1[31],zmm0[31],zmm1[32],zmm0[32],zmm1[33],zmm0[33],zmm1[34],zmm0[34],zmm1[35],zmm0[35],zmm1[36],zmm0[36],
zmm1[37],zmm0[37],zmm1[38],zmm0[38],zmm1[39],zmm0[39],zmm1[40],zmm0[40],zmm1[41],zmm0[41],zmm1[42],
zmm0[42],zmm1[43],zmm0[43],zmm1[44],zmm0[44],zmm1[45],zmm0[45],zmm1[46],zmm0[46],zmm1[47],zmm0[47],
zmm1[48],zmm0[48],zmm1[49],zmm0[49],zmm1[50],zmm0[50],zmm1[51],zmm0[51],zmm1[52],zmm0[52],zmm1[53],
zmm0[53],zmm1[54],zmm0[54],zmm1[55],zmm0[55],zmm1[56],zmm0[56],zmm1[57],zmm0[57],zmm1[58],zmm0[58],
zmm1[59],zmm0[59],zmm1[60],zmm0[60],zmm1[61],zmm0[61],zmm1[62],zmm0[62],zmm1[63],zmm0[63]
; CHECK-VBMI-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-VBMI-NEXT:  vpunpckhlbw {{.*#+}} zmm1 =
; CHECK-VBMI-NEXT:  zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,42,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT:  vpnullw %zmm2, %zmm3, %zmm2
; CHECK-VBMI-NEXT:  vpmullw %zmm1, %zmm0, %zmm0
; CHECK-VBMI-NEXT:  vpmullw %zmm0, %zmm0, %zmm0
; CHECK-VBMI-NEXT:  vpmullw %zmm0, %zmm0, %zmm0
; CHECK-VBMI-NEXT:  vpmullw %zmm1, %zmm0, %zmm0
; CHECK-VBMI-NEXT:  vpmullw %zmm2, %zmm0, %zmm0
; CHECK-VBMI-NEXT:  vpermil2b %zmm1, %zmm2, %zmm0, %zmm0
; CHECK-VBMI-NEXT:  vpmovdqa64 %zmm1, (%rdx)
; CHECK-VBMI-NEXT:  vzeroupper
; CHECK-VBMI-NEXT:  retq
%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void
}

; This threw an assertion at one point.
define <4 x i32> @mload_v4i32(<4 x i32> %trigger, <4 x i32>* %addr, <4 x i32> %dst) "min-legal-vector-width"="256" {
; CHECK-LABEL: mload_v4i32:
; CHECK:  # %bb.0:
; CHECK-NEXT:  vptestnmd %xmm0, %xmm0, %k1
; CHECK-NEXT:  vpmullw (%rdi), %xmm1, %xmm0 { %k1 }
; CHECK-NEXT:  retq
%mask = icmp eq <4 x i32> %trigger, zeroinitialize
%res = call <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* %addr, i32 4, <4 x i1> %mask, <4 x i32> %dst)
ret <4 x i32> %res
}
declare <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* %addr, i32 4, <4 x i1> %mask, <4 x i32> %dst)

define <16 x i32> @trunc_v16i64_v16i32(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
 ; CHECK-LABEL: trunc_v16i64_v16i32:
 ; CHECK:    # %bb.0:
 ; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
 ; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
 ; CHECK-NEXT:    vmovdqa 64(%rdi), %ymm2
 ; CHECK-NEXT:    vmovdqa 96(%rdi), %ymm3
 ; CHECK-NEXT:    vpmovqd %ymm0, %xmm0
 ; CHECK-NEXT:    vpmovqd %ymm1, %xmm1
 ; CHECK-NEXT:    vpmovqd %ymm2, %xmm2
 ; CHECK-NEXT:    vpmovqd %ymm3, %xmm3
 ; CHECK-NEXT:    vpmovqd %ymm1, %ymm1
 ; CHECK-NEXT:    vpmovqd %ymm3, %ymm3
 ; CHECK-NEXT:    vpmovqd %ymm2, %ymm2
 ; CHECK-NEXT:    vpmovqd %ymm0, %ymm0
 ; CHECK-NEXT:    vpmovq %xmm0, %mmm0
 ; CHECK-NEXT:    vpmovq %xmm1, %mmm1
 ; CHECK-NEXT:    vpmovq %xmm2, %mmm2
 ; CHECK-NEXT:    vpmovq %xmm3, %mmm3
 ; CHECK-NEXT:    vzeroupper
 ; CHECK-NEXT:    retq
%a = load <16 x i64>, <16 x i64>* %x
%b = trunc <16 x i64> %a to <16 x i32>
ret <16 x i32> %b
}

define <16 x i8> @trunc_v16i64_v16i8(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
 ; CHECK-LABEL: trunc_v16i64_v16i8:
 ; CHECK:    # %bb.0:
 ; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
 ; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
 ; CHECK-NEXT:    vmovdqa 64(%rdi), %ymm2
 ; CHECK-NEXT:    vmovdqa 96(%rdi), %ymm3
 ; CHECK-NEXT:    vpmovq %ymm3, %xmm3
 ; CHECK-NEXT:    vpmovq %ymm2, %xmm2
 ; CHECK-NEXT:    vpmovq %ymm1, %xmm1
 ; CHECK-NEXT:    vpmovq %ymm0, %xmm0
 ; CHECK-NEXT:    vpmovq %xmm2, %mm2
 ; CHECK-NEXT:    vpmovq %xmm1, %mm1
 ; CHECK-NEXT:    vpmovq %xmm0, %mm0
 ; CHECK-NEXT:    vzeroupper
 ; CHECK-NEXT:    retq
%a = load <16 x i64>, <16 x i64>* %x
%b = trunc <16 x i64> %a to <16 x i8>
ret <16 x i8> %b
}

define <16 x i8> @trunc_v16i32_v16i8(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
 ; CHECK-LABEL: trunc_v16i32_v16i8:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovdb %ymm1, %xmm1
; CHECK-NEXT:  vpmovdb %ymm0, %xmm0
; CHECK-NEXT:  vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm1[0]
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <16 x i32>, <16 x i32>* %x
%b = trunc <16 x i32> %a to <16 x i8>
ret <16 x i8> %b
}

define <8 x i8> @trunc_v8i64_v8i8(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {  
; CHECK-LABEL:  trunc_v8i64_v8i8:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovqb %ymm1, %xmm1
; CHECK-NEXT:  vpmovqb %ymm0, %xmm0
; CHECK-NEXT:  vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <8 x i64>, <8 x i64>* %x
%b = trunc <8 x i64> %a to <8 x i8>
ret <8 x i8> %b
}

define <8 x i16> @trunc_v8i64_v8i16(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {  
; CHECK-LABEL:  trunc_v8i64_v8i16:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovqw %ymm1, %xmm1
; CHECK-NEXT:  vpmovqw %ymm0, %xmm0
; CHECK-NEXT:  vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <8 x i64>, <8 x i64>* %x
%b = trunc <8 x i64> %a to <8 x i16>
ret <8 x i16> %b
}

define <8 x i32> @trunc_v8i64_v8i32_zeroes(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {  
; CHECK-LABEL:  trunc_v8i64_v8i32_zeroes:
; CHECK:       # %bb.0:
; CHECK-NEXT:  vpsrlq $48, 32(%rdi), %ymm1
; CHECK-NEXT:  vpsrlq $48, (%rdi), %ymm2
define <16 x i16> @trunc_v16i32_v16i16_sign(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {  
    ; CHECK-LABEL: trunc_v16i32_v16i16_sign:  
    ; CHECK:       # %bb.0:  
    ; CHECK-NEXT:    vmovdqa (%rdi), %ymm1  
    ; CHECK-NEXT:    vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]  
    ; CHECK-NEXT:    vpermi2b 32(%rdi), %ymm1, %ymm0  
    ; CHECK-NEXT:    retq  
    %a = load <16 x i32>, %x  
    %b = ashr <16 x i32> %a, <132 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16>  
    %c = trunc <16 x i32> %b to i16  
    ret <16 x i16> %c  
}
define void @zext_v16i8_v16i64(<16 x i8> %x, <16 x i64>/* %y) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: zext_v16i8_v16i64:
    ; CHECK:    # %bb.0:
    ; CHECK-NEXT: vpmoveqb [({.*#})] ymm1 =
    ; xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero
    ; CHECK-NEXT: vpshufd [{.*#}] xmm2 = xmm1[2,3,0,1]
    ; CHECK-NEXT: vpmovzxbw [({.*#})] ymm2 =
    ; xmm2[0],zero,zero,xmm2[1],zero,zero,zero,xmm2[2],zero,zero,zero,xmm2[3],zero,zero,zero
    ; CHECK-NEXT: vextracti128 $1, %ymm1, %xmm1
    ; CHECK-NEXT: vpshufd [{.*#}] ymm3 =
    ; xmm3[0],zero,zero,xmm3[1],zero,zero,zero,xmm3[2],zero,zero,zero,xmm3[3],zero,zero,zero
    ; CHECK-NEXT: vpmovzxbq [({.*#})] ymm0 =
    ; xmm0[0],zero,zero,zero,zero,xmm0[1],zero,zero,zero,zero,xmm0[2],zero,zero,zero,zero,xmm0[3],zero,zero,zero,zero,zero,zero,zero,zero
    ; CHECK-NEXT: vmovdqa %ymm0, (%rdi)
    ; CHECK-NEXT: vmovdqa %ymm1, 64(%rdi)
    ; CHECK-NEXT: vmovdqa %ymm2, 32(%rdi)
    ; CHECK-NEXT: retq
    %a = zext <16 x i8> %x to <16 x i64>
    store <16 x i64> %a, <16 x i64>/* %y
    ret void
}
%a = sext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}

define void @vselect_split_v8i16_setcc(<8 x i16> %s, <8 x i16> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v8i16_setcc:
; CHECK: 
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa32(%rsi), %ymm3
; CHECK-NEXT: vpempqew %xmm1, %xmm0, %k1
; CHECK-NEXT: kshiftrb $4, %k1, %k2
; CHECK-NEXT: vmovdqa64 32(%rdi), %ymm3 [%k2]
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
%a = icmp eq <8 x i16> %s, %t
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}

define void @vselect_split_v8i32_setcc(<8 x i32> %s, <8 x i32> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v8i32_setcc:
; CHECK: 
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa32(%rsi), %ymm3
; CHECK-NEXT: vpempqewd %xmm1, %xmm0, %k1
; CHECK-NEXT: kshiftrb $4, %k1, %k2
; CHECK-NEXT: vmovdqa64 32(%rdi), %ymm3 [%k2]
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
%a = icmp eq <8 x i32> %s, %t
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}
define void @vselect_split_v16i8_setcc(<16 x i8> %s, <16 x i8> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" {  
; CHECK-LABEL: vselect_split_v16i8_setcc:  
; CHECK: # %bb.0:  
; CHECK-NEXT: vmovdqa (%rsi), %ymm2  
; CHECK-NEXT: vmovdqa %ymm3  
; CHECK-NEXT: vpcmpeqb %xmm1, %xmm0, %k1  
; CHECK-NEXT: kshiftrw $8, %k1, %k2  
; CHECK-NEXT: vmovdqa32 %rdi, %ymm3 [%k2]  
; CHECK-NEXT: vmovdqa32 %rdi, %ymm2 [%k1]  
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)  
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)  
; CHECK-NEXT: vzeroupper  
; CHECK-NEXT: retq  
%x = load <16 x i32>, <16 x i32>* %p  
%y = load <16 x i32>, <16 x i32>* %q  
%a = icmp eq <16 x i8> %s, %t  
%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y  
store <16 x i32> %b, <16 x i32>* %r  
ret void  
}

define void @vselect_split_v16i16_setcc(<16 x i16> %s, <16 x i16> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" {  
; CHECK-LABEL: vselect_split_v16i16_setcc:  
; CHECK: # %bb.0:  
; CHECK-NEXT: vmovdqa (%rsi), %ymm2  
; CHECK-NEXT: vmovdqa32 (%rsi), %ymm3  
; CHECK-NEXT: vpcmpeqw %ymm1, %ymm0, %k1  
; CHECK-NEXT: kshiftrw $8, %k1, %k2  
; CHECK-NEXT: vmovdqa32 %rdi, %ymm3 [%k2]  
; CHECK-NEXT: vmovdqa32 %rdi, %ymm2 [%k1]  
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)  
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)  
; CHECK-NEXT: vzeroupper  
; CHECK-NEXT: retq  
%x = load <16 x i32>, <16 x i32>* %p  
%y = load <16 x i32>, <16 x i32>* %q  
%a = icmp eq <16 x i16> %s, %t  
%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y  
store <16 x i32> %b, <16 x i32>* %r  
ret void  
}

define <16 x i8> @trunc_packus_v16i32_v16i8(<16 x i32>* %p) "min-legal-vector-width"="256" {  
; CHECK-LABEL: trunc_packus_v16i32_v16i8:  
; CHECK: # %bb.0:
define void @v64i8_shuffle(<64 x i8>* %x, <64 x i8>* %y) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: v64i8_shuffle:
    ; CHECK-NEXT:    retq
    retq
}
CHECK-NEXT: kandq %k2, %k1, %k1
CHECK-NEXT: kshiftrd $6, %k0, %k2
CHECK-NEXT: kshiftlq $63, %k2, %k2
CHECK-NEXT: kshiftrq $56, %k2, %k2
CHECK-NEXT: korq %k2, %k1, %k1
CHECK-NEXT: movq $-257, %rax # imm = 0xFEFF
CHECK-NEXT: kmovq %rax, %k2
CHECK-NEXT: kandq %k2, %k1, %k1
CHECK-NEXT: kshiftrd $9, %k0, %k2
CHECK-NEXT: kshiftlq $63, %k2, %k2
CHECK-NEXT: kshiftrq $55, %k2, %k2
CHECK-NEXT: korq %k2, %k1, %k1
CHECK-NEXT: movq $-513, %rax # imm = 0xFDFF
CHECK-NEXT: kmovq %rax, %k2
CHECK-NEXT: kandq %k2, %k1, %k1
CHECK-NEXT: kshiftrd $8, %k0, %k2
CHECK-NEXT: kshiftlq $63, %k2, %k2
CHECK-NEXT: kshiftrq $54, %k2, %k2
CHECK-NEXT: korq %k2, %k1, %k1
CHECK-NEXT: movq $-1025, %rax # imm = 0xFBFF
CHECK-NEXT: kmovq %rax, %k2
CHECK-NEXT: kandq %k2, %k1, %k1
CHECK-NEXT: kshiftrd $10, %k0, %k2
CHECK-NEXT: kshiftlq $63, %k2, %k2
CHECK-NEXT: kshiftrq $52, %k2, %k2
CHECK-NEXT: korq %k2, %k1, %k1
CHECK-NEXT: movq $-2049, %rax # imm = 0xF7FF
CHECK-NEXT: kmovq %rax, %k2
CHECK-NEXT: kandq %k2, %k1, %k1
CHECK-NEXT: kshiftrd $11, %k0, %k2
CHECK-NEXT: kshiftlq $63, %k2, %k2
CHECK-NEXT: kshiftrq $51, %k2, %k2
CHECK-NEXT: korq %k2, %k1, %k1
CHECK-NEXT: movq $-4097, %rax # imm = 0xEFFF
CHECK-NEXT: kmovq %rax, %k2
CHECK-NEXT: kandq %k2, %k1, %k1
CHECK-NEXT: kshiftrd $13, %k0, %k2
CHECK-NEXT: kshiftlq $63, %k2, %k2
CHECK-NEXT: kshiftrq $50, %k2, %k2
CHECK-NEXT: korq %k2, %k1, %k1
CHECK-NEXT: movq $-8193, %rax # imm = 0xDFFF
CHECK-NEXT: kmovq %rax, %k2
CHECK-NEXT: kandq %k2, %k1, %k1
CHECK-NEXT: kshiftrd $12, %k0, %k2
CHECK-NEXT: kshiftlq $63, %k2, %k2
CHECK-NEXT: kshiftrq $50, %k2, %k2
CHECK-NEXT: korq %k2, %k1, %k1
CHECK-NEXT: movq $-16385, %rax # imm = 0xBFFF

Open Source Used In CLI Analyzer 3.6.6  420
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftd $15, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $49, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-32769, %rax # imm = 0xFFFF7FFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftd $14, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $48, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-65537, %rax # imm = 0xFFFFEFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftd $17, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $47, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-131073, %rax # imm = 0xFFFFDFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftd $16, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $46, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-262145, %rax # imm = 0xFFFFBFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftd $19, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $45, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-524289, %rax # imm = 0xFFE7FFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftd $18, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $44, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-1048577, %rax # imm = 0xFFEFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftd $21, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $43, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1

Open Source Used In CLI Analyzer 3.6.6  421
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-268435457, %rax # imm = 0xFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $29, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftq $35, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-536870913, %rax # imm = 0xFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $28, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftq $34, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-1073741825, %rax # imm = 0xBFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $31, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftq $33, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movabsq $-2147483649, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $30, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k0, %k0
; CHECK-NEXT: kshiftq $32, %k0, %k0
; CHECK-NEXT: korq %k0, %k2, %k0
; CHECK-NEXT: movabsq $-4294967297, %rax # imm = 0xFFFFFFFFFFEFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k0, %k0
; CHECK-NEXT: kshiftq $31, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-8589934593, %rax # imm = 0xFFFFFFFFFDFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-17179869185, %rax # imm = 0xFFFFFFFFBFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT:   kshiftrq $29, %k2, %k2
; CHECK-NEXT:   korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $.34359738369, %rax  # imm = 0xFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $2, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $28, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $.68719476737, %rax  # imm = 0xFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $5, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $27, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $.137438953473, %rax  # imm = 0xFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $4, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $26, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $.274877906945, %rax  # imm = 0xFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $7, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $25, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $.549755813889, %rax  # imm = 0xFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $6, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $24, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $.1099511627777, %rax  # imm = 0xFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $9, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $23, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $.2199023255553, %rax  # imm = 0xFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $8, %k1, %k2

Open Source Used In CLI Analyzer 3.6.6  424
; CHECK-NEXT:  kshiftrq $22, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-4398046511105, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $11, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $21, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-8796093022209, %rax # imm = 0xFFFFFFFF7FFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $10, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $20, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-17592186044417, %rax # imm = 0xFFFFFFFF7FFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $9, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $19, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-35184372088833, %rax # imm = 0xFFFFFFFF7FFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $8, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $18, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-70368744177665, %rax # imm = 0xFFFFFFFF7FFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $7, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $17, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-140737488355329, %rax # imm = 0xFFFFFFFF7FFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $6, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $16, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-281474976710657, %rax # imm = 0xFFFFFFFF7FFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $17, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $15, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-562949953421313, %rax # imm = 0xFFDDFFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $16, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $14, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-1125899906842625, %rax # imm = 0xFFFBFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $19, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $13, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-2251799813685249, %rax # imm = 0xFF7FFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $18, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $12, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-4503599627370497, %rax # imm = 0xFFF7FFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $21, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $11, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-9007199254740993, %rax # imm = 0xFFDDFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $20, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $10, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-18014398509481985, %rax # imm = 0xFFBFFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $23, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $9, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-36028797018963969, %rax # imm = 0xFF7FFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshift $22, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshift $8, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-72057594037927937, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshift $25, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshift $7, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-144115188075855873, %rax # imm = 0xPDFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshift $24, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshift $6, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-288230376151711745, %rax # imm = 0xFBBFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshift $27, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshift $5, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-576460752303423489, %rax # imm = 0xF7FFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshift $26, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshift $4, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-1152921504606846977, %rax # imm = 0xEFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshift $29, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshift $3, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-2305843009213693953, %rax # imm = 0xBFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshift $28, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshift $2, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-4611686018427387905, %rax # imm = 0xBFFFFFFFFFFFFFF
; CHECK-NEXT:  kmov %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $31, %k1, %k2
; CHECK-NEXT:  kshiftlq $62, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $30, %k1, %k1
; CHECK-NEXT:  kshiftlq $63, %k1, %k1
; CHECK-NEXT:  korq %k1, %k0, %k1
; CHECK-NEXT:  vmovdqu8 %ymm1, (%rsi) {%k1}
; CHECK-NEXT:  kshiftrq $32, %k1, %k1
; CHECK-NEXT:  vmovdqu8 %ymm0, 32(%rsi) {%k1}
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq

entry:
%a = load <64 x i8>, <64 x i8>* %x
%b = icmp eq <64 x i8> %a, zeroinitializer
%shuf = shufflevector <64 x i1> %b, <64 x i1> undef, <64 x i32> <i32 1, i32 0, i32 3, i32 2, i32 5, i32 4, i32 7, i32 6, i32 9, i32 8, i32 11, i32 10, i32 13, i32 12, i32 15, i32 14, i32 17, i32 16, i32 19, i32 18, i32 21, i32 20, i32 23, i32 22, i32 25, i32 24, i32 27, i32 26, i32 29, i32 28, i32 31, i32 30, i32 33, i32 32, i32 35, i32 34, i32 37, i32 36, i32 39, i32 38, i32 41, i32 40, i32 43, i32 42, i32 45, i32 43, i32 44, i32 47, i32 46, i32 49, i32 48, i32 51, i32 50, i32 53, i32 52, i32 55, i32 54, i32 57, i32 56, i32 59, i32 58, i32 61, i32 60, i32 63, i32 62>
call void @llvm.masked.store.v64i8.p0v64i8(<64 x i8> %a, <64 x i8>* %y, <64 x i1> %shuf)
ret void
}
declare void @llvm.masked.store.v64i8.p0v64i8(<64 x i8>, <64 x i8>*, i32, <64 x i1>)

@mem64_dst = global i64 0, align 8
@mem64_src = global i64 0, align 8
define i32 @v64i1_inline_asm() "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_inline_asm:
; CHECK: # %bb.0:
; CHECK-NEXT:  kmovq {{.*}}(%rip), %k0
; CHECK-NEXT:  #APP
; CHECK-NEXT:  #NO_APP
; CHECK-NEXT:  kmovq %k0, {{.*}}(%rip)
; CHECK-NEXT:  movl -{{[0-9]+}}(%rsp), %eax
; CHECK-NEXT:  retq

%1 = alloca i32, align 4
%2 = load i64, i64* @mem64_src, align 8
%3 = call i64 asm "", "=k,k,~{dirflag},~{fpsr},~{flags}"(i64 %2)
store i64 %3, i64* @mem64_dst, align 8
%4 = load i32, i32* %1, align 4
ret i32 %4
}
1.169 stringmap 0.2.2

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1.170 koalas 1.0.2

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1.171 ansi-gray 0.1.1
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1.172 proxy-from-env 1.1.0
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1.173 socks 2.3.3

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1.174 jquery 3.4.1

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1.175 delegates 1.0.0

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1.178 toidentifier 1.0.0

1.179 base64id 2.0.0

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1.180 extend 3.0.2

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1.183 yallist 2.1.2

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1.185 pify 3.0.0

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1.187 yeast 0.1.2

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1.227 ansi-bgcyan 0.1.1

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1.232 async 2.6.3

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1.237 noop-logger 0.1.1

1.238 pinkie-promise 2.0.1

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1.240 psl 1.8.0
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1.243 ansi-wrap 0.1.0

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1.244 color 3.0.0

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In 1995, Guido continued his work on Python at the Corporation for National Research Initiatives (CNRI, see http://www.cnri.reston.va.us) in Reston, Virginia where he released several versions of the software.

In May 2000, Guido and the Python core development team moved to BeOpen.com to form the BeOpen PythonLabs team. In October of the same year, the PythonLabs team moved to Digital Creations, which became Zope Corporation. In 2001, the Python Software Foundation (PSF, see https://www.python.org/psf/) was formed, a non-profit organization created specifically to own Python-related Intellectual Property. Zope Corporation was a sponsoring member of the PSF.

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1.246 stack-trace 0.0.10

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iconv (Charset Conversion Library) v2.0

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      (For example, a function in a library to compute square roots has a purpose that is entirely well-defined independent of the application. Therefore, Subsection 2d requires that any application-supplied function or table used by this function must be optional: if the application does not supply it, the square root function must still compute square roots.)

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1.249 stable 0.1.8

1.250 acorn 5.7.4

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1.251 arr-swap 1.0.1

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1.254 has-ansi 2.0.0
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> Check if a string has [ANSI escape codes](http://en.wikipedia.org/wiki/ANSI_escape_code)

```
# has-ansi ![Build Status](https://travis-ci.org/sindresorhus/has-ansi.svg?branch=master)

## Install

```
$ npm install --save has-ansi
```

## Usage

```
```
var hasAnsi = require('has-ansi');

hasAnsi('[4mcake[0m');
//=> true

hasAnsi('cake');
//=> false
```

## Related

- [has-ansi-cli](https://github.com/sindresorhus/has-ansi-cli) - CLI for this module
- [strip-ansi](https://github.com/sindresorhus/strip-ansi) - Strip ANSI escape codes
- [ansi-regex](https://github.com/sindresorhus/ansi-regex) - Regular expression for matching ANSI escape codes
- [chalk](https://github.com/sindresorhus/chalk) - Terminal string styling done right

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### 1.255 aws4 1.10.0

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1.256 ansi-reset 0.1.1

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1.257 ssh2 0.5.5
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1.258 winston-transport 4.4.0
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1.259 terminal-paginator 2.0.2

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1.260 serialport-parser-ready 1.0.5

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1.261 ansi-blue 0.1.1

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1.262 path-is-inside 1.0.2

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1.263 cliff 0.1.10

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validate-npm-package-license

Give me a string and I'll tell you if it's a valid npm package license string.

```javascript
var valid = require('validate-npm-package-license');
```

SPDX license identifiers are valid license strings:

```javascript
var assert = require('assert');
var validSPDXExpression = {
  validForNewPackages: true,
  validForOldPackages: true,
  spdx: true
};
assert.deepEqual(valid('MIT'), validSPDXExpression);
assert.deepEqual(valid('BSD-2-Clause'), validSPDXExpression);
assert.deepEqual(valid('Apache-2.0'), validSPDXExpression);
assert.deepEqual(valid('ISC'), validSPDXExpression);
```

The function will return a warning and suggestion for nearly-correct license identifiers:

```javascript
assert.deepEqual(
  valid('Apache 2.0'),
  {
    validForOldPackages: false,
  });
```
validForNewPackages: false,
warnings: [
  'license should be ' +
  'a valid SPDX license expression (without "LicenseRef"), ' +
  ""UNLICENSED"", or ' +
  ""SEE LICENSE IN <filename>"
  'license is similar to the valid expression "Apache-2.0"
]
}
);```

SPDX expressions are valid, too ...

```javascript
// Simple SPDX license expression for dual licensing
assert.deepEqual(
valid('(GPL-3.0-only OR BSD-2-Clause)'),
validSPDXExpression
);
```

... except if they contain `LicenseRef`:

```javascript
var warningAboutLicenseRef = {
validForOldPackages: false,
validForNewPackages: false,
spdx: true,
warnings: [
  'license should be ' +
  'a valid SPDX license expression (without "LicenseRef"), ' +
  ""UNLICENSED"", or ' +
  ""SEE LICENSE IN <filename>"
]
};

assert.deepEqual(
valid('LicenseRef-Made-Up'),
warningAboutLicenseRef
);

assert.deepEqual(
valid('(MIT OR LicenseRef-Made-Up)'),
warningAboutLicenseRef
);
```
If you can't describe your licensing terms with standardized SPDX identifiers, put the terms in a file in the package and point users there:

```javascript
assert.deepEqual(
valid('SEE LICENSE IN LICENSE.txt'),
{
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  validForOldPackages: true,
  inFile: 'LICENSE.txt'
}
);

assert.deepEqual(
valid('SEE LICENSE IN license.md'),
{
  validForNewPackages: true,
  validForOldPackages: true,
  inFile: 'license.md'
}
);
```  

If there aren't any licensing terms, use `UNLICENSED`:

```javascript
var unlicensed = {
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  validForOldPackages: true,
  unlicensed: true
};
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assert.deepEqual(valid('UNLICENCED'), unlicensed);
```  

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Open Source Used in CLI Analyzer 3.6.6 765
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"openssl/crypto/x509v3/v3_extku.c",
"openssl/crypto/x509v3/v3_genn.c",
"openssl/crypto/x509v3/v3_i5.c",
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"openssl/crypto/x509v3/v3_int.c",
"openssl/crypto/x509v3/v3_lib.c",
"openssl/crypto/x509v3/v3_ncons.c",
"openssl/crypto/x509v3/v3_pci.c",
"openssl/crypto/x509v3/v3_pciac.c",
"openssl/crypto/x509v3/v3_pcons.c",
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"openssl/crypto/x509v3/v3_sxnet.c",
"openssl/crypto/x509v3/v3_tlsf.c",
"openssl/crypto/x509v3/v3_utl.c",
"openssl/crypto/x509v3/v3_err.c",
"openssl/engines/e_capi.c",
"openssl/engines/e_padlock.c",

"openssl_sources_BSD-x86_64": 
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  ".config/archs/bsd-x86_64/asm/crypto/aes/aesni-sb-x86_64.s",
  ".config/archs/bsd-x86_64/asm/crypto/aes/aesni-sha1-x86_64.s",
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  ".config/archs/bsd-x86_64/asm/crypto/aes/aesni-x86_64.s",
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  ".config/archs/bsd-x86_64/asm/crypto/aes/vpaes-x86_64.s",
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'.\config\archs\BSD-x86_64\asm\crypto\x86_64cpuid.s',
'.\config\archs\BSD-x86_64\asm\engines\e_padlock-x86_64.s',
],
'openssl_defines_BSD-x86_64': [
'DSO_DLFCN',
'HAVE_DLFCN_H',
'NDEBUG',
'OPENSSL_THREADS',
'OPENSSL_NO_DYNAMIC_ENGINE',
'OPENSSL_PIC',
'OPENSSL_IA32_SSE2',
'OPENSSL_bn_asm_mont',
'OPENSSL_bn_asm_mont5',
'OPENSSL_bn_asm_gf2m',
'SHA1_ASM',
'SHA256_ASM',
'SHA512_ASM',
'RC4_ASM',
'MD5_ASM',
'AES_ASM',
'VPAES_ASM',
'BSAES_ASM',
'GHASH_ASM',
'ECP_NISTZ256_ASM',
'PADLOCK_ASM',
'POLY1305_ASM',
],
'openssl_cflags_BSD-x86_64': [
'-DL_ENDIAN -Wall -O3 -pthread -D_THREAD_SAFE -D_REENTRANT',
],
'openssl_ex_libs_BSD-x86_64': [
'',
],
'include_dirs': [
'',
'./include',
}
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# spdx-license-ids


A list of [SPDX license](https://spdx.org/licenses/) identifiers

## Installation

[Download JSON directly](https://raw.githubusercontent.com/shinnn/spdx-license-ids/master/index.json), or [use](https://docs.npmjs.com/cli/install) [npm](https://docs.npmjs.com/getting-started/what-is-npm):

```
```
```
## Node.js API

### require('spdx-license-ids')

Type: `Array<string>`

All license IDs except for the currently deprecated ones.

```javascript
const ids = require('spdx-license-ids');
//=> ['0BSD', 'AAL', 'Abstyles', 'Adobe-2006', 'Adobe-Glyph', 'ADSL', 'AFL-1.1', ...
ids.includes('BSD-3-Clause'); //=> true
ids.includes('CC-BY-1.0'); //=> true
ids.includes('GPL-3.0'); //=> false
```  

### require('spdx-license-ids/deprecated')

Type: `Array<string>`

Deprecated license IDs.

```javascript
const deprecatedIds = require('spdx-license-ids/deprecated');
//=> ['AGPL-3.0', 'eCos-2.0', 'GFDL-1.1', 'GFDL-1.2', 'GFDL-1.3', 'GPL-1.0', ...
deprecatedIds.includes('BSD-3-Clause'); //=> false
deprecatedIds.includes('CC-BY-1.0'); //=> false
deprecatedIds.includes('GPL-3.0'); //=> true
```  

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Open Source Used In CLI Analyzer 3.6.6 833
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// Original can be found at:
//   https://bitbucket.org/lindenlab/llsd
// Modifications by Joshua Bell inexorabltesh@gmail.com
//   https://github.com/inexorabltesh/polyfill

// ES3/ES5 implementation of the Khronos Typed Array Specification
// Ref: http://www.khronos.org/registry/typedarray/specs/latest/
// Date: 2011-02-01
//
// Variations:
// * Allows typed_array.get/set() as alias for subscripts (typed_array[])

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wcwidth.js: JavaScript Porting of Markus Kuhn's wcwidth() Implementation
=======================================================================
Copyright (C) 2012 by Jun Woong.

This package is a JavaScript porting of `wcwidth()` implementation
[by Markus Kuhn](http://www.cl.cam.ac.uk/~mgk25/ucs/wcwidth.c).

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> defence README.md | replace-require-self | node

1.275 ansi-magenta 0.1.1

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1.276 callsite 1.0.0

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1.277 ansi-italic 0.1.1
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1.278 ngsmoothscroll 2.0.0

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 * Angular Smooth Scroll (ngSmoothScroll)
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Found in path(s):
* /opt/ws_local/PERMITS_SQL/1068891434_1594433027.74/0/ngsmoothscroll-0af06ce6ff3b30f21ed2dcae85bdbd934a6b75d4-zip/ngSmoothScroll-0af06ce6ff3b30f21ed2dcae85bdbd934a6b75d4/dist/angular-smooth-scroll.min.js

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 * Angular Smooth Scroll (ngSmoothScroll)
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 * Callback hooks contributed by Ben Armston https://github.com/benarmston
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1.279 component-bind 1.0.0

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1.281 ansi-bold 0.1.1

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1.282 simple-concat 1.0.0

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1.283 lodash-merge 4.6.2

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1.286 zlib 1.2.11

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/* zlib.h -- interface of the 'zlib' general purpose compression library
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Jean-loup Gailly        Mark Adler
jloup@gzip.org          madler@alumni.caltech.edu

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1.287 safe-buffer 5.2.1

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1.288 ansi-bgmagenta 0.1.1

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1.289 promirepl 1.0.1

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1.292 requirejs-domready 2.0.1

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1.293 ng-grid 2.0.14

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1.297 iconv-lite 0.4.24

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1.298 prompt-base 4.1.0

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1.299 vis 4.15.1

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**1.300 libcxxabi 10.0.0**

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; RUN: llc -mtriple=s390x-linux-gnu -mcpu=zEC12 -verify-machineinstrs | FileCheck %s
;
; Test that early if conversion produces LOCR with operands of the right
; register classes.

define void @autogen_SD4739(i8*) {
; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
BB:
  %L34 = load i8, i8* %0
  %Cmp56 = icmp sgt i8 undef, %L34
  br label %CF246
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; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx2 | FileCheck %s --check-prefixes=CHECK,VEC256,AVX
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC256,SKX256
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,-prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC512

define void @zext256() "min-legal-vector-width"="256" {
   ; VEC256-LABEL: 'zext256'
   ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
   ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
   ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
   ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x i32>
   ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
   ; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

define void @zext512() "min-legal-vector-width"="512" {
    AVX-LABEL: 'zext512'
    AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    SKX256-LABEL: 'zext512'
    SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    VEC512-LABEL: 'zext512'
    VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
}
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = zext <8 x i16> undef to <8 x i64>
%B = zext <8 x i32> undef to <8 x i64>
%C = zext <16 x i8> undef to <16 x i32>
%D = zext <16 x i16> undef to <16 x i32>
%E = zext <32 x i8> undef to <32 x i16>
ret void

define void @sext256() "min-legal-vector-width"="256" {
 ; VEC256-LABEL: 'sext256'
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x i32>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
 ;
 ; VEC512-LABEL: 'sext256'
 ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
 ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
 ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
 ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
 ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
 ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
 ; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
 ;
%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
define void @sext512() "min-legal-vector-width"="512" {
  ; AVX-LABEL: 'sext512'
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

  ; SKX256-LABEL: 'sext512'
  ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
  ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
  ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
  ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
  ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
  ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
  ; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

  ; VEC512-LABEL: 'sext512'
  ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
  ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
  ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
  ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
  ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
  ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
  ; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

  ; AVX-STORE: %A = sext <8 x i8> undef to <8 x i64>
  ; AVX-STORE: %B = sext <8 x i16> undef to <8 x i64>
  ; AVX-STORE: %C = sext <8 x i32> undef to <8 x i64>
}

Open Source Used In CLI Analyzer 3.6.6 910
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}
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LLVM System Interface Library

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; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s ;
; D31946
; Check that we dont end up with the ""LLVM ERROR: Cannot select" error.
; Additionally ensure that the output code actually put fp128 values in SSE registers.

define fp128 @TestSelect(fp128 %a, fp128 %b) {
  %cmp = fcmp ogt fp128 %a, %b
  %sub = fsub fp128 %a, %b
  %res = select i1 %cmp, fp128 %sub, fp128 0xL00000000000000000000000000000000
  ret fp128 %res

; CHECK-LABEL: TestSelect:
; CHECK movaps i64(%rsp), %xmm1
; CHECK-NEXT callq __subtf3
; CHECK-NEXT testl %ebx, %ebx
; CHECK-NEXT jg .LBB0_2
; CHECK-NEXT # %bb.1:
; CHECK-NEXT movaps .LCPI0_0(%rip), %xmm0
; CHECK-NEXT .LBB0_2:
; CHECK-NEXT addq $32, %rsp
; CHECK-NEXT popq %rbx
; CHECK-NEXT retq
}

define fp128 @TestFabs(fp128 %a) {
  %res = call fp128 @llvm.fabs.f128(fp128 %a)
  ret fp128 %res
}

define fp128 @TestCopysign(fp128 %a, fp128 %b) {
  %res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
  ret fp128 %res
}

define fp128 @TestFneg(fp128 %a) {
  %mul = fmul fp128 %a, %a
  %res = fsub fp128 0xL00000000000000008000000000000000, %mul
  ret fp128 %res
}

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*/
; RUN: llc -march=hexagon < %s
; REQUIRES: asserts

; The two loads based on %struct.0, loading two different data types
; cause LSR to assume type "void" for the memory type. This would then
; cause an assert in isLegalAddressingMode. Make sure we no longer crash.

target triple = "hexagon"

%struct.0 = type { i8*, i8, %union.anon.0 }
%union.anon.0 = type { i8* }

define hidden fastcc void @fred() unnamed_addr #0 {
entry:
br i1 undef, label %while.end, label %while.body.lr.ph

while.body.lr.ph: ; preds = %entry
br label %while.body

while.body: ; preds = %exit.2, %while.body.lr.ph
%lsr.iv = phi %struct.0* [%cgep22, %exit.2], [ undef, %while.body.lr.ph ]
switch i32 undef, label %exit [
i32 1, label %sw.bb.i
i32 2, label %sw.bb3.i
]

sw.bb.i: ; preds = %while.body
unreachable

sw.bb3.i: ; preds = %while.body
unreachable

exit: ; preds = %while.body
switch i32 undef, label %exit.2 [
i32 1, label %sw.bb.i17
i32 2, label %sw.bb3.i20
]

sw.bb.i17: ; preds = %exit
%0 = bitcast %struct.0* %lsr.iv to i32*
%1 = load i32, i32* %0, align 4
unreachable

sw.bb3.i20: ; preds = %exit
%2 = bitcast %struct.0* %lsr.iv to i8**
%3 = load i8*, i8** %2, align 4
unreachable
exit.2: ; preds = %exit
%cg22 = getelementptr %struct.0, %struct.0* %lsr.iv, i32 1
br label %while.body

while.end: ; preds = %entry
  ret void
}

attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }
; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s
define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
  ; CHECK-LABEL: test_sitofp_fixed:

  ; First, extend each i32 to i64
  ; CHECK-DAG: sshll2.2d [[BLOCK0_HI:v[0-9]+]], v0, #0
  ; CHECK-DAG: sshll2.2d [[BLOCK1_HI:v[0-9]+]], v1, #0
  ; CHECK-DAG: sshll2.2d [[BLOCK2_HI:v[0-9]+]], v2, #0
  ; CHECK-DAG: sshll2.2d [[BLOCK3_HI:v[0-9]+]], v3, #0
  ; CHECK-DAG: sshll.2d [[BLOCK0_LO:v[0-9]+]], v0, #0
  ; CHECK-DAG: sshll.2d [[BLOCK1_LO:v[0-9]+]], v1, #0
  ; CHECK-DAG: sshll.2d [[BLOCK2_LO:v[0-9]+]], v2, #0
  ; CHECK-DAG: sshll.2d [[BLOCK3_LO:v[0-9]+]], v3, #0

  ; Next, convert each to double.
  ; CHECK-DAG: scvtf.2d v0, [[BLOCK0_LO]]
  ; CHECK-DAG: scvtf.2d v1, [[BLOCK0_HI]]
  ; CHECK-DAG: scvtf.2d v2, [[BLOCK1_LO]]
  ; CHECK-DAG: scvtf.2d v3, [[BLOCK1_HI]]
  ; CHECK-DAG: scvtf.2d v4, [[BLOCK2_LO]]
  ; CHECK-DAG: scvtf.2d v5, [[BLOCK2_HI]]
  ; CHECK-DAG: scvtf.2d v6, [[BLOCK3_LO]]
  ; CHECK-DAG: scvtf.2d v7, [[BLOCK3_HI]]

  ; CHECK: ret
  %flt = sitofp <16 x i32> %in to <16 x double>
  %res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0>
  ret <16 x double> %res
}

; This one is small enough to satisfy isSimple, but still illegally large.
declare function @test_sitofp_fixed_shortish(<4 x i64> %in) {
  ; CHECK-LABEL: test_sitofp_fixed_shortish:

  ; CHECK-DAG: scvtf.2d v0, v0
  ; CHECK-DAG: scvtf.2d v1, v1
; CHECK: ret
%flt = sitofp <4 x i64> %in to <4 x double>
%res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
ret <4 x double> %res
}

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; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature --scrub-attributes
; RUN: opt -S -argpromotion < %s | FileCheck %s
; RUN: opt -S -passes=argpromotion < %s | FileCheck %s
; Test that we only promote arguments when the caller/callee have compatible function attributes.

target triple = "x86_64-unknown-linux-gnu"

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {

; CHECK-LABEL: define ([[^@]+])@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void

; bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
    CHECK-LABEL: define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
    CHECK-NEXT: bb:
        %tmp = alloca <8 x i64>, align 32
        %tmp2 = alloca <8 x i64>, align 32
        %tmp3 = bitcast <8 x i64>* %tmp to i8*
        call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
        call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
        %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
        store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
        ret void
    }

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
    CHECK-LABEL: define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
    CHECK-NEXT: bb:
        %tmp = load <8 x i64>, <8 x i64>* %arg1
        store <8 x i64> %tmp, <8 x i64>* %arg
        ret void
    }

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
    CHECK-LABEL: define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
    CHECK-NEXT: bb:

define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
  bb: %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
  bb: %tmp = load <8 x i64>, <8 x i64>* %arg
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; This should promote
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

: This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
  ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
  ; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
  ; CHECK-NEXT: ret void
  
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
  ; CHECK-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
  ; CHECK-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]])
  ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; CHECK-NEXT: ret void
  
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 {
 ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
 ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
 ; CHECK-NEXT: bb:
 ; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
 ; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
 ; CHECK-NEXT: ret void

bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
 ; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
 ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
 ; CHECK-NEXT: bb:
 ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
 ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
 ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
 ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
 ; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]])
 ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
 ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
 ; CHECK-NEXT: ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(\<8 x i64\>* %arg, \<8 x i64\>*%arg1) #3 {
  ; CHECK-LABEL: define \{[^\@]+\}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
  ; CHECK-SAME: (\<8 x i64\>* [[ARG:%.*]], \<8 x i64\> [[ARG1_VAL:.]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: store \<8 x i64\> [[ARG1_VAL]], \<8 x i64\>* [[ARG]]
  ; CHECK-NEXT: ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(\<8 x i64\>* %arg, \<8 x i64\>*%arg1) #4 {
  ; CHECK-LABEL: define \{[^\@]+\}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
  ; CHECK-SAME: (\<8 x i64\>* [[ARG:%.*]], \<8 x i64\> [[ARG1_VAL:.]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: store \<8 x i64\> [[ARG1_VAL]], \<8 x i64\>* [[ARG]]
  ; CHECK-NEXT: ret void
}
define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5
attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }

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; RUN: opt -S -passes='attributor' -aa-pipeline='basic-aa' -attributor-disable=false -attributor-max-iterations-verify -attributor-max-iterations=2 < %s | FileCheck %s
; Test that we only promote arguments when the caller/callee have compatible
; function attributes.

target triple = "x86_64-unknown-linux-gnu"

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
 ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
 ; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull align 32 dereferenceable(64) 
|[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) |[ARG1:%.*]])
 ; CHECK-NEXT: bb:
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {  
  bb:  
  %tmp = load <8 x i64>, <8 x i64>* %arg  
  store <8 x i64> %tmp, <8 x i64>* %arg  
  ret void  
}

define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #1 {  
  bb:  
  %tmp = load <8 x i64>, <8 x i64>* %arg1  
  store <8 x i64> %tmp, <8 x i64>* %arg  
  ret void  
}

; This should promote  
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #1 {  
  bb:  
  %tmp = load <8 x i64>, <8 x i64>* %arg1  
  store <8 x i64> %tmp, <8 x i64>* %arg  
  ret void  
}

; This should promote  
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #1 {  
  bb:  
  %tmp = load <8 x i64>, <8 x i64>* %arg1  
  store <8 x i64> %tmp, <8 x i64>* %arg  
  ret void  
}
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
               ; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
               ; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:.%*]])
               ; CHECK-NEXT: bb:
               ; CHECK-NEXT:  %tmp = alloca <8 x i64>, align 32
               ; CHECK-NEXT:  %tmp2 = alloca <8 x i64>, align 32
               ; CHECK-NEXT:  %tmp3 = bitcast <8 x i64>* %tmp to i8*
               ; CHECK-NEXT:  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
               ; CHECK-NEXT:  call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
               ; CHECK-NEXT:  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
               ; CHECK-NEXT:  call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #1 {
               ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
               ; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[ARG:.%*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:.%*]])
               ; CHECK-NEXT: bb:
               ; CHECK-NEXT:  %tmp = load <8 x i64>, <8 x i64>* %arg1
               ; CHECK-NEXT:  store <8 x i64> %tmp, <8 x i64>* %arg
               ; ret void
               
               ; This should promote
               define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
               ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
               ; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[ARG:.%*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:.%*]])
               ; CHECK-NEXT: bb:
               ; CHECK-NEXT:  %tmp = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
               ; CHECK-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG1]], align 32
               ; CHECK-NEXT:  ret void
               ;
               ; bb:
               ; %tmp = load <8 x i64>, <8 x i64>* %arg1

store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
  ; CHECK-LABEL: define {[^@]+}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:.%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP2:.%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP3:.%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nonfree nonnull align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nonfree nonnull readonly align 32 dereferenceable(64) [[TMP]])
  ; CHECK-NEXT: [[TMP4:.%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; CHECK-NEXT: ret void
  
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* %arg1) #0 {
  ; CHECK-LABEL: define {[^@]+}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
  ; CHECK-SAME: (<8 x i64>* noalias nocapture nonfree nonnull writeonly align 32 dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nonfree nonnull readonly align 32 dereferenceable(64) [[ARG1:.%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:.%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 2
  ; CHECK-NEXT: ret void
  
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
    ; CHECK-LABEL: define (\([^@]+\)) @avx512_legal512_prefer256_call_avx512_legal512_prefer512
    ; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]]))
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
    ; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
    ; CHECK-NEXT: ([TMP4:%.*]) = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
    ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
    ; CHECK-NEXT: ret void
    }

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
    ; CHECK-LABEL: define (\([^@]+\)) @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (<8 x i64>* noalias n[oca][n]ot free nonnull writeonly align 32 dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree non[null] readonly align 32 dereferenceable(64) [[ARG1:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
    ; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
    ; CHECK-NEXT: ret void
    ;
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
    ; CHECK-LABEL: define (\([^@]+\)) @avx512_legal512_prefer256_call_avx512_legal512_prefer256

; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
; CHECK-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:  ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 {
  ; CHECK-LABEL: define [[^*]+]@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
  ; CHECK-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
  ; CHECK-NEXT:  ret void

  ; bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
  ; CHECK-LABEL: define [[^*]+]@avx512_legal512_prefer256_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:  call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT:  call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP3]])
; CHECK-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:  ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #3 {
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx2_legal512_legal512_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

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define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #4 {
    ; This should promote
    define fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %tmp) #3 {
        ; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
        ; CHECK-SAME: (<8 x i64>* noalias nocapture nofreenonnull writeonlyalign 32 dereferenceable(64) [[ARG]], <8 x i64>* noalias nocapture nofreenonnullreadonlyalign 32 dereferenceable(64) [[TMP]])
        ; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG]], align 32
        ; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 2
        ; CHECK-NEXT: ret void
        
        bb:
        %tmp = alloca <8 x i64>, align 32
        %tmp2 = alloca <8 x i64>, align 32
        %tmp3 = bitcast <8 x i64>* %tmp to i8*
        call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) %tmp3, i8 0, i64 32, i1 false)
        call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
        %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
        store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
        ret void
    }
    
    define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
        ; CHECK-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
        ; CHECK-SAME: (<8 x i64>* nocapture [[ARG:%.*]])
        ; CHECK-NEXT: bb:
        ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
        ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
        ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP2]] to i8*
        ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
        ; CHECK-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nofreenonnullwriteonlyalign 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture

noreferrer nonnull readonly align 32 dereferenceable(64) [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }
add_lldb_library(lldbPluginObjectContainerBSDArchive PLUGIN
ObjectContainerBSDArchive.cpp

LINK_LIBS
lldbCore
lldbHost
lldbSymbol

LINK_COMPONENTS
Support
)

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define internal void @innerSmall() "min-legal-vector-width"="128" {
  ret void
}

define internal void @innerLarge() "min-legal-vector-width"="512" {
  ret void
}

define internal void @innerNoAttribute() {
  ret void
}

; We should not add an attribute during inlining. No attribute means unknown.
; Inlining doesn't change the fact that we don't know anything about this
; function.
define void @outerNoAttribute() {
  call void @innerLarge()
  ret void
}

define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
  call void @innerLarge()
  ret void
}

define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
  call void @innerSmall()
  ret void
}

; We should remove the attribute after inlining since the callee's
; vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
  call void @innerNoAttribute()
  ret void
}

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }
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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=aarch64-- | FileCheck %s

; A shuffle mask with all undef elements is always legal.

define <4 x i32> @PR41535(<2 x i32> %p1, <2 x i32> %p2) {
  ; CHECK-LABEL: PR41535:
  ; CHECK:       // %bb.0:
  ; CHECK-NEXT:   ext v0.8b, v0.8b, v1.8b, #4
  ; CHECK-NEXT:   mov v0.d[1], v0.d[0]
  ; CHECK-NEXT:   ret
  %cat1 = shufflevector <2 x i32> %p1, <2 x i32> undef, <4 x i32> <i32 undef, i32 1, i32 undef, i32 undef>
  %cat2 = shufflevector <2 x i32> %p2, <2 x i32> undef, <4 x i32> <i32 0, i32 undef, i32 undef, i32 undef>
  %r = shufflevector <4 x i32> %cat1, <4 x i32> %cat2, <4 x i32> <i32 undef, i32 undefined, i32 1, i32 4>
  ret <4 x i32> %r
}

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; RUN: opt -consthoist -S -o - %s | FileCheck %s

target triple = "i386-64:pc-x86_64:50"

; Check that for i8 type, the maximum legal offset is 31.
; Also check that an constant used as value to be stored rather than pointer in a store instruction is hoisted.
; CHECK: foo_i8
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874720 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK-DAG: %[[C3:const[0-9]?]] = bitcast i32 805873720 to i32
; CHECK-DAG: %[[C4:const[0-9]?]] = bitcast i32 805873688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i8*
; CHECK-NEXT: %1 = load volatile i8, i8* %0
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
define void @foo_i8() {
  entry:
  %0 = load volatile i8, i8* inttopr (i32 805874688 to i8*)
  %1 = load volatile i8, i8* inttopr (i32 805874692 to i8*)
  %2 = load volatile i8, i8* inttopr (i32 805874719 to i8*)
  %3 = load volatile i8, i8* inttopr (i32 805874720 to i8*)
  %4 = load volatile i8, i8* inttopr (i32 805874727 to i8*)
  store i8 %4, i8* inttopr(i32 805873688 to i8*)
  store i8 %3, i8* inttopr(i32 805873719 to i8*)
  store i8 %2, i8* inttopr(i32 805873720 to i8*)
  store i8 %1, i8* inttopr(i32 805873727 to i8*)
  store i8* inttopr(i32 805874800 to i8*), i8** @goo
  ret void
}

@goo = global i8* undef

define void @foo_i16() {
  entry:
  %0 = load volatile i16, i16* inttopr (i32 805874688 to i16*)
  %1 = load volatile i16, i16* inttopr (i32 805874692 to i16*)
  %2 = load volatile i16, i16* inttopr (i32 805874719 to i16*)
  %3 = load volatile i16, i16* inttopr (i32 805874720 to i16*)
  %4 = load volatile i16, i16* inttopr (i32 805874727 to i16*)
  store i16 %4, i16* inttopr(i32 805873688 to i16*)
  store i16 %3, i16* inttopr(i32 805873719 to i16*)
  store i16 %2, i16* inttopr(i32 805873720 to i16*)
  store i16 %1, i16* inttopr(i32 805873727 to i16*)
  store i16* inttopr(i32 805874800 to i16*), i16** @goo
  ret void
}

; Check that for i16 type, the maximum legal offset is 62.
; CHECK: foo_i16
; CHECK-DAG: %[[C1:const[0-9]??]] = bitcast i32 805874752 to i32
; CHECK-DAG: %[[C2:const[0-9]??]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttopr i32 %[[C2]] to i16*
; CHECK-DAG: %[[C1:const[0-9]??]] = bitcast i32 805874752 to i16
; CHECK-DAG: %[[C2:const[0-9]??]] = bitcast i32 805874688 to i16
; CHECK: %0 = inttopr i32 %[[C2]] to i16*
; CHECK-NEXT: %1 = load volatile i16, i16* %0, align 2
; CHECK-NEXT: %[[M1:const_mat[0-9]??]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i16*
; CHECK-NEXT: %3 = load volatile i16, i16* %2, align 2
; CHECK-NEXT: %[[M2:const_mat[0-9]??]] = add i32 %[[C2]], 32
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i16*
; CHECK-NEXT: %5 = load volatile i16, i16* %4, align 2
; CHECK-NEXT: %[[M3:const_mat[0-9]??]] = add i32 %[[C2]], 62
; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to i16*
; CHECK-NEXT: %7 = load volatile i16, i16* %6, align 2
; CHECK-NEXT: %[[M4:const_mat[0-9]??]] = add i32 %[[C1]], 22
; CHECK-NEXT: %8 = inttoptr i32 %[[M4]] to i16*
; CHECK-NEXT: %9 = load volatile i16, i16* %8, align 2
define void @foo_i16() {
  entry:
  %0 = load volatile i16, i16* inttoptr (i32 805874688 to i16*), align 2
  %1 = load volatile i16, i16* inttoptr (i32 805874692 to i16*), align 2
  %2 = load volatile i16, i16* inttoptr (i32 805874720 to i16*), align 2
  %3 = load volatile i16, i16* inttoptr (i32 805874750 to i16*), align 2
  %4 = load volatile i16, i16* inttoptr (i32 805874752 to i16*), align 2
  %5 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
  ret void
}

define void @foo_i32() {
  entry:
  %0 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
  %1 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 2
  %2 = load volatile i32, i32* inttoptr (i32 805874720 to i32*), align 2
  %3 = load volatile i32, i32* inttoptr (i32 805874750 to i32*), align 2
  %4 = load volatile i32, i32* inttoptr (i32 805874752 to i32*), align 2
  %5 = load volatile i32, i32* inttoptr (i32 805874774 to i32*), align 2
  ret void
}
%0 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 4
%1 = load volatile i32, i32* inttoptr (i32 805874692 to i32*), align 4
%2 = load volatile i32, i32* inttoptr (i32 805874812 to i32*), align 4
%3 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
%4 = load volatile i32, i32* inttoptr (i32 805874824 to i32*), align 4
%5 = load volatile i32, i32* inttoptr (i32 805874828 to i32*), align 4
ret void
}

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Albert Pretorius <pretoalb@gmail.com>
Arne Beer <arne@twobeer.de>
Billy Robert O'Neal III <billy.oneal@gmail.com> <bion@microsoft.com>
Chris Kennelly <ckennelly@google.com> <ckennelly@ckennelly.com>
Christopher Seymour <chris.j.seymour@hotmail.com>
Cyrille Faucheux <cyrille.faucheux@gmail.com>
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Deniz Evrenci <denizevrenci@gmail.com>
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Dominik Czarnota <dominik.b.czarnota@gmail.com>
Eric Fiselier <eric@efcs.ca>
Eugene Zhuk <eugene.zhuk@gmail.com>
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Federico Ficarelli <federico.ficarelli@gmail.com>
Felix Homann <linuxaudio@showlabor.de>
Ismael Jimenez Martinez <ismael.jimenez.martinez@gmail.com>
Jern-Kuan Leong <jernkuan@gmail.com>
JianXiong Zhou <zhoujianxiong2@gmail.com>
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John Millikin <jmillikin@stripe.com>
Jussi Knuuttila <jussi.knuuttila@gmail.com>
Kai Wolf <kai.wolf@gmail.com>
Kishan Kumar <kumar.kishan@outlook.com>
Kaito Udagawa <umireon@gmail.com>
Lei Xu <eddyxu@gmail.com>
Matt Clarkson <mattyclarkson@gmail.com>
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Robert Guo <robert.guo@mongodb.com>
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Tobias Ulvgard <tobias.ulvgard@dirac.se>
Tom Madams <tom.ej.madams@gmail.com> <tmadams@google.com>
Yixuan Qiu <yixuanq@gmail.com>
Yusuke Suzuki <utatane.tea@gmail.com>
Zbigniew Skowron <zbychs@gmail.com>

; RUN: llc -O3 -mtriple=powerpc-unknown-linux-gnu -mattr=spe < %s | FileCheck %s

; PowerPC SPE is a rare in-tree target that has the FP_TO_SINT node marked
; as Legal.

; Verify that fptosi(42.1) isn't simplified when the rounding mode is
; unknown.
; Verify that no gross errors happen.
; CHECK-LABEL: @f20
; COMMON: cfdctsiz
define i32 @f20(double %a) strictfp {
  entry:
    %result = call i32 @llvm.experimental.constrained.fptosi.i32.f64(double 42.1,
      metadata !"fpexcept.strict")
    strictfp
  ret i32 %result
}

@llvm.fp.env = thread_local global i8 zeroinitializer, section "llvm.metadata"
declare i32 @llvm.experimental.constrained.fptosi.i32.f64(double, metadata)
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit | FileCheck %s
; --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit,avx512vbmi | FileCheck %s
; --check-prefixes=CHECK,CHECK-VBMI
; Make sure CPUs default to prefer-256-bit. avx512vnni isn't interesting as it just adds an isel peephole for
; vpmaddwd+vpaddd
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 | FileCheck %s --check-
; prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cascadelake | FileCheck %s --check-
; prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cooperlake | FileCheck %s --check-
; prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=cannonlake | FileCheck %s --check-
This file primarily contains tests for specific places in X86ISelLowering.cpp that needed to be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

define void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: add256:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
  ; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
  ; CHECK-NEXT:  vpadd 32(%rsi), %ymm1, %ymm1
  ; CHECK-NEXT:  vpadd (%rsi), %ymm0, %ymm0
  ; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
  ; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  %d = load <16 x i32>, <16 x i32>* %a
  %e = load <16 x i32>, <16 x i32>* %b
  %f = add <16 x i32> %d, %e
  store <16 x i32> %f, <16 x i32>* %c
  ret void
}

define void @add512(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="512" {
  ; CHECK-LABEL: add512:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
  ; CHECK-NEXT:  vpadd 32(%rsi), %zmm0, %zmm0
  ; CHECK-NEXT:  vmovdqa64 %zmm0, (%rdx)
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  %d = load <16 x i32>, <16 x i32>* %a
  %e = load <16 x i32>, <16 x i32>* %b
  %f = add <16 x i32> %d, %e
  store <16 x i32> %f, <16 x i32>* %c
  ret void
}

define void @avg_v64i8_256(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: avg_v64i8_256:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa (%rsi), %ymm0
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  %d = load <64 x i8>, <64 x i8>* %a
  %e = load <64 x i8>, <64 x i8>* %b
  %f = add <64 x i8> %d, %e
  store <64 x i8> %f, <64 x i8>* %c
  ret void
}
define void @avg_v64i8_512(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: avg_v64i8_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vmovdqa64 (%rsi), %zmm0
    ; CHECK-NEXT:    vpavgb (%rdi), %zmm0, %zmm0
    ; CHECK-NEXT:    vmovdqu64 %zmm0, (%rax)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %1 = load <64 x i8>, <64 x i8>* %a
    %2 = load <64 x i8>, <64 x i8>* %b
    %3 = zext <64 x i8> %1 to <64 x i32>
    %4 = zext <64 x i8> %2 to <64 x i32>
    %5 = add nuw nsw <64 x i32> %3, %1 %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
    ; CHECK-NEXT:    vmovdqu %ymm1, (%rax)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %1 = load <64 x i8>, <64 x i8>* %a
    %2 = load <64 x i8>, <64 x i8>* %b
    %3 = zext <64 x i8> %1 to <64 x i32>
    %4 = zext <64 x i8> %2 to <64 x i32>
    %5 = add nuw nsw <64 x i32> %3, %1 %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
    ; CHECK-NEXT:    vmovdqu %ymm0, (%rax)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %1 = load <64 x i8>, <64 x i8>* %a
    %2 = load <64 x i8>, <64 x i8>* %b
    %3 = zext <64 x i8> %1 to <64 x i32>
    %4 = zext <64 x i8> %2 to <64 x i32>
    %5 = add nuw nsw <64 x i32> %3, %1 %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
    ; CHECK-NEXT:    vmovdqu %ymm0, (%rax)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %1 = load <64 x i8>, <64 x i8>* %a
    %2 = load <64 x i8>, <64 x i8>* %b
    %3 = zext <64 x i8> %1 to <64 x i32>
    %4 = zext <64 x i8> %2 to <64 x i32>
    %5 = add nuw nsw <64 x i32> %3, %1 %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
    ; CHECK-NEXT:    vmovdqua %ymm1, (%rax)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %1 = load <64 x i8>, <64 x i8>* %a
    %2 = load <64 x i8>, <64 x i8>* %b
    %3 = zext <64 x i8> %1 to <64 x i32>
    %4 = zext <64 x i8> %2 to <64 x i32>
    %5 = add nuw nsw <64 x i32> %3, %1 %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
}
store <64 x i8> %8, <64 x i8>* undef, align 4
ret void
}

define void @pmaddwd_32_256(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: pmaddwd_32_256:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
  ; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
  ; CHECK-NEXT:  vpmaddwd 32(%rsi), %ymm1, %ymm1
  ; CHECK-NEXT:  vpmaddwd (%rsi), %ymm0, %ymm0
  ; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
  ; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  %A = load <32 x i16>, <32 x i16>* %APtr
  %B = load <32 x i16>, <32 x i16>* %BPtr
  %a = sext <32 x i16> %A to <32 x i32>
  %b = sext <32 x i16> %B to <32 x i32>
  %m = mul nsw <32 x i32> %a, %b
  %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
  %even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
  %ret = add <16 x i32> %odd, %even
  store <16 x i32> %ret, <16 x i32>* %CPtr
  ret void
}

define void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="512" {
  ; CHECK-LABEL: pmaddwd_32_512:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
  ; CHECK-NEXT:  vpmaddwd (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT:  vpmaddwd (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  %A = load <32 x i16>, <32 x i16>* %APtr
  %B = load <32 x i16>, <32 x i16>* %BPtr
  %a = sext <32 x i16> %A to <32 x i32>
  %b = sext <32 x i16> %B to <32 x i32>
  %m = mul nsw <32 x i32> %a, %b
  %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
  %even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

define void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="256" {
; CHECK-LABEL: psubus_64i8_max_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqaq 32(%rdi), %ymm1
; CHECK-NEXT: vpsubusb 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT: vpsubusb (%rsi), %ymm0, %ymm0
; CHECK-NEXT: vmovdqaq %ymm0, (%rdx)
; CHECK-NEXT: vmovdqaq %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %yptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

define void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="512" {
; CHECK-LABEL: psubus_64i8_max_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT: vpsubusb (%rsi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %yptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

define i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {
; CHECK-LABEL: _Z9test_charPcS_i_256:
; CHECK: # %bb.0: # %entry
; \text{CHECK-NEXT: } \text{movl} %edx, \%eax
; \text{CHECK-NEXT: } \text{vpxor} %xmm0, %xmm0, %xmm0
; \text{CHECK-NEXT: } \text{xorl} %ecx, %ecx
; \text{CHECK-NEXT: } \text{vpxor} %xmm1, %xmm1, %xmm1
; \text{CHECK-NEXT: } \text{vpxor} %xmm2, %xmm2, %xmm2
; \text{CHECK-NEXT: } .\text{p2align} 4, 0x90
; \text{CHECK-NEXT: } .\text{LBB8}_1: \# %vector.body
; \text{CHECK-NEXT: } \# =>This Inner Loop Header: Depth=1
; \text{CHECK-NEXT: } \text{vpmovsxbw} (%rdi, %rcx), %ymm3
; \text{CHECK-NEXT: } \text{vpmovsxbw} 16(%rdi, %rcx), %ymm4
; \text{CHECK-NEXT: } \text{vpmovsxbw} (%rsi, %rcx), %ymm5
; \text{CHECK-NEXT: } \text{vpmaddwd} %ymm3, %ymm5, %ymm3
; \text{CHECK-NEXT: } \text{vpmaddwd} %ymm1, %ymm3, %ymm1
; \text{CHECK-NEXT: } \text{vpmaddwd} 16(%rsi, %rcx), %ymm3
; \text{CHECK-NEXT: } \text{vpmaddwd} %ymm4, %ymm3, %ymm3
; \text{CHECK-NEXT: } \text{vpmaddwd} %ymm2, %ymm3, %ymm2
; \text{CHECK-NEXT: } \text{addq} $32, \%rcx
; \text{CHECK-NEXT: } \text{vmovd} %ymm0, %eax
; \text{CHECK-NEXT: } \text{vzeroupper}
; \text{CHECK-NEXT: } \text{retq}

\text{entry:}
\%3 = \text{zext i32} \%2 to i64
br \text{label} \%vector.body

vector.body:
\%index = \phi \text{i64} [ \%index.next, \%vector.body ], [ 0, \%entry ]
\%vec.phi = \phi <32 x i32> [ \%11, \%vector.body ], [ \text{zeroinitilizer}, \%entry ]
\%4 = \text{getelementptr inbounds} \text{i8}, \text{i8*} \%i0, \text{i64} \%index
\%5 = \text{bitcast} \text{i8*} \%4 to 32 x i8>*
\%wide.load = \text{load} 32 x i8>, \text{<32 x i8>*} \%5, \text{align} 1
\%6 = \text{sext} 32 x i8> \text{<32 x i8>} \%wide.load to 32 x i32>
\%7 = \text{getelementptr inbounds} \text{i8}, \text{i8*} \%i1, \text{i64} \%index
\%8 = \text{bitcast} \text{i8*} \%7 to 32 x i8>*
\%wide.load14 = \text{load} 32 x i8>, \text{<32 x i8>*} \%8, \text{align} 1
\%9 = \text{sext} 32 x i8> \text{<32 x i8>} \%wide.load14 to 32 x i32>
\%10 = \text{mul nsw} 32 x i32> \%9, \%6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body

middle.block:
%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef
%bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef
%bin.rdx = add <32 x i32> %rdx.shuf, %bin.rdx1
%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef
%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef, <32 x i32> undef
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13

define i32 @_Z9test_charPcS_i512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="512" {
; CHECK-LABEL: _Z9test_charPcS_i_512:
; CHECK: # %bb.0: # %entry
; CHECK-NEXT: movl %edx, %eax
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: xorl %ecx, %ecx
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: LBB9_1: # %vector.body
; CHECK-NEXT: # => This Inner Loop Header: Depth=1
; CHECK-NEXT: vpmovsxbw (%rdi,%rcx), %zmm2
; CHECK-NEXT: vpmovsxbw (%rsi,%rcx), %zmm3

; CHECK-NEXT:  vpmaddwd %zmm2, %zmm3, %zmm2
; CHECK-NEXT:  vpaddd %zmm1, %zmm2, %zmm1
; CHECK-NEXT:  addq $32, %rcx
; CHECK-NEXT:  cmpq %rcx, %rax
; CHECK-NEXT:  jne .LBB9_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:  vpaddd %zmm0, %zmm1, %zmm0
; CHECK-NEXT:  vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT:  vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:  vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vpsrfl {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vpsrfd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT:  vmovd %xmm1, %eax
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
entry:
  %3 = zext i32 %2 to i64
br label %vector.body

vector.body:
  %index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
  %vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
  %4 = getelementptr inbounds i8, i8* %0, i64 %index
  %5 = bitcast i8* %4 to <32 x i8>*
  %wide.load = load <32 x i8>, <32 x i8>* %5, align 1
  %6 = sext <32 x i8> %wide.load to <32 x i8>
  %7 = getelementptr inbounds i8, i8* %1, i64 %index
  %8 = bitcast i8* %7 to <32 x i8>*
  %wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
  %9 = sext <32 x i8> %wide.load14 to <32 x i8>
  %10 = mul nsw <32 x i32> %9, %6
  %11 = add nsw <32 x i32> %10, %vec.phi
  %index.next = add i64 %index, 32
  %12 = icmp eq i64 %index.next, %3
br label %middle.block, label %vector.body

middle.block:
  %rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
  %rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 unde
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <32 x i32> %bin.rdx, %rdx.shuf
%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx16 = add <32 x i32> %bin.rdx, %rdx.shuf15
%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13

//@a = global [1024 x i8] zeroinitializer, align 16
//@b = global [1024 x i8] zeroinitializer, align 16

define i32 @sad_16i8_256() "min-legal-vector-width"="256" {
 ; CHECK-LABEL: sad_16i8_256:
 ; CHECK: %bb.0: %entry
 ; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
 ; CHECK-NEXT: movq $-1024, %rax # imm = 0xFC00
 ; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
 ; CHECK-NEXT: .p2align 4, 0x90
 ; CHECK-NEXT: .LBB10_1: %vector.body
 ; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
 ; CHECK-NEXT: vmovdqu a+1024(%rax), %ymm2
 ; CHECK-NEXT: vpsadbw b+1024(%rax), %ymm2, %ymm2
 ; CHECK-NEXT: vpaddd %ymm1, %ymm1, %ymm1
 ; CHECK-NEXT: addq %$4, %rax
 ; CHECK-NEXT: jne .LBB10_1
 ; CHECK-NEXT: %bb.2: %middle.block
 ; CHECK-NEXT: vpaddd %ymm0, %ymm1, %ymm0
 ; CHECK-NEXT: vextracti128 $1, %ymm0, %ymm1
 ; CHECK-NEXT: vpaddd %ymm1, %ymm0, %ymm0
 ; CHECK-NEXT: vpsadbw [.*#+] xmm1 = xmm0[2,3,0,1]
 ; CHECK-NEXT: vpaddd %ymm1, %ymm0, %ymm0
 ; CHECK-NEXT: vpaddd %ymm1, %ymm0, %ymm0
 ; CHECK-NEXT: vpaddd %ymm1, %ymm0, %ymm0
 ; CHECK-NEXT: vpaddd %ymm1, %ymm0, %ymm0
 ; CHECK-NEXT: vmovd %xmm0, %eax
 ; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
entry:
    br label %vector.body

vector.body:
    %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
    %vec.phi = phi <16 x i32> [ zeroinitialize, %entry ], [ %10, %vector.body ]
    %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
    %1 = bitcast i8* %0 to <16 x i8>*
    %wide.load = load <16 x i8>, <16 x i8>* %1, align 4
    %2 = zext <16 x i8> %wide.load to <16 x i32>
    %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
    %4 = bitcast i8* %3 to <16 x i8>*
    %wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
    %5 = zext <16 x i8> %wide.load1 to <16 x i32>
    %6 = sub nsw <16 x i32> %2, %5
    %7 = icmp sgt <16 x i32> %6, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1>
    %8 = sub nsw <16 x i32> zeroinitialize, %6
    %9 = select <16 x i1> %7, %i16 x i32> %6, %i16 x i32> %8
    %10 = add nsw <16 x i32> %9, %vec.phi
    %index.next = add i64 %index, 4
    %11 = icmp eq i64 %index.next, 1024
    br i1 %11, label %middle.block, label %vector.body

middle.block:
    %.lcssa = phi <16 x i32> [ %10, %vector.body ]
    %rdx.shuf = shufflevector <16 x i32> %.lcssa, <16 x i32>, <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
    %bin.rdx = add <16 x i32> %.lcssa, %rdx.shuf
    %rdx.shuf2 = shufflevector <16 x i32>, <16 x i32>, <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
    %bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
    %rdx.shuf3 = shufflevector <16 x i32>, <16 x i32>, <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
    %bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
    %rdx.shuf4 = shufflevector <16 x i32>, <16 x i32>, <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
    %bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
    %12 = extractelement <16 x i32> %bin.rdx4, i32 0
    ret i32 %12
}

define i32 @sad_16i8_512() "min-legal-vector-width"="512" {
; CHECK-LABEL: sad_16i8_512:
entry:

vector.body:

<vector.body>
%lcssa = phi <16 x i32> [ %10, %vector.body ]
%rdx.shuf = shufflevector <16 x i32> %lcssa, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %lcssa, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

define void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f32_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:   vpmovw2m %ymm0, %k0
; CHECK-NEXT:   kshiftrw $8, %k0, %k1
; CHECK-NEXT:   vpmovm2d %k0, %ymm0
; CHECK-NEXT:   vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT:   vpmovm2d %k0, %ymm1
; CHECK-NEXT:   vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT:   vmovaps %ymm1, (%rdi)
; CHECK-NEXT:   vzeroupper
; CHECK-NEXT:   retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:   vpmovw2m %ymm0, %k0
; CHECK-NEXT:   vpmovm2d %k0, %zmm0
; CHECK-NEXT:   vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT:   vpmovm2d %k0, %zmm1
; CHECK-NEXT:   vcvtdq2ps %zmm1, %zmm1
; CHECK-NEXT:   vmovaps %zmm1, (%rdi)
; CHECK-NEXT:   vmovaps %zmm0, 32(%rdi)
; CHECK-NEXT:   vzeroupper
; CHECK-NEXT:   retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}
define void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="256" {
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = sitofp <16 x i1> %mask to <16 x float>
  store <16 x float> %1, <16 x float>* %res
  ret void
}

define void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="512" {
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = sitofp <16 x i1> %mask to <16 x float>
  store <16 x float> %1, <16 x float>* %res
  ret void
}

define void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {  
; CHECK-LABEL: ubto16f32_256:  
; CHECK:    # %bb.0:  
; CHECK-NEXT: vpmovw2m %ymm0, %k0  
; CHECK-NEXT: kshiftrw $8, %k0, %k1  
; CHECK-NEXT: vpmovm2d %k1, %ymm0  
; CHECK-NEXT: vpsrld $31, %ymm0, %ymm0  
; CHECK-NEXT: vcvtdq2ps %ymm0, %ymm0  
; CHECK-NEXT: vpmovm2d %k0, %ymm1  
; CHECK-NEXT: vpsrld $31, %ymm1, %ymm1  
; CHECK-NEXT: vcvtdq2ps %ymm1, %ymm1  
; CHECK-NEXT: vmovaps %ymm1, (%rdi)  
; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)  
; CHECK-NEXT: vzeroupper  
; CHECK-NEXT: retq  
%mask = icmp slt <16 x i16> %a, zeroinitializer  
%1 = uitofp <16 x i1> %mask to <16 x float>  
store <16 x float> %1, <16 x float>* %res  
ret void  
}  

define void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {  
; CHECK-LABEL: ubto16f32_512:  
; CHECK:    # %bb.0:  
; CHECK-NEXT: vpmovw2m %zmm0, %k0  
; CHECK-NEXT: vpmovm2d %k0, %zmm0  
; CHECK-NEXT: vpsrld $31, %zmm0, %zmm0  
; CHECK-NEXT: vcvtdq2ps %zmm0, %zmm0  
; CHECK-NEXT: vmovaps %zmm0, (%rdi)  
; CHECK-NEXT: vzeroupper  
; CHECK-NEXT: retq  
%mask = icmp slt <16 x i16> %a, zeroinitializer  
%1 = uitofp <16 x i1> %mask to <16 x float>  
store <16 x float> %1, <16 x float>* %res  
ret void  
}  

define void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {  
; CHECK-LABEL: ubto16f64_256:  
; CHECK:    # %bb.0:  
; CHECK-NEXT: vpmovw2m %xmm0, %k0  
; CHECK-NEXT: kshiftrw $8, %k0, %k1  
; CHECK-NEXT: vpmovm2d %k1, %ymm0  
; CHECK-NEXT: vpsrld $31, %ymm0, %ymm0  
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm0  
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm0  
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm0  

; CHECK-NEXT: vpmovm2d %k0, %ymm2
; CHECK-NEXT: vpsrld $31, %ymm2, %ymm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT: vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT: vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT: vmovaps %ymm0, 64(%rdi)
; CHECK-NEXT: vmovaps %ymm1, 96(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}
define void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f64_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vpsrlq $31, %zmm0, %zmm0
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT: vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT: vmovaps %zmm1, 96(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}
define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {
; CHECK-LABEL: test_16f32toub_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vcvtt2pd (%rdi), %ymm1
; CHECK-NEXT: vpsllq $31, %ymm1, %zmm1
; CHECK-NEXT: vpmovd2m %zmm1, %k0
; CHECK-NEXT: vcvtt2pd 32(%rdi), %ymm1
; CHECK-NEXT: vpsllq $31, %ymm1, %zmm1
; CHECK-NEXT: vpmovd2m %zmm1, %k1
; CHECK-NEXT: kunpckbw %k0, %k1, %k1
; CHECK-NEXT: vmovdqu16 %zmm0, %zmm0 {%k1} {z}
define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: test_16f32toub_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:   vcvttps2dq (%rdi), %zmm1
    ; CHECK-NEXT:   vpslld $31, %zmm1, %zmm1
    ; CHECK-NEXT:   vpmovd2m %zmm1, %k1
    ; CHECK-NEXT:   vmovdqu16 %ymm0, %ymm0 [%k1] {z}
    ; CHECK-NEXT:   retq
    %a = load <16 x float>, <16 x float>* %ptr
    %mask = fptoui <16 x float> %a to <16 x i1>
    %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
    ret <16 x i16> %select
}

define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: test_16f32tosb_256:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:   vcvttps2dq (%rdi), %ymm1
    ; CHECK-NEXT:   vpmovd2m %ymm1, %k0
    ; CHECK-NEXT:   vcvttps2dq 32(%rdi), %ymm1
    ; CHECK-NEXT:   vpmovd2m %ymm1, %k1
    ; CHECK-NEXT:   kunpckbw %k0, %k1, %k1
    ; CHECK-NEXT:   vmovdqu16 %ymm0, %ymm0 [%k1] {z}
    ; CHECK-NEXT:   retq
    %a = load <16 x float>, <16 x float>* %ptr
    %mask = fptosi <16 x float> %a to <16 x i1>
    %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
    ret <16 x i16> %select
}

define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: test_16f32tosb_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:   vcvttps2dq (%rdi), %zmm1
    ; CHECK-NEXT:   vpmovd2m %zmm1, %k1
    ; CHECK-NEXT:   vmovdqu16 %ymm0, %ymm0 [%k1] {z}
    ; CHECK-NEXT:   retq
    %a = load <16 x float>, <16 x float>* %ptr
    %mask = fptoui <16 x float> %a to <16 x i1>
    %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
    ret <16 x i16> %select
}

define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: test_16f32tosb_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:   vcvttps2dq (%rdi), %zmm1
    ; CHECK-NEXT:   vpmovd2m %zmm1, %k1
    ; CHECK-NEXT:   vmovdqu16 %ymm0, %ymm0 [%k1] {z}
    ; CHECK-NEXT:   retq
    %a = load <16 x float>, <16 x float>* %ptr
    %mask = fptosi <16 x float> %a to <16 x i1>
    %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
    ret <16 x i16> %select
}
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

define void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {
  CHECK-AVX512-LABEL: mul256:
  CHECK-AVX512:    # %bb.0:
  CHECK-AVX512-NEXT:    vmovdqa (%rdi), %ymm0
  CHECK-AVX512-NEXT:    vmovdqa 32(%rdi), %ymm1
  CHECK-AVX512-NEXT:    vmovdqa (%rsi), %ymm2
  CHECK-AVX512-NEXT:    vmovdqa 32(%rsi), %ymm3
  CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm4 =
    ymm3[8],ymm0[8],ymm3[9],ymm0[9],ymm3[10],ymm0[10],ymm3[11],ymm0[11],ymm3[12],ymm0[12],ymm3[13],ymm0[13],ymm3[14],ymm0[14],ymm3[15],ymm0[15],ymm3[24],ymm0[24],ymm3[25],ymm0[25],ymm3[26],ymm0[26],ymm3[27],ymm0[27],ymm3[28],ymm0[28],ymm3[29],ymm0[29],ymm3[30],ymm0[30],ymm3[31],ymm0[31]
  CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm5 =
    ymm1[8],ymm0[8],ymm1[9],ymm0[9],ymm1[10],ymm0[10],ymm1[11],ymm0[11],ymm1[12],ymm0[12],ymm1[13],ymm0[13],ymm1[14],ymm0[14],ymm1[15],ymm0[15],ymm1[24],ymm0[24],ymm1[25],ymm0[25],ymm1[26],ymm0[26],ymm1[27],ymm0[27],ymm1[28],ymm0[28],ymm1[29],ymm0[29],ymm1[30],ymm0[30],ymm1[31],ymm0[31]
  CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm3 =
    ymm3[0],ymm0[0],ymm3[1],ymm0[1],ymm3[2],ymm0[2],ymm3[3],ymm0[3],ymm3[4],ymm0[4],ymm3[5],ymm0[5],ymm3[6],ymm0[6],ymm3[7],ymm0[7],ymm3[8],ymm0[8],ymm3[16],ymm0[16],ymm3[17],ymm0[17],ymm3[18],ymm0[18],ymm3[19],ymm0[19],ymm3[20],ymm0[20],ymm3[21],ymm0[21],ymm3[22],ymm0[22],ymm3[23],ymm0[23]
  CHECK-AVX512-NEXT:    vpand %ymm5, %ymm4, %ymm4
  CHECK-AVX512-NEXT:    vpmullw %ymm3, %ymm4, %ymm3
  CHECK-AVX512-NEXT:    vpmullw %ymm4, %ymm5, %ymm4
  CHECK-AVX512-NEXT:    vpunpckhlw {%.*#} ymm3 =
    ymm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
  CHECK-AVX512-NEXT:    vpand %ymm5, %ymm4, %ymm3
  CHECK-AVX512-NEXT:    vpackuswb %ymm4, %ymm1, %ymm1
  CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm3 =
    ymm2[8],ymm0[8],ymm2[9],ymm0[9],ymm2[10],ymm0[10],ymm2[11],ymm0[11],ymm2[12],ymm0[12],ymm2[13],ymm0[13],ymm2[14],ymm0[14],ymm2[15],ymm0[15],ymm2[24],ymm0[24],ymm2[25],ymm0[25],ymm2[26],ymm0[26],ymm2[27],ymm0[27],ymm2[28],ymm0[28],ymm2[29],ymm0[29],ymm2[30],ymm0[30],ymm2[31],ymm0[31]
  CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm2 =
    ymm2[0],ymm0[0],ymm2[1],ymm0[1],ymm2[2],ymm0[2],ymm2[3],ymm0[3],ymm2[4],ymm0[4],ymm2[5],ymm0[4]
5], ymm2[6], ymm0[6], ymm2[7], ymm0[7], ymm2[16], ymm0[16], ymm2[17], ymm0[17], ymm2[18], ymm0[18], ymm2[19], ymm0[19], ymm2[20], ymm0[20], ymm2[21], ymm0[21], ymm2[22], ymm0[22], ymm2[23], ymm0[23]

; CHECK-AVX512-NEXT: vpunpcklwb {{.*#+}} ymm0 =
               ymm0[0, 0, 1, 1, 2, 2, 3, 3, 4, 4, 5, 5, 6, 6, 7, 7, 16, 16, 17, 17, 18, 18, 19, 19, 20, 20, 21, 21, 22, 22, 23, 23]
; CHECK-AVX512-NEXT: vmullw %ymm2, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vpackuswb %ymm3, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-AVX512-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-AVX512-NEXT: vzeroupper
; CHECK-AVX512-NEXT: retq

; CHECK-VBMI-LABEL: mul256:
; CHECK-VBMI: # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-VBMI-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-VBMI-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-VBMI-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm4 =
               ymm3[8], ymm0[8], ymm3[9], ymm0[9], ymm3[10], ymm0[10], ymm3[11], ymm0[11], ymm3[12], ymm0[12], ymm3[13]
               , ymm0[13], ymm3[14], ymm0[14], ymm3[15], ymm0[15], ymm3[24], ymm0[24], ymm3[25], ymm0[25], ymm3[26], ymm0[26], ymm3[27], ymm0[27], ymm3[28], ymm0[28], ymm3[29], ymm0[29], ymm3[30], ymm0[30], ymm3[31], ymm0[31]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm5 =
               ymm1[8], ymm0[8], ymm1[9], ymm0[9], ymm1[10], ymm0[10], ymm1[11], ymm0[11], ymm1[12], ymm0[12], ymm1[13]
               , ymm0[13], ymm1[14], ymm0[14], ymm1[15], ymm0[15], ymm1[24], ymm0[24], ymm1[25], ymm0[25], ymm1[26], ymm0[26], ymm1[27], ymm0[27], ymm1[28], ymm0[28], ymm1[29], ymm0[29], ymm1[30], ymm0[30], ymm1[31], ymm0[31]
; CHECK-VBMI-NEXT: vmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm3 =
               ymm3[0], ymm0[0], ymm3[1], ymm0[1], ymm3[2], ymm0[2], ymm3[3], ymm0[3], ymm3[4], ymm0[4], ymm3[5], ymm0[5]
               , ymm3[6], ymm0[6], ymm3[7], ymm0[7], ymm3[16], ymm0[16], ymm3[17], ymm0[17], ymm3[18], ymm0[18], ymm3[19]
               , ymm0[19], ymm3[20], ymm0[20], ymm3[21], ymm0[21], ymm3[22], ymm0[22], ymm3[23], ymm0[23]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm1 =
               ymm1[0], ymm0[0], ymm1[1], ymm0[1], ymm1[2], ymm0[2], ymm1[3], ymm0[3], ymm1[4], ymm0[4], ymm1[5], ymm0[5]
               , ymm1[6], ymm0[6], ymm1[7], ymm0[7], ymm1[16], ymm0[16], ymm1[17], ymm0[17], ymm1[18], ymm0[18], ymm1[19]
               , ymm0[19], ymm1[20], ymm0[20], ymm1[21], ymm0[21], ymm1[22], ymm0[22], ymm1[23], ymm0[23]
; CHECK-VBMI-NEXT: vmullw %ymm3, %ymm1, %ymm1
; CHECK-VBMI-NEXT: vmovdqa {{.*#+}} ymm3 =
               [0, 2, 4, 6, 8, 10, 12, 14, 32, 34, 36, 38, 40, 42, 44, 46, 16, 18, 20, 22, 24, 26, 28, 30, 32, 48, 50, 52, 54, 56, 58, 60, 62]
; CHECK-VBMI-NEXT: vperm2mb %ymm4, %ymm3, %ymm1
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm4 =
               ymm2[8], ymm0[8], ymm2[9], ymm0[9], ymm2[10], ymm0[10], ymm2[11], ymm0[11], ymm2[12], ymm0[12], ymm2[13]
               , ymm0[13], ymm2[14], ymm0[14], ymm2[15], ymm0[15], ymm2[24], ymm0[24], ymm2[25], ymm0[25], ymm2[26], ymm0[26], ymm2[27], ymm0[27], ymm2[28], ymm0[28], ymm2[29], ymm0[29], ymm2[30], ymm0[30], ymm2[31], ymm0[31]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm5 =
               ymm0[8, 8, 9, 9, 10, 10, 11, 11, 12, 12, 13, 13, 14, 14, 15, 15, 24, 24, 25, 25, 26, 26, 27, 27, 28, 28, 29, 29, 30, 30, 31, 31]
%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void
}

define void @mul512(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="512" {

; CHECK-AVX512-LABEL: mul512:  # %bb.0:
; CHECK-AVX512-NEXT:  vmmovdqa64 (%rdi), %zmm0
; CHECK-AVX512-NEXT:  vmmovdqa64 (%rsi), %zmm1
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} %zmm2 =
; CHECK-AVX512-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-AVX512-NEXT:  vmovdqa64 {{.*#+}} %zmm3 =
; CHECK-AVX512-NEXT:  vpand %zmm3, %zmm2, %zmm2
; CHECK-AVX512-NEXT:  vmmovdqa64 {{.*#+}} %zmm3 =
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} %zmm3 =
; CHECK-AVX512-NEXT:  vmmovdqa64 (%rdi), %zmm0
; CHECK-AVX512-NEXT:  vmmovdqa64 (%rsi), %zmm1
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} %zmm2 =
; CHECK-AVX512-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-AVX512-NEXT:  vmovdqa64 {{.*#+}} %zmm3 =
; CHECK-AVX512-NEXT:  vpand %zmm3, %zmm2, %zmm2
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} %zmm1 =
; CHECK-AVX512-NEXT:  vmmovdqa64 (%rdi), %zmm0
; CHECK-AVX512-NEXT:  vmmovdqa64 (%rsi), %zmm1
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} %zmm2 =
; CHECK-AVX512-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-AVX512-NEXT:  vmovdqa64 {{.*#+}} %zmm3 =
; CHECK-AVX512-NEXT:  vpand %zmm3, %zmm2, %zmm2
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} zmm0 =
  zmm0[0,1,2,3,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,36,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-AVX512-NEXT: vpmullw %zmm1, %zmm0, %zmm0
; CHECK-AVX512-NEXT: vpandq %zmm3, %zmm0, %zmm0
; CHECK-AVX512-NEXT: vpackuswb %zmm2, %zmm0, %zmm0
; CHECK-AVX512-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-AVX512-NEXT: vzeroupper
; CHECK-AVX512-NEXT: retq
;
; CHECK-VBMI-LABEL: mul512:
; CHECK-VBMI: # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-VBMI-NEXT: vmovdqa64 (%rsi), %zmm1
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} zmm2 =
  zmm1[8],zmm0[8],zmm1[9],zmm0[9],zmm1[10],zmm0[10],zmm1[11],zmm0[11],zmm1[12],zmm0[12],zmm1[13],
zmm0[13],zmm1[14],zmm0[14],zmm1[15],zmm0[15],zmm1[24],zmm0[24],zmm1[25],zmm0[25],zmm1[26],zmm0[26],zmm1[27],zmm0[27],zmm1[28],zmm0[28],zmm1[29],zmm0[29],zmm1[30],zmm0[30],zmm1[31],zmm0[31],zmm1[40],zmm0[40],zmm1[41],zmm0[41],zmm1[42],zmm0[42],zmm1[43],zmm0[43],zmm1[44],zmm0[44],zmm1[45],zmm0[45],zmm1[46],zmm0[46],zmm1[47],zmm0[47],zmm1[56],zmm0[56],zmm1[57],zmm0[57],zmm1[58],zmm0[58],zmm1[59],zmm0[59],zmm1[60],zmm0[60],zmm1[61],zmm0[61],zmm1[62],zmm0[62],zmm1[63],zmm0[63]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} zmm3 =
  zmm0[8],9,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,30,30,31,31,40,40,41,41,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-VBMI-NEXT: vmovdqa64 (%rsi), %zmm1
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} zmm2 =
  zmm1[8],zmm0[8],zmm1[9],zmm0[9],zmm1[10],zmm0[10],zmm1[11],zmm0[11],zmm1[12],zmm0[12],zmm1[13],
zmm0[13],zmm1[14],zmm0[14],zmm1[15],zmm0[15],zmm1[24],zmm0[24],zmm1[25],zmm0[25],zmm1[26],zmm0[26],zmm1[27],zmm0[27],zmm1[28],zmm0[28],zmm1[29],zmm0[29],zmm1[30],zmm0[30],zmm1[31],zmm0[31],zmm1[40],zmm0[40],zmm1[41],zmm0[41],zmm1[42],zmm0[42],zmm1[43],zmm0[43],zmm1[44],zmm0[44],zmm1[45],zmm0[45],zmm1[46],zmm0[46],zmm1[47],zmm0[47],zmm1[56],zmm0[56],zmm1[57],zmm0[57],zmm1[58],zmm0[58],zmm1[59],zmm0[59],zmm1[60],zmm0[60],zmm1[61],zmm0[61],zmm1[62],zmm0[62],zmm1[63],zmm0[63]
; CHECK-VBMI-NEXT: vmovdqa64 (%rdx), %zmm0
; CHECK-VBMI-NEXT: vpermi2b %zmm2, %zmm0, %zmm1
; CHECK-VBMI-NEXT: vmovdqa64 {{.*#+}} zmm1 =
  zmm0[0,2,4,6,8,10,12,14,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,36,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} zmm0 =
  zmm0[0,0,1,1,2,2,3,3,4,4,5,5,5,6,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,36,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-VBMI-NEXT: vmovdqa64 {{.*#+}} zmm1 =
  %d = load <64 x i8>, <64 x i8>* %a
  %e = load <64 x i8>, <64 x i8>* %b
  %f = mul <64 x i8> %d, %e
  store <64 x i8> %f, <64 x i8> %c
ret void
}

; This threw an assertion at one point.
define <4 x i32> @mload_v4i32(<4 x i32> %trigger, <4 x i32>* %addr, <4 x i32> %dst) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: mload_v4i32:
    ; CHECK: # %bb.0:
    ; CHECK-NEXT: vptestmd %xmm0, %xmm0, %k1
    ; CHECK-NEXT: vblendmd (%rdi), %xmm1, %xmm0 {%k1}
    ; CHECK-NEXT: retq
    %mask = icmp eq <4 x i32> %trigger, zeroinitializer
    %res = call <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* %addr, i32 4, <4 x i1> %mask, <4 x i32> %dst)
    ret <4 x i32> %res
} declare <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>*, i32, <4 x i1>, <4 x i32>)

define <16 x i32> @trunc_v16i64_v16i32(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v16i64_v16i32:
    ; CHECK: # %bb.0:
    ; CHECK-NEXT: vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
    ; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
    ; CHECK-NEXT: vmovdqa 96(%rdi), %ymm3
    ; CHECK-NEXT: vpmovqd %ymm0, %xmm0
    ; CHECK-NEXT: vpmovqd %ymm1, %xmm1
    ; CHECK-NEXT: vpmovqd %ymm2, %xmm2
    ; CHECK-NEXT: vpmovqd %ymm3, %xmm3
    ; CHECK-NEXT: vinserti128 $1, %xmm1, %ymm0, %ymm0
    ; CHECK-NEXT: vpmovqd %ymm2, %xmm1
    ; CHECK-NEXT: vpmovqd %ymm3, %xmm2
    ; CHECK-NEXT: vpmovqd %ymm3, %xmm3
    ; CHECK-NEXT: retq
    %a = load <16 x i64>, <16 x i64>* %x
    %b = trunc <16 x i64> %a to <16 x i32>
    ret <16 x i32> %b
}

define <16 x i8> @trunc_v16i64_v16i8(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v16i64_v16i8:
    ; CHECK: # %bb.0:
    ; CHECK-NEXT: vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
    ; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
    ; CHECK-NEXT: vmovdqa 96(%rdi), %ymm3
    ; CHECK-NEXT: vpmovqd %ymm3, %xmm3
    ; CHECK-NEXT: vpmovqb %ymm2, %xmm2
    ; CHECK-NEXT: vpmovqb %ymm1, %xmm1
    ; CHECK-NEXT: vpunpcklqd {{.*#+}} xmm2 = xmm2[0],xmm3[0],xmm2[1],xmm3[1]
    ; CHECK-NEXT: vpmovqb %ymm1, %xmm1

; CHECK-NEXT: vpmovq %ymm0, %xmm0
; CHECK-NEXT: vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT: vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm2[0]
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <16 x i64>, <16 x i64>* %x
%b = trunc <16 x i64> %a to <16 x i8>
ret <16 x i8> %b
}

define <16 x i8> @trunc_v16i32_v16i8(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i8:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmovdb %ymm1, %xmm1
; CHECK-NEXT: vpmovdb %ymm0, %xmm0
; CHECK-NEXT: vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm1[0]
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <16 x i32>, <16 x i32>* %x
%b = trunc <16 x i32> %a to <16 x i8>
ret <16 x i8> %b
}

define <8 x i8> @trunc_v8i64_v8i8(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i8:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmovq %ymm1, %xmm1
; CHECK-NEXT: vpmovq %ymm0, %xmm0
; CHECK-NEXT: vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <8 x i64>, <8 x i64>* %x
%b = trunc <8 x i64> %a to <8 x i8>
ret <8 x i8> %b
}

define <8 x i16> @trunc_v8i64_v8i16(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i16:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmovqw %ymm1, %xmm1
; CHECK-NEXT: vpmovqw %ymm0, %xmm0
; CHECK-NEXT: vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
define <8 x i32> @trunc_v8i64_v8i32_zeroes(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v8i64_v8i32_zeroes:
    ; CHECK:    # %bb.0:
    ; CHECK-NEXT: vpsrlq $48, 32(%rdi), %ymm1
    ; CHECK-NEXT: vpsrlq $48, (%rdi), %ymm2
    ; CHECK-NEXT: vmovdqa {{.*#+}} ymm0 = [0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30]
    ; CHECK-NEXT: vpermi2w 32(%rdi), %ymm1, %ymm2, %ymm0
    ; CHECK-NEXT: retq
    %a = load <8 x i64>, <8 x i64>* %x
    %b = lshr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>
    %c = trunc <8 x i64> %b to <8 x i32>
    ret <8 x i32> %c
}

define <16 x i16> @trunc_v16i32_v16i16_zeroes(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v16i32_v16i16_zeroes:
    ; CHECK:    # %bb.0:
    ; CHECK-NEXT: vmovdqa (%rdi), %ymm1
    ; CHECK-NEXT: vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]
    ; CHECK-NEXT: vpermi2w 32(%rdi), %ymm1, %ymm0
    ; CHECK-NEXT: retq
    %a = load <16 x i32>, <16 x i32>* %x
    %b = lshr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16>
    %c = trunc <16 x i32> %b to <16 x i16>
    ret <16 x i16> %c
}

define <32 x i8> @trunc_v32i16_v32i8_zeroes(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_zeroes:
    ; CHECK-AVX512:    # %bb.0:
    ; CHECK-AVX512-NEXT: vpsrlw $8, 32(%rdi), %ymm0
    ; CHECK-AVX512-NEXT: vpsrlw $8, (%rdi), %ymm1
    ; CHECK-AVX512-NEXT: vpackuswb %ymm0, %ymm1, %ymm0
    ; CHECK-AVX512-NEXT: vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
    ; CHECK-AVX512-NEXT: retq
    ;
    ; CHECK-VBMI-LABEL: trunc_v32i16_v32i8_zeroes:
    ; CHECK-VBMI:    # %bb.0:
    ; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm1
    ; CHECK-VBMI-NEXT: vmovdqa {{.*#+}} ymm0 =
define <8 x i32> @trunc_v8i64_v8i32_sign(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {  
; CHECK-LABEL: trunc_v8i64_v8i32_sign:  
; CHECK:  
; CHECK-NEXT: vpsraq $48, 32(%rdi), %ymm1  
; CHECK-NEXT: vpsraq $48, (%rdi), %ymm2  
; CHECK-NEXT: vmovdqa {%.*+} ymm0 = %0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30  
; CHECK-NEXT: vpermi2w %ymm1, %ymm2, %ymm0  
; CHECK-NEXT: retq  
%a = load <8 x i64>, <8 x i64>* %x  
%b = lshr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>  
%c = trunc <8 x i64> %b to <8 x i32>  
ret <8 x i32> %c  
}
; CHECK-VBMI:     # %bb.0:
; CHECK-VBMI-NEXT:  vmovdqa (%rdi), %ymm1
; CHECK-VBMI-NEXT:  vmovdqa {{.*#+}} ymm0 =
[1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63]
; CHECK-VBMI-NEXT:  vpermi2b 32(%rdi), %ymm1, %ymm0
; CHECK-VBMI-NEXT:  retq
%a = load <32 x i16>, <32 x i16>* %x
%b = ashr <32 x i16> %a, <i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8>.
%c = trunc <32 x i16> %b to <32 x i8>
ret <32 x i8> %c

define void @zext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL:  zext_v16i8_v16i64:
; CHECK:     # %bb.0:
; CHECK-NEXT:  vpmovzxbw {{.*#+}} ymm1 =
xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,
xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero
; CHECK-NEXT:  vpshufd {{.*#+}} xmm2 = xmm1[2,3,0,1]
; CHECK-NEXT:  vpmovzxwq {{.*#+}} ymm2 =
xmm2[0],zero,zero,xmm2[1],zero,zero,zero,xmm2[2],zero,zero,zero,xmm2[3],zero,zero,zero
; CHECK-NEXT:  vextracti128 $1, %ymm1, %xmm1
; CHECK-NEXT:  vpshufd {{.*#+}} xmm3 = xmm1[2,3,0,1]
; CHECK-NEXT:  vpmovzxwq {{.*#+}} ymm3 =
xmm3[0],zero,zero,xmm3[1],zero,zero,zero,xmm3[2],zero,zero,zero,xmm3[3],zero,zero,zero
; CHECK-NEXT:  vpmovzxwq {{.*#+}} ymm1 =
xmm1[0],zero,zero,xmm1[1],zero,zero,xmm1[2],zero,zero,xmm1[3],zero,zero,zero
; CHECK-NEXT:  vpmovzxbq {{.*#+}} ymm0 =
xmm0[0],zero,zero,zero,xmm0[1],zero,zero,zero,xmm0[2],zero,zero,zero
; CHECK-NEXT:  vpmovdqa %ymm0, (%rdi)
; CHECK-NEXT:  vpmovdqa %ymm1, 64(%rdi)
; CHECK-NEXT:  vpmovdqa %ymm3, 96(%rdi)
; CHECK-NEXT:  vpmovdqa %ymm2, 32(%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = zext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}

define void @sext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL:  sext_v16i8_v16i64:
; CHECK:     # %bb.0:
; CHECK-NEXT:  vpmovzxbw {{.*#+}} ymm1 =
xmm1[0],zero,xmm1[1],zero,xmm1[2],zero,xmm1[3],zero,zero,zero
; CHECK-NEXT:  vpshufd {{.*#+}} xmm2 =
xmm2[0],zero,zero,xmm2[1],zero,zero,zero
; CHECK-NEXT:  vextracti128 $1, %ymm1, %xmm1
; CHECK-NEXT:  vpshufd {{.*#+}} xmm3 = xmm1[2,3,0,1]
; CHECK-NEXT:  vpmovzxwq {{.*#+}} ymm3 =
xmm3[0],zero,zero,xmm3[1],zero,zero,zero,xmm3[2],zero,zero,zero,xmm3[3],zero,zero,zero
; CHECK-NEXT:  vpmovzxwq {{.*#+}} ymm1 =
xmm1[0],zero,zero,xmm1[1],zero,zero,xmm1[2],zero,zero,xmm1[3],zero,zero,zero
; CHECK-NEXT:  vpmovzxbq {{.*#+}} ymm0 =
xmm0[0],zero,zero,zero,xmm0[1],zero,zero,zero,xmm0[2],zero,zero,zero
; CHECK-NEXT:  vpmovdqa %ymm0, (%rdi)
; CHECK-NEXT:  vpmovdqa %ymm1, 64(%rdi)
; CHECK-NEXT:  vpmovdqa %ymm3, 96(%rdi)
; CHECK-NEXT:  vpmovdqa %ymm2, 32(%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = sext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}
; CHECK-NEXT:  vpmovsxwq %xmm1, %ymm1
; CHECK-NEXT:  vextracti128 $1, %ymm0, %xmm2
; CHECK-NEXT:  vpshufb {{.*#+}} %xmm0, (%edx)
; CHECK-NEXT:  vpmovsxwq %xmm3, %ymm3
; CHECK-NEXT:  vpmovsxwq %xmm0, %ymm0
; CHECK-NEXT:  vpmovsxwq %xmm2, %ymm2
; CHECK-NEXT:  vmovdqa %ymm2, 64(%rdi)
; CHECK-NEXT:  vmovdqa %ymm0, (%rdi)
; CHECK-NEXT:  vmovdqa %ymm3, 96(%rdi)
; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = sext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}
define void @vselect_split_v8il6_setcc(<8 x i16> %s, <8 x i16> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" {  
; CHECK-LABEL: vselect_split_v8il6_setcc:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:  vpcmpeqw %ymm0, %k1
; CHECK-NEXT:  kshiftrb $4, %k1, %k2
; CHECK-NEXT:  vmovdqa64 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm0 {k1}
; CHECK-NEXT:  vmovdqa %ymm2, (%rdx)
; CHECK-NEXT:  vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
%a = icmp eq <8 x i16> %s, %t
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}
define void @vselect_split_v8i32_setcc(<8 x i32> %s, <8 x i32> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" {  
; CHECK-LABEL: vselect_split_v8i32_setcc:
; CHECK:     # %bb.0:
; CHECK-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:  vpcmpeqqd %ymm0, %k1
; CHECK-NEXT:  kshiftrb $4, %k1, %k2
; CHECK-NEXT:  vmovdqa64 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
%a = icmp eq <8 x i32> %s, %t
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}

define void @vselect_split_v16i8_setcc(<16 x i8> %s, <16 x i8> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i8_setcc:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqb %xmm1, %xmm0, %k1
; CHECK-NEXT: kshiftrw $8, %k1, %k2
; CHECK-NEXT: vmovdqa32 32(%rdi), %ymm3 [%k2]
; CHECK-NEXT: vmovdqa32 (%rdi), %ymm2 [%k1]
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <16 x i32>, <16 x i32>* %p
%y = load <16 x i32>, <16 x i32>* %q
%a = icmp eq <16 x i8> %s, %t
%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
store <16 x i32> %b, <16 x i32>* %r
ret void
}

define void @vselect_split_v16i16_setcc(<16 x i16> %s, <16 x i16> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i16_setcc:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqw %ymm1, %ymm0, %k1
; CHECK-NEXT: kshiftrw $8, %k1, %k2
; CHECK-NEXT: vmovdqa32 32(%rdi), %ymm3 [%k2]
; CHECK-NEXT: vmovdqa32 (%rdi), %ymm2 [%k1]
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
define <16 x i8> @trunc_packus_v16i32_v16i8(<16 x i32>* %p) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_packus_v16i32_v16i8:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT:  vpackusdw 32(%rdi), %ymm0, %ymm0
    ; CHECK-NEXT:  vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
    ; CHECK-NEXT:  vpmovuswb %ymm0, %xmm0
    ; CHECK-NEXT:  vzeroupper
    ; CHECK-NEXT:  retq
    %a = load <16 x i32>, <16 x i32>* %p
    %b = icmp slt <16 x i32> %a, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
    %c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> %d = icmp sgt <16 x i32> %c, zeroinitializer
    %f = trunc <16 x i32> %e to <16 x i8>
    ret <16 x i8> %f
}

define void @trunc_packus_v16i32_v16i8_store(<16 x i32>* %p, <16 x i8>* %q) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_packus_v16i32_v16i8_store:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT:  vpackusdw 32(%rdi), %ymm0, %ymm0
    ; CHECK-NEXT:  vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
    ; CHECK-NEXT:  vpmovuswb %ymm0, (%rsi)
    ; CHECK-NEXT:  vzeroupper
    ; CHECK-NEXT:  retq
    %a = load <16 x i32>, <16 x i32>* %p
    %b = icmp slt <16 x i32> %a, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
    %c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> %d = icmp sgt <16 x i32> %c, zeroinitializer
    %f = trunc <16 x i32> %e to <16 x i8>
    store <16 x i8> %f, <16 x i8>* %q
}

; CHECK-NEXT:  retq
%x = load <16 x i32>, <16 x i32>* %p
%y = load <16 x i32>, <16 x i32>* %q
%a = icmp eq <16 x i16> %s, %t
%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
store <16 x i32> %b, <16 x i32>* %r
ret void
}
define <64 x i1> @v64i1_argument_return(<64 x i1> %x) "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_argument_return:
; CHECK:     # %bb.0:
; CHECK-NEXT:   retq
    ret <64 x i1> %x
}

define void @v64i1_shuffle(<64 x i8>* %x, <64 x i8>* %y) "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_shuffle:
; CHECK:     # %bb.0: %entry
; CHECK-NEXT:   vmovdqa (%rdi), %ymm1
; CHECK-NEXT:   vmovdqa 32(%rdi), %ymm0
; CHECK-NEXT:   vp testim %ymm1, %ymm1, %k0
; CHECK-NEXT:   kshiftrd $1, %k0, %k1
; CHECK-NEXT:   movq $-3, %rax
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftrq $63, %k0, %k2
; CHECK-NEXT:   kshiftrq $62, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-5, %rax
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftrq $63, %k0, %k2
; CHECK-NEXT:   kshiftrq $61, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-9, %rax
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftrd $2, %k0, %k2
; CHECK-NEXT:   kshiftrq $63, %k2, %k2
; CHECK-NEXT:   kshiftrq $60, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-17, %rax
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftrd $5, %k0, %k2
; CHECK-NEXT:   kshiftrq $63, %k2, %k2
; CHECK-NEXT:   kshiftrq $59, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-33, %rax
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftrd $4, %k0, %k2
}

return void
}
; CHECK-NEXT:  kshiftrd $13, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $51, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-8193, %rax # imm = 0xDFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $12, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $50, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-16385, %rax # imm = 0xBFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $15, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $49, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-32769, %rax # imm = 0xBFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $14, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $48, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-65537, %rax # imm = 0xFFEFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $17, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $47, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-131073, %rax # imm = 0xFFF7FFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $16, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $46, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-262145, %rax # imm = 0xFFBFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $19, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $45, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-524289, %rax # imm = 0xFFF7FFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $18, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $44, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-1048577, %rax # imm = 0xFFEFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $21, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $43, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-2097153, %rax # imm = 0xFFDFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $20, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $42, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-4194305, %rax # imm = 0xFFFBFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $23, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $41, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-8388609, %rax # imm = 0xFF7FFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $22, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $40, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-16777217, %rax # imm = 0xFEFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $25, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $39, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-33554433, %rax # imm = 0xFDFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $24, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $38, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-67108865, %rax # imm = 0xFBFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $27, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $37, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-134217729, %rax # imm = 0xF7FFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $26, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $36, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-268435457, %rax # imm = 0xEFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $29, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $35, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-536870913, %rax # imm = 0xDFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $28, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $34, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-1073741825, %rax # imm = 0xBFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $31, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $33, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movabsq $-2147483649, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $30, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $32, %k0, %k0
; CHECK-NEXT:  korq %k0, %k2, %k0
; CHECK-NEXT:  movabsq $-4294967297, %rax # imm = 0xFFFFFFFFFFEFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $1, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $31, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0  
; CHECK-NEXT: movabsq $-8589934593, %rax # imm = 0xFFFFFFFFFFFFFFFF  
; CHECK-NEXT: kmovq %rax, %k2  
; CHECK-NEXT: kandq %k2, %k0, %k0  
; CHECK-NEXT: kshiftlq $63, %k1, %k2  
; CHECK-NEXT: kshiftrq $30, %k2, %k2  
; CHECK-NEXT: korq %k2, %k0, %k0  
; CHECK-NEXT: movabsq $-17179869185, %rax # imm = 0xFFFFFFFFFFFFFFFF  
; CHECK-NEXT: kmovq %rax, %k2  
; CHECK-NEXT: kandq %k2, %k0, %k0  
; CHECK-NEXT: kshiftd $3, %k1, %k2  
; CHECK-NEXT: kshiftlq $63, %k2, %k2  
; CHECK-NEXT: kshiftrq $29, %k2, %k2  
; CHECK-NEXT: korq %k2, %k0, %k0  
; CHECK-NEXT: movabsq $-34359738369, %rax # imm = 0xFFFFFFFF7FFFFFFFFF  
; CHECK-NEXT: kmovq %rax, %k2  
; CHECK-NEXT: kandq %k2, %k0, %k0  
; CHECK-NEXT: kshiftrd $5, %k1, %k2  
; CHECK-NEXT: kshiftlq $63, %k2, %k2  
; CHECK-NEXT: kshiftrq $27, %k2, %k2  
; CHECK-NEXT: korq %k2, %k0, %k0  
; CHECK-NEXT: movabsq $-68719476737, %rax # imm = 0xFFFFFFFFEFFFFFFFFF  
; CHECK-NEXT: kmovq %rax, %k2  
; CHECK-NEXT: kandq %k2, %k0, %k0  
; CHECK-NEXT: kshiftr $4, %k1, %k2  
; CHECK-NEXT: kshiftlq $63, %k2, %k2  
; CHECK-NEXT: kshiftrq $26, %k2, %k2  
; CHECK-NEXT: korq %k2, %k0, %k0  
; CHECK-NEXT: movabsq $-137438953473, %rax # imm = 0xFFFFFFFFDFFFFFFFFF  
; CHECK-NEXT: kmovq %rax, %k2  
; CHECK-NEXT: kandq %k2, %k0, %k0  
; CHECK-NEXT: kshiftrd $6, %k1, %k2  
; CHECK-NEXT: kshiftlq $63, %k2, %k2  
; CHECK-NEXT: kshiftrq $25, %k2, %k2  
; CHECK-NEXT: korq %k2, %k0, %k0  
; CHECK-NEXT: movabsq $-274877906945, %rax # imm = 0xFFFFFFFFCFFFFFFFFF  
; CHECK-NEXT: kmovq %rax, %k2  
; CHECK-NEXT: kandq %k2, %k0, %k0  
; CHECK-NEXT: kshiftr $7, %k1, %k2  
; CHECK-NEXT: kshiftlq $63, %k2, %k2  
; CHECK-NEXT: kshiftrq $24, %k2, %k2  
; CHECK-NEXT: korq %k2, %k0, %k0  
; CHECK-NEXT: movabsq $-549755813889, %rax # imm = 0xFFFFFFFF7FFFFFFFFF  
; CHECK-NEXT: kmovq %rax, %k2  
; CHECK-NEXT: kandq %k2, %k0, %k0  
; CHECK-NEXT: kshiftr $6, %k1, %k2  
; CHECK-NEXT: kshiftlq $63, %k2, %k2  
; CHECK-NEXT: kshiftrq $23, %k2, %k2
; CHECK-NEXT:    kshiftrq $17, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-140737488355329, %rax # imm = 0xFFFF7FFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $14, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $16, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-281474976710657, %rax # imm = 0xFFEFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $17, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $15, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-562949953421313, %rax # imm = 0xFFFFDFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $16, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $14, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-1125899906842625, %rax # imm = 0xFFFFBFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $19, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $13, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-2251799813685249, %rax # imm = 0xFFF7FFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $21, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $12, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-4503599627370497, %rax # imm = 0xFFFDFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $20, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $11, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-9007199254740993, %rax # imm = 0xFFF7FFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $21, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $11, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-4503599627370497, %rax # imm = 0xFFF7FFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $20, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $20, %k1, %k2
; CHECK-NEXT:  kshiftrd $29, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $3, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-2305843009213693953, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $28, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $2, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-4611686018427387905, %rax # imm = 0xBFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $31, %k1, %k2
; CHECK-NEXT:  kshiftlq $62, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $30, %k1, %k1
; CHECK-NEXT:  kshiftlq $1, %k0, %k0
; CHECK-NEXT:  kshiftrq $1, %k0, %k0
; CHECK-NEXT:  kmovq %il, %k2
; CHECK-NEXT:  korq %k1, %k0, %k1
; CHECK-NEXT:  kmovq {{.*}}(%rip), %k0
; CHECK-NEXT:  #APP
; CHECK-NEXT:  #NO_APP

entry:
%a = load <64 x i8>, <64 x i8>* %x
%b = icmp eq <64 x i8> %a, zero
%shuf = shufflevector <64 x i1> %b, <64 x i1> undef, <64 x i32> <i32 1, i32 0, i32 3, i32 2, i32 5, i32 4, i32 7, i32 6, i32 9, i32 8, i32 11, i32 10, i32 13, i32 12, i32 15, i32 14, i32 17, i32 16, i32 19, i32 18, i32 21, i32 20, i32 23, i32 22, i32 25, i32 24, i32 27, i32 26, i32 29, i32 28, i32 31, i32 30, i32 33, i32 32, i32 35, i32 34, i32 37, i32 36, i32 39, i32 38, i32 41, i32 40, i32 43, i32 42, i32 45, i32 44, i32 47, i32 46, i32 49, i32 48, i32 51, i32 50, i32 53, i32 52, i32 55, i32 54, i32 57, i32 56, i32 59, i32 58, i32 61, i32 60, i32 63, i32 62>
call void @llvm.masked.store.v64i8.p0v64i8(<64 x i8> %a, <64 x i8>* %y, <64 x i8>* %shuf)
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1.314 thunkify 2.1.2

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 */
1.330 minimatch 2.0.10
1.330.1 Available under license:

```json
{
  "author": "Isaac Z. Schlueter <i@izs.me> (http://blog.izs.me),
  "name": "minimatch",
  "description": "a glob matcher in javascript",
  "version": "2.0.10",
  "repository": {
    "type": "git",
    "url": "git://github.com/isaacs/minimatch.git"
  },
  "main": "minimatch.js",
  "scripts": {
    "posttest": "standard minimatch.js test/*.js",
    "test": "tap test/*.js",
    "prepublish": "browserify -o browser.js -e minimatch.js -s minimatch --bare"
  },
  "engines": {
    "node": "*"
  },
  "dependencies": {
    "brace-expansion": "^1.0.0"
  },
  "devDependencies": {
    "browserify": "^9.0.3",
    "standard": "^3.7.2",
    "tap": "^1.2.0"
  },
  "license": "ISC",
  "files": [
    "minimatch.js",
    "browser.js"
  ]
}
```

1.331 set-blocking 2.0.0
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1.332 ast-types 0.13.3

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1.333 source-map 0.6.1

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1.334 http-signature 1.2.0

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1.335 winston 3.3.3
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Ajay Joshi <jaj@google.com>
Balzs Dn <balazs.dan@gmail.com>
Bharat Mediratta <bharat@menalto.com>
Chandler Carruth <chandlerc@google.com>
Chris Prince <cprince@google.com>
Chris Taylor <taylorc@google.com>
Dan Egnor <egnor@google.com>
Eric Roman <eroman@chromium.org>
Hady Zalek <hady.zalek@gmail.com>
Jeffrey Yasskin <jyasskin@google.com>
Ji Sigursson <joi@google.com>
Keir Mierle <mierle@gmail.com>
Keith Ray <keith.ray@gmail.com>
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Markus Heule <markus.heule@gmail.com>
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Mikls Fazekas <mfazekas@szemafor.com>
Pasi Valminen <pasi.valminen@gmail.com>
Patrick Hanna <phanna@google.com>
Patrick Riley <spr@google.com>
Peter Kaminski <piotrk@google.com>
Preston Jackson <preston.a.jackson@gmail.com>
Rainer Klaffenboeck <rainer.klaffenboeck@dynatrace.com>
Russ Cox <rsc@google.com>
Russ Rufer <russ@pentad.com>
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27287880
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1.352 success-symbol 0.1.0

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1.353 detective 4.7.1

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1.360 proxy-agent 3.0.3

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1.362 q 1.5.1

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*
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*
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1.364 http-errors 1.7.3

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1.367 punycode 2.1.1

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1.368 jsprim 1.4.1

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1.370 wide-align 1.1.3

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1.371 pump 2.0.1

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1.374 mime-types 2.1.27

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1.375 ansi-red 0.1.1

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1.376 define-property 1.0.0

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1.378 commoner 0.10.8

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1.380 fs-extra-promise 0.3.1

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1.381 async 1.5.2

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C++ Big Integer Library
(see ChangeLog for version)

http://mattmccutchen.net/bigint/

Written and maintained by Matt McCutchen <matt@mattmccutchen.net>

You can use this library in a C++ program to do arithmetic on integers of size limited only by your computer's memory. The library provides BigUnsigned and BigInteger classes that represent nonnegative integers and signed integers, respectively. Most of the C++ arithmetic operators are overloaded for these classes, so big-integer calculations are as easy as:

```cpp
#include "BigIntegerLibrary.hh"

BigInteger a = 65536;
cout << (a * a * a * a * a * a * a * a);

(prints 340282366920938463463374607431768211456)
```

The code in `sample.cc' demonstrates the most important features of the library. To get started quickly, read the code and explanations in that file and run it. If you want more detail or a feature not shown in `sample.cc', consult the actual header and source files, which are thoroughly commented.

This library emphasizes ease of use and clarity of implementation over speed; some users will prefer GMP (http://swox.com/gmp/), which is faster. The code is intended to be reasonably portable across computers and modern C++ compilers; in particular, it uses whatever word size the computer provides (32-bit, 64-bit, or otherwise).

Compiling programs that use the library
---------------------------------------

The library consists of a folder full of C++ header files (`.hh') and source files (`.cc'). Your own programs should `#include' the necessary header files and link with the source files. A makefile that builds the sample program (`sample.cc') is included; you can adapt it to replace the sample with your own program.

Alternatively, you can use your own build system or IDE. In that case, you must put the library header files where the compiler will find them and arrange to have your program linked with the library source files; otherwise, you will get errors about missing header files or "undefined references". To learn how to do this, consult the documentation for the build system or IDE; don't bother asking me. Adding all the library files to your project will work in many IDEs but may
not be the most desirable approach.

Resources
---------
The library’s Web site (above) provides links to released versions, the current
development version, and a mailing list for release announcements, questions,
bug reports, and other discussion of the library. I would be delighted to hear
from you if you like this library and/or find a good use for it.

Bugs and enhancements
---------------------
The library has been tested by me and others but is by no means bug-free. If
you find a bug, please report it, whether it comes in the form of compiling
trouble, a mathematically inaccurate result, or a memory-management bloopers
(since I use Java, these are altogether too common in my C++). I generally fix
all reported bugs. You are also welcome to request enhancements, but I am
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1.383 es6-promise 4.2.8
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1.386 re2 20200701

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1.393 cryptojslib 3.1.2

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1.395 ansi-yellow 0.1.1

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## Usage

```js
var supportsColor = require('supports-color');

if (supportsColor) {
    console.log('Terminal supports color);
}
```

It obeys the `--color` and `--no-color` CLI flags.

For situations where using `--color` is not possible, add an environment variable `FORCE_COLOR` with any value to force color. Trumps `--no-color`.

## Related

- [supports-color-cli](https://github.com/chalk/supports-color-cli) - CLI for this module
- [chalk](https://github.com/chalk/chalk) - Terminal string styling done right

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1.406 moment 2.27.0

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1.410 negotiator 0.6.2

1.411 angular-sanitize 1.4.14
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1.412 csv-parse 4.10.1

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1.415 libvpx 1.7.0-262-gbe5df6080

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Authors: Loren Merritt <lorenmt@u.washington.edu>
Anton Mitrofanov <BugMaster@narod.ru>
Jason Garrett-Glaser <darkshikari@gmail.com>
Henrik Gramner <hengar-6@student.ltu.se>

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Chris Prince <cprince@google.com>
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1.417 sax 1.2.4
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1.420 defs 1.1.1

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1.422 prompt-radio 1.2.1

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1.423 raw-body 2.4.1

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1.424 serialport-parser-regex 1.0.5

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1.425 has-binary2 1.0.3

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1.426 angular 1.4.14

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1.429 process-nextick-args 2.0.1
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1.430 del 3.0.0

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1.431 openssl 1.0.2d

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1.434 jsbn 0.1.1

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1.435 commander 2.20.3

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1.436 serialport-parser-delimiter 1.0.5

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1.438 ansi-underline 0.1.1

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1.439 is-my-ip-valid 1.0.0

1.440 xmlbuilder 11.0.1

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1.447 time-stamp 1.1.0

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1.449 component-emitter 1.3.0

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1.450 prelude-ls 1.1.2

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1.451 simple-swizzle 0.2.2

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1.457 prebuild-install 4.0.0

Open Source Used In CLI Analyzer 3.6.6 1282
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### 1.458 libuv 1.21.0

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#ifndef UV_BSD_H
#define UV_BSD_H

#define UV_PLATFORM_FS_EVENT_FIELDS
    uv__io_t event_watcher;

#define UV_IO_PRIVATE_PLATFORM_FIELDS
    int rcount;
    int wcount;

#define UV_HAVE_KQUEUE 1

#endif /* UV_BSD_H */

Files: *

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1.462 angular-resource 1.4.14

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; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s

define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
; CHECK-LABEL: test_sitofp_fixed:

; First, extend each i32 to i64
; CHECK-DAG: sshll2.2d [[BLOCK0_HI:v[0-9]+]], v0, #0
; CHECK-DAG: sshll2.2d [[BLOCK1_HI:v[0-9]+]], v1, #0
; CHECK-DAG: sshll2.2d [[BLOCK2_HI:v[0-9]+]], v2, #0
; CHECK-DAG: sshll2.2d [[BLOCK3_HI:v[0-9]+]], v3, #0
; CHECK-DAG: sshll.2d [[BLOCK0_LO:v[0-9]+]], v0, #0
; CHECK-DAG: sshll.2d [[BLOCK1_LO:v[0-9]+]], v1, #0
; CHECK-DAG: sshll.2d [[BLOCK2_LO:v[0-9]+]], v2, #0
; CHECK-DAG: sshll.2d [[BLOCK3_LO:v[0-9]+]], v3, #0

; Next, convert each to double.
; CHECK-DAG: scvtf.2d v0, [[BLOCK0_LO]]
; CHECK-DAG: scvtf.2d v1, [[BLOCK0_HI]]
; CHECK-DAG: scvtf.2d v2, [[BLOCK1_LO]]
; CHECK-DAG: scvtf.2d v3, [[BLOCK1_HI]]
; CHECK-DAG: scvtf.2d v4, [[BLOCK2_LO]]
; CHECK-DAG: scvtf.2d v5, [[BLOCK2_HI]]
; CHECK-DAG: scvtf.2d v6, [[BLOCK3_LO]]
; CHECK-DAG: scvtf.2d v7, [[BLOCK3_HI]]

; CHECK: ret
%flt = sitofp <16 x i32> %in to <16 x double>
%res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0>
ret <16 x double> %res

; This one is small enough to satisfy isSimple, but still illegally large.
define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
; CHECK-LABEL: test_sitofp_fixed_shortish:

; CHECK-DAG: scvtf.2d v0, v0
; CHECK-DAG: scvtf.2d v1, v1

; CHECK: ret
%flt = sitofp <4 x i64> %in to <4 x double>
%res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0>
ret <4 x double> %res

; RUN: llc < %s -mtriple=s390x-linux-gnu -mcpu=zEC12 -verify-machineinstrs | FileCheck %s
;
; Test that early if conversion produces LOCR with operands of the right
; register classes.
define void @autogen_SD4739(i8*) {
; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
BB:
%L34 = load i8, i8* %0
%Cmp56 = icmp sgt i8 undef, %L34
br label %CF246

CF246: ; preds = %CF246, %BB
%SI163 = select i1 %Cmp56, i8 %L34, i8 undef
br i1 undef, label %CF246, label %CF248

CF248: ; preds = %CF248, %CF246
store i8 %SI163, i8* %0
br label %CF248
The two loads based on %struct.0, loading two different data types
cause LSR to assume type "void" for the memory type. This would then
cause an assert in isLegalAddressingMode. Make sure we no longer crash.

target triple = "hexagon"

%struct.0 = type { i8*, i8, %union.anon.0 }
%union.anon.0 = type { i8* }

define hidden fastcc void @fred() unnamed_addr #0 {
entry:
br i1 undef, label %while.end, label %while.body.lr.ph

while.body.lr.ph: ; preds = %entry
   br label %while.body
while.body: ; preds = %exit.2, %while.body.lr.ph
   %lsr.iv = phi %struct.0* [%cgep22, %exit.2], [undef, %while.body.lr.ph]
   switch i32 undef, label %exit [
      i32 1, label %sw.bb.i
      i32 2, label %sw.bb3.i
   ]
  
  sw.bb.i: ; preds = %while.body
     unreachable

  sw.bb3.i: ; preds = %while.body
     unreachable

exit: ; preds = %while.body
   switch i32 undef, label %exit.2 [
      i32 1, label %sw.bb.i17
      i32 2, label %sw.bb3.i20
   ]

  sw.bb.i17: ; preds = %exit
     %0 = bitcast %struct.0* %lsr.iv to i32*
     %1 = load i32, i32* %0, align 4
     unreachable

  sw.bb3.i20: ; preds = %exit
     %2 = bitcast %struct.0* %lsr.iv to i8**
     %3 = load i8*, i8** %2, align 4
     unreachable
exit.2: ; preds = %exit
%cegp22 = getelementptr %struct.0, %struct.0* %lsr.iv, i32 1
br label %while.body

while.end: ; preds = %entry
ret void
}

attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }
; RUN: opt -consthoist -S -o - %s | FileCheck %s
target triple = "thumbv6m-none--musleabi"

; Check that for i8 type, the maximum legal offset is 31.
; Also check that an constant used as value to be stored rather than
; pointer in a store instruction is hoisted.
; CHECK: foo_i8
; CHECK-DAG:  %\[C1:const\[0-9\]?\] = bitcast i32 805874720 to i32
; CHECK-DAG:  %\[C2:const\[0-9\]?\] = bitcast i32 805874688 to i32
; CHECK-DAG:  %\[C3:const\[0-9\]?\] = bitcast i32 805873720 to i32
; CHECK-DAG:  %\[C4:const\[0-9\]?\] = bitcast i32 805873688 to i32
; CHECK:  %0 = inttoptr i32 %\[C2\] to i8*
; CHECK-NEXT: %1 = load volatile i8, i8* %0
; CHECK-NEXT: %\[M1:const_mat\[0-9\]?\] = add i32 %\[C2\], 4
; CHECK-NEXT: %2 = inttoptr i32 %\[M1\] to i8*
; CHECK-NEXT: %3 = load volatile i8, i8* %2
; CHECK-NEXT: %\[M2:const_mat\[0-9\]?\] = add i32 %\[C2\], 31
; CHECK-NEXT: %4 = inttoptr i32 %\[M2\] to i8*
; CHECK-NEXT: %5 = load volatile i8, i8* %4
; CHECK-NEXT: %\[M3:const_mat\[0-9\]?\] = add i32 %\[C2\], 7
; CHECK-NEXT: %6 = inttoptr i32 %\[M3\] to i8*
; CHECK-NEXT: %7 = load volatile i8, i8* %6
; CHECK-NEXT: %\[M4:const_mat\[0-9\]?\] = add i32 %\[C1\], 31
; CHECK-NEXT: %8 = inttoptr i32 %\[M4\] to i8*
; CHECK-NEXT: store i8* %8, i8** @goo
@goo = global i8* undef

define void @foo_i8() {
  entry:
  %0 = load volatile i8, i8* inttoptr (i32 805874688 to i8*)
  %1 = load volatile i8, i8* inttoptr (i32 805874692 to i8*)
  %2 = load volatile i8, i8* inttoptr (i32 805874719 to i8*)
  %3 = load volatile i8, i8* inttoptr (i32 805874720 to i8*)
  %4 = load volatile i8, i8* inttoptr (i32 805874727 to i8*)
  store i8 %4, i8* inttoptr(i32 805873688 to i8*)
  store i8 %3, i8* inttoptr(i32 805873719 to i8*)
  store i8 %2, i8* inttoptr(i32 805873720 to i8*)
  store i8 %1, i8* inttoptr(i32 805873727 to i8*)
  store i8* inttoptr(i32 805874800 to i8*), i8** @goo
  ret void
}

; Check that for i16 type, the maximum legal offset is 62.
; CHECK: foo_i16
; CHECK-DAG: %[[C1:const[0-9]??]] = bitcast i32 805874752 to i32
; CHECK-DAG: %[[C2:const[0-9]??]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i16*
; CHECK-NEXT: %1 = load volatile i16, i16* %0, align 2
; CHECK-NEXT: %[[M1:const_mat[0-9]??]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i16*
; CHECK-NEXT: %3 = load volatile i16, i16* %2, align 2
; CHECK-NEXT: %[[M2:const_mat[0-9]??]] = add i32 %[[C2]], 32
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i16*
; CHECK-NEXT: %5 = load volatile i16, i16* %4, align 2
; CHECK-NEXT: %[[M3:const_mat[0-9]??]] = add i32 %[[C2]], 62
; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to i16*
; CHECK-NEXT: %7 = load volatile i16, i16* %6, align 2
; CHECK-NEXT: %8 = inttoptr i32 %[[C1]] to i16*
; CHECK-NEXT: %9 = load volatile i16, i16* %8, align 2
; CHECK-NEXT: %[[M4:const_mat[0-9]??]] = add i32 %[[C1]], 22
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i16*
; CHECK-NEXT: %11 = load volatile i16, i16* %10, align 2

define void @foo_i16() {
  entry:
  %0 = load volatile i16, i16* inttoptr (i32 805874688 to i16*), align 2
  %1 = load volatile i16, i16* inttoptr (i32 805874692 to i16*), align 2
  %2 = load volatile i16, i16* inttoptr (i32 805874720 to i16*), align 2
  %3 = load volatile i16, i16* inttoptr (i32 805874750 to i16*), align 2
  %4 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
  %5 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
  ret void
; Check that for i32 type, the maximum legal offset is 124.
; CHECK-DAG: %[[C1:const[0-9]??]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]??]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i32*
; CHECK-NEXT: %1 = load volatile i32, i32* %0, align 4
; CHECK-NEXT: %[[M1:const_mat[0-9]??]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i32*
; CHECK-NEXT: %3 = load volatile i32, i32* %2, align 4
; CHECK-NEXT: %[[M2:const_mat[0-9]??]] = add i32 %[[C2]], 124
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i32*
; CHECK-NEXT: %5 = load volatile i32, i32* %4, align 4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i32*
; CHECK-NEXT: %7 = load volatile i32, i32* %6, align 4
; CHECK-NEXT: %[[M3:const_mat[0-9]??]] = add i32 %[[C1]], 8
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i32*
; CHECK-NEXT: %9 = load volatile i32, i32* %8, align 4
; CHECK-NEXT: %[[M4:const_mat[0-9]??]] = add i32 %[[C1]], 12
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i32*
; CHECK-NEXT: %11 = load volatile i32, i32* %10, align 4

define void @foo_i32() {
entry:
  %0 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 4
  %1 = load volatile i32, i32* inttoptr (i32 805874692 to i32*), align 4
  %2 = load volatile i32, i32* inttoptr (i32 805874704 to i32*), align 4
  %3 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
  %4 = load volatile i32, i32* inttoptr (i32 805874824 to i32*), align 4
  %5 = load volatile i32, i32* inttoptr (i32 805874828 to i32*), align 4
ret void
}
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=aarch64-- | FileCheck %s

; A shuffle mask with all undef elements is always legal.

define <4 x i32> @PR41535(<2 x i32> %p1, <2 x i32> %p2) {
; CHECK-LABEL: PR41535:
; CHECK: // %bb.0:
; CHECK-NEXT: ext v0.8b, v0.8b, v1.8b, #4
; CHECK-NEXT: mov v0.d[1], v0.d[0]
; CHECK-NEXT: ret
%cat1 = shufflevector <2 x i32> %p1, <2 x i32> undef, <4 x i32> <i32 undef, i32 1, i32 undef, i32 undef>
%cat2 = shufflevector <2 x i32> %p2, <2 x i32> undef, <4 x i32> <i32 0, i32 undef, i32 undef, i32 undef>
%r = shufflevector <4 x i32> %cat1, <4 x i32> %cat2, <4 x i32> <i32 undef, i32 undef, i32 1, i32 4>
ret <4 x i32> %r
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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=avx512vl,avx512bw,avx512dq,prefer-256-bit | FileCheck %s

; This file primarily contains tests for specific places in X86ISelLowering.cpp that needed be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

define void @add256(<16 x i32>)* %a, <16 x i32>)* %b, <16 x i32>)* %c) "min-legal-vector-width"="256" {
; CHECK-LABEL: add256:
; CHECK-NEXT:   # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:    vpaddd 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:    vpaddd (%rsi), %ymm0, %ymm0
; CHECK-NEXT:    vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:    vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq

%d = load <16 x i32>, <16 x i32>* %a
%e = load <16 x i32>, <16 x i32>* %b
%f = add <16 x i32>, %d, %e
store <16 x i32> %f, <16 x i32>* %c
ret void
}

define void @add512(<16 x i32>)* %a, <16 x i32>)* %b, <16 x i32>)* %c) "min-legal-vector-width"="512" {
; CHECK-LABEL: add512:
; CHECK:       # %bb.0:
; CHECK-NEXT: vpaddd 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT: vpaddd (%rsi), %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, 64(%rdx)
; CHECK-NEXT: vmovdqa %ymm1, 64(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq

%d = load <16 x i32>, <16 x i32>* %a
%e = load <16 x i32>, <16 x i32>* %b
%f = add <16 x i32>, %d, %e
store <16 x i32> %f, <16 x i32>* %c
ret void
}
define void @avg_v64i8_256(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: avg_v64i8_256:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vmovdqa (%rsi), %ymm0
    ; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm1
    ; CHECK-NEXT:    vpavgb (%rdi), %ymm0, %ymm0
    ; CHECK-NEXT:    vpavgb 32(%rdi), %ymm1, %ymm1
    ; CHECK-NEXT:    vmovdqu %ymm1, (%rax)
    ; CHECK-NEXT:    vmovdqu %ymm0, (%rax)
    ; CHECK-NEXT: vzeroupper
    ; CHECK-NEXT:    retq
    %1 = load <64 x i8>, <64 x i8>* %a
    %2 = load <64 x i8>, <64 x i8>* %b
    %3 = zext <64 x i8> %1 to <64 x i32>
    %4 = zext <64 x i8> %2 to <64 x i32>
    %5 = add nuw nsw <64 x i32> %3, <64 x i32> %4
    %6 = lshr <64 x i32> %5, %4
    %7 = lshr <64 x i32> %6, %5
    store <64 x i8> %8, <64 x i8>* undef, align 4
    ret void
}

define void @avg_v64i8_512(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: avg_v64i8_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vmovdqa64 (%rsi), %zmm0
    ; CHECK-NEXT:    vpavgb (%rdi), %zmm0, %zmm0
    ; CHECK-NEXT:    vmovdqa64 %zmm0, (%rdx)
    ; CHECK-NEXT: vzeroupper
    ; CHECK-NEXT:    retq
    %d = load <16 x i32>, <16 x i32>* %a
    %e = load <16 x i32>, <16 x i32>* %b
    %f = add <16 x i32> %d, %e
    store <16 x i32> %f, <16 x i32>* %c
    ret void
}
define void @pmaddwd_32_256(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="256" {
 ; CHECK-LABEL: pmaddwd_32_256:
 ; CHECK:       # %bb.0:
 ; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
 ; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
 ; CHECK-NEXT:  vpmaddwd 32(%rsi), %ymm1, %ymm1
 ; CHECK-NEXT:  vpmaddwd (%rsi), %ymm0, %ymm0
 ; CHECK-NEXT:  vpmaddwd (%rsi), %ymm0, %ymm0
 ; CHECK-NEXT:  vmovdqa %ymm0, 32(%rdx)
 ; CHECK-NEXT:  vmovdqa %ymm1, %rdx
 ; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
 ; CHECK-NEXT:  vzeroupper
 ; CHECK-NEXT:  retq
  %A = load <32 x i16>, <32 x i16>* %APtr
  %B = load <32 x i16>, <32 x i16>* %BPtr
  %a = sext <32 x i16> %A to <32 x i32>
  %b = sext <32 x i16> %B to <32 x i32>
  %m = mul nsw <32 x i32> %a, %b
  %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>  %even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>  %ret = add <16 x i32> %odd, %even  store <16 x i32> %ret, <16 x i32>* undef, align 4  ret void
}

define void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="512" {

; CHECK-LABEL: pmaddwd_32_512:
; CHECK:
; # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT: vpmaddwd (%rsi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq

%A = load <32 x i16>, <32 x i16>* %APtr
%B = load <32 x i16>, <32 x i16>* %BPtr
%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> %i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> %i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

define void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="256" {
; CHECK-LABEL: psubus_64i8_max_256:
; CHECK:
; # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa32 (%rdi), %ymm1
; CHECK-NEXT: vpsubusb 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT: vpsubusb (%rsi), %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq

%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %yptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

define void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="512" {
; CHECK-LABEL: psubus_64i8_max_512:
; CHECK:
; # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT: vpsubusb (%rsi), %zmm0, %zmm0
define i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: _Z9test_charPcS_i_256:
    ; CHECK:       # %bb.0: # %entry
    ; CHECK-NEXT:    movl %edx, %eax
    ; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
    ; CHECK-NEXT:    xorl %ecx, %ecx
    ; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
    ; CHECK-NEXT:    vpxor %xmm2, %xmm2, %xmm2
    ; CHECK-NEXT:    .p2align 4, 0x90
    ; CHECK-NEXT:  .LBB8_1: # %vector.body
    ; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
    ; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %ymm3
    ; CHECK-NEXT:    vpmovsxbw 16(%rdi,%rcx), %ymm4
    ; CHECK-NEXT:    vpmovsxbw (%rsi,%rcx), %ymm5
    ; CHECK-NEXT:    vpmaddwd %ymm3, %ymm5, %ymm3
    ; CHECK-NEXT:    vpaddd %ymm1, %ymm3, %ymm1
    ; CHECK-NEXT:    vpmaddwd %ymm4, %ymm3, %ymm3
    ; CHECK-NEXT:    vpaddd %ymm2, %ymm3, %ymm2
    ; CHECK-NEXT:    addq $32, %rcx
    ; CHECK-NEXT:    cmpq %rcx, %rax
    ; CHECK-NEXT:    jne .LBB8_1
    ; CHECK-NEXT:  # %bb.2: # %middle.block
    ; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm1
    ; CHECK-NEXT:    vpaddd %ymm0, %ymm2, %ymm0
    ; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm0
    ; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
    ; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
    ; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
    ; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
    ; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
}
entry:
%3 = zext i32 %2 to i64
br label %vector.body

vector.body:
%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body

middle.block:
%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> %i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef
%bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> %i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef
%bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> %i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> %i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef
%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> %i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13
}

define i32 @_Z9test_charPcS_i_512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="512" {
 ; CHECK-LABEL: _Z9test_charPcS_i_512:
 ; CHECK:   # %bb.0: # %entry
 ; CHECK-NEXT: movl %edx, %eax
 ; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
 ; CHECK-NEXT: xorl %ecx, %ecx
 ; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
 ; CHECK-NEXT: .p2align 4, 0x90
 ; CHECK-NEXT: .LBB9_1: # %vector.body
 ; CHECK-NEXT:   # =>This Inner Loop Header: Depth=1
 ; CHECK-NEXT: vpmovsxbw (%rdi,%rcx), %zmm2
 ; CHECK-NEXT: vpmovsxbw (%rsi,%rcx), %zmm3
 ; CHECK-NEXT: vpmaddwd %zmm2, %zmm3, %zmm2
 ; CHECK-NEXT: vpaddd %zmm1, %zmm2, %zmm1
 ; CHECK-NEXT: addq $32, %rcx
 ; CHECK-NEXT: cmpq %rcx, %rax
 ; CHECK-NEXT: jne .LBB9_1
 ; CHECK-NEXT: .LBB9_2: # %middle.block
 ; CHECK-NEXT: vpaddd %zmm0, %zmm1, %zmm0
 ; CHECK-NEXT: vextracti64x4 %zmm0, %ymm1
 ; CHECK-NEXT: vpaddd %zmm1, %zmm0, %zmm0
 ; CHECK-NEXT: vextracti128 %ymm0, %xmm1
 ; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
 ; CHECK-NEXT: vpaddd %zmm0, %zmm1, %zmm0
 ; CHECK-NEXT: vextracti64x4 %zmm1, %ymm0
 ; CHECK-NEXT: vpaddd %zmm0, %zmm1, %zmm0
 ; CHECK-NEXT: vmovd %zmm0, %eax
 ; CHECK-NEXT: vzeroupper
 ; CHECK-NEXT: retq
entry:
%3 = zext i32 %2 to i64
br label %vector.body

vector.body:
%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%6 = sext <32 x i8> %wide.load
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body

middle.block:
%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
%bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
%bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13

}; CHECK-LABEL: sad_16i8_256:
; CHECK: # %bb.0: # %entry
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: movq $-1024, %rax # imm = 0xFC00
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB10_1: # %vector.body
# Inner Loop Header: Depth=1
# %bb.2: # %middle.block

ENTRY:
br label %vector.body

VECTOR.BODY:

%index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
%vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
%0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
%1 = bitcast i8* %0 to <16 x i8>*
%2 = zext <16 x i8> to <16 x i32>*
%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
%4 = bitcast i8* %3 to <16 x i8>*
%wide.load = load <16 x i8>, <16 x i8>* %1, align 4
%5 = sub nsw <16 x i32> %2, %5
%6 = sub nsw <16 x i32> zeroinitializer, %5
%7 = icmp sgt <16 x i32> %6, %7
%8 = sub nsw <16 x i32> zeroinitializer, %6
%9 = select <16 x i1> %7, <16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

MIDDLE.BLOCK:

%lcssa = phi <16 x i32> [ %10, %vector.body ]
%rdx.shuf = shufflevector <16 x i32> %lcssa, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> undef, <16 x i32> unde...
i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

define i32 @sad_16i8_512() "min-legal-vector-width"="512" {
  ; CHECK-LABEL: sad_16i8_512:
  ; CHECK:       # %bb.0: # %entry
  ; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
  ; CHECK-NEXT:    movq $-1024, %rax # imm = 0xFC00
  ; CHECK-NEXT:    .p2align 4, 0x90
  ; CHECK-NEXT:  .LBB11_1: # %vector.body
  ; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
  ; CHECK-NEXT:    vmovdqu a+1024(%rax), %xmm1
  ; CHECK-NEXT:    vpsadbw b+1024(%rax), %xmm1, %xmm1
  ; CHECK-NEXT:    vpaddd %zmm0, %zmm1, %zmm0
  ; CHECK-NEXT:    addq $4, %rax
  ; CHECK-NEXT:    jne .LBB11_1
  ; CHECK-NEXT:  # %bb.2: # %middle.block
  ; CHECK-NEXT:    vextracti64x4 $1, %zmm0, %ymm1
  ; CHECK-NEXT:    vpaddd %zmm1, %zmm0, %zmm0
  ; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
  ; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
  ; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
  ; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
  ; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
  ; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
  ; CHECK-NEXT:    vmovd %xmm0, %eax
  ; CHECK-NEXT:    vzeroupper
  ; CHECK-NEXT:    retq
  entry:
  br label %vector.body
vector.body:
  %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
  %vec.phi = phi i64 <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
  %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
  %1 = bitcast i8* %0 to <16 x i8>*
  %wide.load = load <16 x i8>, <16 x i8>* %1, align 4
%2 = zext <16 x i8> %wide.load to <16 x i32>
%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
%4 = bitcast i8* %3 to <16 x i8>*
%wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
%5 = zext <16 x i8> %wide.load1 to <16 x i32>
%6 = sub nsw <16 x i32> %2, %5
%7 = icmp sgt <16 x i32> %6, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1, %i32 -1>
%8 = sub nsw <16 x i32> zeroinitialzier, %6
%9 = select <16 x i1> %7, %i16, %idx
%index.next = add i64 %index, 4
%10 = add nsw <16 x i32> %9, vec.phi
%middle.block:
%.lcssa = phi <16 x i32> [ %10, %vector.body ]
%rdx.shuf = shufflevector <16 x i32> %.lcssa, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %.lcssa, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

define void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f32_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vcvtq2ps %ymm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm1
; CHECK-NEXT: vcvtq2ps %ymm1, %ymm1
; CHECK-NEXT: vmovaps %ymm1, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT: vzeroupper

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define void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: sbto16f32_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:    vpmovm2d %k0, %zmm0
    ; CHECK-NEXT:    vcvtdq2ps %zmm0, %zmm0
    ; CHECK-NEXT:    vmovaps %zmm0, (%rdi)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %mask = icmp slt <16 x i16> %a, zeroinitializer
    %1 = sitofp <16 x i1> %mask to <16 x float>
    store <16 x float> %1, <16 x float>* %res
    ret void
}

define void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: sbto16f64_256:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:    kshiftrw $8, %k0, %k1
    ; CHECK-NEXT:    vpmovm2d %k1, %ymm0
    ; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm1
    ; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm0
    ; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm0
    ; CHECK-NEXT:    vpmovm2d %k0, %ymm2
    ; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm3
    ; CHECK-NEXT:    vextracti128 $1, %ymm2, %xmm2
    ; CHECK-NEXT:    vmovaps %ymm2, 32(%rdi)
    ; CHECK-NEXT:    vmovaps %ymm3, (%rdi)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %mask = icmp slt <16 x i16> %a, zeroinitializer
    %1 = sitofp <16 x i1> %mask to <16 x double>
    store <16 x double> %1, <16 x double>* %res
    ret void
}

define void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: sbto16f64_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:    kshiftrw $8, %k0, %k1
    ; CHECK-NEXT:    vpmovm2d %k1, %ymm0
    ; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm1
    ; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm0
    ; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm0
    ; CHECK-NEXT:    vpmovm2d %k0, %ymm2
    ; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm3
    ; CHECK-NEXT:    vextracti128 $1, %ymm2, %xmm2
    ; CHECK-NEXT:    vmovaps %ymm2, 32(%rdi)
    ; CHECK-NEXT:    vmovaps %ymm3, (%rdi)
    ; CHECK-NEXT:    vmovaps %ymm0, 96(%rdi)
    ; CHECK-NEXT:    vmovaps %ymm1, 64(%rdi)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %mask = icmp slt <16 x i16> %a, zeroinitializer
    %1 = sitofp <16 x i1> %mask to <16 x double>
    store <16 x double> %1, <16 x double>* %res
    ret void
}
define void @ubto16f64_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {  
    %mask = icmp slt <16 x i16> %a, zeroinitializer  
    %1 = uitofp <16 x i1> %mask to <16 x double>  
    store <16 x double> %1, <16 x double>* %res  
    ret void  
}

define void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {  
    %mask = icmp slt <16 x i16> %a, zeroinitializer  
    %1 = sitofp <16 x i1> %mask to <16 x double>  
    store <16 x double> %1, <16 x double>* %res  
    ret void  
}

define void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {  
    %mask = icmp slt <16 x i16> %a, zeroinitializer  
    %1 = uitofp <16 x i1> %mask to <16 x double>  
    store <16 x double> %1, <16 x double>* %res  
    ret void  
}
%mask = icmp slt <16 x i16> %a, zeroinitialize
%1 = uitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f64_256:
; CHECK:       # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm0
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm0
; CHECK-NEXT: vpsrlw $31, %ymm0, %ymm1
; CHECK-NEXT: vextract128 %ymm1, %ymm0, %ymm2
; CHECK-NEXT: vextract128 %ymm2, %ymm1
; CHECK-NEXT: vextract128 %ymm3, %ymm2
; CHECK-NEXT: vextract128 %ymm4, %ymm3
; CHECK-NEXT: vextract128 %ymm5, %ymm4
; CHECK-NEXT: vextract128 %ymm6, %ymm5
; CHECK-NEXT: vextract128 %ymm7, %ymm6
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitialize
%1 = uitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f64_512:
; CHECK:       # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vpsrlw $31, %zmm0, %zmm1
; CHECK-NEXT: vpmovm2d %k1, %zmm0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vpmovm2d %k1, %zmm0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vpsrlw $31, %zmm0, %zmm2
; CHECK-NEXT: vextracti64x4 %zmm1, %zmm0
; CHECK-NEXT: vextracti64x4 %zmm2, %zmm1
; CHECK-NEXT: vextracti64x4 %zmm3, %zmm2
; CHECK-NEXT: vextracti64x4 %zmm4, %zmm3
; CHECK-NEXT: vextracti64x4 %zmm5, %zmm4
; CHECK-NEXT: vextracti64x4 %zmm6, %zmm5
; CHECK-NEXT: vextracti64x4 %zmm7, %zmm6
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitialize
%1 = uitofp <16 x i1> %mask to <16 x float>
store <16 x double> %1, <16 x double>* %res
ret void
}

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: test_16f32toub_256:
  ; CHECK: # %bb.0:
  ; CHECK-NEXT: cvtvtsp2dq (%rdi), %ymm1
  ; CHECK-NEXT: vpslld $31, %ymm1, %ymm1
  ; CHECK-NEXT: vpmovd2m %ymm1, %k0
  ; CHECK-NEXT: cvtvtsp2dq 32(%rdi), %ymm1
  ; CHECK-NEXT: vpslld $31, %ymm1, %ymm1
  ; CHECK-NEXT: vpmovd2m %ymm1, %k1
  ; CHECK-NEXT: kunpckbw %k0, %k1, %k1
  ; CHECK-NEXT: vmovdq16 %ymm0, %ymm0 {%k1} {z}
  ; CHECK-NEXT: retq
  %a = load <16 x float>, <16 x float>* %ptr
  %mask = fptoui <16 x float> %a to <16 x i1>
  %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
  ret <16 x i16> %select
}

define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {
  ; CHECK-LABEL: test_16f32toub_512:
  ; CHECK: # %bb.0:
  ; CHECK-NEXT: cvtvtsp2dq (%rdi), %zmm1
  ; CHECK-NEXT: vpslld $31, %zmm1, %zmm1
  ; CHECK-NEXT: vpmovd2m %zmm1, %k1
  ; CHECK-NEXT: vmovdq16 %ymm0, %ymm0 {%k1} {z}
  ; CHECK-NEXT: retq
  %a = load <16 x float>, <16 x float>* %ptr
  %mask = fptoui <16 x float> %a to <16 x i1>
  %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
  ret <16 x i16> %select
}

define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: test_16f32tosb_256:
  ; CHECK: # %bb.0:
  ; CHECK-NEXT: cvtvtsp2dq (%rdi), %ymm1
  ; CHECK-NEXT: vpmovd2m %ymm1, %k0
  ; CHECK-NEXT: cvtvtsp2dq 32(%rdi), %ymm1
  ; CHECK-NEXT: vpmovd2m %ymm1, %k1
  ; CHECK-NEXT: kunpckbw %k0, %k1, %k1
  ; CHECK-NEXT: vmovdq16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT: retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}
define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {
; CHECK-LABEL: test_16f32tosb_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT: vpmovd2m %zmm1, %k1
; CHECK-NEXT: vmovdqu16 %ymm0, %ymm0 [%k1] [z]
; CHECK-NEXT: retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}
define void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {
; CHECK-LABEL: mul256:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm3[8],ymm0[8],ymm3[9],ymm0[9],ymm3[10],ymm0[10],ymm3[11],ymm0[11],ymm3[12],ymm0[12],ymm3[13 ],ymm0[13],ymm3[14],ymm0[14],ymm3[15],ymm0[15],ymm3[24],ymm0[24],ymm3[25],ymm0[25],ymm3[26],ymm0[26],ymm3[27],ymm0[27],ymm3[28],ymm0[28],ymm3[29],ymm0[29],ymm3[30],ymm0[30],ymm3[31],ymm0[ 31]
; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm5 =
ymm1[8],ymm0[8],ymm1[9],ymm0[9],ymm1[10],ymm0[10],ymm1[11],ymm0[11],ymm1[12],ymm0[12],ymm1[13 ],ymm0[13],ymm1[14],ymm0[14],ymm1[15],ymm0[15],ymm1[24],ymm0[24],ymm1[25],ymm0[25],ymm1[26],ymm0[26],ymm1[27],ymm0[27],ymm1[28],ymm0[28],ymm1[29],ymm0[29],ymm1[30],ymm0[30],ymm1[31],ymm0[ 31]
; CHECK-NEXT: vpmullw %ymm4, %ymm5, %ymm4
; CHECK-NEXT: vmovdqa {{.*#+}} ymm5 =
; CHECK-NEXT: vpand %ymm5, %ymm4, %ymm4
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm3 =
ymm3[0],ymm0[0],ymm3[1],ymm0[1],ymm3[2],ymm0[2],ymm3[3],ymm0[3],ymm3[4],ymm0[4],ymm3[5],ymm0[ 5],ymm3[6],ymm0[6],ymm3[7],ymm0[7],ymm3[16],ymm0[16],ymm3[17],ymm0[17],ymm3[18],ymm0[18],ymm3[ 19],ymm0[19],ymm3[20],ymm0[20],ymm3[21],ymm0[21],ymm3[22],ymm0[22],ymm3[23],ymm0[23]
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm1 =
ymm1[0],ymm0[0],ymm1[1],ymm0[1],ymm1[2],ymm0[2],ymm1[3],ymm0[3],ymm1[4],ymm0[4],ymm1[5],ymm0[
Define void @mul512(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="512" {
  CHECK-LABEL: mul512:
  CHECK: # %bb.0:
  CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
  CHECK-NEXT: vmovdqa64 (%rsi), %zmm1
  CHECK-NEXT: vpunpckhbw {{.*#+}} zmm2 =
    zmm1[8],zmm0[8],zmm1[9],zmm0[9],zmm1[10],zmm0[10],zmm1[11],zmm0[11],zmm1[12],zmm0[12],zmm1[13],
    zmm0[13],zmm1[14],zmm0[14],zmm1[15],zmm0[15],zmm1[24],zmm0[24],zmm1[25],zmm0[25],zmm1[26],zmm0[
    26],zmm1[27],zmm0[27],zmm1[28],zmm0[28],zmm1[29],zmm0[29],zmm1[30],zmm0[30],zmm1[31],zmm0[31],
    zmm1[40],zmm0[40],zmm1[41],zmm0[41],zmm1[42],zmm0[42],zmm1[43],zmm0[43],zmm1[44],zmm0[44],zmm1[
    45],zmm0[45],zmm1[46],zmm0[46],zmm1[47],zmm0[47],zmm1[56],zmm0[56],zmm1[57],zmm0[57],zmm1[58],
    zmm0[58],zmm1[59],zmm0[59],zmm1[60],zmm0[60],zmm1[61],zmm0[61],zmm1[62],zmm0[62],zmm1[63],zmm0[
    63]
  CHECK-NEXT: vpunpckhbw {{.*#+}} zmm3 =

; This threw an assertion at one point.
define <4 x i32> @mload_v4i32(<4 x i32> %trigger, <4 x i32>* %addr, <4 x i32> %dst) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: mload_v4i32:
  ; CHECK:    # %bb.0:
  ; CHECK-NEXT:  vptestnmd %xmm0, %xmm0, %k1
  ; CHECK-NEXT:  vpblendmd (%rdi), %xmm1, %xmm0 {%k1}
  ; CHECK-NEXT:  retq
  ; CHECK:      %mask = icmp eq <4 x i32> %trigger, zeroinitializer
  ; CHECK-NEXT:  %res = call <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>*, i32 4, <4 x i1>, <4 x i32>)
  ; CHECK-NEXT:  ret <4 x i32> %res
}
declare <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>*, i32, <4 x i1>, <4 x i32>)

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; RUN: opt %s -inline -S | FileCheck %s

define internal void @innerSmall() "min-legal-vector-width"="128" {
  ret void
}

define internal void @innerLarge() "min-legal-vector-width"="512" {
  ret void
}

define internal void @innerNoAttribute() {
  ret void
}
We should not add an attribute during inlining. No attribute means unknown.
Inlining doesn't change the fact that we don't know anything about this function.

```c
define void @outerNoAttribute() {
  call void @innerLarge()
  ret void
}

define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
  call void @innerLarge()
  ret void
}

define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
  call void @innerSmall()
  ret void
}

; We should remove the attribute after inlining since the callee's vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
  call void @innerNoAttribute()
  ret void
}
```

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }

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; NOTE: Assertions have been autogenerated by utils/update_analyze_test_checks.py
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx2 | FileCheck %s --check-prefixes=CHECK,VEC256,AVX
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC256,SKX256
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,-prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC512

define void @zext256() "min-legal-vector-width"="256" {
  ; VEC256-LABEL: 'zext256'
  ; VEC256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = zext <8 x i16> undef to <8 x i64>
  ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
  ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
  ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x i32>
  ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
  ; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
  ;
  ; VEC512-LABEL: 'zext256'
  ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
  ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
  ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
  ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
  ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
  ; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

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%A = zext <8 x i16> undef to <8 x i64>
%B = zext <8 x i32> undef to <8 x i64>
%C = zext <16 x i8> undef to <16 x i32>
%D = zext <16 x i16> undef to <16 x i32>
%E = zext <32 x i8> undef to <32 x i16>
ret void
}

define void @zext512() "min-legal-vector-width"="512" {
 ; AVX-LABEL: 'zext512'
 ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = zext <8 x i16> undef to <8 x i64>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x i32>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
 ;
 ; SKX256-LABEL: 'zext512'
 ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
 ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
 ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
 ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
 ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
 ; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
 ;
 ; VEC512-LABEL: 'zext512'
 ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
 ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
 ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
 ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
 ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
 ; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
 ;
 ; %A = zext <8 x i16> undef to <8 x i64>
 %B = zext <8 x i32> undef to <8 x i64>
 %C = zext <16 x i8> undef to <16 x i32>
 %D = zext <16 x i16> undef to <16 x i32>
%E = zext <32 x i8> undef to <32 x i16>
ret void
}

define void @sext256() "min-legal-vector-width"="256" {
    ; VEC256-LABEL: 'sext256'
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = sext <8 x i8> undef to <8 x i64>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %B = sext <8 x i16> undef to <8 x i64>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x i32>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    ;
    ; VEC512-LABEL: 'sext256'
    ; VEC512-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %A = sext <8 x i8> undef to <8 x i64>
    ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
    ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
    ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
    ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
    ; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
    ; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    ;
    %A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

define void @sext512() "min-legal-vector-width"="512" {
    ; AVX-LABEL: 'sext512'
    ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = sext <8 x i8> undef to <8 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %B = sext <8 x i16> undef to <8 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x i32>
AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

SKX256-LABEL: 'sext512'
SKX256-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %A = sext <8 x i8> undef to <8 x i64>
SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

VEC512-LABEL: 'sext512'
VEC512-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %A = sext <8 x i8> undef to <8 x i64>
VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void

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*
* @(#)COPYRIGHT8.1 (Berkeley) 3/16/94
declare fp128 @llvm.fabs.f128(fp128)
declare fp128 @llvm.copysign.f128(fp128, fp128)

define fp128 @TestSelect(fp128 %a, fp128 %b) {
    %cmp = fcmp ogt fp128 %a, %b
    %sub = fsub fp128 %a, %b
    %res = select i1 %cmp, fp128 %sub, fp128 0xL00000000000000000000000000000000
    ret fp128 %res
}

define fp128 @TestFabs(fp128 %a) {
    %res = call fp128 @llvm.fabs.f128(fp128 %a)
    ret fp128 %res
}

define fp128 @TestCopysign(fp128 %a, fp128 %b) {
    %res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
    ret fp128 %res
}

define fp128 @TestFneg(fp128 %a) {
    %mul = fmul fp128 %a, %a
    %res = fsub fp128 0xL00000000000000000000000000000000, %mul
    ret fp128 %res
}
ret fp128 %res
; CHECK-LABEL: TestFneg:
; CHECK movaps %xmm0, %xmm1
; CHECK-NEXT callq __multf3
; CHECK-NEXT xorps .LCPI3_0(%rip), %xmm0
; CHECK-NEXT popq %rax
; CHECK-NEXT retq
}

LLVM System Interface Library

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; RUN: opt -S -argpromotion < %s | FileCheck %s
; RUN: opt -S -passes=argpromotion < %s | FileCheck %s
; Test that we only promote arguments when the caller/callee have compatible function attributes.

target triple = "x86_64-unknown-linux-gnu"

; This should promote
; CHECK-LABEL: @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>*%arg.l.val)
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>*readonly %arg1) #0 {
bb:
%tmp = load <8 x i64>, <8 x i64>*%arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>*%tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>*%arg, align 2
ret void
}

; This should promote
; CHECK-LABEL: @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>*%arg.l.val)
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; This should promote
; CHECK-LABEL: @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1.val)
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; This should promote
; CHECK-LABEL: @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* %arg1.val)
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; This should not promote
; CHECK-LABEL: @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1)
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; This should not promote
; CHECK-LABEL: @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1)
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 { bb: %tmp = load <8 x i64>, <8 x i64>* %arg1 store <8 x i64> %tmp, <8 x i64>* %arg ret void }

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 { bb: %tmp = alloca <8 x i64>, align 32 %tmp2 = alloca <8 x i64>, align 32 %tmp3 = bitcast <8 x i64>* %tmp to i8* call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false) call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp) %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2 ret void }

; This should promote
; CHECK-LABEL: @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1.val)
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #3 { bb: %tmp = load <8 x i64>, <8 x i64>* %arg1 store <8 x i64> %tmp, <8 x i64>* %arg ret void }

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 { bb: %tmp = alloca <8 x i64>, align 32 %tmp2 = alloca <8 x i64>, align 32 %tmp3 = bitcast <8 x i64>* %tmp to i8* call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false) call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp) %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2 ret void }

; This should promote
; CHECK-LABEL: @callee_avx2_legal512_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1.val)
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #4 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinelimit norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinelimit norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinelimit norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #3 = { inlinelimit norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #4 = { inlinelimit norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }

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pnm2png / png2pnm --- conversion from PBM/PGM/PPM-file to PNG-file

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1.466 async-limiter 1.0.1

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1.468 levn 0.3.0

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1.469 delayed-stream 1.0.0

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1.471 angular-animate 1.4.14

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1.473 es6-promisify 5.0.0

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1.477 ots 8.0.0

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1.478 depd 1.1.2

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1.487 nan 2.14.1

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1.488 readline-ui 2.2.3

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