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1.4 CRC-16-CCITT 1.0

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1.5 crc32.c N/A

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*
* First, the polynomial itself and its table of feedback terms. The
* polynomial is
* \( X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X^1 + X^0 \)
*
* Note that we take it "backwards" and put the highest-order term in
* the lowest-order bit. The \( X^{32} \) term is "implied"; the LSB is the
* \( X^{31} \) term, etc. The \( X^0 \) term (usually shown as "+1") results in
* the MSB being 1
*
* Note that the usual hardware shift register implementation, which
* is what we're using (we're merely optimizing it by doing eight-bit
* chunks at a time) shifts bits into the lowest-order term. In our
* implementation, that means shifting towards the right. Why do we
* do it this way? Because the calculated CRC must be transmitted in
* order from highest-order term to lowest-order term. UARTs transmit
* characters in order from LSB to MSB. By storing the CRC this way
* we hand it to the UART in the order low-byte to high-byte; the UART
* sends each low-bit to high-bit; and the result is transmission bit
* by bit from highest- to lowest-order term without requiring any bit
* shuffling on our part. Reception works similarly
*
* The feedback terms table consists of 256, 32-bit entries. Notes
*
* The table can be generated at runtime if desired; code to do so
* is shown later. It might not be obvious, but the feedback
* terms simply represent the results of eight shift/xor opera
* tions for all combinations of data and CRC register values
* The values must be right-shifted by eight bits by the "updcrc
* logic; the shift must be unsigned (bring in zeroes). On some
* hardware you could probably optimize the shift in assembler by
* using byte-swap instructions
* polynomial $ed88320
*/

1.6 DCE/RPC 1.1 :r0.7
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1.8 X 11 :6
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X Window System, Version 11, Release 6

Release Notes

Stephen Gildea

X Consortium

May 16, 1994

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fonts
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