Open Source Used In Branch Migration Tool Spirit

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* /opt/cola/permits/1130030048_1612432950.65/0/wildfly-elytron-security-manager-action-1-13-1-final-sources-jar/org/wildfly/security/manager/action/WritePropertyIfAbsentAction.java
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1.4 opensaml-xacml-saml-api 3.3.1

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* /opt/ws_local/PERMITS_SQL/1045086033_1591129409.65/0/opensaml-xacml-saml-api-3-3-1-sources-jar/org/opensaml/xacml/profile/saml/XACMLPolicyStatementType.java
* /opt/ws_local/PERMITS_SQL/1045086033_1591129409.65/0/opensaml-xacml-saml-api-3-3-1-sources-jar/org/opensaml/xacml/profile/saml/XACMLAuthzDecisionQueryType.java
* /opt/ws_local/PERMITS_SQL/1045086033_1591129409.65/0/opensaml-xacml-saml-api-3-3-1-sources-jar/org/opensaml/xacml/profile/saml/XACMLPolicyQueryType.java
* /opt/ws_local/PERMITS_SQL/1045086033_1591129409.65/0/opensaml-xacml-saml-api-3-3-1-sources-jar/org/opensaml/xacml/profile/saml/SAMLProfileConstants.java
* /opt/ws_local/PERMITS_SQL/1045086033_1591129409.65/0/opensaml-xacml-saml-api-3-3-1-sources-jar/org/opensaml/xacml/profile/saml/XACMLAuthzDecisionQueryType.java
* /opt/ws_local/PERMITS_SQL/1045086033_1591129409.65/0/opensaml-xacml-saml-api-3-3-1-sources-jar/org/opensaml/xacml/profile/saml/package-info.java
* /opt/ws_local/PERMITS_SQL/1045086033_1591129409.65/0/opensaml-xacml-saml-api-3-3-1-sources-jar/org/opensaml/xacml/profile/saml/ReferencedPoliciesType.java

1.5 cxf-rt-transports-local 3.3.7

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1.6 netty-handler 4.1.50.Final

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  jar/io/netty/handler/ssl/PemValue.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
  jar/io/netty/handler/ssl/DelegatingSslContext.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
  jar/io/netty/handler/ssl/PemX509Certificate.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
  jar/io/netty/handler/flow/package-info.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
  jar/io/netty/handler/ssl/ReferenceCountedOpenSslServerContext.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
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* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/JdkAlpnSslUtils.java
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  * /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1.jar/io/netty/handler/ssl/util/ThreadLocalInsecureRandom.java
  * /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1.jar/io/netty/handler/ssl/JdkSslContext.java
  * /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/JdkSslEngine.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/util/BouncyCastleSelfSignedCertGenerator.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ipfilter/RuleBasedIpFilter.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/SslContext.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/JdkSslServerContext.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
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jar/io/netty/handler/ssl/OpenSslContext.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/util/InsecureTrustManagerFactory.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/CipherSuiteFilter.java
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* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/ApplicationProtocolNegotiator.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/OpenSslDefaultApplicationProtocolNegotiator.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/SupportedCipherSuiteFilter.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
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jar/io/netty/handler/ipfilter/UniqueIpFilter.java
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jar/io/netty/handler/ssl/Java7SslParametersUtils.java
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jar/io/netty/handler/ssl/OpenSslPrivateKeyMethod.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/util/SimpleKeyManagerFactory.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/KeyManagerFactoryWrapper.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/TrustManagerFactoryWrapper.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/SslMasterKeyHandler.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/address/DynamicAddressConnectHandler.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
jar/io/netty/handler/ssl/PseudoRandomFunction.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
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* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/OpenSslSession.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/OpenSslCachingX509KeyManagerFactory.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/OpenSslCachingKeyMaterialProvider.java
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* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/OpenSslTlsv13X509ExtendedTrustManager.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/DefaultOpenSslKeyMaterial.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/OpenSslKeyMaterialProvider.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/OpenSslKeyMaterial.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/OpenSslPrivateKey.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/OpenSslPrivateTrustManager.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/OpenSslPrivateSession.java
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* /opt/ws-local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/address/ResolveAddressHandler.java
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  jar/io/netty/handler/timeout/ReadTimeoutHandler.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
  jar/io/netty/handler/logging/LoggingExceptionHandler.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
  jar/io/netty/handler/timeout/IdleState.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
  jar/io/netty/handler/timeout/ReadTimeOutException.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
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* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
  jar/io/netty/handler/stream/ChunkedFile.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
  jar/io/netty/handler/stream/ChunkedNioStream.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-
  jar/io/netty/handler/stream/ChunkedStream.java
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  jar/io/netty/handler/ssl/package-info.java
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  jar/io/netty/handler/timeout/IdleStateHandler.java
jar/io/netty/handler/timeout/WriteTimeoutHandler.java
* /opt/wsLocal/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1.jar/io/netty/handler/ssl/SslHandler.java
* /opt/wsLocal/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1.jar/io/netty/handler/stream/ChunkedInput.java
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* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/ClientAuth.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/ApplicationProtocolAccessor.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/OpenSslSessionTicketKey.java
* /opt/ws_local/PERMITS_SQL/1068233959_1594326118.13/0/netty-handler-4-1-50-final-sources-1-jar/io/netty/handler/ssl/SslContextBuilder.java

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1.8 python-requests 2.25.1
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lib/gsssd_pname_to_uid.c
uts/common/gssapi/include/gssapi_err_generic.h
uts/common/gssapi/include/mechglueP.h

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lib/kdb/iprop.x
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lib/kdb/kdb_log.c
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  jar/org/wildfly/security/auth/client/CallbackKind.java
* /opt/cola/permits/1130030481_1612433609.54/0/wildfly-elytron-client-1-13-1-final-sources-
  jar/org/wildfly/security/auth/client/ModuleLoader.java
* /opt/cola/permits/1130030481_1612433609.54/0/wildfly-elytron-client-1-13-1-final-sources-
  jar/org/wildfly/security/auth/client/package-info.java
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* /opt/cola/permits/1130030481_1612433609.54/0/wildfly-elytron-client-1-13-1-final-sources-jar/wildfly/security/auth/client/MatchAbstractTypeRule.java
* /opt/ cola/permits/1130030481_1612433609.54/0/wildfly-elytron-client-1-13-1-final-sources-
jar/org/wildfly/security/credential/source/OAuth2CredentialSource.java
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1.26 jackson-datatype-jdk8 2.10.5
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1.27 resteasy-jax-rs 3.13.2.Final

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/**
 * Any exception thrown by a MessageBodyWriter chain that is not an instance of a WriterException is caught internally
 * by the Resteasy runtime and wrapped with an instance of WriterException.
 *
 * If you want to have special exception handling for exceptions thrown by MessageBodyWriters and their interceptors, then write an exception
 * mapper for WriterException.
 *
 * Also, you may extend this class and throw instances of it from your MessageBodyWriters (and interceptors)
 *
 * @author <a href="mailto:bill@burkecentral.com">Bill Burke</a>
 * @version $Revision: 1 $
 */

Found in path(s):
* /opt/cola/permits/1130031281_1612432960.0/0/resteasy-jaxrs-3-13-2-final-sources-jar/org/jboss/resteasy/spi/WriterException.java
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/**
 * Any exception thrown by a MessageBodyReader chain that is not an instance of a ReaderException is caught internally
 * by the Resteasy runtime and wrapped with an instance of ReaderException.
 */
* If you want to have special exception handling for exceptions thrown by MessageBodyReaders, then write an exception mapper for ReaderException.
* Also, you may extend this class and throw instances of it from your MessageBodyReaders (and interceptors)
* @author <a href="mailto:bill@burkecentral.com">Bill Burke</a>
* @version $Revision: 1 $
*/

Found in path(s):
* /opt/cola/permits/1130031281_1612432960.0/0/resteasy-jaxrs-3-13-2-final-sources-jar/org/jboss/resteasy/spi/ReaderException.java
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/ *
* <p>Encodes and decodes to and from Base64 notation.</p>
* <p>Homepage: <a href="http://iharder.net/base64">http://iharder.net/base64</a>.</p>
* <p>Example:</p>
* <p>
* <code>String encoded = Base64.encode( myByteArray );</code></p>
* <br>
* <code>byte[] myByteArray = Base64.decode( encoded );</code></p>
* <p></p>
* <p>The <code>options</code> parameter, which appears in a few places, is used to pass several pieces of information to the encoder. In the "higher level" methods such as encodeBytes( bytes, options ) the options parameter can be used to indicate such things as first gzipping the bytes before encoding them, not inserting linefeeds, and encoding using the URL-safe and Ordered dialects.</p>
* <p>Note, according to <a href="http://www.faqs.org/rfcs/rfc3548.html">RFC3548</a>, Section 2.1, implementations should not add line feeds unless explicitly told to do so. I've got Base64 set to this behavior now, although earlier versions broke lines by default.</p>
* <p>The constants defined in Base64 can be OR-ed together to combine options, so you might make a call like this:</p>
* <p>
* <code>String encoded = Base64.encodeBytes( mybytes, Base64.GZIP | Base64.DO_BREAK_LINES );</code></p>
* <p></p>
* <p>Also...</p>
* <p>
* <code>String encoded = Base64.encodeBytes( crazyString.getBytes() );</code></p>
* <p></p>
* Change Log:
* </p>
* <ul>
* <li>v2.3.7 - Fixed subtle bug when base 64 input stream contained the value 01111111, which is an invalid base 64 character but should not throw an ArrayIndexOutOfBoundsException either. Led to discovery of mishandling (or potential for better handling) of other bad input characters. You should now get an IOException if you try decoding...
* something that has bad characters in it.</li>
* v2.3.6 - Fixed bug when breaking lines and the final byte of the encoded
* string ended in the last column; the buffer was not properly shrunk and
* contained an extra (null) byte that made it into the string.</li>
* v2.3.5 - Fixed bug in {@link #encodeFromFile} where estimated buffer size
* was wrong for files of size 31, 34, and 37 bytes.</li>
* v2.3.4 - Fixed bug when working with gzipped streams whereby flushing
* the Base64.OutputStream closed the Base64 encoding (by padding with equals
* signs) too soon. Also added an option to suppress the automatic decoding
* of gzipped streams. Also added experimental support for specifying a
* class loader when using the
* {@link #decodeToObject(java.lang.String, int, java.lang.ClassLoader)}
* method.</li>
* v2.3.3 - Changed default char encoding to US-ASCII which reduces the internal Java
* footprint with its CharEncoders and so forth. Fixed some javadocs that were
* inconsistent. Removed imports and specified things like java.io.IOException
* explicitly inline.</li>
* v2.3.2 - Reduced memory footprint! Finally refined the "guessing" of how big the
* final encoded data will be so that the code doesn't have to create two output
* arrays: an oversized initial one and then a final, exact-sized one. Big win
* when using the method of methods (and not
* using the gzip options which uses a different mechanism with streams and stuff).</li>
* v2.3.1 - Added and some
* similar helper methods to be more efficient with memory by not returning a
* String but just a byte array.</li>
* v2.3 - <strong>This is not a drop-in replacement!</strong> This is two years of comments
* and bug fixes queued up and finally executed. Thanks to everyone who sent
* me stuff, and I'm sorry I wasn't able to distribute your fixes to everyone else.
* Much bad coding was cleaned up including throwing exceptions where necessary
* instead of returning null values or something similar. Here are some changes
* that may affect you:
* Does not break lines, by default. This is to keep in compliance with
* RFC3548.</li>
* v2.3 - v2.3.1 - Threw exceptions instead of returning null values. Because some operations
* (especially those that may permit the GZIP option) use IO streams, there
* is a possibility of an java.io.IOException being thrown. After some discussion and
* thought, I've changed the behavior of the methods to throw java.io.IOException
* rather than return null if ever there's an error. I think this is more
* appropriate, though it will require some changes to your code. Sorry,
* it should have been done this way to begin with.</li>
* v2.3 - v2.3.1 - Removed all references to System.out, System.err, and the like.</li>
* Shame on me. All I can say is sorry they were ever there.</li>
* v2.3 - v2.3.1 - Throws NullPointerExceptions and IllegalArgumentExceptions as needed
* such as when passed arrays are null or offsets are invalid.</li>
* v2.3 - v2.3.1 - Cleaned up as much javadoc as I could to avoid any javadoc warnings.
* This was especially annoying before for people who were thorough in their
* own projects and then had gobs of javadoc warnings on this file.
* v2.2.1 - Fixed bug using URL_SAFE and ORDERED encodings. Fixed bug when using very small files (~<40 bytes).
* v2.2 - Added some helper methods for encoding/decoding directly from one file to the next. Also added a main() method to support command line encoding/decoding from one file to the next. Also added these Base64 dialects:
* v2.1 - Cleaned up javadoc comments and unused variables and methods. Added some convenience methods for reading and writing to and from files.
* v2.0.2 - Now specifies UTF-8 encoding in places where the code fails on systems with other encodings (like EBCDIC).
* v2.0.1 - Fixed an error when decoding a single byte, that is, when the encoded data was a single byte.
* v2.0 - I got rid of methods that used booleans to set options. Now everything is more consolidated and cleaner. The code now detects when data that's being decoded is gzip-compressed and will decompress it automatically. Generally things are cleaner. You'll probably have to change some method calls that you were making to support the new options format (<code>int</code>s that you "OR" together).
* v1.5.1 - Fixed bug when decompressing and decoding to a byte[] using <code>decode(String s, boolean gzipCompressed)</code>.
* v1.5 - Output stream passes on flush() command but doesn't do anything itself. This helps when using GZIP streams.
* v1.4 - Added helper methods to read/write files.
* v1.3.6 - Fixed bug when decompressing and decoding to a byte[] so that 'position' is reset.
* v1.3.5 - Added flag to turn on and off line breaks. Fixed bug in input stream where last buffer being read, if not completely full, was not returned.
* v1.3.4 - Fixed when "improperly padded stream" error was thrown at the wrong time.
* v1.3.3 - Fixed I/O streams which were totally messed up.
* v1.3.2 - Added some helper methods for encoding/decoding directly from one file to the next. Also added a main() method to support command line encoding/decoding from one file to the next. Also added these Base64 dialects:
* v1.2.1 - Fixed bug using URL_SAFE and ORDERED encodings. Fixed bug when using very small files (~<40 bytes).
* v1.2 - Added some helper methods for encoding/decoding directly from one file to the next. Also added a main() method to support command line encoding/decoding from one file to the next. Also added these Base64 dialects:
* v1.1 - Cleared out javadoc comments and unused variables and methods. Added some convenience methods for reading and writing to and from files.
* v1.0 - Initial release.

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* periodically to check for updates or to contribute improvements.
* </p>
*
* @author Robert Harder
* @author rob@iharder.net
* @version 2.3.7
*/

Found in path(s):
* /opt/cola/permits/1130031281_1612432960.0/0/resteasy-jaxrs-3-13-2-final-sources-jar/org/jboss/resteasy/util/Base64.java

1.28 pax-utils 1.2.8-r0
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1.31 common-spi 5.0.3.Final-redhat-00006

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1.33 wildfly-weld-jpa 21.0.2.Final

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If such an object file uses only numerical parameters, data structure layouts and accessors, and small macros and small inline functions (ten lines or less in length), then the use of the object file is unrestricted, regardless of whether it is legally a derivative work. (Executables containing this object code plus portions of the Library will still fall under Section 6.)

Otherwise, if the work is a derivative of the Library, you may distribute the object code for the work under the terms of Section 6. Any executables containing that work also fall under Section 6, whether or not they are linked directly with the Library itself.

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### 1.34 jline 2.14.6

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1.35 libunistring 0.9.9-3.el8

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#
# BSDLIB_VERSION = 1.0
# BSDLIB_IMAGE = libce
# BSDLIB_MYDIR = et
# BSDLIB_INSTALL_DIR = $(SHLIBDIR)
#
all:: image

real-subdirs:: Makefile
@echo "MKDIR pic"
@mkdir -p pic

BSD_LIB = $(BSDLIB_IMAGE).so.$(BSDLIB_VERSION)
BSDLIB_PIC_FLAG = -fpic

image:$ (BSDLIB_LIB)

$(BSDLIB_LIB): $(OBJS)
(cd pic; ld -Bshareable -o $(BSD_LIB) $(LDFLAGS_SHLIB) $(OBJS))
$(MV) pic/$(BSD_LIB) .
$(RM) -f ../$(BSD_LIB)
(cd ..; $(LN) $(LINK_BUILD_FLAGS) `echo $(my_dir) | sed -e 's;lib/;;'`/$(BSD_LIB) $(BSD_LIB))

install-shlibs install:: $(BSDLIB_LIB)
@echo "INSTALL_PROGRAM $(BSDLIB_INSTALL_DIR)/$(BSD_LIB)"
@$ (INSTALL_PROGRAM) $(BSD_LIB)
$(DESTDIR)$(BSDLIB_INSTALL_DIR)/$(BSD_LIB)
@-$(LDCONFIG)

install-strip: install

install-shlibs-strip:: install-shlibs

uninstall-shlibs uninstall::
$(RM) -f $(DESTDIR)$(BSDLIB_INSTALL_DIR)/$(BSD_LIB)

clean::
$(RM) -rf pic
$(RM) -f $(BSDLIB_LIB)
$(RM) -f ../$(BSD_LIB)

This package was added to the e2fsprogs debian source package by
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It is part of the main e2fsprogs distribution, which can be found at:

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Upstream Author: Theodore Ts'o <tytso@mit.edu>

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Index: tdbsa/tdb.c
===================================================================
--- tdbsa.orig/tdb.c
+++ tdbsa/tdb.c
@@ -4,11 +4,11 @@ Rev: 23371
 Last Changed Date: 2007-06-06 20:14:06 -0400 (Wed, 06 Jun 2007)
 */
 /*
 - Unix SMB/CIFS implementation.
 + trivial database library - standalone version

 - trivial database library - private includes
 -
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Theodore Ts'o
23-June-2007

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That's all there is to it!
This package was added to the e2fsprogs debian source package by Theodore Ts'o <tytso@mit.edu> on Sat Mar 15 15:33:37 EST 2003

It is part of the main e2fsprogs distribution, which can be found at:

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Upstream Author: Theodore Ts'o <tytso@mit.edu>

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Gadi Oxman, August 1995

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<xsl:stylesheet version="1.0"
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<thead>
<tr>
<th>Package</th>
<th>Package Artifact</th>
<th>Package Version</th>
<th>Remote Licenses</th>
<th>Local Licenses</th>
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    <xsl:text>cddl-gplv2-classpath.txt</xsl:text>
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  <xsl:text>antlr-bsd.txt</xsl:text>
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(For example, a function in a library to compute square roots has a purpose that is entirely well-defined independent of the application. Therefore, Subsection 2d requires that any application-supplied function or table used by this function must be optional: if the application does not supply it, the square root function must still compute square roots.)

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If distribution of object code is made by offering access to copy from a designated place, then offering equivalent access to copy the source code from the same place satisfies the requirement to distribute the source code, even though third parties are not compelled to copy the source along with the object code.

5. A program that contains no derivative of any portion of the Library, but is designed to work with the Library by being compiled or linked with it, is called a "work that uses the Library". Such a work, in isolation, is not a derivative work of the Library, and therefore falls outside the scope of this License.

However, linking a "work that uses the Library" with the Library creates an executable that is a derivative of the Library (because it contains portions of the Library), rather than a "work that uses the library". The executable is therefore covered by this License. Section 6 states terms for distribution of such executables.

When a "work that uses the Library" uses material from a header file
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Whether this is true is especially significant if the work can be
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threshold for this to be true is not precisely defined by law.

If such an object file uses only numerical parameters, data
structure layouts and accessors, and small macros and small inline
functions (ten lines or less in length), then the use of the object
file is unrestricted, regardless of whether it is legally a derivative
work. (Executables containing this object code plus portions of the
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Otherwise, if the work is a derivative of the Library, you may
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1.47 jaxb-xjc 2.3.3-b02

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1.48 pyyaml 5.4.1-1.ph4

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1.51 h2 1.4.197

1.52 libverto 0.3.0-5.el8

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* /opt/ws_local/PERMITS_SQL/1074947796_1596001801.74/0/wildfly-client-config-1-0-1-final-sources-1.jar/org/wildfly/client/config/AbstractDelegatingXMLStreamReader.java
* /opt/ws_local/PERMITS_SQL/1074947796_1596001801.74/0/wildfly-client-config-1-0-1-final-sources-1.jar/org/wildfly/client/config/ClientConfiguration.java
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* /opt/cola/permits/1130030289_1612432996.46/0/wildfly-elytron-credential-1-13-1-final-sources-jar/org/wildfly/security/key/RawSecretKeyFactory.java
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* /opt/cola/permits/1130030289_1612432996.46/0/wildfly-elytron-credential-1-13-1-final-sources-
  jar/org/wildfly/security/password/interfaces/RawSunUnixMD5CryptPassword.java
* /opt/cola/permits/1130030289_1612432996.46/0/wildfly-elytron-credential-1-13-1-final-sources-
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* /opt/cola/permits/1130030289_1612432996.46/0/wildfly-elytron-credential-1-13-1-final-sources-
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* /opt/cola/permits/1130030289_1612432996.46/0/wildfly-elytron-credential-1-13-1-final-sources-jar/org/wildfly/security/password/interfaces/OneTimePassword.java
* /opt/cola/permits/1130030289_1612432996.46/0/wildfly-elytron-credential-1-13-1-final-sources-jar/org/wildfly/security/credential/SecretKeyCredential.java
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1.67 resteasy-jsapi 3.13.2.Final

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cmd/krb5/slave/kpropd_rpc.c
lib/gss_mechs/mach_krb5/et/kdb5_err.c
lib/gss_mechs/mech_spnego/mech/gssapiP_spnego.h
lib/gss_mechs/mech_spnego/mech/spnego_mech.c
lib/krb5/kadm5/kadm_host_srv_names.c
lib/krb5/kdb/kdb_convert.c
lib/krb5/kdb/kdb_hdr.h
lib/krb5/kdb/kdb_log.c
lib/krb5/kdb/kdb_log.h
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The implementations of GSSAPI mechglue in GSSAPI-SPNEGO in "src/lib/gssapi", including the following files:

- lib/gssapi/generic/gssapi_err_generic.et
- lib/gssapi/mechglue/g_accept_sec_context.c
- lib/gssapi/mechglue/g_acquire_cred.c
- lib/gssapi/mechglue/g_canon_name.c
- lib/gssapi/mechglue/g_compare_name.c
- lib/gssapi/mechglue/g_context_time.c
- lib/gssapi/mechglue/g_delete_sec_context.c
- lib/gssapi/mechglue/g_dsp_name.c
- lib/gssapi/mechglue/g_dsp_status.c
- lib/gssapi/mechglue/g_dup_name.c
- lib/gssapi/mechglue/g_exp_sec_context.c
- lib/gssapi/mechglue/g_export_name.c
- lib/gssapi/mechglue/g_glue.c
- lib/gssapi/mechglue/g_imp_name.c
- lib/gssapi/mechglue/g_imp_sec_context.c
- lib/gssapi/mechglue/g_init_sec_context.c

---
and the initial implementation of incremental propagation, including
the following new or changed files:

include/iprop_hdr.h
kadmin/server/ipropd_svc.c
lib/kdb/iprop.x
lib/kdb/kdb_convert.c
lib/kdb/kdb_log.c
lib/kdb/kdb_log.h
lib/krb5/error_tables/kdb5_err.et
kprop/kpropd_rpc.c
kprop/kproplog.c

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Python was created in the early 1990s by Guido van Rossum at Stichting
Mathematisch Centrum (CWI, see http://www.cwi.nl) in the Netherlands
as a successor of a language called ABC. Guido remains Python's
principal author, although it includes many contributions from others.

In 1995, Guido continued his work on Python at the Corporation for
National Research Initiatives (CNRI, see http://www.cnri.reston.va.us)
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In May 2000, Guido and the Python core development team moved to
BeOpen.com to form the BeOpen PythonLabs team. In October of the same
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1.73 jetty-servlet 9.4.24.v20191120

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The following artifacts are EPL and ASL2.
* org.eclipse.jetty.orbit:javax.security.auth.message

The following artifacts are EPL and CDDL 1.0.
* org.eclipse.jetty.orbit:javax.mail.glassfish

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Oracle

The following artifacts are CDDL + GPLv2 with classpath exception.
https://glassfish.dev.java.net/nonav/public/CDDL/GPL.html

* javax.servlet:javax.servlet-api
* javax.annotation:javax.annotation-api
* javax.transaction:javax.transaction-api
* javax.websocket:javax.websocket-api

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Oracle OpenJDK

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* java.sun.security.ssl

These artifacts replace/modify OpenJDK classes. The modifications are hosted at github and both modified and original are under GPL v2 with classpath exceptions.
http://openjdk.java.net/legal/gplv2+ce.html

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```java
org.ow2.asm:asm-commons
org.ow2.asm:asm
```

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Apache

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```java
org.apache.taglibs:taglibs-standard-spec
org.apache.taglibs:taglibs-standard-impl
```

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MortBay

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```java
org.mortbay.jasper:apache-jsp
org.apache.tomcat:tomcat-jasper
org.apache.tomcat:tomcat-juli
org.apache.tomcat:tomcat-jsp-api
org.apache.tomcat:tomcat-el-api
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-api
org.apache.tomcat:tomcat-util-scan
org.apache.tomcat:tomcat-util
org.mortbay.jasper:apache-el
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-el-api
```

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Mortbay

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https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

```java
org.eclipse.jetty.toolchain:jetty-schemas
```

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1.74 jackson-module-paranamer 2.10.5

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# Jackson JSON processor

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1.81 cxf-xjc-runtime 3.3.0

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1.82 python-dateutil 2.6.0

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1.83 file 5.35-4+deb10u1

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1.84 pyjwt 1.7.1

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1.85 apt 1.8.2.2

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1.87 artemis-jms-client 2.10.1

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bzip2/libbzip2 version 1.0.8 of 13 July 2019

--------------------------------------------------------------------------

1.92 xz 5.2.5-r0

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Schema for XML Signatures
http://www.w3.org/2000/09/xmldsig#
$Revision: 1.2 $ on $Date: 2005/06/03 03:09:54 $ by $Author: cantor$

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1.103 wildfly-core-management-subsystem

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1.104 flask-migrate 2.1.1

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```python
import io, sys
from setuptools import setup

def main():
    python_version = sys.version_info[:2]
    if python_version < (2,7):
        raise SystemExit("Sorry, Python 2.7 or newer required")

    package_data = {}
    exec(open('idna/package_data.py').read(), package_data)

    arguments = {
        'name': 'idna',
        'packages': ['idna'],
        'version': package_data['__version__'],
        'description': 'Internationalized Domain Names in Applications (IDNA)',
        'long_description': io.open("README.rst", encoding="UTF-8").read(),
        'author': 'Kim Davies',
        'author_email': 'kim@cynosure.com.au',
        'license': 'BSD-like',
        'url': 'https://github.com/kjd/idna',
        'classifiers': [
            'Development Status :: 5 - Production/Stable',
            'Intended Audience :: Developers',
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            'Operating System :: OS Independent',
            'Programming Language :: Python',
            'Programming Language :: Python :: 2',
            'Programming Language :: Python :: 2.7',
```
{'Programming Language :: Python :: 3',
'Programming Language :: Python :: 3.4',
'Programming Language :: Python :: 3.5',
'Programming Language :: Python :: 3.6',
'Programming Language :: Python :: 3.7',
'Programming Language :: Python :: 3.8',
'Programming Language :: Python :: Implementation :: CPython',
'Programming Language :: Implementation :: CPYthon',
'Topic :: Internet :: Name Service (DNS)',
'Topic :: Software Development :: Libraries :: Python Modules',
'Topic :: Utilities',
]
'python_requires': '>=2.7, !=3.0.*, !=3.1.*, !=3.2.*, !=3.3.*',
}

setup(**arguments)

if __name__ == '__main__':
    main()

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  * /opt/cola/permits/1110905341_1606871385.15/0/kjd-idna-v2-10-0-ge5c11db-1-tar-gz/kjd-idna-b8defb9/setup.py

1.120 wildfly-clustering-ee-hotrod 21.0.2.Final

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The End

1.124 jansi-native 1.7

1.125 resteasy-jackson-provider 3.13.2.Final

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1.127 iputils 20180629-2+deb10u1

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1.130 infinispan-cachestore-remote

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    <xsl:param name="version"/>
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    <xsl:variable name="uppercase" select="'ABCDEFGHIJKLMNOPQRSTUVWXYZ'" />
    <xsl:template match="/"/>
</xsl:stylesheet>
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<th>Local Licenses</th>
</tr>
</thead>
</table>
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  <xsl:when test="contains($remainder, $delimiter)">
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      <xsl:with-param name="txt" select="$txt"/>
      <xsl:with-param name="remainder" select="substring-after($remainder, $delimiter)"/>
      <xsl:with-param name="delimiter" select="$delimiter"/>
    </xsl:call-template>
  </xsl:when>
  <xsl:otherwise>
    <xsl:variable name="lastIndex" select="string-length(substring($txt, 1, string-length($txt)-string-length($remainder)))+1"/>
    <xsl:choose>
      <xsl:when test="string-length($remainder)=0">
        <xsl:value-of select="string-length($txt)"/>
      </xsl:when>
      <xsl:when test="$lastIndex>0">
        <xsl:value-of select="($lastIndex - string-length($delimiter))"/>
      </xsl:when>
      <xsl:otherwise>
        <xsl:value-of select="0"/>
      </xsl:otherwise>
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  </xsl:otherwise>
</xsl:choose>
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  <xsl:param name="filename"/>
  <xsl:choose>
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    </xsl:when>
    <xsl:when test="contains($filename, 'bsd') and contains($filename, '3-clause')">
      <xsl:text>bsd-3-clause.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'apache') and contains($filename, '1.1')">
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    </xsl:when>
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    </xsl:when>
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      <xsl:text>apache license 2.0.txt</xsl:text>
    </xsl:when>
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      <xsl:text>cddl-gplv2-classpath.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'common public license')">
      <xsl:text>common public license 1.0.txt</xsl:text>
    </xsl:when>
  </xsl:choose>
</xsl:template>
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1.135 picketlink-idm-simple-schema

2.5.5.SP12-redhat-00009

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1.137 python-dateutil 2.8.1

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dateutil - Extensions to the standard Python datetime module.

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1.138 click 7.1.2

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# binary only, patch it back to the system, and then use a wrapper

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* /opt/cola/permits/1160566381_1620335255.38/0/pallets-click-7-1-2-0-g1784558-1-tar-gz/pallets-click-1784558/src/click/_compat.py

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import io
import re

from setuptools import find_packages
from setuptools import setup

with io.open("README.rst", "rt", encoding="utf8") as f:
    readme = f.read()

with io.open("src/click/__init__.py", "rt", encoding="utf8") as f:
    version = re.search(r'__version__ = "(.*)"', f.read()).group(1)

setup(
    name="click",
    version=version,
    url="https://palletsprojects.com/p/click/",
    project_urls={
        "Documentation": "https://click.palletsprojects.com/",
        "Code": "https://github.com/pallets/click",
        "Issue tracker": "https://github.com/pallets/click/issues",
    },
    license="BSD-3-Clause",
    maintainer="Pallets",
    maintainer_email="contact@palletsprojects.com",
    description="Composable command line interface toolkit",
    long_description=readme,
    packages=find_packages("src"),
    package_dir={'': "src"},
    include_package_data=True,
    python_requires=">=2.7, !=3.0.*, !=3.1.*, !=3.2.*, !=3.3.*, !=3.4.*",
    classifiers=[
        "Development Status :: 5 - Production/ Stable",
        "Intended Audience :: Developers",
        "License :: OSI Approved :: BSD License",
    ]
)
As the userbase of Click grows, more and more major feature requests pop up in Click's bugtracker. As reasonable as it may be for those features to be bundled with Click instead of being a standalone project, many of those requested features are either highly experimental or have unproven practical use, while potentially being a burden to maintain.

This is why click-contrib_ exists. The GitHub organization is a collection of possibly experimental third-party packages whose featureset does not belong into Click, but also a playground for major features that may be added to Click in the future. It is also meant to coordinate and concentrate effort on writing third-party extensions for Click, and to ease the effort of searching for such extensions. In that sense it could be described as a low-maintenance alternative to extension repositories of other frameworks.

Please note that the quality and stability of those packages may be different than what you expect from Click itself. While published under a common organization, they are still projects separate from Click.

.. _click-contrib: https://github.com/click-contrib/
1784558/src/click/parser.py
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Including attribution to #612

Found in path(s):
* /opt/cola/permits/1160566381_1620335255.38/0/pallets-click-7-1-2-0-g1784558-1-tar-gz/pallets-click-
1784558/tests/test_formatting.py
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1.139 jetty 9.4.24.v20191120
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iD8DBQFHacMO+jg6q+ULyBMRAky4AJ9CdNKsng8n2aFcPQAvcEPXxEjJACgrvJM
C/W/GuQffCJykkL2j9j/Ag=
=ufUh
-----END PGP SIGNATURE-----

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Eclipse

The following artifacts are EPL.
* org.eclipse.jetty.orbit:org.eclipse.jdt.core

The following artifacts are EPL and ASL2.
* org.eclipse.jetty.orbit:javax.security.auth.message

The following artifacts are EPL and CDDL 1.0.
* org.eclipse.jetty.orbit:javax.mail.glassfish

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Oracle

The following artifacts are CDDL + GPLv2 with classpath exception.
https://glassfish.dev.java.net/nonav/public/CDDL/GPL.html

* javax.servlet:javax.servlet-api
* javax.annotation:javax.annotation-api
* javax.transaction:javax.transaction-api
* javax.websocket:javax.websocket-api

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Oracle OpenJDK

If ALPN is used to negotiate HTTP/2 connections, then the following artifacts may be included in the distribution or downloaded when ALPN module is selected.

* java.sun.security.ssl

These artifacts replace/modify OpenJDK classes. The modifications are hosted at github and both modified and original are under GPL v2 with
classpath exceptions.
http://openjdk.java.net/legal/gplv2+ce.html

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OW2

The following artifacts are licensed by the OW2 Foundation according to the terms of http://asm.ow2.org/license.html

org.ow2.asm:asm-commons
org.ow2.asm:asm

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Apache

The following artifacts are ASL2 licensed.

org.apache.taglibs:taglibs-standard-spec
org.apache.taglibs:taglibs-standard-impl

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MortBay

The following artifacts are ASL2 licensed. Based on selected classes from following Apache Tomcat jars, all ASL2 licensed.

org.mortbay.jasper:apache-jsp
org.apache.tomcat:tomcat-jasper
org.apache.tomcat:tomcat-juli
org.apache.tomcat:tomcat-jsp-api
org.apache.tomcat:tomcat-el-api
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-api
org.apache.tomcat:tomcat-util-scan
org.apache.tomcat:tomcat-util

org.mortbay.jasper:apache-el
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-el-api

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https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

org.eclipse.jetty.toolchain:jetty-schemas

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Assorted

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Schedule A

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Full name: Gregory John Wilkins
E-Mail: gregw@eclipse.com
Mailing Address: 62 Church St. Balmain, NSW 2041, Australia

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1.142 pinentry 1.1.1-r0

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### 1.153 util-linux 2.32.1-24.el8

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Python was created in the early 1990s by Guido van Rossum at Stichting Mathematisch Centrum (CWI, see http://www.cwi.nl) in the Netherlands as a successor of a language called ABC. Guido remains Python's principal author, although it includes many contributions from others.

In 1995, Guido continued his work on Python at the Corporation for National Research Initiatives (CNRI, see http://www.cnri.reston.va.us) in Reston, Virginia where he released several versions of the software.

In May 2000, Guido and the Python core development team moved to BeOpen.com to form the BeOpen PythonLabs team. In October of the same year, the PythonLabs team moved to Digital Creations (now Zope Corporation, see http://www.zope.com). In 2001, the Python Software Foundation (PSF, see http://www.python.org/psf/) was formed, a non-profit organization created specifically to own Python-related Intellectual Property. Zope Corporation is a sponsoring member of the PSF.

All Python releases are Open Source (see http://www.opensource.org for the Open Source Definition). Historically, most, but not all, Python releases have also been GPL-compatible; the table below summarizes the various releases.

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A. HISTORY OF THE SOFTWARE
==========================

Python was created in the early 1990s by Guido van Rossum at Stichting
Mathematisch Centrum (CWI, see http://www.cwi.nl) in the Netherlands
as a successor of a language called ABC. Guido remains Python’s
principal author, although it includes many contributions from others.

In 1995, Guido continued his work on Python at the Corporation for
National Research Initiatives (CNRI, see http://www.cnri.reston.va.us)
in Reston, Virginia where he released several versions of the
software.

In May 2000, Guido and the Python core development team moved to
BeOpen.com to form the BeOpen PythonLabs team. In October of the same
year, the PythonLabs team moved to Digital Creations (now Zope
Corporation, see http://www.zope.com). In 2001, the Python Software
Foundation (PSF, see http://www.python.org/psf/) was formed, a
non-profit organization created specifically to own Python-related
Intellectual Property. Zope Corporation is a sponsoring member of
the PSF.

All Python releases are Open Source (see http://www.opensource.org for
the Open Source Definition). Historically, most, but not all, Python
releases have also been GPL-compatible; the table below summarizes
the various releases.

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cabundle.crt -- Bundle of CA Root Certificates

Certificate data from Mozilla as of: Thu Nov  3 19:04:19 2011#
This is a bundle of X.509 certificates of public Certificate Authorities
(CA). These were automatically extracted from Mozilla's root certificates
file (certdata.txt). This file can be found in the mozilla source tree:
It contains the certificates in PEM format and therefore
can be directly used with curl / libcurl / php_curl, or with
an Apache+mod_ssl webserver for SSL client authentication.
Just configure this file as the SSLCACertificateFile.
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1.167 pytest-cov 2.7.1

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jar/io/undertow/servlet/spec/UpgradeServletOutputStream.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-
jar/io/undertow/servlet/core/DeploymentImpl.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-
jar/io/undertow/servlet/handlers/security/ServletSingleSignOnAuthenticationMechanism.java
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jar/io/undertow/servlet/spec/ServletOutputStreamImpl.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-
jar/io/undertow/servlet/api/ErrorPage.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-
jar/io/undertow/servlet/core/ManagedListener.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-
jar/io/undertow/servlet/core/LifecycleInterceptorInvocation.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-
jar/io/undertow/servlet/api/CrawlerSessionManagerConfig.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-
jar/io/undertow/servlet/api/SessionManagerFactory.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-
jar/io/undertow/servlet/api/ListenerInfo.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-
jar/undertow/servlet/handlers/DefaultServlet.java

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* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/core/ManagedServlets.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/core/ManagedServlet.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/predicate/DirectoryPredicate.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/api/SingleConstraintMatch.java
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* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/core/DeploymentManagerImpl.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/spec/ServletCookieAdaptor.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/api/MimeMapping.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/api/FilterMappingInfo.java
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* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/attribute/ServletRequestCharacterEncodingAttribute.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/api/WebResourceCollection.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/api/LoggingExceptionHandler.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/handlers/security/ServletAuthenticationCallHandler.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/api/ServletInfo.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/spec/FilterRegistrationImpl.java
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* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/handlers/security/ServletFormAuthenticationMechanism.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources.jar/io/undertow/servlet/UndertowServletLogger.java
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* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-jar/io/undertow/servlet/predicate/FilePredicate.java
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* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-jar/io/undertow/servlet/api/ClassIntrospector.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-jar/io/undertow/servlet/api/ThreadSetupHandler.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-jar/io/undertow/servlet/api/DeploymentInfo.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-jar/io/undertow/servlet/api/ClassIntrospector.java
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-jar/io/undertow/servlet/api/ThreadSetupHandler.java

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 */
/**
 * Servlet specific extension to {@link SinglePortConfidentialityHandler}
 *
 * @author <a href="mailto:darran.lofthouse@jboss.com">Darran Lofthouse</a>
 */
/**
 * Use the HttpServerExchange supplied to check if this request is already 'sufficiently' confidential.
 *
 * Here we say 'sufficiently' as sub-classes can override this and maybe even go so far as querying the actual
 * SSLSession.
 *
 * @param exchange - The {@link HttpServerExchange} for the request being processed.
 * @return true if the request is 'sufficiently' confidential, false otherwise.
 */

Found in path(s):
* /opt/cola/permits/1130030376_1612432719.06/0/undertow-servlet-2-2-2-final-sources-jar/io/undertow/servlet/handlers/security/ServletConfidentialityConstraintHandler.java

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 *
 */
protected String noConfidentialPortAvailable$str() {
    return "UT010053: No confidential port is available to redirect the current request.";
}

public final IllegalStateException noConfidentialPortAvailable() {
    final IllegalStateException result = new IllegalStateException(String.format(getLoggingLocale(),
        noConfidentialPortAvailable$str()));
}

1.169 java-getopt 1.0.13

1.169.1 Available under license:

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Version 2, June 1991

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1.170 wildfly-security-vault-tool 21.0.2.Final
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* /opt/ws_local/PERMITS_SQL/1063930911_1593103343.43/0/jandex-2-1-3-final-sources.jar/org/jboss/jandex/Utils.java
* /opt/ws_local/PERMITS_SQL/1063930911_1593103343.43/0/jandex-2-1-3-final-sources.jar/org/jboss/jandex/FieldInfoGenerator.java
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* /opt/ws_local/PERMITS_SQL/1063930911_1593103343.43/0/jandex-2-1-3-final-sources.jar/org/jboss/jandex/ThrowsTypeTarget.java
* /opt/ws_local/PERMITS_SQL/1063930911_1593103343.43/0/jandex-2-1-3-final-sources.jar/org/jboss/jandex/TypeParameterBoundTypeTarget.java
* /opt/ws_local/PERMITS_SQL/1063930911_1593103343.43/0/jandex-2-1-3-final-sources.jar/org/jboss/jandex/EmptyTypeTarget.java
* /opt/ws_local/PERMITS_SQL/1063930911_1593103343.43/0/jandex-2-1-3-final-sources.jar/org/jboss/jandex/PositionBasedTypeTarget.java
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jar/org/jboss/jandex/TypeTarget.java
* /opt/ws_local/PERMITS_SQL/1063930911_1593103343.43/0/jandex-2-1-3-final-sources-
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jar/org/jboss/jandex/IndexWriterImpl.java
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jar/org/jboss/jandex/IndexReaderV2.java

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* /opt/ws_local/PERMITS_SQL/1063930911_1593103343.43/0/jandex-2-1-3-final-sources-
jar/org/jboss/jandex/PackedDataOutputStream.java
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jar/org/jboss/jandex/ClassInfo.java
* /opt/ws_local/PERMITS_SQL/1063930911_1593103343.43/0/jandex-2-1-3-final-sources-
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* /opt/ws_local/PERMITS_SQL/1063930911_1593103343.43/0/jandex-2-1-3-final-sources-
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jar/jboss/jandex/MethodParameterInfo.java
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jar/jboss/jandex/UnsupportedVersion.java
* /opt/ws_local/PERMITS_SQL/1063930911_1593103343.43/0/jandex-2-1-3-final-sources-
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1.181 libgpg-error 1.41-r0

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The project maintains the following source code repositories:

* https://github.com/eclipse-ee4j/jacc

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### 1.188 slf4j-jboss-logmanager 1.0.4.GA

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1.189 pytz 2021.1

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1.190 opentracing-noop 0.31.0

1.191 libsemanage 2.8-2

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*/opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/tree/ElementQNameIterator.java
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*/opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/ElementHandler.java
*/opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/CDATA.java
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*/opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/rule/Rule.java
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*/opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-
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jar/org/dom4j/ProcessingInstruction.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/util/UserDataElement.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/util/PerThreadSingleton.java
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* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/util/XMLErrorHandler.java
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* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/tree/FlyweightEntity.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/tree/AbstractProcessingInstruction.java
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* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/io/ElementStack.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/jaxb/JAXBWriter.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/dtd/ExternalEntityDecl.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/swing/XMLTableDefinition.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/io/XPP3Reader.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/NodeFilter.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/XPathException.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/XPath.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/rule/pattern/NodeTypePattern.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/dtd/ExternalEntityDecl.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/swing/XMLTableDefinition.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/io/XPP3Reader.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/jaxb/JAXBWriter.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/bean/BeanAttribute.java
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- /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/tree/AbstractCDATA.java
- /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/swing/DocumentTreeModel.java
- /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/tree/FlyweightProcessingInstruction.java
- /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/util/ProxyDocumentFactory.java
- /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/io/PruningElementStack.java
- /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/DocumentType.java
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- /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/tree/DefaultProcessingInstruction.java
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- /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/dom/DOMText.java
- /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/xpath/DefaultXPath.java
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jar/org/dom4j/CharacterData.java
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jar/org/dom4j/jaxb/JAXBReader.java
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* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/io/SAXReader.java
* /opt/ws_local/PERMITS_SQL/1034543185_1588830303.8/0/dom4j-2-1-3-sources-jar/org/dom4j/io/SAXHelper.java
1.195 hibernate-search-serialization-avro

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Glenn Randers-Pehrson
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September 29, 2017

1.200 p11-kit 0.23.14-5.el8_0

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1.201 e2fsprogs 1.45.7-r0
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This is the Debian GNU/Linux prepackaged version of the static EXT2 file system consistency checker (e2fsck.static). The EXT2 utilities were written by Theodore Ts'o <tytso@mit.edu> and Remy Card <card@masi.ibp.fr>.

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# In order to use this stub, the following makefile variables must be defined.

# BSDLIB_VERSION = 1.0
# BSDLIB_IMAGE = libce
# BSDLIB_MYDIR = et
# BSDLIB_INSTALL_DIR = $(SHLIBDIR)
#
all:: image
real-subdirs:: Makefile
@echo "MKDIR pic"
@mkdir -p pic

BSD_LIB = $(BSDLIB_IMAGE).so.$(BSDLIB_VERSION)
BSD_LIB_PIC_FLAG = -fpic

image:$(BSD_LIB)

$(BSD_LIB): $(OBJ)
(cd pic; ld -Bshareable -o $(BSD_LIB) $(LDFLAGS_SHLIB) $(OBJ))
$(MV) pic/$(BSD_LIB) .
$(RM) -f $(BSD_LIB)
(cd ..; $(LN) $(LINK_BUILD_FLAGS) \ `echo $(my_dir) | sed 's;lib/;;'"/$(BSD_LIB) $(BSD_LIB))

install-shlibs install:: $(BSD_LIB)
@echo "INSTALL_PROGRAM $(BSDLIB_INSTALL_DIR)/$(BSD_LIB)"
@$(INSTALL_PROGRAM) $(BSD_LIB) $(DESTDIR)$(BSDLIB_INSTALL_DIR)/$(BSD_LIB)
@-$(LDCONFIG)

install-strip: install

install-shlibs-strip:: install-shlibs

uninstall-shlibs uninstall::
$(RM) -f $(DESTDIR)$(BSDLIB_INSTALL_DIR)/$(BSD_LIB)

clean::
$(RM) -rf pic
$(RM) -f $(BSD_LIB)
$(RM) -f ../$BSD_LIB

This package was added to the e2fsprogs debian source package by
Theodore Ts'o <tytso@mit.edu> on Sat Mar 15 15:33:37 EST 2003

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Index: tdbsa/tdb.c

===================================================================
--- tdbsa.orig/tdb.c
+++ tdbsa/tdb.c
@@ -4,11 +4,11 @@
Last Changed Date: 2007-06-06 20:14:06 -0400 (Wed, 06 Jun 2007)
*/
/ *
- Unix SMB/CIFS implementation.
+ trivial database library - standalone version

- trivial database library - private includes
-
- Copyright (C) Andrew Tridgell              2005
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Theodore Ts'o
23-June-2007

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[This is the first released version of the library GPL. It is numbered 2 because it goes with version 2 of the ordinary GPL.]

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The precise terms and conditions for copying, distribution and modification follow. Pay close attention to the difference between a "work based on the library" and a "work that uses the library". The former contains code derived from the library, while the latter only works together with the library.

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That's all there is to it!
This package was added to the e2fsprogs debian source package by Theodore Ts'o <tytso@mit.edu> on Sat Mar 15 15:33:37 EST 2003

It is part of the main e2fsprogs distribution, which can be found at:

http://sourceforge.net/projects/e2fsprogs

Upstream Author: Theodore Ts'o <tytso@mit.edu>

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This is the Debian GNU/Linux prepackaged version of the ss
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This package was put together by Yann Dirson <dirson@debian.org>,
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Gadi Oxman, August 1995

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When a program is linked with a library, whether statically or using
a shared library, the combination of the two is legally speaking a
combined work, a derivative of the original library. The ordinary
General Public License therefore permits such linking only if the
entire combination fits its criteria of freedom. The Lesser General Public License permits more lax criteria for linking other code with the library.

We call this license the \texttt{Lesser} General Public License because it does more to protect the user's freedom than the ordinary General Public License. It also provides other free software developers more advantage over competing non-free programs. These disadvantages are the reason we use the ordinary General Public License for many libraries. However, the Lesser license provides advantages in certain special circumstances.

For example, on rare occasions, there may be a special need to encourage the widest possible use of a certain library, so that it becomes a de-facto standard. To achieve this, non-free programs must be allowed to use the library. A more frequent case is that a free library does the same job as widely used non-free libraries. In this case, there is little to gain by limiting the free library to free software only, so we use the Lesser General Public License.

In other cases, permission to use a particular library in non-free programs enables a greater number of people to use a large body of free software. For example, permission to use the GNU C Library in non-free programs enables many more people to use the whole GNU operating system, as well as its variant, the GNU/Linux operating system.

Although the Lesser General Public License is more protective of the users' freedom, it does ensure that the user of a program that is linked with the Library has the freedom and the wherewithal to run that program using a modified version of the Library.

The precise terms and conditions for copying, distribution and modification follow. Pay close attention to the difference between a "work based on the library" and a "work that uses the library". The former contains code derived from the library, whereas the latter must be combined with the library in order to run.

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If a facility in the modified Library refers to a function or a table of data to be supplied by an application program that uses the facility, other than as an argument passed when the facility is invoked, then you must make a good faith effort to ensure that, in the event an application does not supply such function or table, the facility still operates, and performs whatever part of its purpose remains meaningful.

(For example, a function in a library to compute square roots has a purpose that is entirely well-defined independent of the application. Therefore, Subsection 2d requires that any application-supplied function or table used by this function must be optional: if the application does not supply it, the square root function must still compute square roots.)

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threshold for this to be true is not precisely defined by law.

If such an object file uses only numerical parameters, data structure layouts and accessors, and small macros and small inline functions (ten lines or less in length), then the use of the object file is unrestricted, regardless of whether it is legally a derivative work. (Executables containing this object code plus portions of the Library will still fall under Section 6.)

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- Use a suitable shared library mechanism for linking with the Library. A suitable mechanism is one that (1) uses at run time a copy of the library already present on the user's computer system, rather than
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@subheading END OF TERMS AND CONDITIONS

@page
@subheading How to Apply These Terms to Your New Libraries

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Open Source Used In Branch Migration Tool Spirit 1936
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@page

@heading Appendix: How to Apply These Terms to Your New Programs

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Also add information on how to contact you by electronic and paper mail.

If the program is interactive, make it output a short notice like this when it starts in an interactive mode:

```
Gnomovision version 69, Copyright (C) @var{year} @var{name of author}
Gnomovision comes with ABSOLUTELY NO WARRANTY; for details type `show w'.
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```

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```
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- the libintl.jar Java library,
- the GNU.Gettext.dll C# library,
- the gettext.sh shells script function library.
The following parts are under the GPL, see file COPYING in the toplevel directory:
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Version 2.1, February 1999

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1.210 typing 3.7.4.3
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A. HISTORY OF THE SOFTWARE

Python was created in the early 1990s by Guido van Rossum at Stichting Mathematisch Centrum (CWI, see http://www.cwi.nl) in the Netherlands as a successor of a language called ABC. Guido remains Python's principal author, although it includes many contributions from others.

In 1995, Guido continued his work on Python at the Corporation for National Research Initiatives (CNRI, see http://www.cnri.reston.va.us) in Reston, Virginia where he released several versions of the software.

In May 2000, Guido and the Python core development team moved to BeOpen.com to form the BeOpen PythonLabs team. In October of the same year, the PythonLabs team moved to Digital Creations (now Zope Corporation, see http://www.zope.com). In 2001, the Python Software Foundation (PSF, see http://www.python.org/psf/) was formed, a non-profit organization created specifically to own Python-related Intellectual Property. Zope Corporation is a sponsoring member of the PSF.

All Python releases are Open Source (see http://www.opensource.org for the Open Source Definition). Historically, most, but not all, Python releases have also been GPL-compatible; the table below summarizes the various releases.
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Open Source Used in Branch Migration Tool Spirit 2412
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Version 2.1, February 1999
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DRuntime: Runtime Library for the D Programming Language

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1.242 pycparser 2.20

1.242.1 Available under license :

pycparser -- A C parser in Python

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1.243 apk-tools 2.12.5-r0

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/*
 * <p>Encodes and decodes to and from Base64 notation.</p>
 * <p>Homepage: <a href="http://iharder.net/base64">http://iharder.net/base64</a>.</p>
 *
 * <p>Example:</p>
 *
 * <code>String encoded = Base64.encode( myByteArray );</code>
 * <br/>
 * <code>byte[] myByteArray = Base64.decode( encoded );</code>
 *
 * <p>The <tt>options</tt> parameter, which appears in a few places, is used to pass
* several pieces of information to the encoder. In the "higher level" methods such as
* encodeBytes( bytes, options ) the options parameter can be used to indicate such
* things as first gzipping the bytes before encoding them, not inserting linefeeds,
* and encoding using the URL-safe and Ordered dialects.</p>
* 
* <p>Note, according to <a href="http://www.faqs.org/rfcs/rfc3548.html">RFC3548</a>,
* Section 2.1, implementations should not add line feeds unless explicitly told
* to do so. I've got Base64 set to this behavior now, although earlier versions
* broke lines by default.</p>
* 
* <p>The constants defined in Base64 can be OR-ed together to combine options, so you
* might make a call like this:</p>
* 
* <code>String encoded = Base64.encodeBytes( mybytes, Base64.GZIP | Base64.DO_BREAK_LINES );</code>
* <p>to compress the data before encoding it and then making the output have newline characters.</p>
* <p>Also...</p>
* <code>String encoded = Base64.encodeBytes( crazyString.getBytes() );</code>
* 
* 
* Change Log:
* 
* <ul>
*  <li>v2.3.7 - Fixed subtle bug when base 64 input stream contained the
*   value 01111111, which is an invalid base 64 character but should not
*   throw an ArrayIndexOutOfBoundsException either. Led to discovery of
*   mishandling (or potential for better handling) of other bad input
*   characters. You should now get an IOException if you try decoding
*   something that has bad characters in it.</li>
*  <li>v2.3.6 - Fixed bug when breaking lines and the final byte of the encoded
*   string ended in the last column; the buffer was not properly shrunk and
*   contained an extra (null) byte that made it into the string.</li>
*  <li>v2.3.5 - Fixed bug in [ @link #encodeFromIn ] where estimated buffer size
*   was wrong for files of size 31, 34, and 37 bytes.</li>
*  <li>v2.3.4 - Fixed bug when working with gzipped streams whereby flushing
*   the Base64OutputStream closed the Base64 encoding (by padding with equals
*   signs) too soon. Also added an option to suppress the automatic decoding
*   of gzipped streams. Also added experimental support for specifying a
*   class loader when using the
*   [ @link #decodeToObject(java.lang.String, int, java.lang.ClassLoader) ]
*   method.</li>
*  <li>v2.3.3 - Changed default char encoding to US-ASCII which reduces the internal Java
*   footprint with its CharEncoders and so forth. Fixed some javadocs that were
*   inconsistent. Removed imports and specified things like java.io.IOException
*   explicitly inline.</li>
*  <li>v2.3.2 - Reduced memory footprint! Finally refined the "guessing" of how big the
*   final encoded data will be so that the code doesn't have to create two output
* arrays: an oversized initial one and then a final, exact-sized one. Big win
* when using the [@link #encodeBytesToBytes(byte[]) family of methods (and not
* using the gzip options which uses a different mechanism with streams and stuff).</li>
* v2.3.1 - Added [@link #encodeBytesToBytes(byte[], int, int, int}) and some
* similar helper methods to be more efficient with memory by not returning a
* String but just a byte array.</li>
* v2.3 - *This is not a drop-in replacement!* This is two years of comments
* and bug fixes queued up and finally executed. Thanks to everyone who sent
* me stuff, and I'm sorry I wasn't able to distribute your fixes to everyone else.
* Much bad coding was cleaned up including throwing exceptions where necessary
* instead of returning null values or something similar. Here are some changes
* that may affect you:
* ul>
* v2.2.1 - Fixed bug using URL_SAFE and ORDERED encodings. Fixed bug
* when using very small files (~&lt; 40 bytes).</li>
* v2.2 - Added some helper methods for encoding/decoding directly from
* one file to the next. Also added a main() method to support command line
* encoding/decoding from one file to the next. Also added these Base64 dialects:
* ol>
* The default is RFC3548 format.</li>
* Calling Base64.setFormat(Base64 BASE64_FORMAT.URLSAFE_FORMAT) generates
* URL and file name friendly format as described in Section 4 of RFC3548.
* Calling Base64.setFormat(Base64 BASE64_FORMAT.ORDERED_FORMAT) generates
* URL and file name friendly format that preserves lexical ordering as described
* Special thanks to Jim Kellerman at &lt;a href="http://www.powerset.com/">http://www.powerset.com/</a>
* for contributing the new Base64 dialects.
* v2.1 - Cleaned up javadoc comments and unused variables and methods. Added some convenience methods for reading and writing to and from files.
* v2.0.2 - Now specifies UTF-8 encoding in places where the code fails on systems with other encodings (like EBCDIC).
* v2.0.1 - Fixed an error when decoding a single byte, that is, when the encoded data was a single byte.
* v2.0 - I got rid of methods that used booleans to set options. Now everything is more consolidated and cleaner. The code now detects when data that's being decoded is gzip-compressed and will decompress it automatically. Generally things are cleaner. You'll probably have to change some method calls that you were making to support the new options format (int's that you "OR" together).
* v1.5.1 - Fixed bug when decompressing and decoding to a byte[] using decode(String s, boolean gzipCompressed).
* v1.5 - Output stream pases on flush() command but doesn't do anything itself. This helps when using GZIP streams.
* v1.4 - Added helper methods to read/write files.
* v1.3.6 - Fixed OutputStream.flush() so that 'position' is reset.
* v1.3.5 - Added flag to turn on and off line breaks. Fixed bug in input stream where last buffer being read, if not completely full, was not returned.
* v1.3.4 - Fixed when "improperly padded stream" error was thrown at the wrong time.
* v1.3.3 - Fixed I/O streams which were totally messed up.

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Please visit http://iharder.net/base64 periodically to check for updates or to contribute improvements.

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Public License. It also provides other free software developers of an advantage over competing non-free programs. These disadvantages are the reason we use the ordinary General Public License for many libraries. However, the Lesser license provides advantages in certain special circumstances.

For example, on rare occasions, there may be a special need to encourage the widest possible use of a certain library, so that it becomes a de-facto standard. To achieve this, non-free programs must be allowed to use the library. A more frequent case is that a free library does the same job as widely used non-free libraries. In this case, there is little to gain by limiting the free library to free software only, so we use the Lesser General Public License.

In other cases, permission to use a particular library in non-free programs enables a greater number of people to use a large body of free software. For example, permission to use the GNU C Library in non-free programs enables many more people to use the whole GNU operating system, as well as its variant, the GNU/Linux operating system.

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(For example, a function in a library to compute square roots has a purpose that is entirely well-defined independent of the application. Therefore, Subsection 2d requires that any application-supplied function or table used by this function must be optional: if the application does not supply it, the square root function must still compute square roots.)

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@item
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@page
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@var{one line to give the program's name and a brief idea of what it does.}
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@end smallexample

Also add information on how to contact you by electronic and paper mail.
If the program is interactive, make it output a short notice like this when it starts in an interactive mode:

@example
Gnomovision version 69, Copyright (C) @var{year} @var{name of author}
Gnomovision comes with ABSOLUTELY NO WARRANTY; for details type `show w'.
This is free software, and you are welcome to redistribute it under certain conditions; type `show c' for details.
@end example

The hypothetical commands @samp{show w} and @samp{show c} should show the appropriate parts of the General Public License. Of course, the commands you use may be called something other than @samp{show w} and @samp{show c}; they could even be mouse-clicks or menu items---whatever suits your program.

You should also get your employer (if you work as a programmer) or your school, if any, to sign a ``copyright disclaimer'' for the program, if necessary. Here is a sample; alter the names:

@example
Yoyodyne, Inc., hereby disclaims all copyright interest in the program `Gnomovision' (which makes passes at compilers) written by James Hacker.

@var{signature of Ty Coon}, 1 April 1989
Ty Coon, President of Vice
@end example

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- the libintl.jar Java library,
- the GNU.Gettext.dll C# library,
- the gettext.sh shells script function library.

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- the _programs_ gettext, ngettext, envsubst,
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Version 2.1, February 1999

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as the successor of the GNU Library Public License, version 2, hence
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*L
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1.261 pyparsing 2.4.7

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1.262 ecj 4.6.1

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1.264 alpine-baselayout 3.2.0-r8

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=aarch64-- | FileCheck %s

; A shuffle mask with all undef elements is always legal.

define <4 x i32> @PR41535(<2 x i32> %p1, <2 x i32> %p2) {
; CHECK-LABEL: PR41535:
; CHECK: // %bb.0:
; CHECK-NEXT: ext v0.8b, v0.8b, v1.8b, #4
; CHECK-NEXT: mov v0.d[1], v0.d[0]
; CHECK-NEXT: ret
%cat1 = shufflevector <2 x i32> %p1, <2 x i32> undef, <4 x i32> <i32 undef, i32 1, i32 undef, i32 undef>
%cat2 = shufflevector <2 x i32> %p2, <2 x i32> undef, <4 x i32> <i32 0, i32 undef, i32 undef, i32 undef>
%r = shufflevector <4 x i32> %cat1, <4 x i32> %cat2, <4 x i32> <i32 undef, i32 undef, i32 1, i32 4>
ret <4 x i32> %r
define void @autogen_SD4739(i8*) {
    ; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
    BB:
    %L34 = load i8, i8* %0
    %Cmp56 = icmp sgt i8 undef, %L34
    br label %CF246

    CF246: ; preds = %CF246, %BB
    %Sl163 = select i1 %Cmp56, i8 %L34, i8 undef
    br i1 undef, label %CF246, label %CF248

    CF248: ; preds = %CF248, %CF246
    store i8 %Sl163, i8* %0
    br label %CF248
}

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; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s

define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
  ; CHECK-LABEL: test_sitofp_fixed:

  ; First, extend each i32 to i64
  ; CHECK-DAG: sshll2.2d [[BLOCK0_HI:v[0-9]+]], v0, #0
  ; CHECK-DAG: sshll2.2d [[BLOCK1_HI:v[0-9]+]], v1, #0
  ; CHECK-DAG: sshll2.2d [[BLOCK2_HI:v[0-9]+]], v2, #0
  ; CHECK-DAG: sshll2.2d [[BLOCK3_HI:v[0-9]+]], v3, #0
  ; CHECK-DAG: sshll.2d [[BLOCK0_LO:v[0-9]+]], v0, #0
  ; CHECK-DAG: sshll.2d [[BLOCK1_LO:v[0-9]+]], v1, #0
  ; CHECK-DAG: sshll.2d [[BLOCK2_LO:v[0-9]+]], v2, #0
  ; CHECK-DAG: sshll.2d [[BLOCK3_LO:v[0-9]+]], v3, #0
; Next, convert each to double.
; CHECK-DAG: scvtf.2d v0, [[BLOCK0_LO]]
; CHECK-DAG: scvtf.2d v1, [[BLOCK0_HI]]
; CHECK-DAG: scvtf.2d v2, [[BLOCK1_LO]]
; CHECK-DAG: scvtf.2d v3, [[BLOCK1_HI]]
; CHECK-DAG: scvtf.2d v4, [[BLOCK2_LO]]
; CHECK-DAG: scvtf.2d v5, [[BLOCK2_HI]]
; CHECK-DAG: scvtf.2d v6, [[BLOCK3_LO]]
; CHECK-DAG: scvtf.2d v7, [[BLOCK3_HI]]

; CHECK: ret
%flt = sitofp <16 x i32> %in to <16 x double>
%res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0>
ret <16 x double> %res
}

; This one is small enough to satisfy isSimple, but still illegally large.
define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
; CHECK-LABEL: test_sitofp_fixed_shortish:

; CHECK-DAG: scvtf.2d v0, v0
; CHECK-DAG: scvtf.2d v1, v1

; CHECK: ret
%flt = sitofp <4 x i64> %in to <4 x double>
%res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
ret <4 x double> %res
}

; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s
;
; D31946
; Check that we dont end up with the ""LLVM ERROR: Cannot select"" error.
; Additionally ensure that the output code actually put fp128 values in SSE registers.

declare fp128 @llvm.fabs.f128(fp128)
declare fp128 @llvm.copysign.f128(fp128, fp128)

define fp128 @TestSelect(fp128 %a, fp128 %b) {
; CHECK-LABEL: TestSelect:
; CHECK: # %bb.0:
; CHECK-NEXT: pushq %rbx
; CHECK-NEXT: .cfi_def_cfa_offset 16
; CHECK-NEXT: subq $32, %rsp
; CHECK-NEXT: .cfi_def_cfa_offset 48
; CHECK-NEXT: .cfi_offset %rbx, -16
; CHECK-NEXT:    movaps %xmm0, %xmm1
; CHECK-NEXT:    callq __multf3
; CHECK-NEXT:    xorps [{.*}(%rip), %xmm0
; CHECK-NEXT:    popq %rax
; CHECK-NEXT:    .cfi_def_cfa_offset 8
; CHECK-NEXT:    retq
%mul = fmul fp128 %a, %a
%res = fsub fp128 0xL00000000000000008000000000000000, %mul
ret fp128 %res
}

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; RUN: opt %s -inline -S | FileCheck %s

define internal void @innerSmall() "min-legal-vector-width"="128" {
  ret void
}

define internal void @innerLarge() "min-legal-vector-width"="512" {
  ret void
}

define internal void @innerNoAttribute() {
  ret void
}

; We should not add an attribute during inlining. No attribute means unknown.
; Inlining doesn't change the fact that we don't know anything about this
; function.
define void @outerNoAttribute() {
  call void @innerLarge()
  ret void
}

define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
  call void @innerLarge()
  ret void
}
define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
    call void @innerSmall()
    ret void
}

; We should remove the attribute after inlining since the callee's
; vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
    call void @innerNoAttribute()
    ret void
}

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }
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; RUN: opt -consthoist -S -o - %s | FileCheck %s
target triple = "thumbv6m-none--musleabi"
; Check that for i8 type, the maximum legal offset is 31.
; Also check that an constant used as value to be stored rather than
; pointer in a store instruction is hoisted.
; CHECK: foo_i8
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874720 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK-DAG: %[[C3:const[0-9]?]] = bitcast i32 805873720 to i32
; CHECK-DAG: %[[C4:const[0-9]?]] = bitcast i32 805873688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i8*
; CHECK-NEXT: %1 = load volatile i8, i8* %0
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i8*
; CHECK-NEXT: %3 = load volatile i8, i8* %2
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i8*
; CHECK-NEXT: %5 = load volatile i8, i8* %4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i8*
; CHECK-NEXT: %7 = load volatile i8, i8* %6
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i8*
; CHECK-NEXT: %9 = load volatile i8, i8* %8
; CHECK-NEXT: %10 = inttoptr i32 %[[C4]] to i8*
; CHECK-NEXT: store i8 %9, i8* %10
; CHECK-NEXT: %11 = inttoptr i32 %[[M4]] to i8*
; CHECK-NEXT: store i8 %7, i8* %11
; CHECK-NEXT: %12 = inttoptr i32 %[[C3]] to i8*
; CHECK-NEXT: store i8 %5, i8* %12
; CHECK-NEXT: %13 = inttoptr i32 %[[M5]] to i8*
; CHECK-NEXT: store i8 %3, i8* %13
; CHECK-NEXT: %14 = inttoptr i32 %[[M6]] to i8*
; CHECK-NEXT: store i8 %14, i8** @goo

@goo = global i8* undef

define void @foo_i8() {
  entry:
  %0 = load volatile i8, i8* inttoptr (i32 805874688 to i8*)
  %1 = load volatile i8, i8* inttoptr (i32 805874692 to i8*)
  %2 = load volatile i8, i8* inttoptr (i32 805874719 to i8*)
  %3 = load volatile i8, i8* inttoptr (i32 805874720 to i8*)
  %4 = load volatile i8, i8* inttoptr (i32 805874727 to i8*)
  store i8 %4, i8* inttoptr(i32 805873688 to i8*)
  store i8 %3, i8* inttoptr(i32 805873719 to i8*)
  store i8 %2, i8* inttoptr(i32 805873720 to i8*)
}
store i8 %1, i8* inttoptr(i32 805873727 to i8*)
store i8* inttoptr(i32 805874800 to i8*), i8** @goo
ret void
}

; Check that for i16 type, the maximum legal offset is 62.
; CHECK: foo_i16
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874752 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i16*
; CHECK-NEXT: %1 = load volatile i16, i16* %0, align 2
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i16*
; CHECK-NEXT: %3 = load volatile i16, i16* %2, align 2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 32
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i16*
; CHECK-NEXT: %5 = load volatile i16, i16* %4, align 2
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C2]], 62
; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to i16*
; CHECK-NEXT: %7 = load volatile i16, i16* %6, align 2
; CHECK-NEXT: %8 = inttoptr i32 %[[C1]] to i16*
; CHECK-NEXT: %9 = load volatile i16, i16* %8, align 2
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 22
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i16*
; CHECK-NEXT: %11 = load volatile i16, i16* %10, align 2

define void @foo_i16() {
entry:
%0 = load volatile i16, i16* inttoptr (i32 805874688 to i16*), align 2
%1 = load volatile i16, i16* inttoptr (i32 805874692 to i16*), align 2
%2 = load volatile i16, i16* inttoptr (i32 805874720 to i16*), align 2
%3 = load volatile i16, i16* inttoptr (i32 805874750 to i16*), align 2
%4 = load volatile i16, i16* inttoptr (i32 805874752 to i16*), align 2
%5 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
ret void
}

; Check that for i32 type, the maximum legal offset is 124.
; CHECK: foo_i32
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i32*
; CHECK-NEXT: %1 = load volatile i32, i32* %0, align 4
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i32*
; CHECK-NEXT: %3 = load volatile i32, i32* %2, align 4
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 124
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i32*
define void @foo_i32() {
entry:
  %0 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 4
  %1 = load volatile i32, i32* inttoptr (i32 805874692 to i32*), align 4
  %2 = load volatile i32, i32* inttoptr (i32 805874812 to i32*), align 4
  %3 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
  %4 = load volatile i32, i32* inttoptr (i32 805874824 to i32*), align 4
  %5 = load volatile i32, i32* inttoptr (i32 805874828 to i32*), align 4
  ret void
}

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; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature --scrub-attributes
; RUN: opt -S -argpromotion < %s | FileCheck %s
; RUN: opt -S -passes=argpromotion < %s | FileCheck %s
; Test that we only promote arguments when the caller/callee have compatible function attribues.

target triple = "x86_64-unknown-linux-gnu"

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {  
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512 
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* [[ARG1_VAL:%.*]]) 
; CHECK-NEXT: bb: 
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {  
%tmp = load <8 x i64>, <8 x i64>* %arg  
store <8 x i64> %tmp, <8 x i64>* %arg  
ret void  
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {  
%tmp = load <8 x i64>, <8 x i64>* %arg  
store <8 x i64> %tmp, <8 x i64>* %arg  
ret void  
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {  
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256  
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])  
; CHECK-NEXT: bb:  
; CHECK-NEXT: [[TMP:.%.*]] = alloca <8 x i64>, align 32  
; CHECK-NEXT: [[TMP2:.%.*]] = alloca <8 x i64>, align 32  
; CHECK-NEXT: [[TMP3:.%.*]] = bitcast <8 x i64>* [[TMP]] to i8*  
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)  
; CHECK-NEXT: [[TMP_VAL:.%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]  
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])  
; CHECK-NEXT: [[TMP4:.%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32  
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2  
; CHECK-NEXT: ret void  
}
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
  ; This should promote
  define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
  }
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
  ; This should promote
  define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
  }
}
i64* [[TMP2]], <8 x i64>* [[TMP_VAL]])
; CHECK-NEXT:  [[TMP4:.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:  ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL:  define {{\[^@\]+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME:  (<8 x i64>* [[ARG:.*]], <8 x i64>* readonly [[ARG1:.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:  [[TMP:.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
; CHECK-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
; CHECK-NEXT:  ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
; CHECK-LABEL:  define {{\[^@\]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME:  (<8 x i64>* [[ARG:.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:  [[TMP:.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP2:.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP3:.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:  call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT:  call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]])
; CHECK-NEXT:  [[TMP4:.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:  ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

: This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 {
    : CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
    : CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
    : CHECK-NEXT: bb:
    ; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
    ; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
    ; CHECK-NEXT: ret void

    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
    : CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
    : CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
    : CHECK-NEXT: bb:
    ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
    ; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]])
    ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
    ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
    ; CHECK-NEXT: ret void

    bb:
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #3 {
  ; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* [[ARG1_VAL:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
  ; CHECK-NEXT: ret void

  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
  ; CHECK-LABEL: define {{[^@]+}}@avx2Legal256Prefer256CallAvx2Legal512Prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
  ; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
  ; CHECK-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP_VAL]])
  ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; CHECK-NEXT: ret void

  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  %tmp2 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #4 {
    ; CHECK-LABEL: define \[
    ; CHECK-SAME: (\[
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
    ; CHECK-NEXT: ret void
    
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
    ; CHECK-LABEL: define \[
    ; CHECK-SAME: (\[
    ; CHECK-NEXT: bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define internal i32 @scalar_callee_avx512_legal256_call_avx512_legal512_prefer256(i32* %X, i32* %Y) #2 {
    ; CHECK-LABEL: define \[
    ; CHECK-SAME: (\[
    ; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
    ; CHECK-NEXT: ret void
    
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}
define i32 @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    %A = alloca i32
    store i32 1, i32* %A
    %C = call i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %A, i32* %B)
    ret i32 %C
}

define i32 @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    %A = load i32, i32* %X
    %B = load i32, i32* %Y
    %C = add i32 %A, %B
    ret i32 %C
}

define internal i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %X, i32* %Y) #2 {
    %A = alloca i32
    store i32 1, i32* %A
    %C = call i32 @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %A, i32* %B)
    ret i32 %C
}

define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %B) #2 {
    %A = alloca i32
    store i32 1, i32* %A
    %C = load i32, i32* %X
    %B = load i32, i32* %Y
    %C = add i32 %A, %B
    ret i32 %C
}

define i32 @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    %A = load i32, i32* %X
    %B = load i32, i32* %Y
    %C = add i32 %A, %B
    ret i32 %C
}

define internal i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %X, i32* %Y) #2 {
    %A = load i32, i32* %X
    %B = load i32, i32* %Y
    %C = add i32 %A, %B
    ret i32 %C
}

define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %B) #2 {
    %A = load i32, i32* %X
    %B = load i32, i32* %Y
    %C = add i32 %A, %B
    ret i32 %C
}

define i32 @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    %A = load i32, i32* %X
    %B = load i32, i32* %Y
    %C = add i32 %A, %B
    ret i32 %C
}
function @llvm_memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5
  attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
  attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
  attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
  attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
  attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
  attributes #5 = { argmemonly nounwind }
 ..........................
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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit,avx512vbmi | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; Make sure CPUs default to prefer-256-bit. avx512vnni isn't interesting as it just adds an isel peephole for vpmaddwd+vpaddd
; This file primarily contains tests for specific places in X86ISelLowering.cpp that needed be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

define void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: add256:
  ; CHECK:
  # %bb.0:
  ; CHECK-NEXT: vmovdqa (%rdi), %ymm0
  ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
  ; CHECK-NEXT: vpaddd 32(%rsi), %ymm0, %ymm1
  ; CHECK-NEXT: vpaddd (%rsi), %ymm0, %ymm0
  ; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
  ; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
  ; CHECK-NEXT: vzeroupper
  ; CHECK-NEXT: retq
  %d = load <16 x i32>, <16 x i32>* %a
  %e = load <16 x i32>, <16 x i32>* %b
  %f = add <16 x i32> %d, %e
  store <16 x i32> %f, <16 x i32>* %c
  ret void
}

define void @add512(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="512" {
  ; CHECK-LABEL: add512:
  ; CHECK:
  # %bb.0:
  ; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
  ; CHECK-NEXT: vmovdqa64 32(%rdi), %zmm1
  ; CHECK-NEXT: vpaddd 32(%rsi), %zmm0, %zmm1
  ; CHECK-NEXT: vpaddd (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
  ; CHECK-NEXT: vmovdqa64 %zmm1, 32(%rdx)
  ; CHECK-NEXT: vzeroupper
  ; CHECK-NEXT: retq
  %d = load <16 x i32>, <16 x i32>* %a
  %e = load <16 x i32>, <16 x i32>* %b
  %f = add <16 x i32> %d, %e
  store <16 x i32> %f, <16 x i32>* %c

ret void
}
define void @avg_v64i8_256(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="256" {
; CHECK-LABEL: avg_v64i8_256:
; CHECK:
# %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT: vpavgb (%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpavgb 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT: vmovdqu %ymm1, (%rax)
; CHECK-NEXT: vmovdqu %ymm0, (%rax)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%1 = load <64 x i8>, <64 x i8>* %a
%2 = load <64 x i8>, <64 x i8>* %b
%3 = zext <64 x i8> %1 to <64 x i32>
%4 = zext <64 x i8> %2 to <64 x i32>
%5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
%6 = add nuw nsw <64 x i32> %5, %4
%7 = lshr <64 x i32> %6, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
%8 = trunc <64 x i32> %7 to <64 x i8>
store <64 x i8> %8, <64 x i8>* undef, align 4
ret void
}

define void @avg_v64i8_512(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="512" {
; CHECK-LABEL: avg_v64i8_512:
; CHECK:
# %bb.0:
; CHECK-NEXT: vmovdqa64 (%rsi), %zmm0
; CHECK-NEXT: vpavgb (%rdi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqu64 %zmm0, (%rax)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%1 = load <64 x i8>, <64 x i8>* %a
%2 = load <64 x i8>, <64 x i8>* %b
%3 = zext <64 x i8> %1 to <64 x i32>
%4 = zext <64 x i8> %2 to <64 x i32>
%5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,

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Define void @pmaddwd_32_256(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="256" {  
  ; CHECK-LABEL: pmaddwd_32_256:  
  ; CHECK:       # %bb.0:  
  ; CHECK-NEXT: vmovdqa (%rdi), %ymm0  
  ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1  
  ; CHECK-NEXT: vpmaddwd 32(%rsi), %ymm1, %ymm1  
  ; CHECK-NEXT: vpmaddwd (%rsi), %ymm0, %ymm0  
  ; CHECK-NEXT: vmovdqa %ymm0, (%rdx)  
  ; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)  
  ; CHECK-NEXT: vzeroupper  
  ; CHECK-NEXT: retq  
  %A = load <32 x i16>, <32 x i16>* %APtr  
  %B = load <32 x i16>, <32 x i16>* %BPtr  
  %a = sext <32 x i16> %A to <32 x i32>  
  %b = sext <32 x i16> %B to <32 x i32>  
  %m = mul nsw <32 x i32> %a, %b  
  %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>  
  %even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>  
  %ret = add <16 x i32> %odd, %even  
  store <16 x i32> %ret, <16 x i32>* %CPtr  
  ret void  
}

Define void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="512" {  
  ; CHECK-LABEL: pmaddwd_32_512:  
  ; CHECK:       # %bb.0:  
  ; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0  
  ; CHECK-NEXT: vmovdqa64 (%rsi), %zmm0, %zmm0  
  ; CHECK-NEXT: vpmaddwd (%rsi), %zmm0, %zmm0  
  ; CHECK-NEXT: vzeroupper  
  ; CHECK-NEXT: retq  
  %A = load <32 x i16>, <32 x i16>* %APtr  
  %B = load <32 x i16>, <32 x i16>* %BPtr  

%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> %i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> %i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

define void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: psubus_64i8_max_256:
  ; CHECK: # %bb.0:
  ; CHECK-NEXT: vmmovdqa (%rdi), %ymm0
  ; CHECK-NEXT: vmmovdqa 32(%rdi), %ymm1
  ; CHECK-NEXT: vpmsubusb (%rsi), %ymm0, %ymm1
  ; CHECK-NEXT: vpsubusb (%rsi), %ymm1, %ymm0
  ; CHECK-NEXT: vmmovdqa %ymm0, (%rdx)
  ; CHECK-NEXT: vmmovdqa %ymm1, 32(%rdx)
  ; CHECK-NEXT: vzeroupper
  ; CHECK-NEXT: retq
  %x = load <64 x i8>, <64 x i8>* %xptr
  %y = load <64 x i8>, <64 x i8>* %ypr
  %cmp = icmp ult <64 x i8> %x, %y
  %max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
  %res = sub <64 x i8> %max, %y
  store <64 x i8> %res, <64 x i8>* %zptr
  ret void
}

define void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %ypr, <64 x i8>* %zptr) "min-legal-vector-width"="512" {
  ; CHECK-LABEL: psubus_64i8_max_512:
  ; CHECK: # %bb.0:
  ; CHECK-NEXT: vmmovdqa64 (%rdi), %zmm0
  ; CHECK-NEXT: vpsubusb (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT: vmmovdqa64 %zmm0, (%rdx)
  ; CHECK-NEXT: vzeroupper
  ; CHECK-NEXT: retq
  %x = load <64 x i8>, <64 x i8>* %xptr
  %y = load <64 x i8>, <64 x i8>* %ypr
  %cmp = icmp ult <64 x i8> %x, %y
  %max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
  %res = sub <64 x i8> %max, %y
  store <64 x i8> %res, <64 x i8>* %zptr
define i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: _Z9test_charPcS_i_256:
    ; CHECK:       # %bb.0: # %entry
    ; CHECK-NEXT:    movl %edx, %eax
    ; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
    ; CHECK-NEXT:    xorl %ecx, %ecx
    ; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
    ; CHECK-NEXT:    vpxor %xmm2, %xmm2, %xmm2
    ; CHECK-NEXT:    .p2align 4, 0x90
    ; CHECK-NEXT:  .LBB8_1: # %vector.body
    ; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
    ; CHECK-NEXT:    vpmovsxbw 16(%rdi,%rcx), %ymm3
    ; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %ymm4
    ; CHECK-NEXT:    vpmovsxbw 16(%rsi,%rcx), %ymm5
    ; CHECK-NEXT:    vpmaddwd %ymm3, %ymm5, %ymm3
    ; CHECK-NEXT:    vpaddd %ymm2, %ymm3, %ymm2
    ; CHECK-NEXT:    vpmovsxbw (%rsi,%rcx), %ymm3
    ; CHECK-NEXT:    vpmaddwd %ymm4, %ymm3, %ymm3
    ; CHECK-NEXT:    vpaddd %ymm1, %ymm3, %ymm1
    ; CHECK-NEXT:    addq $32, %rcx
    ; CHECK-NEXT:    cmpq %rcx, %rax
    ; CHECK-NEXT:    jne .LBB8_1
    ; CHECK-NEXT:  # %bb.2: # %middle.block
    ; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm1
    ; CHECK-NEXT:    vpaddd %ymm0, %ymm2, %ymm0
    ; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm0
    ; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
    ; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
    ; CHECK-NEXT:    vpmaddwd %ymm4, %ymm3, %ymm3
    ; CHECK-NEXT:      \[ \text{entry:}
    ; CHECK-NEXT:      \text{br label %vector.body}
    ; \text{entry:}
    ; %3 = zext i32 %2 to i64
    ; %vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
    ; \text{vector.body:}
    ; \text{\%index = phi i64 [ \%index.next, %vector.body ], [ 0, \%entry ]}
    ; \text{\%vec.phi = phi \text{\<32 x i32\>} [ \%11, %vector.body ], [ zeroinitializer, \%entry ]}
    ; \text{\%4 = getelementptr inbounds i8, i8* \%0, i64 \%index}
    ; \text{\%5 = bitcast i8* \%4 to \<32 x i8\>*}
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %3, %10
%12 = icmp eq i64 %11, %3
br i1 %12, label %middle.block, label %vector.body

middle.block:
%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 1, i32 2, i32 3, i32 4, i32 5, i32 6, i32 7, i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 2, i32 3, i32 4, i32 5, i32 6, i32 7, i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13
}

define i32 @__Z9test_charPcS_i_512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="512" { ; CHECK-LABEL: __Z9test_charPcS_i_512: ; CHECK: # %bb.0: # %entry ; CHECK-NEXT: movl %edx, %eax ; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
entry:
%3 = zext i32 %2 to i64
br label %vector.body

vector.body:
%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body

middle.block:
%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> %i32 16, i32 17, i32 18, i32 19, i32 20,
define i32 @sad_16i8_256() "min-legal-vector-width"="256" {
    ; CHECK-LABEL: sad_16i8_256:
    ; CHECK:       # %bb.0: # %entry
    ; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
    ; CHECK-NEXT:    movq $-1024, %rax # imm = 0xFC00
    ; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
    ; CHECK-NEXT:    .p2align 4, 0x90
    ; CHECK-NEXT:  .LBB10_1: # %vector.body
    ; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
    ; CHECK-NEXT:    vmovdqu a+1024(%rax), %xmm2
    ; CHECK-NEXT:    vpsadbw b+1024(%rax), %xmm2, %xmm2
    ; CHECK-NEXT:    vpaddd %ymm1, %ymm2, %ymm1
    ; CHECK-NEXT:    addq $4, %rax
    ; CHECK-NEXT:    jne .LBB10_1
    ; CHECK-NEXT:  # %bb.2: # %middle.block
    ; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm0
    ; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
    ; CHECK-NEXT:    %13 = extractelement <32 x i32> %bin.rdx20, i32 0
    ; CHECK-NEXT:    ret i32 %13
}

@a = global [1024 x i8] zeroinitializer, align 16
@b = global [1024 x i8] zeroinitializer, align 16
entry:
    br label %vector.body

vector.body:
    %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
    %vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
    %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
    %1 = bitcast i8* %0 to <16 x i8>*
    %wide.load = load <16 x i8>, <16 x i8>* %1, align 4
    %2 = zext <16 x i8> %wide.load to <16 x i32>
    %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
    %4 = bitcast i8* %3 to <16 x i8>*
    %wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
    %5 = zext <16 x i8> %wide.load1 to <16 x i32>
    %6 = sub nsw <16 x i32> %2, %5
    %7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
    %8 = sub nsw <16 x i32> zeroinitializer, %6
    %9 = select <16 x i1> %7, %6, <16 x i32> %8
    %10 = add nsw <16 x i32> %9, %vec.phi
    %index.next = add i64 %index, 1024
    br i1 %11, label %middle.block, label %vector.body

middle.block:
    %rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef%>
    %bin.rdx = add <16 x i32> %10, %rdx.shuf
    %rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef%>
    %bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
    %rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef%>
    %bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
    %rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef%>
    %bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

define i32 @sad_16i8_512() "min-legal-vector-width"="512" {
; CHECK-LABEL: sad_16i8_512:
; CHECK: # %bb.0: # %entry
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: movq $-1024, %rax # imm = 0xF0C0
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB11_1: # %vector.body
; CHECK-NEXT: #=>This Inner Loop Header: Depth=1
; CHECK-NEXT: vmovdqu a+1024(%rax), %xmm1
; CHECK-NEXT: vpsadbw b+1024(%rax), %xmm1, %xmm1
; CHECK-NEXT: vpaddd %zmm0, %zmm1, %zmm0
; CHECK-NEXT: addq $4, %rax
; CHECK-NEXT: jne .LBB11_1
; CHECK-NEXT: ; %bb.2: # %middle.block
; CHECK-NEXT: vextracti64x4 %1, %zmm0, %ymm1
; CHECK-NEXT: vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT: vextracti128 %1, %ymm0, %xmm1
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vmovd %xmm0, %eax
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
entry:
br label %vector.body

vector.body:
%index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
%vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
%0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
%1 = bitcast i8* %0 to <16 x i8>*
%wide.load = load <16 x i8>, <16 x i8>* %1, align 4
%2 = zext <16 x i8> %wide.load to <16 x i32>
%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
%4 = bitcast i8* %3 to <16 x i8>*
%wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
%5 = zext <16 x i8> %wide.load1 to <16 x i32>
%6 = sub nsw <16 x i32> %2, %5
%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
%8 = sub nsw <16 x i32> zeroinitializer, %6
%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

middle.block:
%rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %10, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> <16 x i32> undef, <16 x i32> <i32 1, i32 2, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> <16 x i32> <16 x i32> undef, <16 x i32> <i32 1, i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

define void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f32_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm1
; CHECK-NEXT: vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT: vmovaps %ymm1, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
define void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="256" {  
; CHECK-LABEL: sbto16f64_256:  
; CHECK:       # %bb.0:  
; CHECK-NEXT:    vpmovw2m %ymm0, %k0  
; CHECK-NEXT:    kshiftrw $8, %k0, %k1  
; CHECK-NEXT:    vpmovm2d %k1, %ymm0  
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm1  
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm0  
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm0  
; CHECK-NEXT:    vpmovm2d %k0, %ymm2  
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm3  
; CHECK-NEXT:    vextracti128 $1, %ymm2, %xmm2  
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm2  
; CHECK-NEXT:    vmovaps %ymm2, 32(%rdi)  
; CHECK-NEXT:    vmovaps %ymm1, (%rdi)  
; CHECK-NEXT:    vmovaps %ymm0, 96(%rdi)  
; CHECK-NEXT:    vmovaps %ymm1, 64(%rdi)  
; CHECK-NEXT:    vzeroupper  
; CHECK-NEXT:    retq  

%mask = icmp slt <16 x i16> %a, zeroinitializer  
%1 = sitofp <16 x i1> %mask to <16 x float>  
store <16 x float> %1, <16 x float>* %res  
ret void  
}

define void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="512" {  
; CHECK-LABEL: sbto16f64_512:  
; CHECK:       # %bb.0:  
; CHECK-NEXT:    vpmovw2m %ymm0, %k0  
; CHECK-NEXT:    kshiftrw $8, %k0, %k1  
; CHECK-NEXT:    vpmovm2d %k1, %ymm0  
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm1  
; CHECK-NEXT:    vextracti64x4 $1, %ymm0, %xmm0  
; CHECK-NEXT:    vcvtdq2pd %ymm0, %xmm0  
; CHECK-NEXT:    vmovaps %ymm0, 96(%rdi)  
; CHECK-NEXT:    vmovaps %ymm1, 64(%rdi)  
; CHECK-NEXT:    vzeroupper  
; CHECK-NEXT:    retq  

%mask = icmp slt <16 x i16> %a, zeroinitializer  
%1 = sitofp <16 x i1> %mask to <16 x double>  
store <16 x double> %1, <16 x double>* %res  
ret void  
}

define void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="512" {  
; CHECK-LABEL: sbto16f64_512:  
; CHECK:       # %bb.0:  
; CHECK-NEXT:    vpmovw2m %ymm0, %k0  
; CHECK-NEXT:    kshiftrw $8, %k0, %k1  
; CHECK-NEXT:    vpmovm2d %k1, %ymm0  
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm1  
; CHECK-NEXT:    vextracti64x4 $1, %ymm0, %xmm0  
; CHECK-NEXT:    vcvtdq2pd %ymm0, %xmm0  
; CHECK-NEXT:    vmovaps %ymm0, 96(%rdi)  
; CHECK-NEXT:    vmovaps %ymm1, 64(%rdi)  
; CHECK-NEXT:    vzeroupper  
; CHECK-NEXT:    retq  

%mask = icmp slt <16 x i16> %a, zeroinitializer  
%1 = sitofp <16 x i1> %mask to <16 x double>  
store <16 x double> %1, <16 x double>* %res  
ret void  
}
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: ubto16f32_256:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:  kshiftrw $8, %k0, %k1
    ; CHECK-NEXT:  vpmovm2d %k1, %ymm0
    ; CHECK-NEXT:  vpsrld $31, %ymm0, %ymm0
    ; CHECK-NEXT:  vcvtqd2ps %ymm0, %ymm0
    ; CHECK-NEXT:  vpmovm2d %k0, %ymm1
    ; CHECK-NEXT:  vpsrld $31, %ymm1, %ymm1
    ; CHECK-NEXT:  vcvtqd2ps %ymm1, %ymm1
    ; CHECK-NEXT:  vmovaps %ymm1, (%rdi)
    ; CHECK-NEXT:  vmovaps %ymm0, 32(%rdi)
    ; CHECK-NEXT:  vzeroupper
    ; CHECK-NEXT:  retq
    %mask = icmp slt <16 x i16> %a, zeroinitializer
    %1 = uitofp <16 x i1> %mask to <16 x float>
    store <16 x float> %1, <16 x float>* %res
    ret void
}

define void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: ubto16f32_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vpmovw2m %zmm0, %k0
    ; CHECK-NEXT:  vpmovm2d %k0, %zmm0
    ; CHECK-NEXT:  vpsrld $31, %zmm0, %zmm0
    ; CHECK-NEXT:  vcvtqd2ps %zmm0, %zmm0
    ; CHECK-NEXT:  vmovaps %zmm0, (%rdi)
    ; CHECK-NEXT:  vmovaps %zmm0, 32(%rdi)
    ; CHECK-NEXT:  vzeroupper
    ; CHECK-NEXT:  retq
    %mask = icmp slt <16 x i16> %a, zeroinitializer
    %1 = uitofp <16 x i1> %mask to <16 x float>
    store <16 x float> %1, <16 x float>* %res
    ret void
}

define void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: ubto16f64_256:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:  kshiftrw $8, %k0, %k1
define void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {  
    %mask = icmp slt <16 x i16> %a, zeroinitializer  
    %1 = uitofp <16 x i1> %mask to <16 x double>  
    store <16 x double> %1, <16 x double>* %res  
    ret void  
}

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {  
    %mask = icmp slt <16 x i16> %a, zeroinitializer  
    %1 = uitofp <16 x i1> %mask to <16 x double>  
    store <16 x double> %1, <16 x double>* %res  
    ret void  
}

define void @test_16f32toub_256(<16 x i16> %passthru) "min-legal-vector-width"="256" {  
    %mask = icmp slt <16 x i16> %a, zeroinitializer  
    %1 = uitofp <16 x i1> %mask to <16 x double>  
    store <16 x double> %1, <16 x double>* %res  
    ret void  
}
define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {  
; CHECK-LABEL: test_16f32toub_512:  
; CHECK:       # %bb.0:  
; CHECK-NEXT:    vcvttps2dq (%rdi), %zmm1  
; CHECK-NEXT:    vpmovd2m %zmm1, %k1  
; CHECK-NEXT:    vcvttps2dq 32(%rdi), %zmm1  
; CHECK-NEXT:    vpmovd2m %zmm1, %k1  
; CHECK-NEXT:    kunpckbw %k0, %k1, %k1  
; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 [%k1] {z}  
; CHECK-NEXT:    retq  
%a = load <16 x float>, <16 x float>* %ptr  
%mask = fptoui <16 x float> %a to <16 x i1>  
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer  
ret <16 x i16> %select  
}  

define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {  
; CHECK-LABEL: test_16f32tosb_256:  
; CHECK:       # %bb.0:  
; CHECK-NEXT:    vcvttps2dq (%rdi), %zmm1  
; CHECK-NEXT:    vpmovd2m %zmm1, %k1  
; CHECK-NEXT:    vcvttps2dq 32(%rdi), %zmm1  
; CHECK-NEXT:    vpmovd2m %zmm1, %k1  
; CHECK-NEXT:    kunpckbw %k0, %k1, %k1  
; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 [%k1] {z}  
; CHECK-NEXT:    retq  
%a = load <16 x float>, <16 x float>* %ptr  
%mask = fptosi <16 x float> %a to <16 x i1>  
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer  
ret <16 x i16> %select  
}  

define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {  
; CHECK-LABEL: test_16f32tosb_512:  
; CHECK:       # %bb.0:  
; CHECK-NEXT:    vcvttps2dq (%rdi), %ymm1  
; CHECK-NEXT:    vpmovd2m %ymm1, %k1  
; CHECK-NEXT:    vcvttps2dq 32(%rdi), %ymm1  
; CHECK-NEXT:    vpmovd2m %ymm1, %k1  
; CHECK-NEXT:    kunpckbw %k0, %k1, %k1  
; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 [%k1] {z}  
; CHECK-NEXT:    retq  
%a = load <16 x float>, <16 x float>* %ptr  
%mask = fptosi <16 x float> %a to <16 x i1>  
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer  
ret <16 x i16> %select  
}
define void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: mul256:
; CHECK-AVX512:  # %bb.0:
; CHECK-AVX512-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-AVX512-NEXT:  vmovdqa (%rsi), %ymm1
; CHECK-AVX512-NEXT:  vmovdqa (%rdx), %ymm2
; CHECK-AVX512-NEXT:  vpand %ymm5, %ymm4, %ymm4
; CHECK-AVX512-NEXT:  vpand %ymm5, %ymm1, %ymm1
; CHECK-AVX512-NEXT:  vpackuswb %ymm4, %ymm1, %ymm1
; CHECK-AVX512-NEXT:  vzeroupper

}
; CHECK-AVX512-NEXT:  retq

; CHECK-AVX512-NEXT:  retq

; CHECK-SEGLABEL:  mul256:
; CHECK-SEGLABEL:  # %bb.0:
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  v punckhbw {[*#]} ymm4 = ymm3[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  v punckhbw {[*#]} ymm5 = ymm1[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  v punckhbw {[*#]} ymm3 = ymm3[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  v punckhbw {[*#]} ymm1 = ymm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  v punckhbw {[*#]} ymm4 = ymm2[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  v punckhbw {[*#]} ymm5 = ymm0[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  v punckhbw {[*#]} ymm3 = ymm2[0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  v punckhbw {[*#]} ymm0 = ymm0[0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  vperm2b %ymm4, %ymm5, %ymm0
; CHECK-SEGLABEL:  CHECK-VBMI-NEXT:  vpmullw %ymm0, %ymm0, %ymm0
; CHECK-SEGLABEL:  vzeroupper
; CHECK-SEGLABEL:  retq

define void @mul512(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="512" {

% d = load <64 x i8>, <64 x i8>* %a
% e = load <64 x i8>, <64 x i8>* %b
% f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void
}

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; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} zmm2 =
ymm1[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,42,42,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT:  vunpckhbw {{.*#+}} zmm3 =
ymm0[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,42,42,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT:  vpmullw %zmm2, %zmm3, %zmm2

; CHECK-AVX512-NEXT:  vunpckhbw {{.*#+}} zmm1 =
ymm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,36,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT:  vunpckhbw {{.*#+}} zmm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,36,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT:  vpmullw %zmm1, %zmm0, %zmm0
; CHECK-AVX512-NEXT:  vpackuswb %zmm2, %zmm0, %zmm0
; CHECK-AVX512-NEXT:  vmovdqa64 %zmm0, (%rdx)
; CHECK-AVX512-NEXT:  vzeroupper
; CHECK-AVX512-NEXT:  retq

; CHECK-VBMI-LABEL: mul512:
; CHECK-VBMI:      # %bb.0:
; CHECK-VBMI-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-VBMI-NEXT:  vmovdqa64 (%rsi), %zmm1
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} zmm2 =
ymm1[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,42,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT:  vunpckhbw {{.*#+}} zmm3 =
ymm0[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,42,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-VBMI-NEXT:  vpermi2b %zmm2, %zmm0, %zmm1
; CHECK-VBMI-NEXT:  vmovdqa64 %zmm0, (%rdx)
; CHECK-VBMI-NEXT:  vzeroupper
; This threw an assertion at one point.
define <4 x i32> @mload_v4i32(<4 x i32> %trigger, <4 x i32>* %addr, <4 x i32> %dst) "min-legal-vector-width"="256" {
; CHECK-LABEL: mload_v4i32:
; CHECK: # %bb.0:
; CHECK-NEXT: vptestnmd %xmm0, %xmm0, %k1
; CHECK-NEXT: vpblendmd (%rdi), %xmm1, %xmm0 {%k1}
; CHECK-NEXT: retq
%mask = icmp eq <4 x i32> %trigger, zeroinitializer
%res = call <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* %addr, i32 4, <4 x i32> %mask, <4 x i32> %dst)
ret <4 x i32> %res
}
declare <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>*, i32, <4 x i1>, <4 x i32>)
define <16 x i32> @trunc_v16i64_v16i32(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i64_v16i32:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
; CHECK-NEXT: vmovdqa 96(%rdi), %ymm3
; CHECK-NEXT: vpmovqd %ymm0, %xmm0
; CHECK-NEXT: vpmovqd %ymm1, %xmm1
; CHECK-NEXT: vpmovqd %ymm2, %xmm2
; CHECK-NEXT: vpmovqd %ymm3, %xmm3
; CHECK-NEXT: vinserti128 $1, %ymm1, %ymm0, %ymm0
; CHECK-NEXT: vpmovqd %ymm2, %xmm1
; CHECK-NEXT: vinserti128 $1, %ymm2, %ymm1, %ymm1
; CHECK-NEXT: vpmovqd %ymm3, %xmm2
; CHECK-NEXT: vinserti128 $1, %ymm3, %ymm2, %ymm2
; CHECK-NEXT: retq
%a = load <16 x i64>, <16 x i64>* %x
%b = trunc <16 x i64> %a to <16 x i32>
ret <16 x i32> %b
}
define <16 x i8> @trunc_v16i64_v16i8(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i64_v16i8:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
define <16 x i64> @trunc_v16i32_v16i8(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
  ; CHECK-LABEL: trunc_v16i32_v16i8:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
  ; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
  ; CHECK-NEXT:  vpmovq %ymm1, %xmm1
  ; CHECK-NEXT:  vpmovq %ymm0, %xmm0
  ; CHECK-NEXT:  vpunpckdqu {{.*#*}} xmm0 = xmm0[0],xmm1[0]
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  %a = load <16 x i32>, <16 x i32>* %x
  %b = trunc <16 x i64> %a to <16 x i8>
  ret <16 x i8> %b
}

define <8 x i8> @trunc_v8i64_v8i8(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
  ; CHECK-LABEL: trunc_v8i64_v8i8:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
  ; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
  ; CHECK-NEXT:  vpmovq %ymm1, %xmm1
  ; CHECK-NEXT:  vpmovq %ymm0, %xmm0
  ; CHECK-NEXT:  vpunpckdqu {{.*#*}} xmm0 = xmm0[0],xmm1[0]
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  %a = load <8 x i64>, <8 x i64>* %x
  %b = trunc <8 x i64> %a to <8 x i8>
  ret <8 x i8> %b
}

define <8 x i16> @trunc_v8i64_v8i16(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
  ; CHECK-LABEL: trunc_v8i64_v8i16:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
  ; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
  ; CHECK-NEXT:  vpmovq %ymm1, %xmm1
  ; CHECK-NEXT:  vpmovq %ymm0, %xmm0
  ; CHECK-NEXT:  vpunpckdqu {{.*#*}} xmm0 = xmm0[0],xmm1[0]
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  %a = load <8 x i64>, <8 x i64>* %x
  %b = trunc <8 x i64> %a to <8 x i8>
  ret <8 x i8> %b
}
define <8 x i32> @trunc_v8i64_v8i32_zeroes(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v8i64_v8i32_zeroes:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vpsrlq $48, 32(%rdi), %ymm1
    ; CHECK-NEXT:  vpmovw %ymm1, %ymm0
    ; CHECK-NEXT:  vpmovw %ymm0, %xmm0
    ; CHECK-NEXT:  vpmovsq {{.*#+}} %ymm0 = [0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30]
    ; CHECK-NEXT:  vpermi2w 32(%rdi), %ymm1, %ymm0
    ; CHECK-NEXT:  retq
    %a = load <8 x i64>, <8 x i64>* %x
    %b = trunc <8 x i64> %a to <8 x i32>
    ret <8 x i32> %b
}

define <16 x i16> @trunc_v16i32_v16i16_zeroes(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v16i32_v16i16_zeroes:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vmovdqa (%rdi), %ymm1
    ; CHECK-NEXT:  vpmovw %ymm1, %ymm0
    ; CHECK-NEXT:  vpmovw %ymm0, %xmm0
    ; CHECK-NEXT:  vpmovsq {{.*#+}} %ymm0 = [0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30]
    ; CHECK-NEXT:  vpermi2w 32(%rdi), %ymm1, %ymm0
    ; CHECK-NEXT:  retq
    %a = load <16 x i32>, <16 x i32>* %x
    %b = lshr <16 x i32> %a, <i32 8, i32 8, i32 8, i32 8, i32 8, i32 8, i32 8, i32 8>
    %c = trunc <16 x i32> %b to <16 x i16>
    ret <16 x i16> %c
}

define <32 x i8> @trunc_v32i16_v32i8_zeroes(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_zeroes:
    ; CHECK-AVX512:       # %bb.0:
    ; CHECK-AVX512-NEXT:  vpsrlw $8, 32(%rdi), %ymm0
    ; CHECK-AVX512-NEXT:  vpmovw %ymm0, %ymm1
    ; CHECK-AVX512-NEXT:  vpackuswb %ymm0, %ymm1, %ymm0
    ; CHECK-AVX512-NEXT:  vpermq {{.*#+}} %ymm0 = ymm0[0,2,1,3]
    ; CHECK-AVX512-NEXT:  retq
    %a = load <32 x i16>, <32 x i16>* %x
    %b = trunc <32 x i16> %a to <32 x i8>
    ret <32 x i8> %b
}
define <8 x i32> @trunc_v8i64_v8i32_sign(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v8i64_v8i32_sign:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpsraq $48, 32(%rdi), %ymm0
    ; CHECK-NEXT:    vpsraq $48, (%rdi), %ymm1
    ; CHECK-NEXT:    vpmovqd %ymm1, %xmm1
    ; CHECK-NEXT:    vpmovqd %ymm0, %xmm0
    ; CHECK-NEXT:    vinserti128 $1, %xmm0, %ymm1, %ymm0
    ; CHECK-NEXT:    retq
    %a = load <8 x i64>, <8 x i64>* %x
    %b = ashr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>
    %c = trunc <8 x i64> %b to <8 x i32>
    ret <8 x i32> %c
}

define <16 x i16> @trunc_v16i32_v16i16_sign(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v16i32_v16i16_sign:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vmovdqa (%rdi), %ymm1
    ; CHECK-NEXT:    vmovdqa {{.*#*}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]
    ; CHECK-NEXT:    vpermi2w 32(%rdi), %ymm1, %ymm0
    ; CHECK-NEXT:    retq
    %a = load <16 x i32>, <16 x i32>* %x
    %b = ashr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16>
    %c = trunc <16 x i32> %b to <16 x i16>
    ret <16 x i16> %c
}

define <32 x i8> @trunc_v32i16_v32i8_sign(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_sign:
    ; CHECK-AVX512:       # %bb.0:
    ; CHECK-AVX512-NEXT:    vpsraw $8, 32(%rdi), %ymm0

define void @zext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {
  ; CHECK-LABEL: zext_v16i8_v16i64:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:   vpmovzxbw {{.*#+}} ymm1 =
  ; CHECK-NEXT:   xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,
  ; CHECK-NEXT:   xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero
  ; CHECK-NEXT:   vpmovzxwq {{.*#+}} ymm2 =
  ; CHECK-NEXT:   xmm2[0],zero,zero,xmm2[1],zero,zero,zero,xmm2[2],zero,zero,xmm2[3],zero,zero,xmm2[4],zero,zero,
  ; CHECK-NEXT:   vextracti128 $1, %ymm1, %xmm1
  ; CHECK-NEXT:   vpslufd {{.*#+}} xmm3 = xmm1[2,3,0,1]
  ; CHECK-NEXT:   vpmovzxwq {{.*#+}} ymm3 =
  ; CHECK-NEXT:   xmm3[0],zero,zero,zero,xmm3[1],zero,zero,zero,xmm3[2],zero,zero,xmm3[3],zero,zero,zero,
  ; CHECK-NEXT:   vpmovzxwq {{.*#+}} ymm1 =
  ; CHECK-NEXT:   xmm1[0],zero,zero,xmm1[1],zero,zero,zero,xmm1[2],zero,zero,zero,xmm1[3],zero,zero,zero,
  ; CHECK-NEXT:   vpmovzxwq {{.*#+}} ymm0 =
  ; CHECK-NEXT:   xmm0[0],zero,zero,zero,xmm0[1],zero,zero,zero,xmm0[2],zero,zero,zero,xmm0[3],zero,zero,zero,
  ; CHECK-NEXT:   vpmovzxbq {{.*#+}} ymm0 =
  ; CHECK-NEXT:   vpmovzxbw {{.*#+}} ymm1 =
  ; CHECK-NEXT:   vpmovzxbw {{.*#+}} ymm2 =
  ; CHECK-NEXT:   vpmovzxbw {{.*#+}} ymm3 =
  ; CHECK-NEXT:   vzeroupper
  ; CHECK-NEXT:   retq
  %a = zext <16 x i8> %x to <16 x i64>
  store <16 x i64> %a, <16 x i64>* %y
  ret void
}
define void @sext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: sext_v16i8_v16i64:
; CHECK:   % %bb.0:
; CHECK-NEXT: vmovdqa %ymm2, 64(%rdi)
; CHECK-NEXT: vmovdqa %ymm0, (%rdi)
; CHECK-NEXT: vmovdqa %ymm3, 96(%rdi)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = sext <16 x i8> %x to <16 x i64>
store <16 x i64> %x, <16 x i64>* %y
ret void
}

define void @vselect_split_v8i16_setcc(<8 x i16> %s, <8 x i16> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v8i16_setcc:
; CHECK:   % %bb.0:
; CHECK-NEXT: vmovdqa64 32(%rdi), %ymm3 {%k1}
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <8 x i64>, <8 x i64>* %p
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}

define void @vselect_split_v8i32_setcc(<8 x i32> %s, <8 x i32> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v8i32_setcc:
define void @vselect_split_v16i8_setcc(<16 x i8> %s, <16 x i8> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" { 
  ; CHECK-LABEL: vselect_split_v16i8_setcc:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa (%rsi), %ymm2
  ; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm3
  ; CHECK-NEXT:  vpcmpeqd %ymm1, %ymm0, %k1
  ; CHECK-NEXT:  kshiftr $4, %k1, %k2
  ; CHECK-NEXT:  vmovdqa64 32(%rdi), %ymm3 [%k2]
  ; CHECK-NEXT:  vmovdqa64 (%rdi), %ymm2 [%k1]
  ; CHECK-NEXT:  vmovdqa %ymm2, (%rdx)
  ; CHECK-NEXT:  vmovdqa %ymm3, 32(%rdx)
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  \%x = load <8 x i64>, <8 x i64>* %p
  \%y = load <8 x i64>, <8 x i64>* %q
  \%a = icmp eq <8 x i32> %s, %t
  \%b = select <8 x i1> \%a, <8 x i64> \%x, <8 x i64> \%y
  store <8 x i64> \%b, <8 x i64>* \%r
  ret void
}

define void @vselect_split_v16i16_setcc(<16 x i16> %s, <16 x i16> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" { 
  ; CHECK-LABEL: vselect_split_v16i16_setcc:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa (%rsi), %ymm2
  ; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm3
  ; CHECK-NEXT:  vpcmpeqb %xmm1, %xmm0, %k1
  ; CHECK-NEXT:  kshiftrw $8, %k1, %k2
  ; CHECK-NEXT:  vmovdqa32 32(%rdi), %ymm3 [%k2]
  ; CHECK-NEXT:  vmovdqa32 (%rdi), %ymm2 [%k1]
  ; CHECK-NEXT:  vmovdqa %ymm2, (%rdx)
  ; CHECK-NEXT:  vmovdqa %ymm3, 32(%rdx)
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  \%x = load <16 x i32>, <16 x i32>* %p
  \%y = load <16 x i32>, <16 x i32>* %q
  \%a = icmp eq <16 x i8> %s, %t
  \%b = select <16 x i1> \%a, <16 x i32> \%x, <16 x i32> \%y
  store <16 x i32> \%b, <16 x i32>* \%r
  ret void
}

define void @vselect_split_v16i16_setcc(<16 x i16> %s, <16 x i16> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" { 
  ; CHECK-LABEL: vselect_split_v16i16_setcc:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa (%rsi), %ymm2
  ; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm3
  ; CHECK-NEXT:  vpcmpeqw %ymm1, %ymm0, %k1
  ; CHECK-NEXT:  kshiftr $8, %k1, %k2
  ; CHECK-NEXT:  vmovdqa64 32(%rdi), %ymm3 [%k2]
  ; CHECK-NEXT:  vmovdqa64 (%rdi), %ymm2 [%k1]
  ; CHECK-NEXT:  vmovdqa %ymm2, (%rdx)
  ; CHECK-NEXT:  vmovdqa %ymm3, 32(%rdx)
define <16 x i8> @trunc_packus_v16i32_v16i8(<16 x i32>* %p) "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_packus_v16i32_v16i8:
; CHECK:
# %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vpackusdw 32(%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpmovuswb %ymm0, %xmm0
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <16 x i32>, <16 x i32>* %p
%b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255> %c = select <16 x i1> %a, <16 x i32> <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255> %d = icmp sgt <16 x i32> %c, zeroinitializer %e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zeroinitializer %f = trunc <16 x i32> %e to <16 x i8>
ret <16 x i8> %f
}

define void @trunc_packus_v16i32_v16i8_store(<16 x i32>* %p, <16 x i8>* %q) "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_packus_v16i32_v16i8_store:
; CHECK:
# %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vpackusdw 32(%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpmovuswb %ymm0, %xmm0
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <16 x i32>, <16 x i32>* %p
%b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%d = icmp sgt <16 x i32> %c, zeroinitializer
%e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zeroinitializer
%f = trunc <16 x i32> %e to <16 x i8>
store <16 x i8> %f, <16 x i8>* %q
ret void
}

define <64 x i1> @v64i1_argument_return(<64 x i1> %x) "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_argument_return:
; CHECK:
; CHECK-NEXT: retq
ret <64 x i1> %x
}

define void @v64i1_shuffle(<64 x i8>* %x, <64 x i8>* %y) "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_shuffle:
; CHECK:
; CHECK-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm0
; CHECK-NEXT: vptestnmb %ymm1, %ymm1, %k0
; CHECK-NEXT: kshiftrd $1, %k0, %k1
; CHECK-NEXT: movq $-3, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiflq $63, %k0, %k2
; CHECK-NEXT: kshifrq $62, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-5, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $3, %k0, %k2
; CHECK-NEXT: kshiflq $63, %k2, %k2
; CHECK-NEXT: kshifrq $61, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-9, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $5, %k0, %k2
; CHECK-NEXT: kshiflq $63, %k2, %k2
; CHECK-NEXT: kshifrq $60, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-17, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrq $59, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-33, %rax
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $4, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $58, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-65, %rax
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $7, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $57, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-129, %rax
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $6, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $55, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-257, %rax # imm = 0xFEFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $9, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $54, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-513, %rax # imm = 0xFDFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $8, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $53, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-1025, %rax # imm = 0xFBFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $11, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $52, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-2049, %rax # imm = 0xF7FF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $10, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $52, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-4097, %rax # imm = 0xEFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $13, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $51, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-1893, %rax # imm = 0xDFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $12, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $49, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-16385, %rax # imm = 0xBFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $15, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $48, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-32769, %rax # imm = 0xFFFF7FFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $14, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $47, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-65537, %rax # imm = 0xFFFEFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $17, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $46, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-131073, %rax # imm = 0xFFFFDFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $16, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $45, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-262145, %rax # imm = 0xFFFFBFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $19, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $45, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-524289, %rax # imm = 0xFFF7FFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $18, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $44, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-1048577, %rax # imm = 0xFFEFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $21, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $43, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-2097153, %rax # imm = 0xFFDFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $20, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $42, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-4194305, %rax # imm = 0xFFFBBBBB
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $23, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $41, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-8388609, %rax # imm = 0xFF7FFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $22, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $40, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-16777217, %rax # imm = 0xFEFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $25, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $39, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-33554433, %rax # imm = 0xFDFFFFFF
; CHECK-NEXT: kmovq %rax, %k2

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; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftr $24, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $38, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-67108865, %rax # imm = 0xFBFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $27, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $37, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-134217729, %rax # imm = 0xFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftr $26, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $36, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-268435457, %rax # imm = 0xEFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftr $29, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $35, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-536870913, %rax # imm = 0xDFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftr $28, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $34, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-1073741825, %rax # imm = 0xBFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftr $31, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $33, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movabsq $-2147483649, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftr $30, %k0, %k2
; CHECK-NEXT:  kshiftlq $32, %k0, %k0
; CHECK-NEXT:  kshiftrq $32, %k0, %k0
; CHECK-NEXT:  korq %k0, %k2, %k0
; CHECK-NEXT:  movabsq $-549755813889, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $6, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $24, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-1099511627777, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $9, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $23, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-2199023255553, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $8, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $22, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-4398046511105, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $11, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $21, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-8796093022209, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $10, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $20, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-1759218604417, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $13, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $19, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-35184372088833, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $12, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $18, %k2, %k2

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entry:
%a = load <64 x i8>, <64 x i8>* %x
%b = icmp eq <64 x i8> %a, zeroinitializer
%shuf = shufflevector <64 x i1> %b, <64 x i1> undef, <64 x i32> <i32 1, i32 0, i32 3, i32 2, i32 5, i32 4, i32 7, i32 6, i32 9, i32 8, i32 11, i32 10, i32 13, i32 12, i32 15, i32 14, i32 17, i32 16, i32 19, i32 18, i32 21, i32 20, i32 23, i32 22, i32 25, i32 24, i32 27, i32 26, i32 29, i32 28, i32 31, i32 30, i32 33, i32 32, i32 35, i32 34, i32 37, i32 36, i32 39, i32 38, i32 41, i32 40, i32 43, i32 42, i32 45, i32 44, i32 47, i32 46, i32 49, i32 48, i32 51, i32 50, i32 53, i32 52, i32 55, i32 54, i32 57, i32 56, i32 59, i32 58, i32 61, i32 60, i32 63, i32 62>
call void @llvm.masked.store.v64i8.p0v64i8(<64 x i8> %a, <64 x i8>* %y, %shuf)
ret void
@mem64.dst = global i64 0, align 8
@mem64.src = global i64 0, align 8
define i32 @v64i1_inline_asm() "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_inline_asm:
; CHECK:
# %bb.0:
; CHECK-NEXT: kmovq {{.*}}(%rip), %k0
; CHECK-NEXT: #APP
; CHECK-NEXT: #NO_APP
; CHECK-NEXT: kmovq %k0, {{.*}}(%rip)
; CHECK-NEXT: movl -{{[0-9]+}}(%rsp), %eax
; CHECK-NEXT: retq
%1 = alloca i32, align 4
%2 = load i64, i64* @mem64_src, align 8
%3 = call i64 asm "", "=k,k,~{dirflag},~{fpsr},~{flags}"(i64 %2)
store i64 %3, i64* @mem64_dst, align 8
%4 = load i32, i32* %1, align 4
ret i32 %4
}
define void @cmp_v8i64_sext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-vectorwidth"="256" {
; CHECK-LABEL: cmp_v8i64_sext:
; CHECK:
# %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT: vpcmpgtq 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT: vpcmpgtq (%rdi), %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %xptr
%y = load <8 x i64>, <8 x i64>* %yptr
%cmp = icmp slt <8 x i64> %x, %y
%ext = sext <8 x i1> %cmp to <8 x i64>
store <8 x i64> %ext, <8 x i64>* %zptr
ret void
}
define void @cmp_v8i64_zext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-vectorwidth"="256" {
; CHECK-LABEL: cmp_v8i64_zext:
; CHECK:
# %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT: vpcmpgtq 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT: vpcmpgtq (%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpsrlq $63, %ymm1, %ymm1
; CHECK-NEXT: vpsrlq $63, %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)

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define <16 x i8> @var_rotate_v16i8(<16 x i8> %a, <16 x i8> %b) nounwind "min-legal-vector-width"="256" {;
  CHECK-LABEL: var_rotate_v16i8:
  CHECK:
  # %bb.0:
  CHECK-NEXT:  vmovdqa {{.*}} xmm2 = [8,8,8,8,8,8,8,8,8,8,8,8,8,8,8,8]
  CHECK-NEXT:  vpsubb %xmm1, %xmm2, %xmm2
  CHECK-NEXT:  vpmovzxbw {{.*}} ymm1 =
    xmm1[0],zero,xmm1[1],zero,xmm1[2],zero,xmm1[3],zero,xmm1[4],zero,xmm1[5],zero,xmm1[6],zero,xmm1[7],zero,
    xmm1[8],zero,xmm1[9],zero,xmm1[10],zero,xmm1[11],zero,xmm1[12],zero,xmm1[13],zero,xmm1[14],zero,xmm1[15],zero
  CHECK-NEXT:  vpmovzxvw {{.*}} ymm0 =
    xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,
    xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero
  CHECK-NEXT:  vpsllw %ymm0, %ymm2
  CHECK-NEXT:  vpsrlw %ymm0, %ymm3
  CHECK-NEXT:  vpternlogq $216, {{.*}}(%rip), %ymm2, %ymm3
  CHECK-NEXT:  vpsllw %ymm1, %ymm1
  CHECK-NEXT:  vpmovzxvw {{.*}} ymm2 =
    xmm2[0],zero,xmm2[1],zero,xmm2[2],zero,xmm2[3],zero,xmm2[4],zero,xmm2[5],zero,xmm2[6],zero,xmm2[7],zero,
    xmm2[8],zero,xmm2[9],zero,xmm2[10],zero,xmm2[11],zero,xmm2[12],zero,xmm2[13],zero,xmm2[14],zero,xmm2[15],zero
  CHECK-NEXT:  vpsrlw %ymm0, %ymm2
  CHECK-NEXT:  vpor %ymm0, %ymm1, %ymm1
  CHECK-NEXT:  vpmovwb %ymm0, %ymm0
  CHECK-NEXT:  vzeroupper
  CHECK-NEXT:  retq
%
\%b8 = sub <16 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, \%b
\%shl = shl <16 x i8> \%a, \%b
\%lsr = lshr <16 x i8> \%a, \%b8
\%or = or <16 x i8> \%shl, \%lsr
ret <16 x i8> \%or
}
define <32 x i8> @var_rotate_v32i8(<32 x i8> %a, <32 x i8> %b) nounwind "min-legal-vector-width"="256" {;
  CHECK-LABEL: var_rotate_v32i8:
  CHECK:
  # %bb.0:
  CHECK-NEXT:  vpsllw $4, %ymm0, %ymm2
  CHECK-NEXT:  vpsrlw $4, %ymm0, %ymm3
  CHECK-NEXT:  vpternlogq $216, {{.*}}(%rip), %ymm2, %ymm3
  CHECK-NEXT:  vpsllw $5, %ymm1, %ymm1

define <32 x i8> @splatvar_rotate_v32i8(<32 x i8> %a, <32 x i8> %b) nounwind "min-legal-vector-width"="256"
{

    vpbroadcastb %xmm1, %xmm1
    vpand {{.*}}(%rip), %xmm1, %xmm1
    vmovdqa {{.*#+}} xmm2 = xmm1[0],zero,zero,zero,zero,zero,zero,zero,xmm1[1],zero,zero,zero,zero,zero,zero,zero
    vpsubb %xmm1, %xmm4, %xmm1
    vpcmpeqd %xmm4, %xmm4, %xmm4
    vpbroadcastb %xmm2, %ymm2
    vpmovzxbq {{.*#+}} xmm1 = xmm1[0],zero,zero,zero,zero,zero,zero,zero,xmm1[1],zero,zero,zero,zero,zero,zero,zero
     
}

%or = or <32 x i8> %shl, %lshr
ret <32 x i8> %or

define <32 x i8> @constant_rotate_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {;
CHECK-AVX512-LABEL: constant_rotate_v32i8:
CHECK-AVX512: # %bb.0:
CHECK-AVX512-NEXT: vpsllw $4, %ymm0, %ymm1
CHECK-AVX512-NEXT: vpand {{.*}}(%rip), %ymm1, %ymm1
CHECK-AVX512-NEXT: vbroadcasti128 {{.*##+}} ymm2 = [8192,24640,41088,57536,57344,41152,24704,8256,8192,24640,41088,57536,57344,41152,24704,8256]
CHECK-AVX512-NEXT: # ymm2 = mem[0,1,0,1]
CHECK-AVX512-NEXT: vblendvb %ymm2, %ymm1, %ymm0, %ymm1
CHECK-AVX512-NEXT: vpsllw $2, %ymm1, %ymm3
CHECK-AVX512-NEXT: vpand {{.*}}(%rip), %ymm3, %ymm3
CHECK-AVX512-NEXT: vpsllw $2, %ymm3, %ymm2
CHECK-AVX512-NEXT: vpand {{.*}}(%rip), %ymm2, %ymm2
CHECK-AVX512-NEXT: vpaddl %ymm2, %ymm1, %ymm1, %ymm1
CHECK-AVX512-NEXT: vpsllw $2, %ymm2, %ymm3
CHECK-AVX512-NEXT: vpand {{.*}}(%rip), %ymm3, %ymm3
CHECK-AVX512-NEXT: vpsllw $2, %ymm3, %ymm2
CHECK-AVX512-NEXT: vblendvb %ymm2, %ymm2, %ymm1
CHECK-AVX512-NEXT: vpsllw %ymm0, %ymm0
CHECK-AVX512-NEXT: vpunpcklbw {{.*##+}} ymm0 = ymm0[8],ymm2[8],ymm0[9],ymm2[9],ymm0[10],ymm2[10],ymm0[11],ymm2[11],ymm0[12],ymm2[12],ymm0[13],ymm2[13],ymm0[14],ymm2[14],ymm0[15],ymm2[15],ymm0[24],ymm2[24],ymm0[25],ymm2[25],ymm0[26],ymm2[26],ymm0[27],ymm2[27],ymm0[28],ymm2[28],ymm0[29],ymm2[29],ymm0[30],ymm2[30],ymm0[31],ymm2[31]
CHECK-AVX512-NEXT: vpsllw {{.*}}(%rip), %ymm3, %ymm3
CHECK-AVX512-NEXT: vpsrlw $8, %ymm3, %ymm3
CHECK-AVX512-NEXT: vpunpckhbw {{.*##+}} ymm3 = ymm0[8],ymm2[8],ymm0[9],ymm2[9],ymm0[10],ymm2[10],ymm0[11],ymm2[11],ymm0[12],ymm2[12],ymm0[13],ymm2[13],ymm0[14],ymm2[14],ymm0[15],ymm2[15],ymm0[24],ymm2[24],ymm0[25],ymm2[25],ymm0[26],ymm2[26],ymm0[27],ymm2[27],ymm0[28],ymm2[28],ymm0[29],ymm2[29],ymm0[30],ymm2[30],ymm0[31],ymm2[31]
CHECK-AVX512-NEXT: vpsllw {{.*}}(%rip), %ymm3, %ymm3
CHECK-AVX512-NEXT: vpsrlw $8, %ymm3, %ymm3
CHECK-AVX512-NEXT: vpackuswb %ymm3, %ymm0, %ymm0
CHECK-AVX512-NEXT: vpor %ymm0, %ymm1, %ymm0
CHECK-AVX512-NEXT: retq
;
CHECK-VBMI-LABEL: constant_rotate_v32i8:
CHECK-VBMI: # %bb.0:
CHECK-VBMI-NEXT: vpsllw $4, %ymm0, %ymm1
CHECK-VBMI-NEXT: vpand {{.*}}(%rip), %ymm1, %ymm1
CHECK-VBMI-NEXT: vbroadcasti128 {{.*##+}} ymm2 = [8192,24640,41088,57536,57344,41152,24704,8256,8192,24640,41088,57536,57344,41152,24704,8256]
CHECK-VBMI-NEXT: # ymm2 = mem[0,1,0,1]
CHECK-VBMI-NEXT: vblendvb %ymm2, %ymm1, %ymm0, %ymm1
CHECK-VBMI-NEXT: vpsllw $2, %ymm1, %ymm3
CHECK-VBMI-NEXT: vpand {{.*}}(%rip), %ymm3, %ymm3
; CHECK-VDIM-NEXT:  vpaddb %ymm2, %ymm2, %ymm2
; CHECK-VDIM-NEXT:  vpblendvb %ymm2, %ymm3, %ymm1, %ymm1
; CHECK-VDIM-NEXT:  vpaddb %ymm1, %ymm1, %ymm3
; CHECK-VDIM-NEXT:  vpaddb %ymm2, %ymm2, %ymm2
; CHECK-VDIM-NEXT:  vpblendvb %ymm2, %ymm3, %ymm1, %ymm1
; CHECK-VDIM-NEXT:  vpxor %xmm2, %xmm2, %xmm2
; CHECK-VDIM-NEXT:  vpunpckhbw {{.*#+}} ymm3 = ymm0[8],ymm2[8],ymm0[9],ymm2[9],ymm0[10],ymm2[10],ymm0[11],ymm2[11],ymm0[12],ymm2[12],ymm0[13 ],ymm2[13],ymm0[14],ymm2[14],ymm0[15],ymm2[15],ymm0[24],ymm2[24],ymm0[25],ymm2[25],ymm0[26],ymm2[26],ymm0[27],ymm2[27],ymm0[28],ymm2[28],ymm0[29],ymm2[29],ymm0[30],ymm2[30],ymm0[31],ymm2[31]
; CHECK-VDIM-NEXT:  vpsllw {{.*}}(%rip), %ymm3, %ymm3
; CHECK-VDIM-NEXT:  vpunpcklbw {{.*#+}} ymm0 = ymm0[0],ymm2[0],ymm0[1],ymm2[1],ymm0[2],ymm2[2],ymm0[3],ymm2[3],ymm0[4],ymm2[4],ymm0[5],ymm2[5],ymm0[6],ymm2[6],ymm0[7],ymm2[7],ymm0[16],ymm2[16],ymm0[17],ymm2[17],ymm0[18],ymm2[18],ymm0[19],ymm2[19],ymm0[20],ymm2[20],ymm0[21],ymm2[21],ymm0[22],ymm2[22],ymm0[23],ymm2[23]
; CHECK-VDIM-NEXT:  vpsllw {{.*}}(%rip), %ymo0, %ymn0
; CHECK-VDIM-NEXT:  vpsllw {{.*}}(%rip), %ymm0, %ymm0
; CHECK-VDIM-NEXT:  vpsllw %4, %ymo0, %ymm1
; CHECK-VDIM-NEXT:  vpsrlw $4, %ymm0, %ymn0
; CHECK-VDIM-NEXT:  vpternlogq $216, {{.*}}(%rip), %ymm1, %ymm0
; CHECK-VDIM-NEXT:  retq

%shl = shl <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 9, i8 10, i8 11, i8 12, i8 13, i8 14, i8 15, i8 16, i8 17, i8 18, i8 19, i8 20, i8 21, i8 22, i8 23, i8 24, i8 25, i8 26, i8 27, i8 28, i8 29, i8 30, i8 31,
%lshr = lshr <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 9, i8 10, i8 11, i8 12, i8 13, i8 14, i8 15, i8 16, i8 17, i8 18, i8 19, i8 20, i8 21, i8 22, i8 23, i8 24, i8 25, i8 26, i8 27, i8 28, i8 29, i8 30, i8 31, i8 32
%or = or %shl, %lshr
ret <32 x i8> %or

define <32 x i8> @splatconstant_rotate_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL:  splatconstant_rotate_v32i8:
; CHECK-NEXT:  # %bb.0:
; CHECK-NEXT:  vpsllw %4, %ymm0, %ymm1
; CHECK-NEXT:  vpsrlw $4, %ymm0, %ymm0
; CHECK-NEXT:  vpternlogq $216, {{.*}}(%rip), %ymm1, %ymm0
; CHECK-NEXT:  retq

%shl = shl <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 9, i8 10, i8 11, i8 12, i8 13, i8 14, i8 15, i8 16, i8 17, i8 18, i8 19, i8 20, i8 21, i8 22, i8 23, i8 24, i8 25, i8 26, i8 27, i8 28, i8 29, i8 30, i8 31, i8 32
%lshr = lshr <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 9, i8 10, i8 11, i8 12, i8 13, i8 14, i8 15, i8 16, i8 17, i8 18, i8 19, i8 20, i8 21, i8 22, i8 23, i8 24, i8 25, i8 26, i8 27, i8 28, i8 29, i8 30, i8 31, i8 32
%or = or %shl, %lshr
ret <32 x i8> %or
}

define <32 x i8> @splatconstant_rotate_mask_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL:  splatconstant_rotate_mask_v32i8:
; CHECK-NEXT:  # %bb.0:
; CHECK-NEXT:  vpsllw %4, %ymm0, %ymm1
; CHECK-NEXT:  vpsrlw $4, %ymm0, %ymm0
; CHECK-NEXT:  vpternlogq $216, {{.*}}(%rip), %ymm1, %ymm0
; CHECK-NEXT:  retq

%shl = shl <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 9, i8 10, i8 11, i8 12, i8 13, i8 14, i8 15, i8 16, i8 17, i8 18, i8 19, i8 20, i8 21, i8 22, i8 23, i8 24, i8 25, i8 26, i8 27, i8 28, i8 29, i8 30, i8 31, i8 32
%lshr = lshr <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 9, i8 10, i8 11, i8 12, i8 13, i8 14, i8 15, i8 16, i8 17, i8 18, i8 19, i8 20, i8 21, i8 22, i8 23, i8 24, i8 25, i8 26, i8 27, i8 28, i8 29, i8 30, i8 31, i8 32
%or = or %shl, %lshr
ret <32 x i8> %or
}
; CHECK-NEXT:  vpsllw $4, %ymm0, %ymm1
; CHECK-NEXT:  vpsrlw $4, %ymm0, %ymm0
; CHECK-NEXT:  vpternlogq $216, [%.r]([%.rip]), %ymm1, %ymm0
; CHECK-NEXT:  vpand [%.r]([%.rip]), %ymm0, %ymm0
; CHECK-NEXT:  retq

%shl = shl <32 x i8> %a, <i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4>
%lshr = lshr <32 x i8> %a, <i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4>
%rmask = and <32 x i8> %lshr, <i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55>
%lmask = and <32 x i8> %shl, <i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33>
%or = or <32 x i8> %lmask, %rmask
ret <32 x i8> %or
}

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add_lldb_library(lldbPluginObjectContainerBSDArchive PLUGIN
ObjectContainerBSDArchive.cpp

LINK_LIBS
  lldbCore
  lldbHost
  lldbSymbol

LINK_COMPONENTS
  Support

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target triple = "hexagon"

%struct.0 = type { i8*, i8, %union.anon.0 }
%union.anon.0 = type { i8* }

define hidden fastcc void @fred() unnamed_addr #0 {
  entry:
  br i1 undef, label %while.end, label %while.body.lr.ph
while.body.lr.ph: ; preds = %entry
    br label %while.body

while.body: ; preds = %exit.2, %while.body.lr.ph
    %lsr.iv = phi %struct.0* [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
    switch i32 undef, label %exit [ 
      i32 1, label %sw.bb.i
      i32 2, label %sw.bb3.i
    ]

sw.bb.i: ; preds = %while.body
    unreachable

sw.bb3.i: ; preds = %while.body
    unreachable

exit: ; preds = %while.body
    switch i32 undef, label %exit.2 [ 
      i32 1, label %sw.bb.i17
      i32 2, label %sw.bb3.i20
    ]

sw.bb.i17: ; preds = %exit
    %0 = bitcast %struct.0* %lsr.iv to i32*
    %1 = load i32, i32* %0, align 4
    unreachable

sw.bb3.i20: ; preds = %exit
    %2 = bitcast %struct.0* %lsr.iv to i8**
    %3 = load i8*, i8** %2, align 4
    unreachable

exit.2: ; preds = %exit
    %cgep22 = getelementptr %struct.0, %struct.0* %lsr.iv, i32 1
    br label %while.body

while.end: ; preds = %entry
    ret void
}
Open Source Used In Branch Migration Tool Spirit
; IS__TUNIT_OPM-LABEL: define [{[^@]+}]{@avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__TUNIT_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM-LABEL: define [{[^@]+}]{@avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP0]])
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM-LABEL: define [{[^@]+}]{@avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nonfree nonnull writeonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void

define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]]) #1 {


bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}


This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {


bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}
open source used in branch migration tool spirit
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store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #0 {

; NOT_TUNIT_NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64)
[ARG:.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:.*]])
; NOT_TUNIT_NPM-NEXT: bb:
; NOT_TUNIT_NPM-NEXT: [[TMP:.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: ret void
;
; IS_TUNIT_NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS_TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64)
[ARG:.*]], <8 x i64> [[TMP0:.*]])
; IS_TUNIT_NPM-NEXT: bb:
; IS_TUNIT_NPM-NEXT: [[ARG1_PRIV:.*]] = alloca <8 x i64>, align 64
; IS_TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS_TUNIT_NPM-NEXT: [[TMP:.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_TUNIT_NPM-NEXT: ret void

bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {

; IS_TUNIT_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS_TUNIT_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:.*]])
; IS_TUNIT_OPM-NEXT: bb:
; IS_TUNIT_OPM-NEXT: [[TMP:.*]] = alloca <8 x i64>, align 64
; IS_TUNIT_OPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_TUNIT_OPM-NEXT: [[TMP:.*]] = load <8 x i64>, <8 x i64>* [[ARG]], align 64
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS_TUNIT_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* nocapture nofree nonnull
dereferenceable(64) dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64
dereferenceable(64) [[TMP]])
; IS__UNIT_OPM-NEXT:   [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__UNIT_OPM-NEXT:   store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__UNIT_OPM-NEXT:   ret void

; IS__UNIT_NPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__UNIT_NPM-SAME:   (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; IS__UNIT_NPM-NEXT:   bb:
; IS__UNIT_NPM-NEXT:   [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__UNIT_NPM-NEXT:   [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__UNIT_NPM-NEXT:   [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__UNIT_NPM-NEXT:   call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__UNIT_NPM-NEXT:   [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__UNIT_NPM-NEXT:   call fastcc void
   @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* nocapture nonnull
   align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]])
; IS__UNIT_NPM-NEXT:   [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__UNIT_NPM-NEXT:   store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__UNIT_NPM-NEXT:   ret void

; IS__CGSCC_OPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__CGSCC_OPM-SAME:   (<8 x i64>* nocapture writeonly 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_OPM-NEXT:   bb:
; IS__CGSCC_OPM-NEXT:   [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:   [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:   [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT:   call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT:   call fastcc void
   @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* nocapture nonnull
   align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nonnull readonly align 64
dereferenceable(64) [[TMP]])
; IS__CGSCC_OPM-NEXT:   [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT:   store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT:   ret void

; IS__CGSCC_NPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__CGSCC_NPM-SAME:   (<8 x i64>* nocapture writeonly 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT:   bb:
; IS__CGSCC_NPM-NEXT:   [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:   [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:   [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT:   call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT:   call fastcc void
   @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* nocapture nonnull
   align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree
   nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]])
; IS__CGSCC_NPM-NEXT:   [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT:   store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT:   ret void

; IS__CGSCC_NPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__CGSCC_NPM-SAME:   (<8 x i64>* nocapture writeonly 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT:   bb:
; IS__CGSCC_NPM-NEXT:   [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:   [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:   [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT:   call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT:   call fastcc void
   @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree
   nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree
   nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_NPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT:  ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
    bb:
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
    bb:
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ret void
}
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocomm nopref nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocomm nopref nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 {
;
; NOT_TUNIT_NPM-LABEL: define
{{[@]+}} @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocomm nopref nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocomm nopref nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; NOT_TUNIT_NPM-NEXT: bb:
; NOT_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: ret void

; IS_TUNIT_NPM-LABEL: define
{{[@]+}} @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS_TUNIT_NPM-SAME: (<8 x i64>* noalias nocomm nopref nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* noalias nocomm nopref nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; IS_TUNIT_NPM-NEXT: bb:
; IS_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_TUNIT_NPM-NEXT: ret void

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bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
  IS__TUNIT_OPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal256_prefer256 IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
  IS__TUNIT_OPM-NEXT: bb:
    IS__TUNIT_OPM-NEXT: [[TMP:.%.*]] = alloca <8 x i64>, align 32
    IS__TUNIT_OPM-NEXT: [[TMP2:.%.*]] = alloca <8 x i64>, align 32
    IS__TUNIT_OPM-NEXT: [[TMP3:.%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  IS__TUNIT_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nonnull readonly align 64 dereferenceable(64) [[TMP]])
  IS__TUNIT_OPM-NEXT: [[TMP4:.%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
  IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  IS__TUNIT_OPM-NEXT: ret void
  IS__CGSCC_OPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal256_prefer256 IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
  IS__CGSCC_OPM-NEXT: bb:
    IS__CGSCC_OPM-NEXT: [[TMP:.%.*]] = alloca <8 x i64>, align 32
    IS__CGSCC_OPM-NEXT: [[TMP2:.%.*]] = alloca <8 x i64>, align 32
    IS__CGSCC_OPM-NEXT: [[TMP3:.%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  IS__CGSCC_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* noalias nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nonnull readonly align 64 dereferenceable(64) [[TMP]])
  IS__CGSCC_OPM-NEXT: [[TMP4:.%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
  IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  IS__CGSCC_OPM-NEXT: ret void
  IS__CGSCC_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* noalias nocapture nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]])
  IS__CGSCC_OPM-NEXT: bb:
    IS__CGSCC_OPM-NEXT: [[TMP:.%.*]] = alloca <8 x i64>, align 32
    IS__CGSCC_OPM-NEXT: [[TMP2:.%.*]] = alloca <8 x i64>, align 32
    IS__CGSCC_OPM-NEXT: [[TMP3:.%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])

; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void

; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])

; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void

; bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #3 {
;
; NOT_TUNIT_NPM-LABEL: define 
({[^@]+}) @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; NOT_TUNIT_NPM-NEXT: bb:
; NOT_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: ret void
define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64> * %arg) #4 {
  %tmp = load <8 x i64>, <8 x i64> * %arg
  store <8 x i64> %tmp, <8 x i64> * %arg
  ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64> * %arg) #4 {
  %tmp = load <8 x i64>, <8 x i64> * %arg
  store <8 x i64> %tmp, <8 x i64> * %arg
  ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64> * %arg) #4 {
  %tmp = load <8 x i64>, <8 x i64> * %arg
  store <8 x i64> %tmp, <8 x i64> * %arg
  ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64> * %arg) #4 {
  %tmp = load <8 x i64>, <8 x i64> * %arg
  store <8 x i64> %tmp, <8 x i64> * %arg
  ret void
}
; IS__TUNIT_NPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT:  ret void
;
; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
  (8 x i64>* nocapture nonnull writeonly 2 dereferenceable(64) [[ARG:.%*]])
  IS__CGSCC_OPM-NEXT: bb:
  ; IS__CGSCC_OPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; IS__CGSCC_OPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; IS__CGSCC_OPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; IS__CGSCC_OPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; IS__CGSCC_OPM-NEXT:  call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* nocapture nonfree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nonnull readonly align 64 dereferenceable(64) [[TMP]])
  ; IS__CGSCC_OPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
  ; IS__CGSCC_OPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; IS__CGSCC_OPM-NEXT:  ret void
;
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
  (8 x i64>* nocapture nonnull writeonly 2 dereferenceable(64) [[ARG:.%*]])
  IS__CGSCC_NPM-NEXT: bb:
  ; IS__CGSCC_NPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; IS__CGSCC_NPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; IS__CGSCC_NPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; IS__CGSCC_NPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  ; IS__CGSCC_NPM-NEXT:  call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
  ; IS__CGSCC_NPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
  ; IS__CGSCC_NPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; IS__CGSCC_NPM-NEXT:  ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #4 {

; NOT_TUNIT_NPM-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64))
[[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; NOT_TUNIT_NPM-NEXT: bb:
; NOT_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: ret void
;
; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64))
[[ARG:%.*]], <8 x i64> [[TMP0:%.*]])
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {

; IS__TUNIT_OPM-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_OPM-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {

; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[ARG:%.*]], i8 0, i64 32, i1 false)
; IS__TUNIT_NPM-NEXT: bb:
@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__TUNIT_OPM-NEXT: call fastcc void
@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])

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%tmp = alloca <8 x i64>, align 32

bb:

%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*

call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [%tmp3], i8 0, i64 32, i1 false)

%tmp0 = load <8 x i64>, <8 x i64>* %tmp, align 64

call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nonfree nonnull writeonly align 64 dereferenceable(64) [%tmp2], <8 x i64>* [%tmp0])

%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 64
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

bb:

%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*

call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [%tmp3], i8 0, i64 32, i1 false)

call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nonfree nonnull writeonly align 64 dereferenceable(64) [%tmp2], <8 x i64>* noalias nocapture nonfree nonnull readonly align 64 dereferenceable(64) [%tmp])

%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 64
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

bb:

%tmp = alloca <8 x i64>, align 32

%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }

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; RUN: llc -O3 -mtriple=powerpc-unknown-linux-gnu -mcpu=e500 -mattr=spe < %s | FileCheck %s

; PowerPC SPE is a rare in-tree target that has the FP_TO_SINT node marked
; as Legal.

; Verify that fptosi(42.1) isn't simplified when the rounding mode is
; unknown.
; Verify that no gross errors happen.
; CHECK-LABEL: @f20
; COMMON: cfdctsiz
define i32 @f20(double %a) strictfp {
entry:
%result = call i32 @llvm.experimental.constrained.fptosi.i32.f64(double 42.1,
    metadata !"fpexcept.strict")
    
strictfp

ret i32 %result
}

@llvm.fp.env = thread_local global i8 zeroinitializer, section "llvm.metadata"
declare i32 @llvm.experimental.constrained.fptosi.i32.f64(double, metadata)

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==============================================================================
; NOTE: Assertions have been autogenerated by utils/update_analyze_test_checks.py
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx2 | FileCheck %s --check-prefixes=CHECK,VEC256,AVX
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC256,AVX512VL256
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,-prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC512,AVX512VL512
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC512,AVX512VL512
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,-prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC512,AVX512VL512
define void @zext256() "min-legal-vector-width"="256" {
 ; VEC256-LABEL: 'zext256'
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x i32>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

 ; AVX512VL512-LABEL: 'zext256'
 ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
 ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
 ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
 ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
 ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
 ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

 ; SKX512-LABEL: 'zext256'
 ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
 ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
 ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
 ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
 ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
 ; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

 ;
 ; %A = zext <8 x i16> undef to <8 x i64>
 %B = zext <8 x i32> undef to <8 x i64>
 %C = zext <16 x i8> undef to <16 x i32>
 %D = zext <16 x i16> undef to <16 x i32>
 %E = zext <32 x i8> undef to <32 x i16>
 ret void
}

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define void @zext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'zext512'
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL256-LABEL: 'zext512'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'zext512'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'zext512'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
define void @sext256() "min-legal-vector-width"="256" {
    %A = zext <8 x i16> undef to <8 x i64>
    %B = zext <8 x i32> undef to <8 x i64>
    %C = zext <16 x i8> undef to <16 x i32>
    %D = zext <16 x i16> undef to <16 x i32>
    %E = zext <32 x i8> undef to <32 x i16>
    ret void
}

define void @sext256() "min-legal-vector-width"="256" {
    %A = zext <8 x i16> undef to <8 x i64>
    %B = zext <8 x i32> undef to <8 x i64>
    %C = zext <16 x i8> undef to <16 x i32>
    %D = zext <16 x i16> undef to <16 x i32>
    %E = zext <32 x i8> undef to <32 x i16>
    ret void
}

define void @sext256() "min-legal-vector-width"="256" {
    %A = zext <8 x i16> undef to <8 x i64>
    %B = zext <8 x i32> undef to <8 x i64>
    %C = zext <16 x i8> undef to <16 x i32>
    %D = zext <16 x i16> undef to <16 x i32>
    %E = zext <32 x i8> undef to <32 x i16>
    ret void
}

define void @sext256() "min-legal-vector-width"="256" {
    %A = zext <8 x i16> undef to <8 x i64>
    %B = zext <8 x i32> undef to <8 x i64>
    %C = zext <16 x i8> undef to <16 x i32>
    %D = zext <16 x i16> undef to <16 x i32>
    %E = zext <32 x i8> undef to <32 x i16>
    ret void
}
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; SKX512-LABEL: 'sext256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

define void @sext512() "min-legal-vector-width"="512" {
    %A = sext <8 x i8> undef to <8 x i64>
    %B = sext <8 x i16> undef to <8 x i64>
    %C = sext <8 x i32> undef to <8 x i64>
    %D = sext <16 x i8> undef to <16 x i32>
    %E = sext <16 x i16> undef to <16 x i32>
    %F = sext <32 x i8> undef to <32 x i16>
    ret void
}

%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

define void @trunc256() "min-legal-vector-width"="256" {
  ; AVX-LABEL: 'trunc256'
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
  ; AVX512VL256-LABEL: 'trunc256'
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
  ; AVX512VL512-LABEL: 'trunc256'
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
  ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
define i32 @zext256_vXi1() "min-legal-vector-width"="256" {  
  %A = trunc <8 x i64> undef to <8 x i32>
  %B = trunc <8 x i64> undef to <8 x i16>
  %C = trunc <8 x i64> undef to <8 x i8>
  %D = trunc <16 x i32> undef to <16 x i16>
  %E = trunc <16 x i32> undef to <16 x i8>
  %F = trunc <32 x i16> undef to <32 x i8>
  ret void
}
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL256-LABEL: 'zext256_vXi1'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i64 = zext <16 x i1> undef to <16 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 12 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 12 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 25 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 50 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL512-LABEL: 'zext256_vXi1'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i8 = zext <4 x i1> undef to...
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; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 19 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX256-LABEL: 'zext256_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX512-LABEL: 'zext256_vXi1'
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
%V2i64 = zext <2 x i1> undef to <2 x i64>
%V4i64 = zext <4 x i1> undef to <4 x i64>
%V8i64 = zext <8 x i1> undef to <8 x i64>
%V2i32 = zext <2 x i1> undef to <2 x i32>
%V4i32 = zext <4 x i1> undef to <4 x i32>
%V8i32 = zext <8 x i1> undef to <8 x i32>
%V16i32 = zext <16 x i1> undef to <16 x i32>
%V2i16 = zext <2 x i1> undef to <2 x i16>
%V4i16 = zext <4 x i1> undef to <4 x i16>
%V8i16 = zext <8 x i1> undef to <8 x i16>
%V16i32 = zext <16 x i1> undef to <16 x i16>
%V32i16 = zext <32 x i1> undef to <32 x i16>
%V2i8 = zext <2 x i1> undef to <2 x i8>
%V4i8 = zext <4 x i1> undef to <4 x i8>
%V8i8 = zext <8 x i1> undef to <8 x i8>
%V16i8 = zext <16 x i1> undef to <16 x i8>
%V32i8 = zext <32 x i1> undef to <32 x i8>
%V64i8 = zext <64 x i1> undef to <64 x i8>
ret i32 undef
}
define i32 @sext256_vXi1() “min-legal-vector-width”=”256” {"open-source-used-in-branch-migration-tool-spirit2999"}
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

AVX512VL256-LABEL: 'sext256_vXi1'
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i64 = sext <16 x i1> undef to <16 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i64 = sext <32 x i1> undef to <32 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i64 = sext <16 x i1> undef to <16 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i64 = sext <32 x i1> undef to <32 x i64>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i32 = sext <32 x i1> undef to <32 x i32>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V64i32 = sext <64 x i1> undef to <64 x i32>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V128i32 = sext <128 x i1> undef to <128 x i32>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V64i16 = sext <64 x i1> undef to <64 x i16>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V128i16 = sext <128 x i1> undef to <128 x i16>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 21 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 42 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL512-LABEL: 'sext256_vXi1'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i64 = sext <16 x i1> undef to <16 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i64 = sext <32 x i1> undef to <32 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i32 = sext <32 x i1> undef to <32 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V64i32 = sext <64 x i1> undef to <64 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 15 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
; SKX256-LABEL: 'sext256_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX512-LABEL: 'sext256_vXi1'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
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; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> unde
define i32 @trunc_vXi1() "min-legal-vector-width"="256" {
  ; AVX-LABEL: 'trunc_vXi1'
  ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 46 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 22 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>
}

ret i32 undef
AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>

AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>
AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>
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; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 32 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 17 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 34 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; AVX512VL512-LABEL: 'trunc_vXi1'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 22 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 44 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V64i32 = trunc <64 x i32>
undef to <64 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = trunc <2 x i16>
    undef to <2 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = trunc <4 x i16>
    undef to <4 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16>
    undef to <8 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V16i16 = trunc <16 x i16>
    undef to <16 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 14 for instruction: %V64i16 = trunc <64 x i16>
    undef to <64 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V2i8 = trunc <2 x i8>
    undef to <2 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = trunc <4 x i8>
    undef to <4 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = trunc <8 x i8>
    undef to <8 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64>
    undef to <2 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64>
    undef to <4 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64>
    undef to <8 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64>
    undef to <16 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64>
    undef to <32 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 47 for instruction: %V64i64 = trunc <64 x i64>
    undef to <64 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32>
    undef to <2 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32>
    undef to <4 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32>
    undef to <8 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; %V2i64 = trunc <2 x i64> undef to <2 x i1>
%V4i64 = trunc <4 x i64> undef to <4 x i1>
%V8i64 = trunc <8 x i64> undef to <8 x i1>
%V16i64 = trunc <16 x i64> undef to <16 x i1>
%V32i64 = trunc <32 x i64> undef to <32 x i1>
%V64i64 = trunc <64 x i64> undef to <64 x i1>

%V2i32 = trunc <2 x i32> undef to <2 x i1>
%V4i32 = trunc <4 x i32> undef to <4 x i1>
%V8i32 = trunc <8 x i32> undef to <8 x i1>
%V16i32 = trunc <16 x i32> undef to <16 x i1>
%V32i32 = trunc <32 x i32> undef to <32 x i1>
%V64i32 = trunc <64 x i32> undef to <64 x i1>

%V2i16 = trunc <2 x i16> undef to <2 x i1>
ret i32 undef
}

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Ty Coon, President of Vice
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1.273 kerberos 1.18.3-r1

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    lib/gss_mechs/mech_spnego/mech/gssapiP_spnego.h
    lib/gss_mechs/mech_spnego/mech/spnego_mech.c
    lib/krb5/kadm5/kadm_host_srv_names.c
    lib/krb5/kdb/kdb_convert.c
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    lib/krb5/kdb/kdb_log.h
    lib/libgss/g_accept_sec_context.c
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lib/libgss/g_userok.c
lib/libgss/g_utils.c
lib/libgss/g_verify.c
lib/libgss/gssd_pname_to_uid.c
uts/common/gssapi/include/gssapi_err_generic.h
uts/common/gssapi/include/mechglueP.h

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lib/gssapi/mechglue/g_acquire_cred.c
lib/gssapi/mechglue/g_canon_name.c
lib/gssapi/mechglue/g_compare_name.c
lib/gssapi/mechglue/g_context_time.c
lib/gssapi/mechglue/g_delete_sec_context.c
lib/gssapi/mechglue/g_dsp_name.c
lib/gssapi/mechglue/g_dsp_status.c
lib/gssapi/mechglue/g_dup_name.c
lib/gssapi/mechglue/g_exp_sec_context.c
lib/gssapi/mechglue/g_export_name.c
lib/gssapi/mechglue/g_glue.c
lib/gssapi/mechglue/g_imp_name.c
lib/gssapi/mechglue/g_imp_sec_context.c
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lib/gssapi/mechglue/g_inquire_cred.c
lib/gssapi/mechglue/g_inquire_names.c
lib/gssapi/mechglue/g_process_context.c
and the initial implementation of incremental propagation, including the following new or changed files:

include/iprop_hdr.h
kadmin/server/ipropd_svc.c
lib/kdb/iprop.x
lib/kdb/kdb_convert.c
lib/kdb/kdb_log.c
lib/kdb/kdb_log.h
lib/krb5/error_tables/kdb5_err.et
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A. HISTORY OF THE SOFTWARE
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Python was created in the early 1990s by Guido van Rossum at Stichting Mathematisch Centrum (CWI, see http://www.cwi.nl) in the Netherlands as a successor of a language called ABC. Guido remains Python's principal author, although it includes many contributions from others.

In 1995, Guido continued his work on Python at the Corporation for National Research Initiatives (CNRI, see http://www.cnri.reston.va.us) in Reston, Virginia where he released several versions of the software.

In May 2000, Guido and the Python core development team moved to BeOpen.com to form the BeOpen PythonLabs team. In October of the same year, the PythonLabs team moved to Digital Creations (now Zope Corporation, see http://www.zope.com). In 2001, the Python Software Foundation (PSF, see http://www.python.org/psf/) was formed, a non-profit organization created specifically to own Python-related Intellectual Property. Zope Corporation is a sponsoring member of the PSF.

All Python releases are Open Source (see http://www.opensource.org for the Open Source Definition). Historically, most, but not all, Python releases have also been GPL-compatible; the table below summarizes...
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In 1995, Guido continued his work on Python at the Corporation for National Research Initiatives (CNRI, see http://www.cnri.reston.va.us) in Reston, Virginia where he released several versions of the software.
In May 2000, Guido and the Python core development team moved to BeOpen.com to form the BeOpen PythonLabs team. In October of the same year, the PythonLabs team moved to Digital Creations (now Zope Corporation, see http://www.zope.com). In 2001, the Python Software Foundation (PSF, see http://www.python.org/psf/) was formed, a non-profit organization created specifically to own Python-related Intellectual Property. Zope Corporation is a sponsoring member of the PSF.

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<td>PSF</td>
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<td>PSF</td>
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</tr>
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c-a-bundle.crt -- Bundle of CA Root Certificates

Certificate data from Mozilla as of: Thu Nov 3 19:04:19 2011#
This is a bundle of X.509 certificates of public Certificate Authorities
(CA). These were automatically extracted from Mozilla's root certificates
file (certdata.txt). This file can be found in the mozilla source tree:
It contains the certificates in PEM format and therefore
can be directly used with curl / libcurl / php_curl, or with
an Apache+mod_ssl webserver for SSL client authentication.
Just configure this file as the SSLCA CertificateFile.#

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  <developers>
    <developer>
      <name>Stuart Douglas</name>
      <email>sdouglas@redhat.com</email>
    </developer>
  </developers>

  <licenses>
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      <url>http://www.apache.org/licenses/LICENSE-2.0.txt</url>
    </license>
  </licenses>

  <dependencies>
  </dependencies>

</project>
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</scm>

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  jar/META-INF/maven/org.jboss.classfilewriter/jboss-classfilewriter/jboss-classfilewriter/pom.xml

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Found in path(s):
* /opt/ws_local/PERMITS_SQL/1074946987_1596002093.09/0/jboss-classfilewriter-1.2.4-final-sources-1-
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1.285 libidn 2.2.0-1.el8

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* javax.servlet:javax.servlet-api
* javax.annotation:javax.annotation-api
* javax.transaction:javax.transaction-api
* javax.websocket:javax.websocket-api

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* java.sun.security.ssl

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org.ow2.asm:asm-commons
org.ow2.asm:asm

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org.mortbay.jasper:apache-jsp
org.apache.tomcat:tomcat-jasper
org.apache.tomcat:tomcat-juli
org.apache.tomcat:tomcat-jsp-api
org.apache.tomcat:tomcat-el-api
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-api
org.apache.tomcat:tomcat-util-scan
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org.eclipse.jetty.toolchain:jetty-schemas

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1.291 mock 2.0.0

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1.292 libffi 3.1-22.el8

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1.293 libgcrypt 1.8.4 5
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This package was debianized by Ivo Timmermans <ivo@debian.org> on Fri. 3 Aug 2001 10:02:38 +0200.
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Libgcrypt used to be part of GnuPG but has been taken out into its own package on 2000-12-21.

Most of the stuff in mpi has been taken from an old GMP library version by Torbjorn Granlund <tege@noisy.tmg.se>.

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The ECC code cipher/ecc.c was based on code by Sergi Blanch i Torne, sergi at calcurco dot org.

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* /opt/cola/permits/1130029301_1612433654.56/0/hibernate-validator-cdi-6-0-21-final-sources-jar/org/hibernate/validator/cdi/internal/interceptor/ValidationEnabledAnnotatedConstructor.java
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Metadata-Version: 1.2
Name: pyasn1
Version: 0.4.8
Summary: ASN.1 types and codecs
Home-page: https://github.com/etingof/pyasn1
Author: Ilya Etingof
Author-email: etingof@gmail.com
Maintainer: Ilya Etingof <etingof@gmail.com>
License: BSD
Description: Pure-Python implementation of ASN.1 types and DER/BER/CER codecs (X.208)
Platform: any
Classifier: Development Status :: 5 - Production/Stable
Classifier: Environment :: Console
Classifier: Intended Audience :: Developers
Classifier: Intended Audience :: Education
Classifier: Intended Audience :: Information Technology
Classifier: Intended Audience :: System Administrators
Classifier: Intended Audience :: Telecommunications Industry
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Classifier: Programming Language :: Python :: 2.4
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ASN.1 library for Python
-------------------------

This is a free and open source implementation of ASN.1 types and codecs as a Python package. It has been first written to support particular
protocol (SNMP) but then generalized to be suitable for a wide range of protocols based on
[ASN.1 specification](https://www.itu.int/rec/dologin_pub.asp?lang=e&id=T-REC-X.208-198811-W!!PDF-E&type=items).

Features
--------

* Generic implementation of ASN.1 types (X.208)
* Standards compliant BER/CER/DER codecs
* Dumps/loads ASN.1 structures from Python types
* 100% Python, works with Python 2.4 up to Python 3.7
* MT-safe
* Contributed ASN.1 compiler [Asn1ate](https://github.com/kimgr/asn1ate)

Why using pyasn1
----------------

ASN.1 solves the data serialisation problem. This solution was designed long ago by the wise Ancients. Back then, they did not have the luxury of wasting bits. That is why ASN.1 is designed to serialise data structures of unbounded complexity into something compact and efficient when it comes to processing the data.

That probably explains why many network protocols and file formats still rely on the 30+ years old technology. Including a number of high-profile Internet protocols and file formats.

Quite a number of books cover the topic of ASN.1. [Communication between heterogeneous systems](http://www.oss.com/asn1/dubuisson.html) by Olivier Dubuisson is one of those high quality books freely available on the Internet.

The pyasn1 package is designed to help Python programmers tackling network protocols and file formats at the comfort of their Python prompt. The tool struggles to capture all aspects of a rather complicated ASN.1 system and to represent it on the Python terms.

How to use pyasn1
-----------------

With pyasn1 you can build Python objects from ASN.1 data structures. For example, the following ASN.1 data structure:

```bash
Record ::= SEQUENCE {
  id  INTEGER,
```

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Could be expressed in pyasn1 like this:

```python
class Record(Sequence):
    componentType = NamedTypes(
        NamedType('id', Integer()),
        OptionalNamedType(
            'room', Integer().subtype(
                implicitTag=Tag(tagClassContext, tagFormatSimple, 0)
            )
        ),
        DefaultedNamedType(
            'house', Integer(0).subtype(
                implicitTag=Tag(tagClassContext, tagFormatSimple, 1)
            )
        )
    )
```

It is in the spirit of ASN.1 to take abstract data description and turn it into a programming language specific form. Once you have your ASN.1 data structure expressed in Python, you can use it along the lines of similar Python type (e.g. ASN.1 `SET` is similar to Python `dict`, `SET OF` to `list`):

```python
>>> record = Record()
>>> record['id'] = 123
>>> record['room'] = 321
>>> str(record)
Record:
id=123
room=321
```

Part of the power of ASN.1 comes from its serialisation features. You can serialise your data structure and send it over the network.
Conversely, you can turn serialised ASN.1 content, as received from network or read from a file, into a Python object which you can introspect, modify, encode and send back.

```python
>>> from pyasn1.codec.der.decoder import decode
>>> received_record, rest_of_substrate = decode(substrate, asn1Spec=Record())
>>> for field in received_record:
...    print('{} is {}'.format(field, received_record[field]))
id is 123
room is 321
house is 0
>>> record == received_record
True
>>> received_record.update(room=123)
>>> substrate = encode(received_record)
>>> hexdump(substrate)
00000: 30 06 02 01 7B 80 01 7B
```

The `pyasn1` classes struggle to emulate their Python prototypes (e.g. int, list, dict etc.). But ASN.1 types exhibit more complicated behaviour. To make life easier for a Pythonista, they can turn their `pyasn1` classes into Python built-ins:

```python
>>> from pyasn1.codec.native.encoder import encode
>>> encode(record)
{'id': 123, 'room': 321, 'house': 0}
```

Or vice-versa -- you can initialize an ASN.1 structure from a tree of Python objects:

```python
>>> from pyasn1.codec.native.decoder import decode
>>> record = decode({'id': 123, 'room': 321, 'house': 0}, asn1Spec=Record())
>>> str(record)
Record:
  id=123
  room=321
  ...
With ASN.1 design, serialisation codecs are decoupled from data objects, so you could turn every single ASN.1 object into many different serialised forms. As of this moment, pyasn1 supports BER, DER, CER and Python built-ins codecs. The extremely compact PER encoding is expected to be introduced in the upcoming pyasn1 release.

More information on pyasn1 APIs can be found in the [documentation](http://snmplabs.com/pyasn1/), compiled ASN.1 modules for different protocols and file formats could be found in the pyasn1-modules [repo](https://github.com/etingof/pyasn1-modules).

How to get pyasn1
-----------------

The pyasn1 package is distributed under terms and conditions of 2-clause BSD [license](http://snmplabs.com/pyasn1/license.html). Source code is freely available as a GitHub [repo](https://github.com/etingof/pyasn1).

You could `pip install pyasn1` or download it from [PyPI](https://pypi.org/project/pyasn1).

If something does not work as expected, [open an issue](https://github.com/etingof/pyasn1/issues) at GitHub or post your question [on Stack Overflow](https://stackoverflow.com/questions/ask) or try browsing pyasn1 [mailing list archives](https://sourceforge.net/p/pyasn1/mailman/pyasn1-users/).

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* /opt/cola/permits/1110812511_1607462013.57/0/pyasn1-0-4-8-tar-gz/pyasn1-0.4.8/tests/test_debug.py
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* /opt/cola/permits/1110812511_1607462013.57/0/pyasn1-0-4-8-tar-gz/pyasn1-0.4.8/tests/codec/ber/ber_test_encoder.py
* /opt/cola/permits/1110812511_1607462013.57/0/pyasn1-0-4-8-tar-gz/pyasn1-0.4.8/pyasn1/codec/native/encoder.py
* /opt/cola/permits/1110812511_1607462013.57/0/pyasn1-0-4-8-tar-gz/pyasn1-0.4.8/tests/codec/native/__main__.py

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ASN.1 library for Python

Abstract Syntax Notation One (\`ASN.1\`) <http://en.wikipedia.org/wiki/Abstract_Syntax_Notation_1x>` is a technology for exchanging structured data in a universally understood, hardware agnostic way. Many industrial, security and telephony applications heavily rely on ASN.1.

The \`pyasn1 <https://pypi.org/project/pyasn1/>`_ library implements ASN.1 support in pure-Python.

What is ASN.1

ASN.1 is a large, arguably over-engineered and extremely old data modelling and serialisation tool. It is probably among the first serialisation protocols in the history of computer science and technology.

ASN.1 started its life over 30 years ago as a serialisation mechanism for the first electronic mail (known as X.400). Later on if was split off the e-mail application and become a stand-alone tech still being actively supported by its designers and widely used in industry and technology.

Since then ASN.1 is sort of haunted by its relations with the OSI model -- the first, unsuccessful, version of the Internet. You can read many interesting discussions <https://news.ycombinator.com/item?id=8871453>`_ on that topic.

In the following years, generations of software engineers tackled the serialisation problem many times. We can see that in Google's `ProtoBuffers <https://developers.google.com/protocol-buffers/>`_ or `FlatBuffers <https://google.github.io/flatbuffers/>`_, for example. Interestingly, many new takes on binary protocol design do not depart...
far from ASN.1 from technical perspective. It's more of a matter of striking
a balance between processing overhead, wire format overhead and human
readability.

Looking at what ASN.1 has to offer, it has three loosely coupled parts:

* Data types: the standard introduces a collection of basic data types
  (integers, bits, strings, arrays and records) that can be used for describing
  arbitrarily complex, nested data structures.

* Serialisation protocols: the above data structures could be converted into a
  series of octets for storage or transmission over the wire as well as
  recovered back into their structured form. The system is fully agnostic
  to hardware architectures differences.

* Schema language: ASN.1 data structures could be described in terms
  of a schema language for ASN.1 compiler to turn it into platform-specific
  implementation.

ASN.1 applications
-------------------

Being an old and generally successful standard, ASN.1 is widely
adopted for many uses. To give you an example, these technologies
use ASN.1 for their data exchange needs:

* Signaling standards for the public switched telephone network (SS7 family)
* Network management standards (SNMP, CMIP)
* Directory standards (X.500 family, LDAP)
* Public Key Infrastructure standards (X.509, etc.)
* PBX control (CSTA)
* IP-based Videoconferencing (H.323 family)
* Biometrics (BIP, CBEFF, ACBio)
* Intelligent transportation (SAE J2735)
* Cellular telephony (GSM, GPRS/EDGE, UMTS, LTE)

ASN.1 gotchas
-------------

Apparently, ASN.1 is hard to implement properly. Quality open-source
ASN.1 tools are rare, but ad-hoc implementations are numerous. Judging from the
'statistics <http://cve.mitre.org/cgi-bin/cvekey.cgi?keyword=ASN.1>_ on discovered
security vulnerabilities, many people have implemented ASN.1 parsers
and oftentimes fell victim to its edge cases.

On the bright side, ASN.1 has been around for a long time, it is well understood
and security reviewed.
Documentation
-----------

.. toctree::
:maxdepth: 2

/pyasn1/contents

Use case
-------

.. toctree::
:maxdepth: 2

/example-use-case

Download & Install
------------------

.. toctree::
:maxdepth: 2

/download

Changes
------

All changes and release history is maintained in changelog. There you could also download the latest unreleased pyasn1 tarball containing the latest fixes and improvements.

.. toctree::
:maxdepth: 1

/changelog

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------

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.. toctree::
:maxdepth: 2

/license

Getting help
------------

Books on ASN.1
--------------

The pyasn1 implementation is largely based on reading up the following awesome books:

* `ASN.1 - Communication between heterogeneous systems <http://www.oss.com/asn1/dubuisson.html>`_ by Olivier Dubuisson

Here you can get the official standards which is hard to read:


On the other end of the readability spectrum, here is a quick and sweet write up:


If you are working with ASN.1, we'd highly recommend reading a proper book on the subject.

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* `/opt/cola/permits/1110812511_1607462013.57/0/pyasn1-0.4.8.tar-gz/pyasn1-0.4.8/docs/source/contents.rst`

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* Project home: https://projects.eclipse.org/projects/ee4j.jaxws

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## Source Code

The project maintains the following source code repositories:

* https://github.com/eclipse-ee4j/jws-api
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* https://github.com/eclipse-ee4j/saaj-api

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1.306 opensaml-saml-api 3.3.1

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To do so, attach the following notices to the program. It is safest to attach them to the start of each source file to most effectively convey the exclusion of warranty; and each file should have at least
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```
Gnomovision version 69, Copyright (C) year name of author
Gnomovision comes with ABSOLUTELY NO WARRANTY; for details type `show w'.
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```

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```
Yoyodyne, Inc., hereby disclaims all copyright interest in the program `Gnomovision' (which makes passes at compilers) written by James Hacker.
```

<signature of Ty Coon>, 1 April 1989
Ty Coon, President of Vice

This General Public License does not permit incorporating your program into proprietary programs. If your program is a subroutine library, you may consider it more useful to permit linking proprietary applications with the library. If this is what you want to do, use the GNU Library General Public License instead.
1.309 keyutils 1.5.10-6.el8

1.309.1 Available under license:

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Version 2.1, February 1999

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This option is useful when you wish to copy part of the code of the Library into a program that is not a library.

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## Source Code

The project maintains the following source code repositories:
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1.317 wildfly-management-client-content

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It was originally written by Tatu Saloranta (tatu.saloranta@iki.fi), and has been in development since 2007.
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 * /opt/cola/permits/1135840457_1613613080.13/0/commons-logging-1-1-sources-9.jar/org/apache/commons/logging/LogConfigurationException.java
 * /opt/cola/permits/1135840457_1613613080.13/0/commons-logging-1-1-sources-9.jar/org/apache/commons/logging/impl/Log4JLogger.java
 * /opt/cola/permits/1135840457_1613613080.13/0/commons-logging-1-1-sources-9.jar/org/apache/commons/logging/impl/LogFactoryImpl.java
 * /opt/cola/permits/1135840457_1613613080.13/0/commons-logging-1-1-sources-9.jar/org/apache/commons/logging/LogSource.java
 * /opt/cola/permits/1135840457_1613613080.13/0/commons-logging-1-1-sources-9.jar/org/apache/commons/logging/impl/LogKitLogger.java
 * /opt/cola/permits/1135840457_1613613080.13/0/commons-logging-1-1-sources-9.jar/org/apache/commons/logging/Log.java

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* /opt/cola/permits/1135840457_1613613080.13/0/commons-logging-1-1-sources-9-
  jar/org/apache/commons/logging/impl/ServletContextCleaner.java

1.326 netbase 5.6

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* https://github.com/eclipse-ee4j/jaf

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1.336 slf4j 1.7.30

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1.338 libxml 2.9.9-r0

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1.339 objectweb-asm 7.1

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1.341 xml-commons-resolver 1.2

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1.351 mccabe 0.6.1

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1.355 kerberos 1.17-3+deb10u1

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lib/gssapi/mechglue/g_accept_sec_context.c
lib/gssapi/mechglue/g_acquire_cred.c
lib/gssapi/mechglue/g_canon_name.c
lib/gssapi/mechglue/g_compare_name.c
lib/gssapi/mechglue/g_context_time.c
lib/gssapi/mechglue/g_delete_sec_context.c
lib/gssapi/mechglue/g_dsp_name.c
lib/gssapi/mechglue/g_dsp_status.c
lib/gssapi/mechglue/g_dup_name.c
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lib/gssapi/mechglue/g_export_name.c
lib/gssapi/mechglue/g_glue.c
lib/gssapi/mechglue/g_imp_name.c
lib/gssapi/mechglue/g_imp_sec_context.c
lib/gssapi/mechglue/g_init_sec_context.c
lib/gssapi/mechglue/g_initialize.c
lib/gssapi/mechglue/g_inquire_context.c
lib/gssapi/mechglue/g_inquire_cred.c
lib/gssapi/mechglue/g_inquire_names.c
lib/gssapi/mechglue/g_process_context.c
lib/gssapi/mechglue/g_rel_buffer.c
lib/gssapi/mechglue/g_rel_cred.c
lib/gssapi/mechglue/g_rel_name.c
lib/gssapi/mechglue/g_rel_oid_set.c
lib/gssapi/mechglue/g_seal.c
lib/gssapi/mechglue/g_sign.c
lib/gssapi/mechglue/g_store_cred.c
lib/gssapi/mechglue/g_unseal.c
lib/gssapi/mechglue/g_userok.c
and the initial implementation of incremental propagation, including
the following new or changed files:

include/iprop_hdr.h
kadmin/server/ipropd_svc.c
lib/kdb/iprop.x
lib/kdb/kdb_convert.c
lib/kdb/kdb_log.c
lib/kdb/kdb_log.h
lib/krb5/error_tables/kdb5_err.et
slave/kpropd_rpc.c
slave/kproplog.c

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This option is useful when you wish to copy part of the code of the Library into a program that is not a library.

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* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/BufferedStreamSinkConduit.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/ssl/JsseAcceptingSslStreamConnection.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/AbstractStreamSourceConduit.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/FixedLengthStreamSourceConduit.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/AbstractMessageSourceConduit.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/BufferedStreamSourceConduit.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/MessageSinkConduit.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/BlockingStreamSourceConduit.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/FileChangeEvent.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio/api-3-8-2-final-sources-1.jar/org/xnio/conduits/AbstractSynchronizedSinkConduit.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/AbstractMessageSourceConduit.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/SynchronizedStreamSourceConduit.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/ConduitWritableMessageChannel.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/SaslUnwrappingConduit.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/ssl/AbstractAcceptingSslChannel.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/FileAccess.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/AbstractSynchronizedSinkConduit.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/SynchronizedStreamSourceConduit.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1.jar/org/xnio/conduits/BlockingStreamSourceConduit.java
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  jar/org/xnio/channels/NullStreamSinkChannel.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-
  jar/org/xnio/channels/FixedLengthStreamSinkChannel.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-
  jar/org/xnio/channels/FixedLengthOverflowException.java
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  jar/java/nio/channels/FileChannel.java

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* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/streams/BufferPipeOutputStream.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/channels/ReadTimeoutException.java
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* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/sasl/SaslWrapper.java  
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/**
 * A QOP value specifying authentication plus integrity and confidentiality protection.
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* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/streams/LimitedOutputStream.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/streams/LimitedInputStream.java

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  jar/org/xnio/channels/SplitStreamSourceChannel.java
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  jar/org/xnio/channels/SplitStreamSinkChannel.java
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  jar/org/xnio/channels/ChannelFactory.java
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/\opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/FutureResult.java
/\opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/sasl/SaslStrength.java
/\opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/ByteString.java
/\opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/channels/CloseableChannel.java
/\opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/channels/BlockingReadableByteChannel.java
/\opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/channels/BlockingWritableByteChannel.java
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/\opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/channels/SSLChannel.java
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* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/channels/SuspendableReadChannel.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/channels/StreamSourceChannel.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/channels/ReadableMessageChannel.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/channels/Configurable.java
* /opt/cola/permits/1170841522_1622721493.61/0/xnio-api-3-8-2-final-sources-1-jar/org/xnio/channels/UnsupportedOptionException.java
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* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-jar/javassist/CtField.java
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* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-jar/javassist/bytecode/FieldInfo.java

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jar/javassist/util/proxy/MethodFilter.java
* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-
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* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-
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* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-jar/javassist/ByteArrayClassPath.java
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* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-jar/javassist/convert/Transformer.java
* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-jar/javassist/bytecode/SyntheticAttribute.java
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Found in path(s):
* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-
  jar/javassist/bytecode/annotation/ArrayMemberValue.java
* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-
  jar/javassist/bytecode/annotation/DoubleMemberValue.java
* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-
  jar/javassist/bytecode/annotation/EnumMemberValue.java
* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-
  jar/javassist/bytecode/annotation/MemberValue.java
* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-
  jar/javassist/bytecode/annotation/Annotation.java
* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-
  jar/javassist/bytecode/annotation/CharMemberValue.java
* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-
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* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-
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  jar/javassist/bytecode/annotation/AnnotationMemberValue.java
* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-
  jar/javassist/bytecode/annotation/ByteMemberValue.java
* /opt/cola/permits/1135840536_1613612905.33/0/javassist-3-26-0-ga-sources-4-
  jar/javassist/bytecode/annotation/StringMemberValue.java

1.371 zookeeper 3.5.8
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1.374 rocksdb 11
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former contains code derived from the library, whereas the latter must
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* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/server/admin/CommandResponse.java
* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/MultiResponse.java
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* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-
jar/org/apache/zookeeper/server/watch/WatchesSummary.java
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jar/org/apache/zookeeper/MultiOperationRecord.java
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jar/org/apache/zookeeper/server/watch/WatchesPathReport.java
* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-
jar/org/apache/zookeeper/server/ZooKeeperServerConf.java
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* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/server/ContainerManager.java
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* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/server/DigestCalculator.java
* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/server/persistence/SnapShot.java
* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/Environment.java
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* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/server/DataTreeMXBean.java
* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/server/quorum/auth/QuorumAuthLearner.java
* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/client/FourLetterWordMain.java
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ar/jar/org/apache/zookeeper/StatsTrack.java
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* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-
ar/jar/org/apache/zookeeper/client/HostProvider.java
* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-
ar/jar/org/apache/zookeeper/AddWatchMode.java
* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-
ar/jar/org/apache/zookeeper/server/auth/X509AuthenticationProvider.java
* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-
ar/jar/org/apache/zookeeper/server/ZooKeeperServerShutdownHandler.java
* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-
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* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-
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* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-
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* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/Testable.java
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* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/server/DumbWatcher.java
* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/cli/CliWrapperException.java
* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/common/QuorumXS09Util.java
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* /opt/cola/permits/1102648010_1603824244.11/0/zookeeper-3-6-2-sources-jar/org/apache/zookeeper/server/RequestProcessor.java
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jar/org/apache/zookeeper/common/PathTrie.java

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26. language- less (https://github.com/atom/language- less)
28. language- rust version 0.4.9 (https://github.com/zargony/atom- language- rust)
30. Microsoft/TypeScript- TmLanguage version 0.0.1 (https://github.com/Microsoft/TypeScript- TmLanguage)
31. octicons-code version 3.1.0 (https://octicons.github.com)
32. octicons-font version 3.1.0 (https://octicons.github.com)
33. seti-ui version 0.1.0 (https://github.com/jesseweed/seti-ui)
34. shaders-tmLanguage version 0.1.0 (https://github.com/gjones/shaders-tmLanguage)
35. string_scorer version 0.1.20 (https://github.com/joshaven/string_scorer)
36. sublimehq/Packages (https://github.com/sublimehq/Packages)
37. SublimeText/PowerShell (https://github.com/SublimeText/PowerShell)
38. textmate/asp.vb.net.tmbundle (https://github.com/textmate/asp.vb.net.tmbundle)
39. textmate/c.tmbundle (https://github.com/textmate/c.tmbundle)
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53. textmate/yaml.tmbundle (https://github.com/textmate/yaml.tmbundle)
54. TypeScript-TmLanguage version 0.1.8 (https://github.com/Microsoft/TypeScript-TmLanguage)
55. vscode-swift version 0.0.1 (https://github.com/owensd/vscode-swift)

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That's all there is to it!

1.414 gmp 6.2.1-r0

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1.419 icu 63.1 6+deb10u1

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### Commands to generate dependency files
GEN_DEPS.c=$(CC) -E -MM $(DEFS) $(CPPFLAGS)
GEN_DEPS.cc=$(CXX) -E -MM $(DEFS) $(CPPFLAGS)

### Flags for position independent code
SHAREDLIBCFLAGS = -fPIC
SHAREDLIBCXXFLAGS = -fPIC
SHAREDLIBCPPFLAGS = -DPIC

### Additional flags when building libraries and with threads
THREADSCPPFLAGS = -D_REENTRANT
LIBCPPFLAGS =

### Compiler switch to embed a runtime search path
LD_RPATH=
LD_RPATH_PRE=-Wl,-rpath,

### Compiler switch to embed a library name
LD_SONAME = -Wl,-soname -Wl,$(notdir $(MIDDLE_SO_TARGET))

### Shared library options
LD_SOOPIONS= -Wl,-Bsymbolic

## Shared object suffix
SO = so

## Non-shared intermediate object suffix
STATIC_O = ao

## Compilation rules
%.$(STATIC_O): $(srcdir)/%.c
$(COMPILE.c) $(STATICCPPFLAGS) $(STATICCFLAGS) -o $@ $<

%.o: $(srcdir)/%.c
$(COMPILE.c) $(DYNAMICCPPFLAGS) $(DYNAMICCFLAGS) -o $@ $<

%.$(STATIC_O): $(srcdir)/%.cpp
$(COMPILE.cc) $(STATICCPPFLAGS) $(STATICCXXFLAGS) -o $@ $<

%.o: $(srcdir)/%.cpp
$(COMPILE.cc) $(DYNAMICCPPFLAGS) $(DYNAMICCXXFLAGS) -o $@ $<

## Dependency rules
%.d: $(srcdir)/%.c
@echo "generating dependency information for $<"
@$(SHELL) -ec "$\(\text{GEN\_DEPS\_c}\) $< \n| sed \"s/(^\([^/\n\"]\)\.[^/\n]*\(.*\)/\1.o $@ : /g\" > $@;\n | -s $@ ]\|| rm -f $@’

%.d: $(srcdir)/%.cpp
@echo "generating dependency information for $<"
@$(SHELL) -ec "$\(\text{GEN\_DEPS\_cc}\) $< \n| sed \"s/(^\([^/\n\"]\)\.[^/\n]*\(.*\)/\1.o $@ : /g\" > $@;\n | -s $@ ]\|| rm -f $@’

## Versioned libraries rules
%.$(SO).$(SO_TARGET_VERSION_MAJOR): %.$(SO).$(SO_TARGET_VERSION)
$(RM) $@ && ln -s $<F> $@

%.$(SO): %.$(SO).$(SO_TARGET_VERSION_MAJOR)
$(RM) $@ && ln -s $*F$.SO.%.$(SO).$(SO_TARGET_VERSION) $@

## Bind internal references

# LDflags that pkgdata will use
BIR_LDFLAGS= -Wl,-Bsymbolic

# Dependencies [i.e. map files] for the final library
BIR_DEPS=

## Remove shared library 's'
STATIC_PREFIX_WHEN_USED =
STATIC_PREFIX =

## End BSD-specific setup

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21.0.2.Final

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org.keycloak.models.sessions.infinispan.InfinispanUserSessionProviderFactory

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org.keycloak.models.sessions.infinispan.InfinispanSingleUseTokenStoreProviderFactory

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org.keycloak.models.sessions.infinispan.InfinispanCodeToTokenStoreProviderFactory
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org.keycloak.models.sessions.infinispan.InfinispanTokenRevocationStoreProviderFactory

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org.keycloak.keys.infinispan.InfinispanPublicKeyStorageProviderFactory
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org.keycloak.models.cache.infinispan.InfinispanUserCacheProviderFactory

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1.438 bcel 2.7.1

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1.439 vdx-core 1.1.6

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1.441 isorelax 20090621

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  jar/org/iso_relax/dispatcher/IslandSchemaReader.java

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  jar/org/wildfly/security/auth/util/SimpleRegexRealmMapper.java
* /opt/cola/permits/1130031093_1612433152.03/0/wildfly-elytron-auth-util-1-13-1-final-sources-
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-- vile:txtmode fc=72
-- $Id: COPYING,v 1.6 2018/01/01 12:00:00 tom Exp $
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1.453 wildfly-microprofile-opentracing-smallrye 21.0.2.Final

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1.454 readline 2.0

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1.455 wildfly-cmp 21.0.2.Final

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1.456 reactive-streams 1.0.3

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1.457 cxf-rt-ws-rm 3.3.7

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1.458 infinispan-cachestore-jdbc 11.0.4.Final

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            </head>
            <body>
                <p>The following material has been provided for informational purposes only, and should not be relied upon or construed as a legal opinion or legal advice.</p>
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<xsl:when test="$filename = 'indiana university extreme! lab software license - license.txt'">
<xsl:text>indiana university extreme! lab software license - license.txt"</xsl:when>
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* /opt/ws_local/PERMITS_SQL/1065163923_1593484433.47/0/rxjava-2-2-19-sources-jar/io/reactivex/internal/schedulers/AbstractDirectTask.java

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* /opt/ws_local/PERMITS_SQL/1065163923_1593484433.47/0/rxjava-2-2-19-sources-jar/io/reactivex/subscribers/TestSubscriber.java
* /opt/ws_local/PERMITS_SQL/1065163923_1593484433.47/0/rxjava-2-2-19-sources-jar/io/reactivex/internal/util/ObservableQueueDrain.java
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* /opt/ws_local/PERMITS_SQL/1065163923_1593484433.47/0/rxjava-2-2-19-sources-jar/io/reactivex/internal/operators/observable/ObservableToMaybeMaybe.java

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1.473 jboss-jaxb-intros 1.0.3.GA

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Eclipse

The following artifacts are EPL.
* org.eclipse.jetty.orbit:org.eclipse.jdt.core

The following artifacts are EPL and ASL2.
* org.eclipse.jetty.orbit:javax.security.auth.message

The following artifacts are EPL and CDDL 1.0.
* org.eclipse.jetty.orbit:javax.mail.glassfish
The following artifacts are CDDL + GPLv2 with classpath exception.  
https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

* javax.servlet:javax.servlet-api
* javax.annotation:javax.annotation-api
* javax.transaction:javax.transaction-api
* javax.websocket:javax.websocket-api

Oracle OpenJDK

If ALPN is used to negotiate HTTP/2 connections, then the following artifacts may be included in the distribution or downloaded when ALPN module is selected.

* java.sun.security.ssl

These artifacts replace/modify OpenJDK classes. The modifications are hosted at github and both modified and original are under GPL v2 with classpath exceptions.  
http://openjdk.java.net/legal/gplv2+ce.html

OW2

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org.ow2.asm:asm-commons
org.ow2.asm:asm

Apache

The following artifacts are ASL2 licensed.

org.apache.taglibs:taglibs-standard-spec
org.apache.taglibs:taglibs-standard-impl

MortBay
The following artifacts are ASL2 licensed. Based on selected classes from following Apache Tomcat jars, all ASL2 licensed.

org.mortbay.jasper:apache-jsp
org.apache.tomcat:tomcat-jasper
org.apache.tomcat:tomcat-juli
org.apache.tomcat:tomcat-jsp-api
org.apache.tomcat:tomcat-el-api
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-api
org.apache.tomcat:tomcat-util-scan
org.apache.tomcat:tomcat-util

org.mortbay.jasper:apache-el
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-el-api

------

Mortbay

The following artifacts are CDDL + GPLv2 with classpath exception.

https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

org.eclipse.jetty.toolchain:jettyschemas

------

Assorted

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1.475 jberet-core 1.3.7.Final
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1.476 flask-injector 0.10.1

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Found in path(s):
* /opt/cola/permits/1158394701_1619759996.22/0/flask-injector-0-10-1-1-tar-gz/Flask-Injector-0.10.1/flask_injector.py

No license file was found, but licenses were detected in source scan.

Metadata-Version: 1.1
Name: Flask-Injector
Version: 0.10.1
Summary: Adds Injector, a Dependency Injection framework, support to Flask.
Home-page: https://github.com/alecthomas/flask_injector
Author: Alec Thomas
Author-email: alec@swapoff.org
License: BSD
Description-Content-Type: UNKNOWN
Description: Flask-Injector

.. image:: https://secure.travis-ci.org/alecthomas/flask_injector.png?branch=master
   :alt: Build status
   :target: https://travis-ci.org/alecthomas/flask_injector
Adds `Injector <https://github.com/alecthomas/injector>`_ support to Flask, this way there's no need to use global Flask objects, which makes testing simpler.

Injector is a dependency-injection framework for Python, inspired by Guice.

`Flask-Injector` is compatible with CPython 3.3+.
As of version 0.10.0 it requires Injector version 0.12.0 or greater and Flask 0.12.0 or greater.

GitHub project page: https://github.com/alecthomas/flask_injector

PyPI package page: https://pypi.python.org/pypi/Flask-Injector

Changelog: https://github.com/alecthomas/flask_injector/blob/master/CHANGELOG.rst

Features
--------

Flask-Injector lets you inject dependencies into:

* views (functions and class-based)
* `before_request` handlers
* `after_request` handlers
* `teardown_request` handlers
* template context processors
* error handlers
* Jinja environment globals (functions in `app.jinja_env.globals`)
* Flask-RESTful Resource constructors
* Flask-RestPlus Resource constructors

Flask-Injector supports defining types using function annotations (Python 3), see below.

Example application using Flask-Injector
---------------------------------------

.. code:: python

    import sqlite3
    from flask import Flask, Config
    from flask.views import View
    from flask_injector import FlaskInjector
    from injector import inject

    app = Flask(__name__)

    # Configure your application by attaching views, handlers, context processors etc.:
@app.route("/bar")
def bar():
    return render("bar.html")

# Route with injection
@app.route("/foo")
def foo(db: sqlite3.Connection):
    users = db.execute('SELECT * FROM users').all()
    return render("foo.html")

# Class-based view with injected constructor
class Waz(View):
    @inject
def __init__(self, db: sqlite3.Connection):
        self.db = db

    def dispatch_request(self, key):
        users = self.db.execute('SELECT * FROM users WHERE name=?', (key,)).all()
        return 'waz'

app.add_url_rule('/waz/<key>', view_func=Waz.as_view('waz'))

# In the Injector world, all dependency configuration and initialization is
# performed in modules (http://packages.python.org/injector/#module). The
# same is true with Flask-Injector. You can see some examples of configuring
# Flask extensions through modules below.

# Accordingly, the next step is to create modules for any objects we want made
# available to the application. Note that in this example we also use the
# Injector to gain access to the `flask.Config`:

def configure(binder):
    binder.bind(
        sqlite3.Connection,
        to=sqlite3.Connection(':memory:'),
        scope=request,
    )

# Initialize Flask-Injector. This needs to be run *after* you attached all
# views, handlers, context processors and template globals.

FlaskInjector(app=app, modules=[configure])

# All that remains is to run the application
app.run()

See `example.py` for a more complete example, including `Flask-SQLAlchemy` and `Flask-Cache` integration.

Supporting Flask Extensions
----------------------------

Typically, Flask extensions are initialized at the global scope using a pattern similar to the following.

.. code:: python

    app = Flask(__name__)
    ext = ExtClass(app)

    @app.route(...)
    def view():
        # Use ext object here...

As we don't have these globals with Flask-Injector we have to configure the extension the Injector way - through modules. Modules can either be subclasses of `injector.Module` or a callable taking an `injector.Binder` instance.

.. code:: python

    from injector import Module

    class MyModule(Module):
        @provider
        @singleton
        def provide_ext(self, app: Flask) -> ExtClass:
            return ExtClass(app)

    def main():
        app = Flask(__name__)
        app.config.update(
            EXT_CONFIG_VAR='some_value',
        )

        # attach your views etc. here

        FlaskInjector(app=app, modules=[MyModule])

        app.run()

*Make sure to bind extension objects as singletons.*
Keywords: Dependency Injection, Flask
Platform: any
Classifier: Development Status :: 5 - Production/Stable
Classifier: Intended Audience :: Developers
Classifier: License :: OSI Approved :: MIT License
Classifier: Operating System :: OS Independent
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Classifier: Programming Language :: Python :: Implementation :: CPython

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* /opt/cola/permits/1158394701_1619759996.22/0/flask-injector-0-10-1-1-tar-gz/Flask-Injector-0.10.1/Flask_Injector.egg-info/PKG-INFO
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1.477 metrics-core 2.2.0

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* /opt/cola/permits/1145440743_1616178883.36/0/metrics-core-2-2-0-sources-5-jar/com/yammer/metrics/stats/ThreadLocalRandom.java
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* /opt/cola/permits/1130030515_1612433611.17/0/wildfly-elytron-asn1-1-13-1-final-sources-jar/org/wildfly/security/asn1/ASN1Decoder.java
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* /opt/cola/permits/1130030515_1612433611.17/0/wildfly-elytron-asn1-1-13-1-final-sources-jar/org/wildfly/security/asn1/ASN1.java
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1.481 antlr 2.7.7

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* /opt/cola/permits/1130030167_1612432999.11/0/keycloak-server-spi-12-0-2-sources-jar/org/keycloak/vault/VaultProvider.java
* /opt/cola/permits/1130030167_1612432999.11/0/keycloak-server-spi-12-0-2-sources-jar/org/keycloak/vault/VaultSpi.java
* /opt/cola/permits/1130030167_1612432999.11/0/keycloak-server-spi-12-0-2-sources-jar/org/keycloak/vault/VaultProviderFactory.java
* /opt/cola/permits/1130030167_1612432999.11/0/keycloak-server-spi-12-0-2-sources-jar/org/keycloak/vault/VaultStringSecret.java
* /opt/cola/permits/1130030167_1612432999.11/0/keycloak-server-spi-12-0-2-sources-jar/org/keycloak/vault/VaultCharSecret.java

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* /opt/cola/permits/1130030167_1612432999.11/0/keycloak-server-spi-12-0-2-sources-jar/org/keycloak/models/credential/dto/WebAuthnSecretData.java
* /opt/cola/permits/1130030167_1612432999.11/0/keycloak-server-spi-12-0-2-sources-jar/org/keycloak/credential/CredentialTypeMetadataContext.java
* /opt/cola/permits/1130030167_1612432999.11/0/keycloak-server-spi-12-0-2-sources-jar/org/keycloak/credential/CredentialTypeMetadata.java
* /opt/cola/permits/1130030167_1612432999.11/0/keycloak-server-spi-12-0-2-sources-jar/org/keycloak/models/credential/dto/WebAuthnCredentialData.java

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* /opt/cola/permits/1130030167_1612432999.11/0/keycloak-server-spi-12-0-2-sources-jar/org/keycloak/models/ActionTokenValueModel.java

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* /opt/cola/permits/1130030167_1612432999.11/0/keycloak-server-spi-12-0-2-sources-jar/org/keycloak/storage/role/RoleLookupProvider.java

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org.keycloak.locale.LocaleUpdaterSPI
org.keycloak.storage.UserStorageProviderSpi
org.keycloak.theme.ThemeResourceSpi
org.keycloak.theme.ThemeSelectorSpi
org.keycloak.urls.HostnameSpi

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* /opt/cola/permits/1130030167_1612432999.11/0/keycloak-server-spi-12-0-2-sources-jar/META-INF/services/org.keycloak.provider.Spi

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Eclipse

The following artifacts are EPL.
* org.eclipse.jetty.orbit:org.eclipse.jdt.core

The following artifacts are EPL and ASL2.
* org.eclipse.jetty.orbit:javax.security.auth.message

The following artifacts are EPL and CDDL 1.0.
* org.eclipse.jetty.orbit:javax.mail.glassfish

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Oracle

The following artifacts are CDDL + GPLv2 with classpath exception.
https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

* javax.servlet:javax.servlet-api
* javax.annotation:javax.annotation-api
* javax.transaction:javax.transaction-api
* javax.websocket:javax.websocket-api
Oracle OpenJDK

If ALPN is used to negotiate HTTP/2 connections, then the following artifacts may be included in the distribution or downloaded when ALPN module is selected.

* java.sun.security.ssl

These artifacts replace/modify OpenJDK classes. The modifications are hosted at github and both modified and original are under GPL v2 with classpath exceptions.
http://openjdk.java.net/legal/gplv2+ce.html

OW2

The following artifacts are licensed by the OW2 Foundation according to the terms of http://asm.ow2.org/license.html

org.ow2.asm:asm-commons
org.ow2.asm:asm

Apache

The following artifacts are ASL2 licensed.

org.apache.taglibs:taglibs-standard-spec
org.apache.taglibs:taglibs-standard-impl

MortBay

The following artifacts are ASL2 licensed. Based on selected classes from following Apache Tomcat jars, all ASL2 licensed.

org.mortbay.jasper:apache-jsp
org.apache.tomcat:tomcat-jasper
org.apache.tomcat:tomcat-juli
org.apache.tomcat:tomcat-jsp-api
org.apache.tomcat:tomcat-el-api
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-api
org.apache.tomcat:tomcat-util-scan
org.apache.tomcat:tomcat-util

org.mortbay.jasper:apache-el
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-el-api

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https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

org.eclipse.jetty.toolchain:jetty-schemas

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Assorted

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1.486 gettext 0.19.8.1-r4

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@end enumerate

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@end iftex
@ifinfo
@center END OF TERMS AND CONDITIONS
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@page
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@end example

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@end example
'Gnomovision' (which makes passes at compilers) written by James Hacker.

@var{signature of Ty Coon}, 1 April 1989
Ty Coon, President of Vice
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A. HISTORY OF THE SOFTWARE

Python was created in the early 1990s by Guido van Rossum at Stichting
Mathematisch Centrum (CWI, see http://www.cwi.nl) in the Netherlands
as a successor of a language called ABC. Guido remains Python's
principal author, although it includes many contributions from others.

In 1995, Guido continued his work on Python at the Corporation for
National Research Initiatives (CNRI, see http://www.cnri.reston.va.us)
in Reston, Virginia where he released several versions of the
software.

In May 2000, Guido and the Python core development team moved to
BeOpen.com to form the BeOpen PythonLabs team. In October of the same
year, the PythonLabs team moved to Digital Creations, which became
Zope Corporation. In 2001, the Python Software Foundation (PSF, see
https://www.python.org/psf/) was formed, a non-profit organization
created specifically to own Python-related Intellectual Property.
Zope Corporation was a sponsoring member of the PSF.

All Python releases are Open Source (see http://www.opensource.org for
the Open Source Definition). Historically, most, but not all, Python
releases have also been GPL-compatible; the table below summarizes
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(2) According to Richard Stallman, 1.6.1 is not GPL-compatible, because its license has a choice of law clause. According to CNRI, however, Stallman's lawyer has told CNRI's lawyer that 1.6.1 is "not incompatible" with the GPL.

Thanks to the many outside volunteers who have worked under Guido's direction to make these releases possible.

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1.515 zlib 1.2.11 r3
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1.516 kafka 1.3.5

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1.521 jackson 2.10.5
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Jackson is a high-performance, Free/Open Source JSON processing library. It was originally written by Tatu Saloranta (tatu.saloranta@iki.fi), and has been in development since 2007. It is currently developed by a community of developers, as well as supported commercially by FasterXML.com.

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1.522 codemodel 2.3.3-b02

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## Source Code

The project maintains the following source code repositories:

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* Source: https://github.com/cbeust/testng

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Found in path(s):
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/implementation/bind/ArgumentTypeResolver.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/dynamic/scaffold/MethodRegistry.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/description/modifier/ParameterManifestation.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/description/ModifierReviewable.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/implementation/bind/annotation/IgnoreForBinding.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/implementation/bytecode/assign/primitive/PrimitiveWideningDelegate.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/implementation/bind/inline/RebaseDynamicTypeBuilder.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/matcher/MethodOverrideMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/dynamic/ClassFileLocator.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/dynamic/ClassFileLocator.java

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jar/net/bytebuddy/matcher/EqualityMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/matcher/SignatureTokenMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/implementation/bytecode/assign/package-info.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/implementatio
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jar/net/bytebuddy/implementation/bytecode/assign/primitive/VoidAwareAssigner.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/implementation/bytecode/member/FieldAccess.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/matcher/MethodReturnTypeMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/utility/CompoundList.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/implementation/attribute/AnnotationValueFilter.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/utility/RandomString.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/dynamic/loading/PackageDefinitionStrategy.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/dynamic/scaffold/inline/RedefinitionDynamicTypeBuilder.java
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* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/description/modifier/ModifierContributor.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/matcher/CollectionErasureMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/implementation/attribute/AnnotationAppender.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/implementation/bytecode/constant/DefaultValue.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/dynamic/scaffold/InstrumentedType.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/implementation/bind/ParameterLengthResolver.java
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* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/matcher/CollectionSizeMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/implementation/attribute/package-info.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/ByteBuddy.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/dynamic/scaffold/inline/AbstractInliningDynamicTypeBuilder.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/matcher/DeclaringFieldMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/matcher/ClassLoaderParentMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/matcher/NullMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/matcher/CollectionElementMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/matcher/CollectionSizeMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/matcher/CollectionElementMatcher.java
jar/net/bytebuddy/matcher/PrimitiveTypeMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/implementation/bytecode/member/MethodReturn.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/implementation/MethodAccessorFactory.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/matcher/NameMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/implementation/bytecode/assign/Assigner.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/implementation/auxiliary/TypeProxy.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/agent/builder/LambdaFactory.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/matcher/ModifierMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/utility/StreamDrainer.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/dynamic/scaffold/subclass/SubclassDynamicTypeBuilder.java
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jar/net/bytebuddy/implementation/package-info.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/description/method/MethodDescription.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/matcher/AccessibilityMatcher.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/implementation/bytecode/constant/ClassConstant.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/implementation/bind/annotation/Morph.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/implementation/auxiliary/AuxiliaryType.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
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* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/asm/MemberSubstitution.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/dynamic/VisibilityBridgeStrategy.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/matcher/MethodExceptionTypeMatcher.java
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jar/net/bytebuddy/dynamic/Transformer.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/implementation/bind/annotation/SuperMethod.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/utility/JavaModule.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/description/modifier/SynchronizationState.java
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* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-jar/net/bytebuddy/implementation/auxiliary/MethodCallProxy.java

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jar/net/bytebuddy/jar/asm/Handler.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/TypeReference.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/signature/SignatureReader.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/Symbol.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/Constants.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/ClassWriter.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/SymbolTable.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/ClassVisitor.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/Context.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/ClassReader.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/MethodTooLargeException.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/MethodVisitor.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/ModuleWriter.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/FieldVisitor.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
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* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
jar/net/bytebuddy/jar/asm/FieldWriter.java
* /opt/ws_local/PERMITS_SQL/1013453404_1591357223.5/0/byte-buddy-1-9-11-sources-
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That's all there is to it!

1.526 json-encoder 0.4.4

1.526.1 Available under license:
No license file was found, but licenses were detected in source scan.

Metadata-Version: 1.1
Name: json-encoder
Version: 0.4.4
Summary: json encoder uses singledispatch pattern instead of JSONEncoder class overwrites
Home-page: UNKNOWN
Author: NZME
Author-email: sysadmin@grabone.co.nz
License: UNKNOWN
Description: json-encoder

* json encoder uses `singledispatch pattern` _ instead of JSONEncoder class overwrites.

* No more *json.dumps(data, cls=MyJSONEncoder)* everywhere.

* Comes with default serialization for time, date, datetime, UUID and Decimal

* Easy to use, easy to change serialization behaviour

* Not tight to any json implementation *json, simplejson, ujson* ...
* It parse json float numbers into Decimal objects to prevent python float precision issues.

.. image:: https://travis-ci.org/NZME/json-encoder.svg?branch=master&maxAge=259200
   :target: https://travis-ci.org/NZME/json-encoder

.. image:: https://img.shields.io/pypi/v/json-encoder.svg?maxAge=259200
   :target: https://pypi.python.org/pypi/json-encoder

**Installation**

-------------

.. code-block:: bash

   $ pip install json-encoder

**Quick start**

------------

* Use "json_encoder.json" instead of default python json::

   from json_encoder import json
   
   result = json.dumps(data)

**Configuration**

-------------

* Chose json implementation::

   # simplejson library is used as default json implementation if present
   # otherwise standard python json implementation is used
   # to use other json implementation globally, do:

   import ujson
   from json_encoder import use_json_library

   use_json_library(ujson)

* To change json implementation for concrete call do::

   from json_encoder import json
   import simplejson

   result = json.dumps(data, json=simplejson)

* To make your object JSON serializable do::
# example how to make python fraction object json serializable

from fractions import Fraction
from json_encoder.encoder import json_encoder

@json_encoder.register(Fraction)
def encode_fraction(obj):
    return '{}/{}'.format(obj.numerator, obj.denominator)

* To overwrite JSON serializer behaviour defined in json_encoder.encoder::

    from uuid import UUID
    from six import text_type
    from json_encoder.encoder import json_encoder

    @json_encoder.register(UUID)
def encode_uuid(obj):
        return text_type(obj).replace('-', '')

Requirements
------------

* `singledispatch` >= 3.4.0.3 for python version < 3.4 only

.. _singledispatch pattern: https://docs.python.org/3/library/functools.html#functools.singledispatch
.. _singledispatch: https://bitbucket.org/ambv/singledispatch

Platform: UNKNOWN
Classifier: Development Status :: 3 - Alpha
Classifier: Environment :: Web Environment
Classifier: Intended Audience :: Developers
Classifier: Operating System :: OS Independent
Classifier: Programming Language :: Python
Classifier: Programming Language :: Python :: 2.7
Classifier: Programming Language :: Python :: 3.5

Found in path(s):
* /opt/cola/permits/1158394650_1625142197.8/0/json-encoder-0.4.4.tar.gz/json-encoder-0.4.4/PKG-INFO
* /opt/cola/permits/1158394650_1625142197.8/0/json-encoder-0.4.4.tar.gz/json-encoder-0.4.4/json_encoder.egg-info/PKG-INFO

1.527 wildfly-clustering-marshalling-jboss
21.0.2.Final
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1.528 jre 11.0.9

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version 1.2.5, July 18th, 2005

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Description: Makes the generated copyright headers reproducible
Author: Emmanuel Bourg <ebourg@apache.org>
Forwarded: no

--- a/make/jdk/src/classes/build/tools/cldrconverter/CopyrightHeaders.java
+++ b/make/jdk/src/classes/build/tools/cldrconverter/CopyrightHeaders.java
@@ -26,6 +26,7 @@
package build.tools.cldrconverter;
import java.util.Calendar;
+import java.util.Date;
import java.util.GregorianCalendar;
import java.util.Locale;
import java.util.TimeZone;
@@ -150,8 +151,14 @@
}
private static int getYear() {
-    return new GregorianCalendar(TimeZone.getTimeZone("America/Los_Angeles"),
-                                   Locale.US).get(Calendar.YEAR);
+    Date date = new Date();
+    if (System.getenv("SOURCE_DATE_EPOCH") != null) {
+        date = new Date(1000 * Long.valueOf(System.getenv("SOURCE_DATE_EPOCH")));
+    }
+    GregorianCalendar calendar = new GregorianCalendar(TimeZone.getTimeZone("UTC"), Locale.ENGLISH);
+    calendar.setTime(date);
+    return calendar.get(Calendar.YEAR);
}

// no instantiation
--- a/make/jdk/src/classes/build/tools/generatelsrequivmaps/EquivMapsGenerator.java
+++ b/make/jdk/src/classes/build/tools/generatelsrequivmaps/EquivMapsGenerator.java
@@ -33,9 +33,13 @@
import java.time.ZonedDateTime;
import java.time.ZoneId;
import java.time.ZonedDateTime;
@@ -33,9 +33,13 @@
import java.time.ZonedDateTime;
import java.time.ZoneId;
import java.time.ZonedDateTime;
import java.util.ArrayList;
+import java.util.Calendar;
+import java.util.Date;
+import java.util.GregorianCalendar;
import java.util.List;
import java.util.Locale;
import java.util.Map;
+import java.util.TimeZone;
import java.util.TreeMap;

/**
  @ @ -225,8 +229,15 @@
  + "}"

  private static String getOpenJDKCopyright() {
    int year = ZonedDateTime.now(ZoneId.of("America/Los_Angeles")).getYear();
+    Date date = new Date();
+    if (System.getenv("SOURCE_DATE_EPOCH") != null) {
+      date = new Date(1000 * Long.valueOf(System.getenv("SOURCE_DATE_EPOCH")));
+    }
+    GregorianCalendar calendar = new GregorianCalendar(TimeZone.getTimeZone("UTC"), Locale.ENGLISH);
+    calendar.setTime(date);
+    int year = calendar.get(Calendar.YEAR);
    return String.format(Locale.US, COPYRIGHT, year);
  }

1.529 certifi 2021.5.30
1.529.1 Available under license:

This package contains a modified version of ca-bundle.crt:

ca-bundle.crt -- Bundle of CA Root Certificates

Certificate data from Mozilla as of: Thu Nov 3 19:04:19 2011#
This is a bundle of X.509 certificates of public Certificate Authorities (CA). These were automatically extracted from Mozilla's root certificates file (certdata.txt). This file can be found in the mozilla source tree:
It contains the certificates in PEM format and therefore can be directly used with curl / libcurl / php_curl, or with an Apache+mod_ssl webserver for SSL client authentication.
Just configure this file as the SSLCA CertificateFile.#

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@(#) $RCSfile: certdata.txt,v $ $Revision: 1.80 $ $Date: 2011/11/03 15:11:58 $

1.530 ironjacamar-common-api 1.4.23.Final

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configPropertyConfidential public Boolean getConfigPropertyConfidential(); * Get the confidential id public String
getConfigPropertyConfidentialId();'"

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1.531 cyrus-sasl 2.1.27+dfsg-1+deb10u1

1.531.1 Available under license:

/* CMU libsaasl
 * Tim Martin
 * Rob Earhart
 * Rob Siemborski
 */

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1.532 pcre 8.42-r1

1.532.1 Available under license:

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--------

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The following artifacts are EPL and ASL2.
* org.eclipse.jetty.orbit:javax.security.auth.message

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* org.eclipse.jetty.orbit:javax.mail.glassfish

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https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

* javax.servlet:javax.servlet-api
* javax.annotation:javax.annotation-api
* javax.transaction:javax.transaction-api
* javax.websocket:javax.websocket-api

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Oracle OpenJDK

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* java.sun.security.ssl

These artifacts replace/modify OpenJDK classes. The modifications
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http://openjdk.java.net/legal/gplv2+ce.html

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OW2

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org.ow2.asm:asm-commons
org.ow2.asm:asm

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Apache

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org.apache.taglibs:taglibs-standard-spec
org.apache.taglibs:taglibs-standard-impl

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org.mortbay.jasper:apache-jsp
org.apache.tomcat:tomcat-jasper
org.apache.tomcat:tomcat-juli
org.apache.tomcat:tomcat-jsp-api
org.apache.tomcat:tomcat-el-api
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-api
org.apache.tomcat:tomcat-util-scan
org.apache.tomcat:tomcat-util

org.mortbay.jasper:apache-el
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-el-api

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Mortbay
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https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

org.eclipse.jetty.toolchain:jetty-schemas

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 * <p>The identifier of a client registered within the OAuth2 Authorization Server that will be used to authenticate this server
 * in order to validate bearer tokens arriving to this server.
 * </p>
 * <p>Please note that the client will be usually a confidential client with both an identifier and secret configured in order to authenticate against the token introspection endpoint. In this case, the endpoint must support HTTP BASIC authentication using the client credentials (both id and secret).
 * </p>
 * @param clientId the identifier of a client within the OAuth2 Authorization Server
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 */
**
* Set the `TCP_MD5SIG` option on the socket. See `linux/tcp.h` for more details.
* Keys can only be set on, not read to prevent a potential leak, as they are confidential.
* Allowing them being read would mean anyone with access to the channel could get them.
*

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* /opt/ws_local/PERMITS_SQL/1068253685_1594325782.24/0/netty-transport-native-epoll-4-1-50-final-sources-jar/io/netty/channel/epoll/EpollRecvByteAllocatorStreamingHandle.java
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* /opt/ws_local/PERMITS_SQL/1068253685_1594325782.24/0/netty-transport-native-epoll-4-1-50-final-sources-jar/io/netty/channel/epoll/NativeDatagramPacketArray.java
* /opt/ws_local/PERMITS_SQL/1068253685_1594325782.24/0/netty-transport-native-epoll-4-1-50-final-sources-jar/io/netty/channel/epoll/EpollEventLoop.java

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jar/io/netty/channel/epoll/NativeStaticallyReferencedJniMethods.java
* /opt/ws_local/PERMITS_SQL/1068253685_1594325782.24/0/netty-transport-native-epoll-4-1-50-final-sources-
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* Allowing them being read would mean anyone with access to the channel could get them.
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* Set the {@code TCP_QUICKACK} option on the socket. See <a

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The following artifacts are EPL.
* org.eclipse.jetty.orbit:org.eclipse.jdt.core

The following artifacts are EPL and ASL2.
* org.eclipse.jetty.orbit:javax.security.auth.message

The following artifacts are EPL and CDDL 1.0.
* org.eclipse.jetty.orbit:javax.mail.glassfish

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Oracle

The following artifacts are CDDL + GPLv2 with classpath exception.
https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

* javax.servlet:javax.servlet-api
* javax.annotation:javax.annotation-api
* javax.transaction:javax.transaction-api
* javax.websocket:javax.websocket-api

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Oracle OpenJDK

If ALPN is used to negotiate HTTP/2 connections, then the following artifacts may be included in the distribution or downloaded when ALPN module is selected.

* java.sun.security.ssl

These artifacts replace/modify OpenJDK classes. The modifications are hosted at github and both modified and original are under GPL v2 with classpath exceptions.
http://openjdk.java.net/legal/gplv2+ce.html

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OW2

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org.ow2.asm:asm-commons
org.ow2.asm:asm
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Apache

The following artifacts are ASL2 licensed.

org.apache.taglibs:taglibs-standard-spec
org.apache.taglibs:taglibs-standard-impl

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MortBay

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org.mortbay.jasper:apache-jsp
org.apache.tomcat:tomcat-jasper
org.apache.tomcat:tomcat-juli
org.apache.tomcat:tomcat-jsp-api
org.apache.tomcat:tomcat-el-api
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-api
org.apache.tomcat:tomcat-util-scan
org.apache.tomcat:tomcat-util

org.mortbay.jasper:apache-el
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-el-api

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Mortbay

The following artifacts are CDDL + GPLv2 with classpath exception.

https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

org.eclipse.jetty.toolchain:jetty-schemas

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Assorted

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1.553 wildfly-ormtransformer 21.0.2.Final

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1.555 servlet-api 3.1.0

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<?xml version="1.0"?>
<xsl:stylesheet version="1.0"
   xmlns:xsl="http://www.w3.org/1999/XSL/Transform">
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<table>
<thead>
<tr>
<th>Package</th>
<th>Package Artifact</th>
<th>Package Version</th>
<th>Remote Licenses</th>
<th>Local Licenses</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
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**License Details**

```
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  <xsl:sort select="concat(groupId, '.', artifactId)"/>
  <tr>
    <td><xsl:value-of select="concat(groupId, packageName)"/>
    <td><xsl:value-of select="artifactId"/>
    <td><xsl:value-of select="version"/>
    <td>
    <xsl:for-each select="licenses/license">
      <a href="{./url}"><xsl:value-of select="name"/></a>
    </xsl:for-each>
    </td>
    <td>
    <xsl:for-each select="licenses/license">
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      <xsl:variable name="last-index">
        <xsl:call-template name="last-index-of">
          <xsl:with-param name="txt" select="url"/>
          <xsl:with-param name="delimiter" select="/"/>
        </xsl:call-template>
      </xsl:variable>
      <xsl:variable name="prefix" select="concat($name,' - ')"/>
      <xsl:variable name="postfix" select="substring(url,$last-index+1)"/>
      <xsl:variable name="filename"/>
    </xsl:for-each>
  </td>
</tr>
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  <xsl:text>bsd-2-clause.txt</xsl:text></xsl:when>
<xsl:when test="contains($filename, 'bsd') and contains($filename, '3-clause')">
  <xsl:text>bsd-3-clause.txt</xsl:text></xsl:when>
<xsl:when test="contains($filename, 'apache') and contains($filename, '1.1')">
  <xsl:text>apache-1.1.txt</xsl:text></xsl:when>
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  <xsl:text>apache license 2.0.txt</xsl:text></xsl:when>
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  <xsl:text>cddl-gplv2-classpath.txt</xsl:text></xsl:when>
<xsl:when test="contains($filename, 'common public license')">
  <xsl:text>common public license 1.0.txt</xsl:text></xsl:when>
<xsl:when test="$filename = 'gnu library general public license, version 2 - lgpl-2.0.txt'">
  <xsl:text>gnu library general public license, version 2.txt</xsl:text></xsl:when>
<xsl:when test="$filename = 'the dom4j license - license'">
  <xsl:text>the dom4j license.txt</xsl:text></xsl:when>
<xsl:when test="$filename = 'creative commons attribution 2.5 - legalcode'">
  <xsl:text>creative commons attribution 2.5.html</xsl:text></xsl:when>
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  <xsl:text>cddl-1.1-gpl-1-1.txt</xsl:text></xsl:when>
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<xsl:when test="contains($filename, 'lgpl-2.1')">
  <xsl:text>gnu lesser general public license v2.1 only.txt</xsl:text></xsl:when>
</xsl:when>
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  <xsl:text>gnu general public license, version 2.0.txt</xsl:text>
</xsl:when>
<xsl:when test="contains($filename, 'gnu general public license') and contains($filename, '2.0') and contains($filename, 'exception')">
  <xsl:text>gnu general public license v2.0 only, with classpath exception.txt</xsl:text>
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<xsl:when test="contains($filename, 'gpl-2.0-ce')">
  <xsl:text>gnu general public license v2.0 only, with classpath exception.txt</xsl:text>
</xsl:when>
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  <xsl:text>gnu general public license v2.0 only, with classpath exception.txt</xsl:text>
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  <xsl:text>xstream-bsd.txt</xsl:text>
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  <xsl:text>antlr-bsd.txt</xsl:text>
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  <xsl:text>the antlr 2.7.7 license.txt</xsl:text>
</xsl:when>

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Version 1.1 - 26 February 2007

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* /opt/cola/permits/1130030021_1612432678.93/0/wildfly-elytron-sasl-entity-1-13-1-final-sources-
  jar/org/wildfly/security/sasl/entity/EntitySaslClient.java
* /opt/cola/permits/1130030021_1612432678.93/0/wildfly-elytron-sasl-entity-1-13-1-final-sources-
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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/observers/package-info.java
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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/internal/operators/observable/ObservableJoin.java

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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/internal/operators/flowable/FlowableTake.java
* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/internal/operators/flowable/FlowableAllSingle.java
* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/internal/observers/HashMapSupplier.java
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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/internal/operators/observable/ObservableZipIterable.java
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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/internal/operators/flowable/FlowableSingleSingle.java
* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/internal/operators/maybe/MaybeUnsafeCreate.java
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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/subscribers/ResourceSubscriber.java
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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/core/SingleConverter.java
* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/internal/operators/flowable/FlowableFromPublisher.java
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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/flowable/FlowableObservable.java
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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/flowable/FlowableOnCancelError.java
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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/flowable/FlowableRefCount.java

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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/internal/operators/flowable/FlowableRetryBiPredicate.java

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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/internal/operators/parallel/ParallelFromPublisher.java
* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/internal/operators/single/SingleFromUnsafeSource.java
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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-jar/io/reactivex/rxjava3/internal/operators/mixed/FlowableSwitchMapMaybe.java

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jar/io/reactivex/rxjava3/internal/schedulers/ImmediateThinScheduler.java
* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-
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* /opt/cola/permits/1130030470_1612432673.25/0/rxjava-3-0-4-sources-
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jar/io/reactivex/rxjava3/internal/operators/single/SingleZipIterable.java

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1.561 jetty-util 9.4.33.v20201020

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* javax.annotation:javax.annotation-api
* javax.transaction:javax.transaction-api
* javax.websocket:javax.websocket-api

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Oracle OpenJDK

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* java.sun.security.ssl

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org.ow2.asm:asm-commons
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org.eclipse.jetty.toolchain:jetty-schemas

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  jar/io/netty/channel/DefaultMaxBytesRecvByteBufAllocator.java
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  jar/io/netty/channel/pool/AbstractChannelPoolMap.java
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* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
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  jar/io/netty/channel/group/ChannelGroup.java
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  jar/io/netty/channel/ChannelId.java
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* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
  jar/io/netty/channel/MessageSizeEstimator.java
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  jar/io/netty/channel/ChannelOutboundBuffer.java
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* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
  jar/io/netty/channel/DefaultChannelId.java
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* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
  jar/io/netty/channel/group/ChannelGroupException.java
* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
  jar/io/netty/channel/ChannelProgressivePromise.java
* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
  jar/io/netty/channel/ChannelProgressiveFuture.java
* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
  jar/io/netty/channel/AddressedEnvelope.java
* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
  jar/io/netty/channel/AbstractEventLoopGroup.java
* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
  jar/io/netty/channel/nio/SelectedSelectionKeySet.java
* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
  jar/io/netty/channel/socket/oio/DefaultOioSocketChannelConfig.java
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  jar/io/netty/channel/socket/oio/DefaultOioSocketChannelConfig.java
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 */

/**
 * Handles an I/O event or intercepts an I/O operation, and forwards it to its next handler in
 * its {@link ChannelPipeline}. 
 *
 * <p>
 * {@link ChannelHandler} itself does not provide many methods, but you usually have to implement one of its subtypes:
 * <ul>
 * <li>{@link ChannelInboundHandler} to handle inbound I/O events, and</li>
 * <li>{@link ChannelOutboundHandler} to handle outbound I/O operations.</li>
 * </ul>
 * </p>
 *
 * Alternatively, the following adapter classes are provided for your convenience:
 * <ul>
 * <li>{@link ChannelInboundHandlerAdapter} to handle inbound I/O events.</li>
 * <li>{@link ChannelOutboundHandlerAdapter} to handle outbound I/O operations, and</li>
 * <li>{@link ChannelDuplexHandler} to handle both inbound and outbound events</li>
 * </ul>
* <p>
* For more information, please refer to the documentation of each subtype.
* </p>
*
* <h3>The context object</h3>
*
* A {@link ChannelHandler} is provided with a {@link ChannelHandlerContext} object. A {@link ChannelHandler} is supposed to interact with the
* {@link ChannelPipeline} it belongs to via a context object. Using the
* context object, the {@link ChannelHandler} can pass events upstream or
* downstream, modify the pipeline dynamically, or store the information
* (using [@link AttributeKey]s) which is specific to the handler.
*
* <h3>State management</h3>
*
* A {@link ChannelHandler} often needs to store some stateful information.
* The simplest and recommended approach is to use member variables:
* <pre>
* public interface Message {
*     // your methods here
* }
*
* public class DataServerHandler extends SimpleChannelInboundHandler&lt;Message&gt; {
*     private boolean loggedIn;
* 
*     @Override
*     public void channelRead0(@ChannelHandlerContext ctx, Message message) {
*         if (message instanceof LoginMessage) {
*             authenticate((LoginMessage) message);
*             loggedIn = true;
*         } else if (message instanceof GetDataMessage) {
*             if (loggedIn) {
*                 ctx.writeAndFlush(fetchSecret((GetDataMessage) message));
*             } else {
*                 fail();
*             }
*         }
*     }
* }
* </pre>
* Because the handler instance has a state variable which is dedicated to
* one connection, you have to create a new handler instance for each new
* channel to avoid a race condition where a unauthenticated client can get
* the confidential information:
* <pre>
* // Create a new handler instance per channel.
* // See [@link ChannelInitializer#initChannel(Channel)].
* public class DataServerInitializer extends [@link ChannelInitializer] &lt;[@link Channel] &gt; { 
*   [@code @Override]
*   public void initChannel([@link Channel] channel) { 
*       channel.pipeline().addLast("handler", &lt;new DataServerHandler()&gt;);
*   }
* }
*
* </pre>
*
* &lt;h4&gt;Using [@link AttributeKey]s&lt;/h4&gt;
*
* Although it's recommended to use member variables to store the state of a
* handler, for some reason you might not want to create many handler instances.
* In such a case, you can use [@link AttributeKey]s which is provided by
* [@link ChannelHandlerContext]:
* &lt;pre&gt;
* public interface Message {
*   // your methods here
* }
*}
*
* [@code @Sharable]
* public class DataServerHandler extends [@link SimpleChannelInboundHandler] &lt;Message&gt; { 
*   private final [@link AttributeKey] &lt;[@link Boolean] &gt; auth = 
*     [@link AttributeKey#valueOf(String) AttributeKey.valueOf("auth")];
* }
*
* [@code @Override]
* public void channelRead([@link ChannelHandlerContext] ctx, Message message) { 
*   [@link Attribute] &lt;[@link Boolean] &gt; attr = ctx.attr(auth);
*   if (message instanceof LoginMessage) {
*       authenticate((LoginMessage) o);
*       &lt;b&gt;attr.set(true)&lt;/b&gt;;
*   } else (message instanceof GetDataMessage) { 
*     if (&lt;b&gt;Boolean.TURE.equals(attr.get())&lt;/b&gt;) { 
*       ctx.writeAndFlush(fetchSecret((GetDataMessage) o));
*     } else {
*       fail();
*     }
*   }
* ...
* }
* &lt;/pre&gt;
* Now that the state of the handler is attached to the [@link ChannelHandlerContext], you can add the
* same handler instance to different pipelines:
* &lt;pre&gt;
* public class DataServerInitializer extends [@link ChannelInitializer] &lt;[@link Channel] &gt; { 

```java
private static final DataServerHandler SHARED = new DataServerHandler();

@Override
public void initChannel(Channel channel) {
    channel.pipeline().addLast("handler", SHARED);
}
```

### The `@Sharable` annotation

In the example above which used an `AttributeKey`, you might have noticed the `@Sharable` annotation. If a `ChannelHandler` is annotated with the `@Sharable` annotation, it means you can create an instance of the handler just once and add it to one or more `ChannelPipeline`s multiple times without a race condition. If this annotation is not specified, you have to create a new handler instance every time you add it to a pipeline because it has unshared state such as member variables. This annotation is provided for documentation purpose, just like a [JCIP annotations](http://www.javaconcurrencyinpractice.com/annotations/doc/).

### Additional resources worth reading

Please refer to the `ChannelHandler`, and `ChannelPipeline` to find out more about inbound and outbound operations, what fundamental differences they have, how they flow in a pipeline, and how to handle the operation in your application.

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* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
  jar/io/netty/channel/internal/package-info.java
* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
  jar/io/netty/bootstrap/FailedChannel.java
* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
  jar/io/netty/channel/socket/oio/OioDatagramChannelConfig.java
* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
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* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
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* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
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* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
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  * /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1.jar/io/netty/channel/socket/DefaultServerSocketChannelConfig.java
  * /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1.jar/io/netty/channel/group/ChannelGroupFuture.java
  * /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1.jar/io/netty/channel/socket/nio/NioSocketChannel.java
  * /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1.jar/io/netty/channel/ChannelPromiseNotifier.java
  * /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1.jar/io/netty/channel/oio/package-info.java
  * /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1.jar/io/netty/channel/DefaultChannelPipeline.java
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  * /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1.jar/io/netty/channel/AbstractServerChannel.java
  * /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1.jar/io/netty/channel/local/package-info.java
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  * /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1.jar/io/netty/channel/local/package-info.java
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  * /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
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jar/io/netty/bootstrap/Bootstrap.java
* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-transport-4-1-50-final-sources-1-
jar/io/netty/channel/socket/ServerSocketChannel.java
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jar/io/netty/channel/CompleteChannelFuture.java
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jar/io/netty/bootstrap/package-info.java
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* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-bootstrap/AbstractBootstrapConfig.java
* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-bootstrap/ServerBootstrapConfig.java
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* /opt/ws_local/PERMITS_SQL/1068233910_1594324277.63/0/netty-channel/group/VoidChannelGroupFuture.java
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* /opt/cola/permits/1110674989_1606843959.62/0/hornetq-jms-client-2-4-7-final-sources-3.jar/org/hornetq/jms/client/HornetQXAConnectionFactory.java
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"Source code" for a work means the preferred form of the work for 
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threshold for this to be true is not precisely defined by law.

If such an object file uses only numerical parameters, data
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GCC RUNTIME LIBRARY EXCEPTION

Version 3.1, 31 March 2009

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Alan Beale <biljir@pobox.com> also deserves special credit as he has, in addition to providing the 12Dicts package and being a major contributor to the ENABLE word list, given me an incredible amount of feedback and created a number of special lists (those found in the Supplement) in order to help improve the overall quality of SCOWL.

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From: Brian Kelk <Brian.Kelk@cl.cam.ac.uk>

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1.576 rsync 3.1.3 6
1.576.1 Available under license:

This is Debian's prepackaged version of Andrew Tridgell and Paul Mackerras' rsync utility.

This package provides the rsync program, which is a replacement for rcp that uses the rsync algorithm to transfer only the differences between two sets of files.

This package was put together by Philip Hands <phil@hands.com>, from sources obtained from:
http://rsync.samba.org/ftp/rsync/rsync-2.5.4.tar.gz
The current version was downloaded from:
https://rsync.samba.org/ftp/rsync/src/rsync-3.1.3.tar.gz
on 2018-12-02 by Samuel Henrique <samueloph@debian.org>.

The changes were very minimal - merely adding support for the Debian package maintenance scheme by adding various debian/* files. The only significant change is passing the -4 / -6 options through to ssh. See the debian/patches/ directory.

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Version 3, 29 June 2007

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* /opt/cola/permits/1135869399_1613618193.6/0/javassist-3-25-0-ga-sources-3.jar/javassist/CtPrimitiveType.java
* /opt/cola/permits/1135869399_1613618193.6/0/javassist-3-25-0-ga-sources-3.jar/javassist/bytecode/MethodInfo.java
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* /opt/cola/permits/1135869399_1613618193.6/0/javassist-3-25-0-ga-sources-3.jar/javassist/compiler/ast/Visitor.java
* /opt/cola/permits/1135869399_1613618193.6/0/javassist-3-25-0-ga-sources-3.jar/javassist/util/proxy/ProxyObjectOutputStream.java
* /opt/cola/permits/1135869399_1613618193.6/0/javassist-3-25-0-ga-sources-3.jar/javassist/compiler/Javac.java
* /opt/cola/permits/1135869399_1613618193.6/0/javassist-3-25-0-ga-sources-3.jar/javassist/compiler/CodeConverter.java
* /opt/cola/permits/1135869399_1613618193.6/0/javassist-3-25-0-ga-sources-3.jar/javassist/bytecode/ByteArray.java
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jar/javaassist/bytecode/SyntheticAttribute.java
* /opt/cola/permits/1135869399_1613618193.6/0/javaassist-3-25-0-ga-sources-3-jar/javaassist/expr/ExprEditor.java
* /opt/cola/permits/1135869399_1613618193.6/0/javaassist-3-25-0-ga-sources-3-jar/javaassist/compiler/ProceedHandler.java
* /opt/cola/permits/1135869399_1613618193.6/0/javaassist-3-25-0-ga-sources-3-jar/javaassist/scopedpool/ScopedClassPoolFactoryImpl.java
* /opt/cola/permits/1135869399_1613618193.6/0/javaassist-3-25-0-ga-sources-3-jar/javaassist/convert/TransformNew.java
* /opt/cola/permits/1135869399_1613618193.6/0/javaassist-3-25-0-ga-sources-3-jar/javaassist/bytecode/LineNumberAttribute.java
* /opt/cola/permits/1135869399_1613618193.6/0/javaassist-3-25-0-ga-sources-3-jar/javaassist/bytecode/analysis/Subroutine.java
* /opt/cola/permits/1135869399_1613618193.6/0/javaassist-3-25-0-ga-sources-3-jar/javaassist/CtField.java
* /opt/cola/permits/1135869399_1613618193.6/0/javaassist-3-25-0-ga-sources-3-jar/javaassist/bytecode/LineNumberAttribute.java
* /opt/cola/permits/1135869399_1613618193.6/0/javaassist-3-25-0-ga-sources-3-jar/javaassist/bytecode/ClassFile.java
* /opt/cola/permits/1135869399_1613618193.6/0/javaassist-3-25-0-ga-sources-3-jar/javaassist/Modifier.java
* /opt/cola/permits/1135869399_1613618193.6/0/javaassist-3-25-0-ga-sources-3-jar/javaassist/tools/rmi/RemoteException.java
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* /opt/cola/permits/1135869399_1613618193.6/0/javassist-3-25-0-ga-sources-3-jar/javassist/bytecode/annotation/ByteMemberValue.java
* /opt/cola/permits/1135869399_1613618193.6/0/javassist-3-25-0-ga-sources-3-jar/javassist/bytecode/annotation/EnumMemberValue.java
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* /opt/cola/permits/1135869399_1613618193.6/0/javassist-3-25-0-ga-sources-3-jar/javassist/bytecode/annotation/AnnotationMemberValue.java

1.578 tzdata 2018g-r1

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1.591 wildfly-clustering-ejb-infinispan

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1.592 jaxb-jxc 2.3.3-b02

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1.593 tre 0.8.0
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/*
  tre-python.c - TRE Python language bindings

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Metadata-Version: 1.0
Name: tre
Version: 0.8.0
Summary: Python module for TRE
Home-page: http://laurikari.net/tre/
Author: Ville Laurikari
Author-email: ville@laurikari.net
License: 2-clause BSD
Description: UNKNOWN
Platform: UNKNOWN

Found in path(s):
*/opt/cola/permits/1136308694_1613734944.8/0/tre-0-8-0-2-tar-gz/tre-0.8.0/PKG-INFO

1.594 cxf-rt-databinding-aegis 3.3.7
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1.598 infinispan-commons 11.0.4.Final

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Found in path(s):
* /opt/cola/permits/1130030789_1612433189.8/0/infinispan-commons-11-0-4-final-sources-
jar/org/infinispan/commons/configuration/Json.java
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#
# The table below contains both registered and (common) unregistered types.
# A type that has no unique extension can be ignored -- they are listed
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# content languages and encodings, so choose them carefully.
#
# Internet media types should be registered as described in RFC 4288.
# The registry is at <http://www.iana.org/assignments/media-types/>.
#
# MIME type (lowercased)Extensions
# ================================================================
application/1d-interleaved-parityfec
application/3gpdsdash-qoe-report+xml
application/3gpp-ims+xml
application/a2l
application/activemessage
application/alto-costmap+json
application/alto-costmapfilter+json
application/alto-directory+json
application/alto-endpointcost+json
application/alto-endpointcostparams+json
application/alto-endpointprop+json
application/alto-endpointpropparams+json
application/alto-error+json
application/alto-networkmap+json
application/alto-networkmapfilter+json
application/aml
application/andrew-insetez
application/applefile
application/dec-dx
application/dialog-info+xml
application/dicom
application/dii
application/dit
application/dns
application/docbook+xml
application/dskpp+xml
application/dssc+der
application/dssc+xml
application/dvcs
application/ecmascript
application/edi-consent
application/edi-x12
application/edifact
application/efi
application/emergencycalldata.comment+xml
application/emergencycalldata.deviceinfo+xml
application/emergencycalldata.providerinfo+xml
application/emergencycalldata.serviceinfo+xml
application/emergencycalldata.subscriberinfo+xml
application/emma+xml
application/emotionxml+xml
application/encaprtp
application/epp+xml
application/epub+zip
application/eshop
application/example
application/exi
application/fastinfose
application/fastsoap
application/fdt+xml
application/fits
application/font-tdpfr
application/framework-attributes+xml
application/geo+json
application/gml+xml
application/gpx+xml
application/gxf
application/gzip
application/h224
application/held+xml
application/http
application/hyperstudio
application/ibe-key-request+xml
application/ibe-pkg-reply+xml
application/ibe-pp-data
application/iges
application/im-iscomposing+xml
application/index
application/index.cmd
application/index.obj
application/index.response
application/index.vnd
application/inkml+xml
application/iotp
application/ipfix
application/ipp
application/isup
application/its+xml
application/java-archive
application/java-serialized-object
application/java-vm
application/javascript
application/jose
application/jose+json
application/jrd+json
application/json
application/json-check
application/json-ld+json
application/json-patch+json
application/json-seq
application/json+json
application/jsonml+json
application/jwk+json
application/jwk-set+json
application/jwt
application/kpml-request+xml
application/kpml-response+xml
application/l+json
application/lgr+xml
application/link-format
application/load-control+xml
application/lost+xml
application/lostsync+xml
application/lxf
application/mac-binhex40
application/mac-compactpro
application/macwriteii
application/mads+xml
application/marc+xml
application/marcxml+xml
application/mathematica
application/mathml+xml
application/mathml-content+xml
application/mathml-presentation+xml
application/mbms-associate procedure-description+xml
application/mbms-deregister+xml
application/mbms-envelope+xml
application/mbms-msk+xml
application/mbms-msk-response+xml
application/mbms-protection-description+xml
application/mbms-reception-report+xml
application/mbms-register+xml
application/mbms-register-response+xml
application/mbms-schedule+xml
application/mbms-user-service-description+xml
application/mbox
application/media-policy-dataset+xml
application/media_control+xml
application/mediaservercontrol+xml
application/merge-patch+json
application/metalink+xml
application/metalink4+xml
application/mets+xml
application/mf4
application/mikey
application/mods+xml
application/moss-keys
application/moss-signature
application/mosskey-data
application/mosskey-request
application/mp21
application/mp4
application/mpeg4-generic
application/mpeg4-iod
application/mpeg4-iod-xmt
application/mrb-consumer+xml
application/mrb-publish+xml
application/msc-ivr+xml
application/msc-mixer+xml
application/msword
application/mxf
application/nasdata
application/news-checkgroups
application/news-groupinfo
application/news-transmission
application/nlsml+xml
application/nss
application/ocsp-request
application/ocsp-response
application/octet-stream
application/oda
application/odx
application/oebps-package+xml
application/ogx
application/omdoc+xml
application/omdoc
Open Source Used In Branch Migration Tool Spirit

5529
application/x-xfig
application/x-xliff+xml
application/x-xmllang
application/x-xmllang+xml
application/x-xpinstall
application/x-xz
application/x-zmachine
application/x400-bp
application/xacml+xml
application/xaml+xml
application/xcap-att+xml
application/xcap-caps+xml
application/xcap-diff+xml
application/xcap-el+xml
application/xcap-error+xml
application/xcap-ns+xml
application/xcon-conference-info+xml
application/xcon-conference-info-diff+xml
application/xhtml+xml
application/xhtml-voice+xml
application/xml
application/xml-dtd
application/xml-external-parsed-entity
application/xml-patch+xml
application/xmpp+xml
application/xop+xml
application/xproc+xml
application/xslt+xml
application/xspf+xml
application/xv+xml
application/yang
application/yin+xml
application/zip
application/zlib
audio/1d-interleaved-parityfec
audio/32kadpcm
audio/3gpp
audio/3gpp2
audio/ac3
audio/adpcm
audio/amr
audio/amr-wb
audio/amr-wb+
audio/aptx
audio/asc
audio/atrac-advanced-lossless
audio/atrac-x
audio/atrac3
audio/basic
audio/snd
audio/bv16
audio/bv32
audio/clearmode
audio/cn
audio/dat12
audio/dls
audio/dsr-es201108
audio/dsr-es202050
audio/dsr-es202211
audio/dsr-es202212
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audio/evrc
audio/evrc-qcp
audio/evrc0
audio/evrc1
audio/evrcb
audio/evrcb0
audio/evrcb1
audio/evrcnw
audio/evrcnw0
audio/evrcnw1
audio/evrcwb
audio/evrcwb0
audio/evrcwb1
audio/evs
audio/example
audio/fwdred
audio/g711-0
audio/g719
audio/g722
audio/g7221
audio/g723
audio/g726-16
audio/g726-24
audio/g726-32
audio/g726-40
audio/g728
audio/g729
audio/g7291
audio/g729d
audio/g729e
audio/gsm
audio/gsm-efr
audio/gsm-hr-08
audio/ilbc
audio/ip-mr_v2.5
audio/isac
audio/116
audio/l20
audio/124
audio/18
audio/lpc
audio/midimid midi kar rmi
audio/mobile-xmf
audio/mp4m4a mp4a
audio/mp4a-latm
audio/mpa
audio/mpla-robust
audio/mpegmpga mp2 mp2a mp3 m2a m3a
audio/mpeg4-generic
audio/musepack
audio/oggoga ogg spx
audio/opus
audio/parityfec
audio/pcm a
audio/pcma-wb
audio/pcm a
audio/pcm u
audio/pcm u-wb
audio/prs.sid
audio/qcelp
audio/raptorfec
audio/red
audio/rtp-enc-aescm128
audio/rtp-midi
audio/rtploopback
audio/rtx
audio/s3ms3m
audio/silsil
audio/smv
audio/smv-qcp
audio/smv0
audio/sp-midi
audio/speex
audio/t140c
audio/t38
audio/telephone-event
audio/tone
audio/uemclip
audio/ulpfec
audio/vdvi
audio/vmr-wb
audio/vnd.3gpp.iufp
audio/vnd.4sb
message/feedback-report
message/global
message/global-delivery-status
message/global-disposition-notification
message/global-headers
message/http
message/imdn+xml
message/news
message/partial
message/rfc822eml mime
message/s-http
message/sip
message/sipfrag
message/tracking-status
message/vnd.simp
message/vnd.wfa.wsc
model/example
model/gltf+json
model/iges
model/mesh mesh silo
model/vnd.collada+xml
model/vnd.dwf
model/vnd.flatland.3dml
model/vnd.gdl
model/vnd.gs-gdl
model/vnd.moml+xml
model/vnd.mts
model/vnd.opengex
model/vnd.parasolid.transmit.binary
model/vnd.parasolid.transmit.text
model/vnd.rosette.annotated-data-model
model/vnd.valve.source.compiled-map
model/vnd.vtu
model/vrml
model/vrml
model/x3d+binaryx3db x3dbz
model/x3d+fastinfoset
model/x3d+vrmlx3dv x3dvz
model/x3d+xml
model/x3dv
model/x3d-vrml
multipart/alternative
multipart/appledouble
multipart/byteranges
multipart/digest
multipart/encrypted
multipart/example
multipart/form-data
multipart/header-set
multipart/mixed
multipart/parallel
multipart/related
multipart/report
multipart/signed
multipart/voice-message
multipart/x-mixed-replace
text/1d-interleaved-parityfec
text/cache-manifestappcache
text/calendarics ifb
text/csscss
text/csvcsv
text/csv-schema
text/directory
text/dns
text/ecmascript
text/encaprttp
text/enriched
text/example
text/fwdred
text/grammar-ref-list
text/htmlhtml html
text/javascript
text/jcr-cnd
text/markdown
text/mizar
text/n3n3
text/parameters
text/parityfec
text/plaintext text/conf def list log in
text/provenance-notation
text/prs.fallenstein.rst
text/prs.lines.tagdsc
text/prs.prop.logic
text/raptorfec
text/red
text/rfc822-headers
text/richtextrtx
text/rtf
text/rtp-enc-aescm128
text/rtploopback
text/rtx
text/sgmlsgml sgm
text/t140
text/tab-separated-values tsv
text/troff tr roff man me ms
text/turtle
video/3gpp-tt
video/3gpp23g2
video/bmpega
video/bt656
video/celb
video/dv
video/encaprtpt
video/example
video/h261h261
video/h263h263
video/h263-1998
video/h263-2000
video/h264h264
video/h264-rcdo
video/h264-svc
video/h265
video/iso.segment
video/jpegjgp
video/jpeg2000
video/jpmjpm jpm
video/mj2mj2 mj2
video/mp1s
video/mp2p
video/mp2t
video/mp4mp4 mp4v mpg4
video/mp4v-es
video/mpegmpeg mpg m1v m2v
video/mpeg4-generic
video/mpv
video/nv
video/oggogv
video/parityfec
video/pointer
video/quicktimeqt mov
video/raptorfec
video/raw
video/rtp-enc-aescm128
video/rtploopback
video/rtx
video/smpte292m
video/ulpfec
video/vcl
video/vnd.cctv
video/vnd.dece.hduvh uvvh
video/vnd.dece.mobileuvum uvvm
video/vnd.dece.mp4
video/vnd.dece.pduvp uvvp
video/vnd.dece.sduvs uvvs
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= isConfidentialTransportGuarantee(dep, ep); int currentPort = port.getValue(confidential); Integer hostPort =
getServerConfig().getVirtualHostPort(ep.getService().getVirtualHost(), confidential); String protocol = confidential
? "https://" : "http://"; protected boolean isConfidentialTransportGuarantee(final Deployment dep, final Endpoint ep)
// Fix for JBWS-4196/WFLY-12135. We pick up the attached boolean. If it's true then
isConfidentialTransportGuarantee is true return "CONFIDENTIAL".equals(transportGuarantee); return
"CONFIDENTIAL".equals(transportGuarantee); public Integer getValue(boolean confidential) { return confidential
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1.607 substring 0.2

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Metadata-Version: 1.1
Name: substring
Version: 0.2
Summary: Multi-Operational and Flexible Substring Package
Home-page: https://github.com/VETURISIRAM/SUBSTRING
Author: Sriram Veturi
Author-email: sriram.tutu@gmail.com
License: MIT
Description: #SUBSTRING Version 0.2

##Multi-Operational and Flexible Substring Package

This is indeed a need for the developer community to experience such simple, easy-to-use and extremely user friendly Python package which does your usual job of cutting out a piece of substring from the parent string without writing certain lines of code. Nobody wants to spend their valuable time in writing such simple code when they can work on the bigger and other important contributions to the developers' community. This package has the following two methods associated with it:

###1) substringByChar()

It has four parameters namely, initialString, startChar, endChar, and stepSize(default=1). It would spit out the substring on the basis of the characters entered. For example, consider a string "abcdefghijklmnopqrstuvwxyz" and I can pull out the substring "defghijkl" by just specifying the start and end characters as "d" and "l" respectively. It has also the feature of step size where you can change and get your substrings accordingly.

###2) substringByInd()

It has four parameters namely, initialString, startInd, endInd, and stepSize(default=1). It would spit out the substring on the basis of the indices entered. For example, consider a string "abcdefghijklmnopqrstuvwxyz" and I can pull out the substring "defghijkl" by just specifying the start and end indices as 3 and 11 respectively because
"d" and "l" represent the indices 3 and 11 respectively. It has also the feature of step size where you can change and get your substrings accordingly.

####This package is "Multi-Operational" because it not only gets you the substring of your choice with such ease but also allows you to play around with the step sizes that you want. For example, consider the same string "abcdefghijklmnopqrstuvwxyz", and you can pull out "aceg" by entering the startChar, endChar, stepSize as "a", "g" and 2 respectively.

####With such ease of use, this package efficiently handles all the exceptions caused and lets the user know about them which makes the user experience very rich.

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from setuptools import setup

with open("README.rst", 'r') as f:
    longDescription = f.read()

setup(name='substring',
      version='0.2',
      description='Multi-Operational and Flexible Substring Package',
      long_description=longDescription,
      url='https://github.com/VETURISRIRAM/SUBSTRING',
      author='Sriram Veturi',
      author_email='sriram.tutu@gmail.com',
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      packages=['substring'],
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"Programming Language :: Python :: 3",
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* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-
  jar/io/netty/channel/socket/oio/package-info.java
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* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-
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* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-
  jar/io/netty/channel/EventLoopGroup.java

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* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-jar/io/netty/channel/AbstractServerChannel.java
* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-jar/io/netty/channel/ChannelOutboundHandler.java
* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-jar/io/netty/channel/ChannelException.java
* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-jar/io/netty/channel/socket/nio/NioDatagramChannel.java
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* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-jar/io/netty/channel/AbstractChannelHandlerContext.java
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* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-jar/io/netty/channel/nio/package-info.java
* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-jar/io/netty/channel/socket/nio/NioSocketChannel.java
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* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-jar/io/netty/channel/nio/NioEventLoopGroup.java
* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-jar/io/netty/channel/group/ChannelGroupFutureListener.java
* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-jar/io/netty/channel/EventLoop.java
* /opt/ws_local/PERMITS_SQL/1072948476_1595240756.51/0/netty-transport-4-1-51-final-sources-jar/io/netty/channel/group/ChannelGroupFuture.java
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jar/io/netty/channel/socket/ChannelOutputShutdownException.java
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* Handles an I/O event or intercepts an I/O operation, and forwards it to its next handler in
  * its [@link ChannelPipeline].
  *
  * <h3>Sub-types</h3>
  *
  * [@link ChannelHandler] itself does not provide many methods, but you usually have to implement one of its
  * subtypes:
  *
  * <ul>
  * <li>[@link ChannelInboundHandler] to handle inbound I/O events, and</li>
  * <li>[@link ChannelOutboundHandler] to handle outbound I/O operations.</li>
  * </ul>
  *
  * <p>
  *
  * Alternatively, the following adapter classes are provided for your convenience:
  *
  * <ul>
  * <li>[@link ChannelInboundHandlerAdapter] to handle inbound I/O events,</li>
  * <li>[@link ChannelOutboundHandlerAdapter] to handle outbound I/O operations, and</li>
  * <li>[@link ChannelDuplexHandler] to handle both inbound and outbound events</li>
  * </ul>
  *
  * <p>
  *
  * For more information, please refer to the documentation of each subtype.
  *
  *
  *
  * <h3>The context object</h3>
  *
  * <p>
  *
  * A [@link ChannelHandler] is provided with a [@link ChannelHandlerContext] object. A [@link ChannelHandler]
  * is supposed to interact with the
  * [@link ChannelPipeline] it belongs to via a context object. Using the
  * context object, the [@link ChannelHandler] can pass events upstream or
  * downstream, modify the pipeline dynamically, or store the information
  * (using [@link AttributeKey]s) which is specific to the handler.
  *
  *
  * <h3>State management</h3>
  *
  * A [@link ChannelHandler] often needs to store some stateful information.
  *
  * The simplest and recommended approach is to use member variables:
  *
  * <pre>
  * public interface Message {
  *     // your methods here
  * }
  * */

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*/

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*/
* public class DataServerHandler extends [@link SimpleChannelInboundHandler]\&Message\{ 
*
*     private boolean loggedIn;
* 
*     [@code @Override]
*     public void channelRead0([@link ChannelHandlerContext] ctx, Message message) {
*         if (message instanceof LoginMessage) {
*             authenticate((LoginMessage) message);
*             loggedIn = true;
*         } else (message instanceof GetDataMessage) {
*             if (loggedIn) {
*                 ctx.writeAndFlush(fetchSecret((GetDataMessage) message));
*             } else {
*                 fail();
*             }
*         }
*         ...
* }  
* </pre>

* Because the handler instance has a state variable which is dedicated to
* one connection, you have to create a new handler instance for each new
* channel to avoid a race condition where a unauthenticated client can get
* the confidential information:
* <pre>
* // Create a new handler instance per channel.
* // See [@link ChannelInitializer\#initChannel(Channel)].
* public class DataServerInitializer extends [@link ChannelInitializer]\&{@link Channel}\{ 
*     [@code @Override]
*     public void initChannel([@link Channel] channel) {
*         channel.pipeline().addLast("handler", new DataServerHandler());
*     }
* }  
* </pre>

* <h4>Using [@link AttributeKey]s</h4>

* Although it's recommended to use member variables to store the state of a
* handler, for some reason you might not want to create many handler instances.
* In such a case, you can use [@link AttributeKey]s which is provided by
* [@link ChannelHandlerContext]:
* <pre>
* public interface Message {
*     // your methods here
* }
* 
* {@code @Sharable}
* public class DataServerHandler extends {@link SimpleChannelInboundHandler}@Message&gt; {
*   private final {@link AttributeKey}@{@link Boolean}&gt; auth =
*       {@link AttributeKey#@valueOf(String) AttributeKey.valueOf("auth")};
*   
*   {@code @Override}
*   public void channelRead({@link ChannelHandlerContext} ctx, Message message) {
*     {@link Attribute}@{@link Boolean}&gt; attr = ctx.attr(auth);
*     if (message instanceof LoginMessage) {
*       authenticate((LoginMessage) o);
*       &lt;b&gt;attr.set(true)&lt;/b&gt;;
*     } else (message instanceof GetDataMessage) {
*       if (&lt;b&gt;Boolean.TRUE.equals(attr.get())&lt;/b&gt;) {
*         ctx.writeAndFlush(fetchSecret((GetDataMessage) o));
*       } else {
*         fail();
*       }
*     }
*     ... ...
*   }
* </pre>
* Now that the state of the handler is attached to the {@link ChannelHandlerContext}, you can add the same handler instance to different pipelines:
* &lt;pre&gt;
* public class DataServerInitializer extends {@link ChannelInitializer}@{@link Channel}&gt; {
*   
*   private static final DataServerHandler &lt;b&gt;SHARED&lt;/b&gt; = new DataServerHandler();
*   
*   {@code @Override}
*   public void initChannel({@link Channel} channel) {
*     channel.pipeline().addLast("handler", &lt;b&gt;SHARED&lt;/b&gt;);
*   }
* </pre>
* 
* &lt;h4&gt;The {@code @Sharable} annotation&lt;/h4&gt;
* &lt;p&gt;
* In the example above which used an {@link AttributeKey},
* you might have noticed the {@code @Sharable} annotation.
* &lt;p&gt;
* If a {@link ChannelHandler} is annotated with the {@code @Sharable}
* annotation, it means you can create an instance of the handler just once and add it to one or more {@link ChannelPipeline}s multiple times without
* a race condition.
* &lt;p&gt;
* If this annotation is not specified, you have to create a new handler
* instance every time you add it to a pipeline because it has unshared state
* such as member variables.

* This annotation is provided for documentation purpose, just like


* <h3>Additional resources worth reading</h3>

* Please refer to the [@link ChannelHandler], and

* [@link ChannelPipeline] to find out more about inbound and outbound operations,

* what fundamental differences they have, how they flow in a pipeline, and how to handle

* the operation in your application.

*/

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* org.eclipse.jetty.orbit:javax.mail.glassfish

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* javax.servlet:javax.servlet-api
* javax.annotation:javax.annotation-api
* javax.transaction:javax.transaction-api
* javax.websocket:javax.websocket-api

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Oracle OpenJDK

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* java.sun.security.ssl

These artifacts replace/modify OpenJDK classes. The modifications are hosted at github and both modified and original are under GPL v2 with classpath exceptions.
http://openjdk.java.net/legal/gplv2+ce.html

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org.ow2.asm:asm-commons
org.ow2.asm:asm

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Apache

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org.apache.taglibs:taglibs-standard-spec
org.apache.taglibs:taglibs-standard-impl

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org.mortbay.jasper:apache-jsp
org.apache.tomcat:tomcat-jasper
org.apache.tomcat:tomcat-juli
org.apache.tomcat:tomcat-jsp-api
org.apache.tomcat:tomcat-el-api
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-api
org.apache.tomcat:tomcat-util-scan
org.apache.tomcat:tomcat-util

org.mortbay.jasper:apache-el
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-el-api

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The following artifacts are CDDL + GPLv2 with classpath exception.

https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

org.eclipse.jetty.toolchain:jetty-schemas

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Assorted

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jar/org/wildfly/security/auth/principal/RealmNestedPrincipal.java
* /opt/cola/permits/1130030592_1612433495.22/0/wildfly-elytron-auth-1-13-1-final-sources-
jar/org/wildfly/security/auth/principal/NumericPrincipal.java
* /opt/cola/permits/1130030592_1612433495.22/0/wildfly-elytron-auth-1-13-1-final-sources-
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1.618 zstd 1.4.0

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Jackson is a high-performance, Free/Open Source JSON processing library. It was originally written by Tatu Saloranta (tatu.salaranta@iki.fi), and has been in development since 2007. It is currently developed by a community of developers, as well as supported commercially by FasterXML.com.

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1.626 wildfly-elytron-mechanism-scram

1.13.1.Final

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org.keycloak.provider.wildfly.WildflyCacheManagerProvider

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org.keycloak.provider.wildfly.WildflyPlatform

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org.keycloak.provider.wildfly.ModuleThemeProviderFactory

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1.629 coverage 4.5.1
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Coverage.py was originally written by Gareth Rees, and since 2004 has been
extended and maintained by Ned Batchelder.

Other contributions, including writing code, updating docs, and submitting
useful bug reports, have been made by:

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Alex Gaynor
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1.630 perl 5.28.1-6+deb10u1

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cpan/Locale-Maketext-Simple/t/po_with_i_default/en.po
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dist/ExtUtils-Install/*
dist/Math-BigInt/*
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dist/ExtUtils-Command/*
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dist/I18N-Collate/*
dist/Safe/*
ext/Fcntl/*
ext/FileCache/*
ext/GDBM_File/*
ext/IPC-Open2/*
ext/IPC-Open3/*
ext/NDBM_File/*
ext/ODBM_File/*
ext/Opcode/*
ext/PerlIO-encoding/*
ext/PerlIO-scalar/*
ext/PerlIO-via/*
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The snowball stemmers in
   analysis/common/src/java/net/sf/snowball
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   http://snowball.tartarus.org/

The KStem stemmer in
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analysis/common/src/resources/org/apache/lucene/analysis/ro/stopwords.txt,
analysis/common/src/resources/org/apache/lucene/analysis/bg/stopwords.txt,  
analysis/common/src/resources/org/apache/lucene/analysis/hi/stopwords.txt  

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analysis/common/src/java/org/apache/lucene/analysis/de/GermanMinimalStemmer.java  
analysis/common/src/java/org/apache/lucene/analysis/es/SpanishLightStemmer.java  
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analysis/common/src/java/org/apache/lucene/analysis/pt/PortugueseLightStemmer.java  
analysis/common/src/java/org/apache/lucene/analysis/ru/RussianLightStemmer.java  
analysis/common/src/java/org/apache/lucene/analysis/sv/SwedishLightStemmer.java

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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/internal/storage/pack/PackWriter.java

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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/util/References.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/util/Stats.java

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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/errors/ObjectWritingException.java
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 */
/**
 * A special exception thrown when [@link AutoLFInputStream] is told to
 * throw an exception when attempting to read a binary file. The exception
 * may be thrown at any stage during reading.
 *
 * @since 3.3
 */

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  jar/org/eclipse/jgit/transport/PushProcess.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009090501-r-sources-
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/notes/NotesMergeConflictException.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/internal/transport/http/NetscapeCookieFile.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/util/LRUMap.java
  
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/transport/WalkFetchConnection.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/util/StringUtils.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/transport/resolver/RepositoryResolver.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/util/io/StreamCopyThread.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/transport/resolver/ServiceNotAuthorizedException.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/internal/storage/file/PackBitmapIndexRemapper.java
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*/opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/util/io/IsolatedOutputStream.java
*/opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/internal/storage/reftree/Scanner.java
*/opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/transport/WantNotValidException.java
*/opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/internal/ketch/LagCheck.java
*/opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/util/time/ProposedTimestamp.java

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/**
 * Fetch objects we don't have but that are reachable from advertised refs.
 * @param monitor progress monitor to inform the end-user about the amount of
 * work completed, or to indicate cancellation. Implementations should poll
 * the monitor at regular intervals to look for cancellation requests from the
 * user.
 * @param want one or more refs advertised by this connection that the caller
 * wants to store locally.
 * @param have additional objects known to exist in the destination
 */
repository, especially if they aren't yet reachable by the ref database. Connections should take this set as an addition to what is reachable through all Refs, not in replace of it.

@throws org.eclipse.jgit.errors.TransportException objects could not be copied due to a network failure, protocol error, or error on remote side, or connection was already used for fetch.

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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/util/AttributesHandler.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/lib/TextProgressMonitor.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/lib/ProgressMonitor.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/revwalk/OrRevFilter.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/revwalk/OrTreeFilter.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/revwalk/OrTreeFilter.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/revwalk/AndRevFilter.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/revwalk/PathFilterGroup.java
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  * /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/merge/MergeAlgorithm.java
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  * /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/errors/TransportException.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/revwalk/BitmappedReachabilityChecker.java

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/**
 * [@inheritdoc]
 * <p>
 * Free resources associated with this instance.
 */
* <p>
* If the repository was opened by a static factory method in this class,
* then this method calls [@link Repository#close()] on the underlying
* repository instance. (Whether this actually releases underlying
* resources, such as file handles, may vary; see [@link Repository] for
* more details.)
* <p>
* If the repository was created by a caller and passed into
* [@link #Git(Repository)] or a static factory method in this class, then
* this method does not call close on the underlying repository.
* <p>
* In all cases, after calling this method you should not use this
* [@link Git] instance anymore.
* 
* @since 3.2
*/

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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/transport/BundleWriter.java
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jar/org/eclipse/jgit/api/CheckoutResult.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/revplot/PlotLane.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/lib/RefUpdate.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/lib/ObjectChecker.java

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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/dircache/DirCacheEditor.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/dircache/DirCacheBuilder.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources.jar/org/eclipse/jgit/internal/storage/reftable/BlockReader.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources.jar/org/eclipse/jgit/internal/storage/reftable/BlockSource.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources.jar/org/eclipse/jgit/internal/storage/reftable/ReftableConstants.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources.jar/org/eclipse/jgit/internal/fsck/FsckError.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources.jar/org/eclipse/jgit/internal/fsck/FsckReaderIoStats.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources.jar/org/eclipse/jgit/internal/fsck/FsckReaderIoStats.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/lib/SubmoduleConfig.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/util/FS_POSIX.java

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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/errors/UnsupportedCredentialItem.java
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jar/org/eclipse/jgit/lib/TypedConfigGetter.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/submodule/SubmoduleStatus.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/api/SubmoduleInitCommand.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/api/SubmoduleSyncCommand.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/submodule/SubmoduleStatusType.java

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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/transport/ReceiveCommandErrorHandler.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/internal/storage/file/InflatingBitSet.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/revwalk/BitmapWalker.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/lib/BitmapObject.java
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  jar/org/eclipse/jgit/diff/HistogramDiff.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/util/io/NullOutputStream.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources.jar/org/eclipse/jgit/gitrepo/ManifestParser.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources.jar/org/eclipse/jgit/transport/PushCertificateStore.java
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/revwalk/LIFORevQueue.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/revwalk/FixUninterestingGenerator.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/revwalk/filter/PatternMatchRevFilter.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/revwalk/PendingGenerator.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/util/CachedAuthenticator.java
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  jar/org/eclipse/jgit/api/StashDropCommand.java
* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-
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* /opt/cola/permits/1097482754_1602076455.8/0/org-eclipse-jgit-5-9-0-202009080501-r-sources-jar/org/eclipse/jgit/api/RemoteSetUrlCommand.java

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1.659 wildfly-elytron-mechanism-http

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1.674 wildfly-web-common 21.0.2.Final

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* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
  jar/io/netty/handler/codec/serialization/ObjectDecoder.java
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  jar/io/netty/handler/codec/marshalling/MarshallingDecoder.java
* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
  jar/io/netty/handler/codec/ TooLongFrameException.java
* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
  jar/io/netty/handler/codec/marshalling/MarshallingEncoder.java
* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
  jar/io/netty/handler/codec/SerializerException.java
* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
  jar/io/netty/handler/codec/ThreadLocalUnmarshallerProvider.java
* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
  jar/io/netty/handler/codec/marshalling/MarshallingDecoder.java
* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
  jar/io/netty/handler/codec/marshalling/MarshallingEncoder.java
* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
  jar/io/netty/handler/codec/compression/DecompressionException.java
* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
  jar/io/netty/handler/codec/compression/ThreadLocalUnmarshallerProvider.java
* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
  jar/io/netty/handler/codec/marshalling/LimitingByteInput.java
* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
  jar/io/netty/handler/codec/marshalling/ChannelBufferByteOutput.java
* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
  jar/io/netty/handler/codec/CompilationException.java
* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
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* /opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-
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 */

/**
 * A decoder that splits the received {@link ByteBuf}s dynamically by the
 * value of the length field in the message. It is particularly useful when you
 * decode a binary message which has an integer header field that represents the
 * length of the message body or the whole message.
 * <p>
 * [{@link LengthFieldBasedFrameDecoder}] has many configuration parameters so
 * that it can decode any message with a length field, which is often seen in
 * proprietary client-server protocols. Here are some example that will give
 * you the basic idea on which option does what.
 *
 * <h3>2 bytes length field at offset 0, do not strip header</h3>
 *
 * The value of the length field in this example is \(<tt>12 \text{ (0x0C)}\</tt>\) which
 * represents the length of "HELLO, WORLD". By default, the decoder assumes
 * that the length field represents the number of the bytes that follows the
 * length field. Therefore, it can be decoded with the simplistic parameter
 * combination.
 * <pre>
 * lengthFieldOffset   = 0
 * lengthFieldLength   = 2
 * lengthAdjustment    = 0
 * initialBytesToStrip = 0 (= do not strip header)
 * </pre>
 * BEFORE DECODE (14 bytes)   AFTER DECODE (14 bytes)
Because we can get the length of the content by calling

```java
[ByteBuf#readableBytes()],
```

you might want to strip the length field by specifying `<tt>initialBytesToStrip</tt>`. In this example, we specified `<tt>2</tt>`, that is same with the length of the length field, to strip the first two bytes.

```java
lengthFieldOffset = 0
lengthFieldLength = 2
lengthAdjustment = 0
```

Before decode (14 bytes)         After decode (12 bytes)
```
<table>
<thead>
<tr>
<th>Length</th>
<th>Actual Content</th>
<th>Actual Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000C</td>
<td>&quot;HELLO, WORLD&quot;</td>
<td>&quot;HELLO, WORLD&quot;</td>
</tr>
</tbody>
</table>
```

Because we can get the length of the content by calling

```java
[ByteBuf#readableBytes()],
```

you might want to strip the length field by specifying `<tt>initialBytesToStrip</tt>`. In this example, we specified `<tt>2</tt>`, that is same with the length of the length field, to strip the first two bytes.

```java
lengthFieldOffset = 0
lengthFieldLength = 2
lengthAdjustment = 0
```

Before decode (14 bytes)         After decode (14 bytes)
```
<table>
<thead>
<tr>
<th>Length</th>
<th>Actual Content</th>
<th>Actual Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000C</td>
<td>&quot;HELLO, WORLD&quot;</td>
<td>&quot;HELLO, WORLD&quot;</td>
</tr>
</tbody>
</table>
```

In most cases, the length field represents the length of the message body only, as shown in the previous examples. However, in some protocols, the length field represents the length of the whole message, including the message header. In such a case, we specify a non-zero length field length field length field length field.

```
lengthFieldOffset = 0
lengthFieldLength = 2
lengthAdjustment = -2
```

Before decode (14 bytes)         After decode (14 bytes)
```
<table>
<thead>
<tr>
<th>Length</th>
<th>Actual Content</th>
<th>Actual Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000E</td>
<td>&quot;HELLO, WORLD&quot;</td>
<td>&quot;HELLO, WORLD&quot;</td>
</tr>
</tbody>
</table>
```

In most cases, the length field represents the length of the message body only, as shown in the previous examples. However, in some protocols, the length field represents the length of the whole message, including the message header. In such a case, we specify a non-zero length field length field length field length field.

```
lengthFieldOffset = 0
lengthFieldLength = 2
lengthAdjustment = -2
```

Before decode (14 bytes)         After decode (14 bytes)
```
<table>
<thead>
<tr>
<th>Length</th>
<th>Actual Content</th>
<th>Actual Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000E</td>
<td>&quot;HELLO, WORLD&quot;</td>
<td>&quot;HELLO, WORLD&quot;</td>
</tr>
</tbody>
</table>
```

In most cases, the length field represents the length of the message body only, as shown in the previous examples. However, in some protocols, the length field represents the length of the whole message, including the message header. In such a case, we specify a non-zero length field length field length field length field.

```
lengthFieldOffset = 0
lengthFieldLength = 2
lengthAdjustment = -2
```

Before decode (14 bytes)         After decode (14 bytes)
```
<table>
<thead>
<tr>
<th>Length</th>
<th>Actual Content</th>
<th>Actual Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000E</td>
<td>&quot;HELLO, WORLD&quot;</td>
<td>&quot;HELLO, WORLD&quot;</td>
</tr>
</tbody>
</table>
```
* The following message is a simple variation of the first example. An extra
* header value is prepended to the message. `<tt>lengthAdjustment</tt>` is zero
* again because the decoder always takes the length of the prepended data into
* account during frame length calculation.
* `<pre>`
* `<b>lengthFieldOffset</b>   = <b>2</b> (= the length of Header 1)
* `<b>lengthFieldLength</b>   = <b>3</b>
* `lengthAdjustment    = 0`
* `initialBytesToStrip = 0`
*
* BEFORE DECODE (17 bytes)                      AFTER DECODE (17 bytes)
* +----------+----------+----------------+  +----------+----------+----------------+
* | Header 1 | Length | Actual Content |----->| Header 1 | Length | Actual Content |
* | 0xCAFE   | 0x00000C | "HELLO, WORLD" |      | 0xCAFE   | 0x00000C | "HELLO, WORLD" |
* +----------+----------+----------------+  +----------+----------+----------------+
* </pre>
*
* This is an advanced example that shows the case where there is an extra
* header between the length field and the message body. You have to specify a
* positive `<tt>lengthAdjustment</tt>` so that the decoder counts the extra
* header into the frame length calculation.
* `<pre>`
* `lengthFieldOffset   = 0`
* `lengthFieldLength   = 3`
* `<b>lengthAdjustment</b>    = <b>2</b> (= the length of Header 1)
* `initialBytesToStrip = 0`
*
* BEFORE DECODE (17 bytes)                      AFTER DECODE (17 bytes)
* +----------+----------+----------------+  +----------+----------+----------------+
* | Length | Header 1 | Actual Content |----->| Length | Header 1 | Actual Content |
* | 0x00000C | 0xCAFE | "HELLO, WORLD" |      | 0x00000C | 0xCAFE | "HELLO, WORLD" |
* +----------+----------+----------------+  +----------+----------+----------------+
* </pre>
*
* This is a combination of all the examples above. There are the prepended
* header before the length field and the extra header after the length field.
* The prepended header affects the `<tt>lengthFieldOffset</tt>` and the extra
* header affects the `<tt>lengthAdjustment</tt>`. We also specified a non-zero
* `<tt>initialBytesToStrip</tt>` to strip the length field and the prepended
* header from the frame. If you don't want to strip the prepended header, you
* could specify `<tt>0</tt>` for `<tt>initialBytesToSkip</tt>.
* `<pre>
* lengthFieldOffset = 1 (= the length of HDR1)
* lengthFieldLength = 2
* <b>lengthAdjustment</b>/h = <b>1</b>/h (= the length of HDR2)
* <b>initialBytesToStrip</b>/h = <b>3</b>/h (= the length of HDR1 + LEN)
* 
* BEFORE DECODE (16 bytes) AFTER DECODE (13 bytes)
* +-----------+--------+-----------+                          +-----------+--------+-----------+
* | HDR1 | Length | HDR2 | Actual Content |----->| HDR2 | Actual Content |
* | 0xCA | 0x000C | 0xFE | "HELLO, WORLD" |      | 0xFE | "HELLO, WORLD" |
* +-----------+--------+-----------+                          +-----------+--------+-----------+
* </pre>
* 
* `<h3>2 bytes length field at offset 1 in the middle of 4 bytes header,
* strip the first header field and the length field, the length field
* represents the length of the whole message</h3>`
* 
* Let's give another twist to the previous example. The only difference from
* the previous example is that the length field represents the length of the
* whole message instead of the message body, just like the third example.
* We have to count the length of HDR1 and Length into `<tt>lengthAdjustment</tt>.
* Please note that we don't need to take the length of HDR2 into account
* because the length field already includes the whole header length.
* `<pre>
* lengthFieldOffset = 1
* lengthFieldLength = 2
* <b>lengthAdjustment</b>/h = <b>-3</b>/h (= the length of HDR1 + LEN, negative)
* <b>initialBytesToStrip</b>/h = <b>3</b>/h
* 
* BEFORE DECODE (16 bytes) AFTER DECODE (13 bytes)
* +-----------+--------+-----------+                          +-----------+--------+-----------+
* | HDR1 | Length | HDR2 | Actual Content |----->| HDR2 | Actual Content |
* | 0xCA | 0x0010 | 0xFE | "HELLO, WORLD" |      | 0xFE | "HELLO, WORLD" |
* +-----------+--------+-----------+                          +-----------+--------+-----------+
* </pre>
* @see LengthFieldPrepender
*/

Found in path(s):
* `/opt/ws_local/PERMITS_SQL/1072948336_1595240763.12/0/netty-codec-4-1-51-final-sources-jar/io/netty/handler/codec/LengthFieldBasedFrameDecoder.java`
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* /opt/ws_local/PERMITS_SQL/1074947655_1596001757.62/0/jboss-marshalling-2-0-9-final-sources-1-
  jar/org/jboss/marshalling/_private/SetAccessibleAction.java
* /opt/ws_local/PERMITS_SQL/1074947655_1596001757.62/0/jboss-marshalling-2-0-9-final-sources-1-
  jar/org/jboss/marshalling/_private/GetReflectionFactoryAction.java

1.705 pinentry 1.1.0-2

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1.712 libxcrypt 4.1.1 4.el8

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**1.731 krb5-conf 1.0-r2**

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 cmd/krb5/slave/kpropd_rpc.c
 lib/gss_mechs/mech_krb5/et/kdb5_err.c
 lib/gss_mechs/mech_spnego/mach/gssapiP_spnego.h
 lib/gss_mechs/mech_spnego/mach/spnego_mech.c
 lib/kerb5/kadm5/kadm_host_srv_names.c
 lib/kerb5/kdb/kdb_convert.c
 lib/kerb5/kdb/kdb_hdr.h
 lib/kerb5/kdb/kdb_log.c
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lib/gssapi/mechglue/g_acquire_cred.c
lib/gssapi/mechglue/g_canon_name.c
lib/gssapi/mechglue/g_compare_name.c
lib/gssapi/mechglue/g_context_time.c
lib/gssapi/mechglue/g_delete_sec_context.c
lib/gssapi/mechglue/g_dup_name.c
lib/gssapi/mechglue/g_dup_status.c
lib/gssapi/mechglue/g_dup_name.c
lib/gssapi/mechglue/g_exp_sec_context.c
lib/gssapi/mechglue/g_export_name.c
lib/gssapi/mechglue/g_glue.c
lib/gssapi/mechglue/g_imp_name.c
lib/gssapi/mechglue/g_imp_sec_context.c
lib/gssapi/mechglue/g_init_sec_context.c
and the initial implementation of incremental propagation, including
the following new or changed files:

include/iprop_hdr.h
kadmin/server/ipropd_svc.c
lib/kdb/iprop.x
lib/kdb/kdb_convert.c
lib/kdb/kdb_log.c
lib/kdb/kdb_log.h
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* /opt/ws_local/PERMITS_SQL/1094800831_1601321575.56/0/smallrye-config-source-file-system-1-6-2-sources-jar/io/smallrye/config/source/file/FileSystemConfigSource.java

1.736 alsa-lib 1.2.3.2 1.el8

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set yrange [0:]
set terminal pngcairo font 'Sans, 8' lw 1 size 1400,1024
set xtics rotate by -45
set style histogram errorbars gap 2 lw 1
set style fill solid border -1

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1.744 wildfly-elytron-x500-deprecated

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1.745 curl 7.76.1-r0
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1.748 jboss-el-api-3-0-spec 2.0.0.Final
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c) Accompany the work with a written offer, valid for at least three years, to give the same user the materials specified in Subsection 6a, above, for a charge no more than the cost of performing this distribution.

d) If distribution of the work is made by offering access to copy from a designated place, offer equivalent access to copy the above specified materials from the same place.

e) Verify that the user has already received a copy of these materials or that you have already sent this user a copy.

For an executable, the required form of the "work that uses the Library" must include any data and utility programs needed for reproducing the executable from it. However, as a special exception, the materials to be distributed need not include anything that is normally distributed (in either source or binary form) with the major components (compiler, kernel, and so on) of the operating system on which the executable runs, unless that component itself accompanies the executable.

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# Jackson JSON processor

Jackson is a high-performance, Free/Open Source JSON processing library. It was originally written by Tatu Saloranta (tatu.salaranta@iki.fi), and has been in development since 2007. It is currently developed by a community of developers, as well as supported commercially by FasterXML.com.

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1.758 aiohttp 3.7.4.post0

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1.764 glibc 2.28-10

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1.768 icu 67.1-r2

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## Commands to generate dependency files
GEN_DEPS.c=$(CC) -E -MM $(DEFS) $(CPPFLAGS)
GEN_DEPS.cc=$(CXX) -E -MM $(DEFS) $(CPPFLAGS)

## Flags for position independent code
SHAREDLIBCFLAGS = -fPIC
SHAREDLIBCXXFLAGS = -fPIC
SHAREDLIBCPPFLAGS = -DPIC

## Additional flags when building libraries and with threads
THREADSCPPFLAGS = -D_REENTRANT
LIBCPPFLAGS =

## Compiler switch to embed a runtime search path
LD_RPATH=
LD_RPATH_PRE=-Wl,-rpath,

## Compiler switch to embed a library name
LD_SONAME = -Wl,-soname -Wl,$(notdir $(MIDDLE_SO_TARGET))

## Shared library options
LD_SOOPTIONS= -Wl,-Bsymbolic

## Shared object suffix
SO = so
## Non-shared intermediate object suffix
STATIC_O = ao

## Compilation rules
%.$(STATIC_O): $(srcdir)/%.c
$(COMPILE.c) $(STATICCPPFLAGS) $(STATICCFLAGS) -o $@ $<
%.o: $(srcdir)/%.c
$(COMPILE.c) $(DYNAMICCPPFLAGS) $(DYNAMICCFLAGS) -o $@ $<

%.$(STATIC_O): $(srcdir)/%.cpp
$(COMPILE.cc) $(STATICCPPFLAGS) $(STATICCXXFLAGS) -o $@ $<
%.o: $(srcdir)/%.cpp
$(COMPILE.cc) $(DYNAMICCPPFLAGS) $(DYNAMICCXXFLAGS) -o $@ $<

## Dependency rules
%.d: $(srcdir)/%.c
@echo "generating dependency information for "$<"
@$((SHELL)) -ec "$(GEN_DEPS.c) "$<"
sed \"s/\$(\*\*))/\1.o \$@ : /g\" > $@; \\
[ -s $@ ] || rm -f $@

%.d: $(srcdir)/%.cpp
@echo "generating dependency information for $<"
@$(SHELL) -ec '$(GEN_DEPS.cc) $< \n | sed \"s/\$(\*\*))/\1.o \$@ : /g\" > $@; \\
[ -s $@ ] || rm -f $@'

## Versioned libraries rules

%.$(_SO).$(SO_TARGET_VERSION_MAJOR): %.$(SO).$(SO_TARGET_VERSION)
$(RM) $@ && ln -s ${<F} $@
%.$(SO): %.$(SO).$(SO_TARGET_VERSION_MAJOR)
$(RM) $@ && ln -s ${*F}.$(SO).$(SO_TARGET_VERSION) $@

## Bind internal references

# LDflags that pkgdata will use
BIR_LDFLAGS= -Wl,-Bsymbolic

# Dependencies [i.e. map files] for the final library
BIR_DEPS=

## Remove shared library 's'
STATIC_PREFIX_WHEN_USED =
STATIC_PREFIX =

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When a "work that uses the Library" uses material from a header file that is part of the Library, the object code for the work may be a
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If such an object file uses only numerical parameters, data structure layouts and accessors, and small macros and small inline functions (ten lines or less in length), then the use of the object file is unrestricted, regardless of whether it is legally a derivative work. (Executables containing this object code plus portions of the Library will still fall under Section 6.)

Otherwise, if the work is a derivative of the Library, you may distribute the object code for the work under the terms of Section 6. Any executables containing that work also fall under Section 6, whether or not they are linked directly with the Library itself.

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will operate properly with a modified version of the library, if the user installs one, as long as the modified version is interface-compatible with the version that the work was made with.

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Version 2, June 1991

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<one line to give the program's name and a brief idea of what it does.>
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Section 6 states terms for distribution of such executables.

When a "work that uses the Library" uses material from a header file
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Whether this is true is especially significant if the work can be
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threshold for this to be true is not precisely defined by law.

If such an object file uses only numerical parameters, data
structure layouts and accessors, and small macros and small inline
functions (ten lines or less in length), then the use of the object
file is unrestricted, regardless of whether it is legally a derivative
work. (Executables containing this object code plus portions of the
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Otherwise, if the work is a derivative of the Library, you may
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**1.782 wildfly-elytron-mechanism-gssapi**

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* /opt/cola/permits/1135880235_1613624044.2/0/jakarta-validation-api-2-0-2-sources-3-jar/javax/validation/metadata/CascadableDescriptor.java
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jar/javafx/validation/constraints/Pattern.java
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jar/javafx/validation/Validation.java
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jar/javafx/validation/ValidatorContext.java
* /opt/cola/permits/1135880235_1613624044.2/0/jakarta-validation-api-2-0-2-sources-3-
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* /opt/cola/permits/1135880235_1613624044.2/0/jakarta-validation-api-2-0-2-sources-3-
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jar/javafx/validation/Configuration.java
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jar/javafx/validation/constraints/Size.java
* /opt/cola/permits/1135880235_1613624044.2/0/jakarta-validation-api-2-0-2-sources-3-
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* /opt/cola/permits/1135880235_1613624044.2/0/jakarta-validation-api-2-0-2-sources-3-
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* /opt/cola/permits/1135880235_1613624044.2/0/jakarta-validation-api-2-0-2-sources-3-
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* /opt/cola/permits/1135880235_1613624044.2/0/jakarta-validation-api-2-0-2-sources-3-
jar/javafx/validation/executable/ExecutableValidator.java
* /opt/cola/permits/1135880235_1613624044.2/0/jakarta-validation-api-2-0-2-sources-3-
jar/javafx/validation/ValidationProviderResolver.java
* /opt/cola/permits/1135880235_1613624044.2/0/jakarta-validation-api-2-0-2-sources-3-
jar/javafx/validation/ValidatorFactory.java
* /opt/cola/permits/1135880235_1613624044.2/0/jakarta-validation-api-2-0-2-sources-3-
jar/javafx/validation/metadata/ContainerDescriptor.java
* /opt/cola/permits/1135880235_1613624044.2/0/jakarta-validation-api-2-0-2-sources-3-
jar/javafx/validation/metadata/ConstraintDescriptor.java
* /opt/cola/permits/1135880235_1613624044.2/0/jakarta-validation-api-2-0-2-sources-3-
jar/javafx/validation/metadata/ParameterDescriptor.java
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lib/gssapi/mechglue/g_accept_sec_context.c
lib/gssapi/mechglue/g_acquire_cred.c
lib/gssapi/mechglue/g_canon_name.c
lib/gssapi/mechglue/g_compare_name.c
lib/gssapi/mechglue/g_context_time.c
lib/gssapi/mechglue/g_delete_sec_context.c
and the initial implementation of incremental propagation, including the following new or changed files:

include/iprop_hdr.h
kadmin/server/ipropd_svc.c
lib/kdb/iprop.x
lib/kdb/kdb_convert.c
lib/kdb/kdb_log.c
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1.803 libffi 3.3-r2

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  * /opt/cola/permits/1136663414_1613849809.98/0/zookeeper-3-6-2-sources-2-
    jar/org/apache/zookeeper/server/admin/AdminServer.java
  * /opt/cola/permits/1136663414_1613849809.98/0/zookeeper-3-6-2-sources-2-
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1.812 minio 6.0.0

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* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/Grant.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/ListAllMyBucketsResult.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/PostPolicy.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/InitiateMultipartUploadResult.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/Bucket.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/Part.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/Upload.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/ObjectStat.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/MinioProperties.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/http/Scheme.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/Part.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/Upload.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/Signer.java
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* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/DeleteObject.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/CloudFunctionConfiguration.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/S3Key.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/DeleteError.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/TopicConfiguration.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/NotificationConfiguration.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/Filter.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/DeleteRequest.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/EventType.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/DeletedObject.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/QueueConfiguration.java
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* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/org/apache/commons/validator/routines/InetAddressValidator.java
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 * /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/CopyObjectResult.java

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 * /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/ListBucketResultV1.java
 * /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/messages/ListBucketResult.java

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* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/notification/NotificationEvent.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/notification/EventMeta.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/notification/NotificationInfo.java
* /opt/cola/permits/1158394663_1619759973.62/0/minio-6-0-0-sources-jar/io/minio/notification/Identity.java

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1.813 smallrye-config-common 1.6.2

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1.814 jose-jwt 3.13.2.Final

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1.816 uap-java 1.4.3

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1.818 javassist 3.23.2-GA

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Found in path(s):
  * /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/MemberCodeGen.java
  * /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/stackmap/Tracer.java
  * /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/convert/TransformWriteField.java
  * /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/Symbol.java
  * /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/StringL.java
  * /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/Pair.java
  * /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/tools/reflect/CannotInvokeException.java
  * /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/NewExpr.java

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jar/javassist/bytecode/stackmap/TypedBlock.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/analysis/MultiArrayType.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/BadBytecode.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/ExceptionTable.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ProceedHandler.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/ByteArrayClassPath.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/tools/rmi/StubGenerator.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/tools/rmi/AppletServer.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/AnnotationDefaultAttribute.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/LineNumberAttribute.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/MapMaker.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/convert/TransformAccessArrayField.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/Visitor.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/InstanceOfExpr.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/SubroutineScanner.java
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* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/DotClass.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/Lex.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/Collector.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/InstanceOfExpr.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/analysis/Util.java

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* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/tools/reflect/Loader.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/util/HotSwapper.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/analysis/Analyzer.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/tools/reflect/TransformBefore.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/tools/reflect/CannotReflectException.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/analysis/Subroutine.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/tools/reflect/CannotCreateException.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/Bytecode.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/scopedpool/SoftValueHashMap.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/JvstTypeChecker.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/tools/reflect/ClassMetaobject.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/CodeGen.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/stackmap/TypeTag.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/Declarator.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/DoubleConst.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/DeprecatedAttribute.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/AttributeInfo.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/ArrayInit.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/util/proxy/SecurityActions.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/DeprecatedAttribute.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/StackMapTable.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/expr/NewArray.java

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* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/Mnemonic.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/CtMethod.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/expr/MethodCall.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/convert/TransformFieldAccess.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/StackMap.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/CompileError.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/tools/rmi/ObjectNotFoundException.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/scopedpool/ScopedClassPool.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/URLClassPath.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/tools/rmi/Proxy.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/TypeChecker.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/CodeIterator.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/ParameterAnnotationsAttribute.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/Expr.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/analysis/MultiType.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/.CtNewWrappedConstructor.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/compiler/ast/FieldDecl.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/tools/framedump.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/SourceFileAttribute.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/CannotCompileException.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/expr/ConstructorCall.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/scopedpool/ScopedClassPoolFactoryImpl.java

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* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/annotation/CharMemberValue.java
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* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/annotation/MemberValue.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/annotation/MemberValueVisitor.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/annotation/AnnotationMemberValue.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/annotation/StringMemberValue.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/annotation/ShortMemberValue.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/annotation/DoubleMemberValue.java
* /opt/cola/permits/1136416216_1613765029.38/0/javassist-3-23-2-ga-sources-2-jar/javassist/bytecode/annotation/BooleanMemberValue.java

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Found in path(s):
* /opt/cola/permits/1135892376_1613626859.73/0/asm-util-7-1-sources-2-jar/org/objectweb/asm/util/ASMifierSupport.java
* /opt/cola/permits/1135892376_1613626859.73/0/asm-util-7-1-sources-2-jar/org/objectweb/asm/util/Textifiable.java
* /opt/cola/permits/1135892376_1613626859.73/0/asm-util-7-1-sources-2-jar/org/objectweb/asm/util/ASMifiable.java
* /opt/cola/permits/1135892376_1613626859.73/0/asm-util-7-1-sources-2-jar/org/objectweb/asm/util/TextifierSupport.java

1.828 adduser 3.118

1.828.1 Available under license:

This package was first put together by Ian Murdock <imurdock@debian.org> and was maintained by Steve Phillips <sjp@cvfn.org> from sources written for the Debian Project by Ian Murdock, Ted Hajek <tedhajek@boombox.micro.umn.edu>, and Sven Rudolph <sr1@inf.tu-dresden.de>.

Since Nov 27 1996, it was maintained by Guy Maor <maor@debian.org>. He rewrote most of it.

Since May 20 2000, it is maintained by Roland Bauerschmidt <rb@debian.org>.

Since March 24 2004, it is maintained by Roland Bauerschmidt <rb@debian.org>, and co-maintained by Marc Haber <mh+debian-packages@zugschlus.de>

Since 23 Oct 2005, it has been maintained by Joerg Hoh <joerg@joerghoh.de>

Since June 2006, it has been maintained by Stephen Gran <sgran@debian.org>

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1.829 twitter4j 4.0.7
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"husky": "^4.2.3",
"mocha": "^7.1.0",
"nyc": "^15.0.0",
"prettier": "^1.19.1",
"rimraf": "^3.0.2",
"rollup": "^2.0.6",
"rollup-plugin-babel": "^4.4.0",
"rollup-plugin-filesize": "^6.2.1",
"rollup-plugin-uglify": "^6.0.4",
"sucrase": "^3.12.1",
"typescript": "^3.8.3"
}
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David Megginson, david@megginson.com
2000-05-05

# Dependency License Information

## Why should we track license info?

We need to keep track of the licenses that apply to each third party (non-Keycloak) dependency (maven or otherwise) that Keycloak uses. This information can be used to check if there are conflicts or other issues that could create a legal encumbrance for the users or developers of Keycloak.

## How to determine a dependency's license info

Since the maven ecosystem does not maintain high quality license metadata, no automated process (like license-maven-plugin for example) is acceptable for making the determination of what license applies to a particular maven dependency. The licenses of non-maven dependencies (JavaScript, images, fonts, etc.) must also be determined manually.

To manually determine a license, clone/checkout the source code at the tag or commit that applies to the version of the dependency you're adding or updating (licenses do sometimes change between versions). This is a lot easier to do immediately, especially for non-maven dependencies, as later it may not be clear where the files came from, or what version they were. Once you have the source, look at the readme and search around for license files. For maven projects, you can look at the pom too, but its license information is not always present or correct. It's usually obvious what the license is, but sometimes one part of the source has a different license, or there may be more than one license that applies to your dependency.
## How to store license info

Typically, each zip that gets distributed to users needs to contain a license XML and individual license files, plus an html file generated at build time.

The XML and individual files are maintained in git. When you change or add a dependency that is a part of:

- an adapter, modify `distribution/{saml-adapters,adapters}/*/*/src/main/resources/licenses/rh-sso/licenses.xml`, for example `distribution/saml-adapters/as7-eap6-adapter/eap6-adapter-zip/src/main/resources/licenses/rh-sso/licenses.xml`.

Maven dependencies go into a `licenseSummary/dependencies/dependency` element, and non-maven dependencies go into a `licenseSummary/others/other` element.

Here are some examples of maven dependencies:

```xml
```maven```
<dependency>
  <groupId>org.sonatype.plexus</groupId>
  <artifactId>plexus-sec-dispatcher</artifactId>
  <version>1.3</version>
  <licenses>
    <license>
      <name>Apache Software License 2.0</name>
      <url>http://www.apache.org/licenses/LICENSE-2.0.txt</url> <!-- Source repo contains no license file -->
    </license>
  </licenses>
</dependency>
```maven```
<dependency>
  <groupId>org.antlr</groupId>
  <artifactId>antlr-runtime</artifactId>
  <version>3.5</version>
  <licenses>
    <license>
      <name>BSD 3-clause New or Revised License</name>
    </license>
  </licenses>
</dependency>
```

and non-maven dependencies:

```xml
```maven```
<other>
  <description>jQuery</description>
```maven```
<locations>
  <file>themes/keycloak/common/resources/lib/jquery/jquery-1.10.2.js</file>
</locations>

<licenses>
  <license>
    <name>MIT License</name>
    <url>https://raw.githubusercontent.com/jquery/jquery/1.10.2/MIT-LICENSE.txt</url>
  </license>
</licenses>

<other>
  <description>AngularJS</description>
  <locations>
    <directory>themes/keycloak/common/resources/lib/angular</directory>
  </locations>
  <licenses>
    <license>
      <name>MIT License</name>
      <url>https://raw.githubusercontent.com/angular/angular.js/v1.4.4/LICENSE</url>
    </license>
  </licenses>
</other>

Look at the licenses.xml files in this repository for more examples.

After modifying a license XML, you must run `download-license-files.sh` against it. This script will update the individual license files that are stored in the same directory as the XML.

Example command line:

```
```

The following shell commands must be available for the script to work:

- curl
- dos2unix
- sha256sum
- xmlstarlet

### Product builds

RH-SSO is built on an internal build system. If you've added or updated license data for the product, you might need to import the corresponding dependency artifact into this internal build system.
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# Zocial CSS social buttons

I basically rewrote this entire set so they are full vector buttons, meaning:

- @font-face icons
- custom font file for all social icons
- icon font use private unicode spaces for accessibility
- em sizing based on button font-size
- support for about 83 different services
- buttons and icons supported
- no raster images (sweet)
- works splendidly on any browser supporting @font-face
- CSS3 degrades gracefully in IE8 and below etc.
- also includes generic icon-less primary and secondary buttons

## How to use these buttons

<button class="zocial facebook">Button label here</button>

or

<a class="zocial twitter">Button label</a>

- Can be any element e.g. `a`, `div`, `button` etc.
- Add class of `.zocial`
- Add class for name of service e.g. `.dropbox`, `.twitter`, `.github`
- Done :-)  

Check out [zocial.smcllns.com](http://zocial.smcllns.com) for demo and code examples.

There's also a LESS version from @gustavohenke [here](https://github.com/gustavohenke/zocial-less)

Problems, questions or requests to [@smcllns](http://twitter.com/smcllns)

## How to contribute

Install [Font Custom](http://fontcustom.com/#installation)

Run `fontcustom compile` to build the font.

New fonts are defined by adding them in the `svg/` folder. For color settings see the `templates/zocial.css` file.

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[This is the first released version of the library GPL. It is numbered 2 because it goes with version 2 of the ordinary GPL.]
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If such an object file uses only numerical parameters, data
structure layouts and accessors, and small macros and small inline
functions (ten lines or less in length), then the use of the object
file is unrestricted, regardless of whether it is legally a derivative
work. (Executables containing this object code plus portions of the
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# [Font Awesome v4.3.0](http://fontawesome.io)
### The iconic font and CSS framework

Font Awesome is a full suite of 519 pictographic icons for easy scalable vector graphics on websites, created and maintained by [Dave Gandy](http://twitter.com/davegandy).

Stay up to date with the latest release and announcements on Twitter: [@fontawesome](http://twitter.com/fontawesome).

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### Changelog
- v3.0.0 - all icons redesigned from scratch, optimized for Bootstrap's 14px default
- v3.0.1 - much improved rendering in webkit, various bug fixes
- v3.0.2 - much improved rendering and alignment in IE7
- v3.1.0 - Added 54 icons, icon stacking styles, flipping and rotating icons, removed Sass support
- [v3.1.1 GitHub milestones](https://github.com/FortAwesome/Font-Awesome/issues?milestone=4&page=1&state=closed)
- [v3.2.0 GitHub milestones](https://github.com/FortAwesome/Font-Awesome/issues?milestone=3&page=1&state=closed)
- [v3.2.1 GitHub milestones](https://github.com/FortAwesome/Font-Awesome/issues?milestone=5&page=1&state=closed)
- [v4.0.0 GitHub milestones](https://github.com/FortAwesome/Font-Awesome/issues?milestone=2&page=1&state=closed)
- [v4.0.1 GitHub milestones](https://github.com/FortAwesome/Font-Awesome/issues?milestone=7&page=1&state=closed)
- [v4.0.2 GitHub milestones](https://github.com/FortAwesome/Font-Awesome/issues?milestone=8&page=1&state=closed)
- [v4.0.3 GitHub milestones](https://github.com/FortAwesome/Font-Awesome/issues?milestone=9&page=1&state=closed)
- [v4.1.0 GitHub milestones](https://github.com/FortAwesome/Font-Awesome/issues?milestone=6&page=1&state=closed)
- [v4.2.0 GitHub milestones](https://github.com/FortAwesome/Font-Awesome/issues?milestone=12&page=1&state=closed)
- [v4.3.0 GitHub milestones](https://github.com/FortAwesome/Font-Awesome/issues?q=milestone%3A4.3.0+is%3Aclosed)

## Contributing

Please read through our [contributing guidelines](https://github.com/FortAwesome/Font-Awesome/blob/master/CONTRIBUTING.md).

Included are directions for opening issues, coding standards, and notes on development.

## Versioning

Font Awesome will be maintained under the Semantic Versioning guidelines as much as possible. Releases will be numbered with the following format:

`<major>,<minor>,<patch>`

And constructed with the following guidelines:

* Breaking backward compatibility bumps the major (and resets the minor and patch)
* New additions, including new icons, without breaking backward compatibility bumps the minor (and resets the patch)
* Bug fixes and misc changes bumps the patch

For more information on SemVer, please visit [http://semver.org](http://semver.org).
## Author
- Email: dave@fontawesome.io
- Twitter: http://twitter.com/davegandy
- GitHub: https://github.com/davegandy

## Component
To include as a [component](http://github.com/component/component), just run

    $ component install FortAwesome/Font-Awesome

Or add

"FortAwesome/Font-Awesome": "*"

to the `dependencies` in your `component.json`.

## Hacking on Font Awesome

From the root of the repository, install the tools used to develop.

    $ bundle install
    $ npm install

Build the project and documentation:

    $ bundle exec jekyll build

Or serve it on a local server on http://localhost:7998/Font-Awesome/:

    $ bundle exec jekyll -w serve

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Version: @@@ver@@ Timestamp: @@timestamp@@

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1.850 relaxng-datatype 2.3.3-b02

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@var{signature of Ty Coon}, 1 April 1990
Ty Coon, President of Vice
@end smallexample

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Metadata-Version: 1.0
Name: ketoclient
Version: 0.4
Summary: UNKNOWN
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* /opt/cola/permits/1156778950_1625142493.06/0/ketoclient-0-4-1-zip/ketoclient-0.4/PKG-INFO

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* /opt/ws_local/PERMITS_SQL/1072948616_1595240775.72/0/netty-buffer-4-1-51-final-sources-jar/io/netty/buffer/WrappedUnpooledUnsafeDirectByteBuf.java
* /opt/ws_local/PERMITS_SQL/1072948616_1595240775.72/0/netty-buffer-4-1-51-final-sources-jar/io/netty/buffer/PooledDuplicatedByteBuf.java
* /opt/ws_local/PERMITS_SQL/1072948616_1595240775.72/0/netty-buffer-4-1-51-final-sources-jar/io/netty/buffer/UnpooledUnsafeNoCleanerDirectByteBuf.java
1.857 jackson-annotations 2.10.3
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1.858 cffi 1.14.5

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* /opt/ws_local/PERMITS_SQL/1075084041_1596044813.39/0/netty-transport-native-epoll-4-1-51-final-sources-jar/io/netty/channel/epoll/AbstractEpollServerChannel.java
* /opt/ws_local/PERMITS_SQL/1075084041_1596044813.39/0/netty-transport-native-epoll-4-1-51-final-sources-jar/io/netty/channel/epoll/EpollServerChannelConfig.java
* /opt/ws_local/PERMITS_SQL/1075084041_1596044813.39/0/netty-transport-native-epoll-4-1-51-final-sources-jar/io/netty/channel/epoll/EpollRecvByteAllocatorHandle.java
* /opt/ws_local/PERMITS_SQL/1075084041_1596044813.39/0/netty-transport-native-epoll-4-1-51-final-sources-jar/io/netty/channel/epoll/EpollDomainSocketChannel.java

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* /opt/ws_local/PERMITS_SQL/1075084041_1596044813.39/0/netty-transport-native-epoll-4-1-51-final-sources-jar/io/netty/channel/epoll/EpollChannelOption.java
* /opt/ws_local/PERMITS_SQL/1075084041_1596044813.39/0/netty-transport-native-epoll-4-1-51-final-sources-jar/io/netty/channel/epoll/AbstractEpollChannel.java
* /opt/ws_local/PERMITS_SQL/1075084041_1596044813.39/0/netty-transport-native-epoll-4-1-51-final-sources-jar/io/netty/channel/epoll/EpollITcpInfo.java
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* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-
  jar/org/opensaml/soap/soap11/FaultString.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-
  jar/org/opensaml/soap/wstrust/CanonicalizationAlgorithm.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-
  jar/org/opensaml/soap/wsaddressing/util/package-info.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-
  jar/org/opensaml/soap/wsfed/WSFedObject.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-
  jar/org/opensaml/soap/wssecurity/Created.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-
  jar/org/opensaml/soap/wssecurity/AttributedString.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-
  jar/org/opensaml/soap/soap11/ActorBearing.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-
  jar/org/opensaml/soap/client/SOAPFaultException.java
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  jar/org/opensaml/soap/wssecurity/AttributedURI.java
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  jar/org/opensaml/soap/wstrust/RequestSecurityTokenResponseCollection.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-
  jar/org/opensaml/soap/soap11/MustUnderstandBearing.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-
  jar/org/opensaml/soap/wsaddressing/ProblemHeaderQName.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-
  jar/org/opensaml/soap/wssecurity/WSSecurityConstants.java
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  jar/org/opensaml/soap/soap11/Fault.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-
  jar/org/opensaml/soap/wstrust/Primary.java
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* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-Jar/org/opensaml/soap/wsaddressing/WSAddressingConstants.java
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* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-Jar/org/opensaml/soap/wssecurity/Reference.java
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* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-Jar/org/opensaml/soap/wssecurity/AttributedDateTime.java
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* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-Jar/org/opensaml/soap/wstrust/OperatorContentType.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-Jar/org/opensaml/soap/wssecurity/ReferenceContentType.java
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* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-Jar/org/opensaml/soap/wssecurity/wstrust/IssuedTokens.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-Jar/org/opensaml/soap/wsfed/Address.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-Jar/org/opensaml/soap/wstrust/AllowPostdating.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-Jar/org/opensaml/soap/wssecurity/messaging/WSSecurityContext.java
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-Jar/org/opensaml/soap/wssecurity/package-info.java
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Found in path(s):
* /opt/cola/permits/1111302172_1606896600.2/0/opensaml-soap-api-3-3-1-sources-1-jar/schema/ws-trust-1.3.xsd

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20030314

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1.862 gnutls 3.6.7-4+deb10u6

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This option is useful when you wish to copy part of the code of the Library into a program that is not a library.

4. You may copy and distribute the Library (or a portion or derivative of it, under Section 2) in object code or executable form under the terms of Sections 1 and 2 above provided that you accompany it with the complete corresponding machine-readable source code, which must be distributed under the terms of Sections 1 and 2 above on a medium customarily used for software interchange.

If distribution of object code is made by offering access to copy from a designated place, then offering equivalent access to copy the source code from the same place satisfies the requirement to distribute the source code, even though third parties are not compelled to copy the source along with the object code.

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If such an object file uses only numerical parameters, data structure layouts and accessors, and small macros and small inline functions (ten lines or less in length), then the use of the object file is unrestricted, regardless of whether it is legally a derivative work. (Executables containing this object code plus portions of the Library will still fall under Section 6.)

Otherwise, if the work is a derivative of the Library, you may distribute the object code for the work under the terms of Section 6. Any executables containing that work also fall under Section 6, whether or not they are linked directly with the Library itself.

6. As an exception to the Sections above, you may also combine or link a "work that uses the Library" with the Library to produce a work containing portions of the Library, and distribute that work under terms of your choice, provided that the terms permit modification of the work for the customer's own use and reverse engineering for debugging such modifications.

You must give prominent notice with each copy of the work that the Library is used in it and that the Library and its use are covered by this License. You must supply a copy of this License. If the work during execution displays copyright notices, you must include the copyright notice for the Library among them, as well as a reference directing the user to the copy of this License. Also, you must do one of these things:

a) Accompany the work with the complete corresponding machine-readable source code for the Library including whatever changes were used in the work (which must be distributed under Sections 1 and 2 above); and, if the work is an executable linked with the Library, with the complete machine-readable "work that uses the Library", as object code and/or source code, so that the user can modify the Library and then relink to produce a modified executable containing the modified Library. (It is understood that the user who changes the contents of definitions files in the Library will not necessarily be able to recompile the application to use the modified definitions.)

b) Use a suitable shared library mechanism for linking with the Library. A suitable mechanism is one that (1) uses at run time a
copy of the library already present on the user's computer system, 
rather than copying library functions into the executable, and (2) 
will operate properly with a modified version of the library, if 
the user installs one, as long as the modified version is 
interface-compatible with the version that the work was made with.

c) Accompany the work with a written offer, valid for at 
least three years, to give the same user the materials 
specified in Subsection 6a, above, for a charge no more 
than the cost of performing this distribution.

d) If distribution of the work is made by offering access to copy 
from a designated place, offer equivalent access to copy the above 
specified materials from the same place.

e) Verify that the user has already received a copy of these 
materials or that you have already sent this user a copy.

For an executable, the required form of the "work that uses the 
Library" must include any data and utility programs needed for 
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components (compiler, kernel, and so on) of the operating system on 
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1.867 keyutils 1.6.3-r0
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Because of this blurred distinction, using the ordinary General Public License for libraries did not effectively promote software sharing, because most developers did not use the libraries. We concluded that weaker conditions might promote sharing better.

However, unrestricted linking of non-free programs would deprive the users of those programs of all benefit from the free status of the libraries themselves. This Library General Public License is intended to permit developers of non-free programs to use free libraries, while preserving your freedom as a user of such programs to change the free libraries that are incorporated in them. (We have not seen how to achieve this as regards changes in header files, but we have achieved it as regards changes in the actual functions of the Library.) The hope is that this will lead to faster development of free libraries.

The precise terms and conditions for copying, distribution and modification follow. Pay close attention to the difference between a "work based on the library" and a "work that uses the library". The former contains code derived from the library, while the latter only works together with the library.

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This option is useful when you wish to copy part of the code of
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<signature of Ty Coon>, 1 April 1990
Ty Coon, President of Vice

That's all there is to it!

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1.876 ncurses 6.1-7.20180224.el8

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Files: *
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Calling this script install-sh is preferred over install.sh, to prevent
`make' implicit rules from creating a file called install from it
when there is no Makefile.

This script is compatible with the BSD install script, but was written
from scratch. It can only install one file at a time, a restriction
shared with many OS's install programs.

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-- vile: txtmode file-encoding=utf-8
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-- vile:txtmode fc=72
-- $Id: COPYING,v 1.6 2018/01/01 12:00:00 tom Exp $
Upstream source https://invisible-island.net/ncurses/ncurses.html
This package is used for testing builds of ncurses.

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Upstream source https://invisible-island.net/ncurses/ncurses-examples.html

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* javax.annotation:javax.annotation-api
* javax.transaction:javax.transaction-api
* javax.websocket:javax.websocket-api

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* java.sun.security.ssl

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org.apache.tomcat:tomcat-juli
org.apache.tomcat:tomcat-jsp-api
org.apache.tomcat:tomcat-el-api
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-api
org.apache.tomcat:tomcat-util-scan
org.apache.tomcat:tomcat-util
org.mortbay.jasper:apache-el
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-el-api

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Mortbay

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https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

org.eclipse.jetty.toolchain:jetty-schemas

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1.892 lz4 1.8.3-2.el8

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  STATIC=false;
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package org.apache.jute.compiler.generated;

import org.apache.jute.compiler.*;
import java.util.ArrayList;
import java.util.Hashtable;
import java.io.File;
import java.io.FileReader;
import java.io.FileNotFoundException;
import java.io.IOException;

@SuppressWarnings("unused")
public class Rcc {
    private static Hashtable<String, JRecord> recTab = new Hashtable<String, JRecord>();
    private static String curDir = System.getProperty("user.dir");
    private static String curFileName;
    private static String curModuleName;

    public static void main(String args[]) {
        String language = "java";
        ArrayList<String> recFiles = new ArrayList<String>();
        JFile curFile=null;

        for (int i=0; i<args.length; i++) {
            if ("-l".equalsIgnoreCase(args[i]) || "--language".equalsIgnoreCase(args[i])) {
                language = args[i+1].toLowerCase();
                i++;
            } else {
                recFiles.add(args[i]);
            }
        }

        if (!"c++".equals(language) && !"java".equals(language) && !"c".equals(language)) {
            System.out.println("Cannot recognize language:" + language);
            System.exit(1);
        }

        if (recFiles.size() == 0) {
            System.out.println("No record files specified. Exiting.");
        }
    }
}
System.exit(1);
}
for (int i=0; i<recFiles.size(); i++) {
    curFile = recFiles.get(i);
    File file = new File(curFile);
    try {
        curFile = parseFile(file);
    } catch (FileNotFoundException e) {
        System.out.println("File " + recFiles.get(i) + " Not found.");
        System.exit(1);
    } catch (ParseException e) {
        System.out.println(e.toString());
        System.exit(1);
    }
    System.out.println(recFiles.get(i) + " Parsed Successfully");
    try {
        curFile.genCode(language, new File("."));
    } catch (IOException e) {
        System.out.println(e.toString());
        System.exit(1);
    }
    System.out.println(recFiles.get(i) + " Parsed Successfully");
    try {
        curFile.genCode(language, new File(".")),
    } catch (FileNotFoundException e) {
        System.out.println(e.toString());
        System.exit(1);
    }
}

public static JFile parseFile(File file) throws FileNotFoundException, ParseException {
    curDir = file.getParent();
    curFile = file.getName();
    FileReader reader = new FileReader(file);
    try {
        Rcc parser = new Rcc(reader);
        recTab = new Hashtable<String, JRecord>();
        return parser.Input();
    } finally {
        try {
            reader.close();
        } catch (IOException e) {
        }
    }
}

PARSER_END(Rcc)

SKIP :
{
    "\n"
    "\n"
"r"
}

SPECIAL_TOKEN:
{
  "/": WithinOneLineComment
}

<WithinOneLineComment> SPECIAL_TOKEN:
{
  (<"\n" | "\r" | "\r\n") : DEFAULT
}

<WithinOneLineComment> MORE:
{
  <~[]>
}

SPECIAL_TOKEN:
{
  "/*": WithinMultiLineComment
}

<WithinMultiLineComment> SPECIAL_TOKEN:
{
  "/*/": DEFAULT
}

<WithinMultiLineComment> MORE:
{
  <~[]>
}

TOKEN:
{
  <MODULE_TKN: "module">
  | <RECORD_TKN: "class">
  | <INCLUDE_TKN: "include">
  | <BYTE_TKN: "byte">
  | <BOOLEAN_TKN: "boolean">
  | <INT_TKN: "int">
  | <LONG_TKN: "long">
  | <FLOAT_TKN: "float">
  | <DOUBLE_TKN: "double">
  | <USTRING_TKN: "ustring">
  | <BUFFER_TKN: "buffer">
  | <VECTOR_TKN: "vector">
  | <MAP_TKN: "map">

JFile Input() :
{
    ArrayList<JFile> ilist = new ArrayList<JFile>();
    ArrayList<JRecord> rlist = new ArrayList<JRecord>();
    JFile i;
    ArrayList <JRecord>l;
}
{
    (i = Include())
    { ilist.add(i); } |
    l = Module()
    { rlist.addAll(l); }
}+
<EOF>
{ return new JFile(curFileName, ilist, rlist); }
}

JFile Include() :
{
    String fname;
    Token t;
}
{
    <INCLUDE_TKN>
    t = <CSTRING_TKN>
    {
        JFile ret = null;
        fname = t.image.replaceAll("\\\", "\"" ).replaceAll("\\$", "\"" );
        File file = new File(curDir, fname);
        String tmpDir = curDir;
        String tmpFile = curFileName;
        curDir = file.getParent();
        curFileName = file.getName();
        try {
            FileReader reader = new FileReader(file);
            Rcc parser = new Rcc(reader);
        } catch (Exception e) {
            e.printStackTrace();
        }
    }
}
try {
    ret = parser.Input();
    System.out.println(fname + " Parsed Successfully");
} catch (ParseException e) {
    System.out.println(e.toString());
    System.exit(1);
}
try {
    reader.close();
} catch (IOException e) {
}
} catch (FileNotFoundException e) {
    System.out.println("File " + fname + " Not found.");
    System.exit(1);
}
curDir = tmpDir;
curFileName = tmpFile;
return ret;
}

ArrayList<JRecord> Module() :
{
    String mName;
    ArrayList<JRecord> rlist;
}
{
    <MODULE_TKN>
mName = ModuleName()
    { curModuleName = mName; }
    <LBRACE_TKN>
rlist = RecordList()
    <RBRACE_TKN>
    { return rlist; }
}

String ModuleName() :
{
    String name = ";
    Token t;
}
{
    t = <IDENT_TKN>
    { name += t.image; }
    ( <DOT_TKN>
    t = <IDENT_TKN>
ArrayList<JRecord> RecordList() : 
{
    ArrayList<JRecord> rlist = new ArrayList<JRecord>();
    JRecord r;
}
{
(r = Record())
    { rlist.add(r); }
}+
{ return rlist; }
}

JRecord Record() :
{
    String rname;
    ArrayList<JField> flist = new ArrayList<JField>();
    Token t;
    JField f;
}
{
<RECORD_TKN>
    t = <IDENT_TKN>
        { rname = t.image; }
    <LBRACE_TKN>
        (f = Field())
            { flist.add(f); }
            <SEMICOLON_TKN>
    <RBRACE_TKN>
        { String fqn = curModuleName + "." + rname;
            JRecord r = new JRecord(fqn, flist);
            recTab.put(fqn, r);
            return r;
        }
}

JField Field() :
{
    JType jt;
    Token t;
JType Type() :
{
    JType jt;
    Token t;
    String rname;
}
{
    jt = Map()
    { return jt; }
    jt = Vector()
    { return jt; }
| <BYTE_TKN>
    { return new JByte(); }
| <BOOLEAN_TKN>
    { return new JBoolean(); }
| <INT_TKN>
    { return new JInt(); }
| <LONG_TKN>
    { return new JLong(); }
| <FLOAT_TKN>
    { return new JFloat(); }
| <DOUBLE_TKN>
    { return new JDouble(); }
| <USTRING_TKN>
    { return new JString(); }
| <BUFFER_TKN>
    { return new JBuffer(); }
| rname = ModuleName()
{
    if (rname.indexOf('.', 0) < 0) {
        rname = curModuleName + "." + rname;
    }
    JRecord r = recTab.get(rname);
    if (r == null) {
        System.out.println("Type " + rname + " not known. Exiting.");
        System.exit(1);
    }
    return r;
}
}
JMap Map() :
{
    JType jt1;
    JType jt2;
}
{
    <MAP_TKN>
    <LT_TKN>
        jt1 = Type()
    <COMMA_TKN>
        jt2 = Type()
    <GT_TKN>
    { return new JMap(jt1, jt2); }
}

JVector Vector() :
{
    JType jt;
}
{
    <VECTOR_TKN>
    <LT_TKN>
        jt = Type()
    <GT_TKN>
    { return new JVector(jt); }
}

Found in path(s):
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/generated/rcc.jj
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* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/generated/Rcc.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/generated/ParseException.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/generated/TokenMgrError.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/generated/SimpleCharStream.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/generated/Token.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/generated/RccTokenManager.java

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* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/ConnectRequest.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/GetChildrenResponse.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/ErrorResponse.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/WatcherEvent.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/GetSASLRequest.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/SetACLResponse.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/SetDataRequest.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/GetAllChildrenNumberResponse.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/SyncRequest.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/CreateTTLRequest.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/AuthPacket.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/Create2Response.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/GetDataRequest.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/ExistsRequest.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/server/persistence/FileHeader.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/data/ACL.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/GetACLResponse.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/CreateTxnV0.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/GetChildren2Response.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/CheckVersionTxn.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/data/StatPersisted.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/DeleteTxn.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/DeleteRequest.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/SetDataResponse.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/GetAllChildrenNumberRequest.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/CreateRequest.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/RequestHeader.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/ErrorTxn.java
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* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/txn/SetACL Txn.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/ExistsResponse.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/SyncResponse.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/GetChildrenRequest.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/SetSASLResponse.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/GetEphemeralsResponse.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/txn/SetDataTxn.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/txn/CreateTTLTxn.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/server/quorum/QuorumAuthPacket.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/ReconfigRequest.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/GetChildren2Request.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/txn/Txn.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proxy/CloseSessionTxn.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/AddWatchRequest.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/proto/SetMaxChildrenRequest.java
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* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/zookeeper/txn/TxnDigest.java
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* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/JRecord.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/RecordReader.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/JField.java
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* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/Index.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/IInt.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/JMap.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/BinaryInputArchive.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/JFile.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/JLong.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/JDouble.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/InputArchive.java
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* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/JBuffer.java
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* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/JByte.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/Record.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/JavaGenerator.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/ToStringOutputArchive.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/OutputArchive.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/JBoolean.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/RecordWriter.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/JFloat.java
* /opt/cola/permits/1136663495_1613850785.01/0/zookeeper-jute-3-6-2-sources-1-jar/org/apache/jute/compiler/JString.java

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* org.eclipse.jetty.orbit:org.eclipse.jdt.core

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* org.eclipse.jetty.orbit:javax.mail.glassfish

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https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

* javax.servlet:javax.servlet-api
* javax.annotation:javax.annotation-api
* javax.transaction:javax.transaction-api
* javax.websocket:javax.websocket-api

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Oracle OpenJDK

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* java.sun.security.ssl

These artifacts replace/modify OpenJDK classes. The modifications are hosted at github and both modified and original are under GPL v2 with classpath exceptions.
http://openjdk.java.net/legal/gplv2+ce.html

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org.ow2.asm:asm-commons
org.ow2.asm:asm

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Apache

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org.mortbay.jasper:apache-jsp
org.apache.tomcat:tomcat-jasper
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org.apache.tomcat:tomcat-jsp-api
org.apache.tomcat:tomcat-el-api
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-api
org.apache.tomcat:tomcat-util-scan
org.apache.tomcat:tomcat-util
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org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-el-api

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https://glassfish.dev.java.net/nonav/public/CDDL/GPL.html

org.eclipse.jetty.toolchain:jetty-schemas

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Assorted

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* /opt/cola/permits/1130030222_1612433225.54/0/wildfly-elytron-jaspi-1-13-1-final-sources-jar/org/wildfly/security/auth/jaspi/impl/ElytronServerAuthConfig.java
* /opt/cola/permits/1130030222_1612433225.54/0/wildfly-elytron-jaspi-1-13-1-final-sources-jar/org/wildfly/security/auth/jaspi/impl/AuthenticationModuleDefinition.java
* /opt/cola/permits/1130030222_1612433225.54/0/wildfly-elytron-jaspi-1-13-1-final-sources-jar/org/wildfly/security/auth/jaspi/ElytronAuthConfigFactory.java
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1.910 keyutils 1.6-6

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However, unrestricted linking of non-free programs would deprive the users of those programs of all benefit from the free status of the libraries themselves. This Library General Public License is intended to permit developers of non-free programs to use free libraries, while preserving your freedom as a user of such programs to change the free libraries that are incorporated in them. (We have not seen how to achieve this as regards changes in header files, but we have achieved it as regards changes in the actual functions of the Library.) The hope is that this will lead to faster development of free libraries.

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"Source code" for a work means the preferred form of the work for making modifications to it. For a library, complete source code means all the source code for all modules it contains, plus any associated interface definition files, plus the scripts used to control compilation and installation of the library.

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(For example, a function in a library to compute square roots has a purpose that is entirely well-defined independent of the application. Therefore, Subsection 2d requires that any application-supplied function or table used by this function must be optional: if the application does not supply it, the square root function must still compute square roots.)

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```xml
<?xml version="1.0"?>
<xsl:stylesheet version="1.0"
    xmlns:xsl="http://www.w3.org/1999/XSL/Transform">

    <xsl:output method="html" encoding="utf-8" standalone="no" media-type="text/html" />
    <xsl:param name="product"/>
    <xsl:param name="version"/>
    <xsl:variable name="lowercase" select="'abcdefghijklmnopqrstuvwxyz'" />
    <xsl:variable name="uppercase" select="'ABCDEFGHIJKLMNOPQRSTUVWXYZ'" />

    <xsl:template match="/">
        <html>
            <head>
                <meta http-equiv="Content-Type" content="text/html;charset=utf-8" />
                <link rel="stylesheet" type="text/css" href="licenses.css"/>
            </head>
            <body>
                <p>The following material has been provided for informational purposes only, and should not be relied upon or construed as a legal opinion or legal advice.</p>
                <!-- Read matching templates -->
                <table>
                    <tr>
                        <th>Package</th>
                        <th>Package Artifact</th>
                        <th>Package Version</th>
                        <th>Remote Licenses</th>
                        <th>Local Licenses</th>
                    </tr>
                    <xsl:for-each select="licenseSummary/dependencies/dependency">
                        <xsl:sort select="concat(groupId, '.', artifactId)"/>
                        <tr>
                            <td><xsl:value-of select="concat(groupId, packageName)"/></td>
                            <td><xsl:value-of select="artifactId"/></td>
                            <td><xsl:value-of select="version"/></td>
                            <td>
                                <xsl:for-each select="licenses/license">
                                    <a href="{./url}">{name}</a>
                                </xsl:for-each>
                            </td>
                            <td>
                                <xsl:for-each select="licenses/license">
                                    <xsl:variable name="name" select="translate(name,$uppercase,$lowercase)"/>
                                    <xsl:variable name="last-index" select="last-index-of(./url)"/>
                                    <xsl:call-template name="last-index-of">
                                        <xsl:with-param name="txt" select="url"/>
                                        <xsl:with-param name="delimiter" select="/"/>
                                    </xsl:call-template>
                                </xsl:for-each>
                            </td>
                        </tr>
                    </xsl:for-each>
                </table>
            </body>
        </html>
    </xsl:template>
</xsl:stylesheet>
```
<xsl:template name="remap-local-filename">
  <xsl:param name="filename"/>
  <xsl:choose>
    <xsl:when test="contains($filename, 'bsd') and contains($filename, '2-clause')">
      <xsl:text>bsd-2-clause.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'bsd') and contains($filename, '3-clause')">
      <xsl:text>bsd-3-clause.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'apache') and contains($filename, '1.1')">
      <xsl:text>apache-1.1.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'apache') and contains($filename, '2.0')">
      <xsl:text>apache license 2.0.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'jsr-000107')">
      <xsl:text>apache license 2.0.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'cddl') and contains($filename, 'gplv2')">
      <xsl:text>cddl-gplv2-classpath.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'common public license')">
      <xsl:text>common public license 1.0.txt</xsl:text>
    </xsl:when>
    <xsl:when test="$filename = 'gnu library general public license, version 2 - lgpl-2.0.txt'">
      <xsl:text>gnu library general public license, version 2.txt</xsl:text>
    </xsl:when>
    <xsl:when test="$filename = 'lgpl.txt'">
      <xsl:text>gnu library general public license, version 2.txt</xsl:text>
    </xsl:when>
    <xsl:when test="$filename = 'the dom4j license - license'">
      <xsl:text>the dom4j license.txt</xsl:text>
    </xsl:when>
    <xsl:when test="$filename = 'creative commons attribution 2.5 - legalcode'">
      <xsl:text>creative commons attribution 2.5.html</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'cddl+gpl_1_1')">
      <xsl:text>cddl-1.1-gpl-1-1.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'cddl+gpl-1.1')">
      <xsl:text>cddl-1.1-gpl-1-1.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'cddl.txt')">
      <xsl:text>common development and distribution license 1.1.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'common development') and contains($filename, '1.1')">
      <xsl:text>common development and distribution license 1.1.txt</xsl:text>
    </xsl:when>
    <!-- Add more conditions as needed -->
  </xsl:choose>
</xsl:template>
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Version 1.1 - 26 February 2007

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1.938 webauthn4j 0.12.0.RELEASE

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Jackson is a high-performance, Free/Open Source JSON processing library. It was originally written by Tatu Saloranta (tatu.saloranta@iki.fi), and has been in development since 2007. It is currently developed by a community of developers, as well as supported commercially by FasterXML.com.

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1.948 nghttp2 1.42.0-r1

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set yrange [0:]
set terminal pngcairo font 'Sans, 8' lw 1 size 1400,1024
set xtics rotate by -45
set style histogram errorbars gap 2 lw 1
set style fill solid border -1

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The following artifacts are EPL and ASL2.
* org.eclipse.jetty.orbit:javax.security.auth.message

The following artifacts are EPL and CDDL 1.0.
* org.eclipse.jetty.orbit:javax.mail.glassfish

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Oracle

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https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

  * javax.servlet:javax.servlet-api
  * javax.annotation:javax.annotation-api
  * javax.transaction:javax.transaction-api
  * javax.websocket:javax.websocket-api

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Oracle OpenJDK

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* java.sun.security.ssl

These artifacts replace/modify OpenJDK classes. The modifications are hosted at github and both modified and original are under GPL v2 with classpath exceptions.
http://openjdk.java.net/legal/gplv2+ce.html

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OW2
The following artifacts are licensed by the OW2 Foundation according to the terms of http://asm.ow2.org/license.html

org.ow2.asm:asm-commons
org.ow2.asm:asm

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Apache

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org.apache.taglibs:taglibs-standard-spec
org.apache.taglibs:taglibs-standard-impl

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org.mortbay.jasper:apache-jsp
org.apache.tomcat:tomcat-jasper
org.apache.tomcat:tomcat-juli
org.apache.tomcat:tomcat-jsp-api
org.apache.tomcat:tomcat-el-api
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-api
org.apache.tomcat:tomcat-util-scan
org.apache.tomcat:tomcat-util

org.mortbay.jasper:apache-el
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-el-api

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Mortbay

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https://glassfish.dev.java.net/nonav/public/CDDL-GPL.html

org.eclipse.jetty.toolchain:jetty-schemas

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1.969 bash 5.0 4
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* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecserialization/CompatibleObjectEncoder.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecsmarshalling/ThreadLocalUnmarshallerProvider.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecscompression/JZlibEncoder.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecsmarshalling/MessageToMessageDecoder.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecs/DecoderException.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecs/MessageAggregator.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecsmarshalling/LimitingByteInput.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecs/ReplayingDecoder.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecs/bytes/package-info.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecscompression/ZlibUtil.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecs/MessageAggregator.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecsmarshalling/LimitingByteInput.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecs/ReplayingDecoder.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecs/bytes/package-info.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecscompression/ZlibWrapper.java
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  jar/io/netty/handler/codecscompression/package-info.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecsserialization/WeakReferenceMap.java
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  jar/io/netty/handler/codecscompression/ZlibDecoder.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
  jar/io/netty/handler/codecserialization/CompactObjectOutputStream.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
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jar/io/netty/handler/codec/protobuf/ProtobufVarint32FrameDecoder.java
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jar/io/netty/handler/codec/protobuf/ProtobufVarint32LengthFieldPrepender.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-
jar/io/netty/handler/codec/UnsupportedValueConverter.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-jar/io/netty/handler/codec/HeadersUtils.java
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* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-jar/io/netty/handler/codec/protobuf/ProtobufEncoderNano.java

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* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-jar/io/netty/handler/codec/DateFormatter.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-jar/io/netty/handler/codec/CodecOutputList.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-jar/io/netty/handler/codec/CodecOutputList.java
* /opt/ws_local/PERMITS_SQL/1068233848_1594324549.89/0/netty-codec-4-1-50-final-sources-1-jar/io/netty/handler/codec/string/LineEncoder.java

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 */

/**
 * A decoder that splits the received {@link ByteBuf}s dynamically by the
 * value of the length field in the message. It is particularly useful when you
 * decode a binary message which has an integer header field that represents the
 * length of the message body or the whole message.
 *
 * [{@link LengthFieldBasedFrameDecoder}] has many configuration parameters so
 * that it can decode any message with a length field, which is often seen in
 * proprietary client-server protocols. Here are some example that will give
 * you the basic idea on which option does what.
 *
 * <h3>2 bytes length field at offset 0, do not strip header</h3>
 *
 * The value of the length field in this example is <tt>12 (0x0C)</tt> which
 * represents the length of "HELLO, WORLD". By default, the decoder assumes
 * that the length field represents the number of the bytes that follows the
 * length field. Therefore, it can be decoded with the simplistic parameter
 * combination.
 *
 * <pre>
 * <b>lengthFieldOffset</b> = <b>0</b>
 * <b>lengthFieldLength</b> = <b>2</b>
 * </pre>
 */
* lengthAdjustment = 0
* initialBytesToStrip = 0 (= do not strip header)
*
* BEFORE DECODE (14 bytes)       AFTER DECODE (14 bytes)
* +------------------+          +------------------+
* | Length | Actual Content |----->| Length | Actual Content |
* | 0x000C | "HELLO, WORLD" |      | 0x000C | "HELLO, WORLD" |
* +------------------+          +------------------+
* </pre>
*
* \(<h3>2 bytes length field at offset 0, strip header</h3>\)
*
* Because we can get the length of the content by calling
* \{@link ByteBuf#readableBytes()\}, you might want to strip the length
* field by specifying \(<tt>initialBytesToStrip</tt>\). In this example, we
* specified \(<tt>2</tt>\), that is same with the length of the length field, to
* strip the first two bytes.
* <pre>
* lengthFieldOffset = 0
* lengthFieldLength = 2
* lengthAdjustment = 0
* \(<b>initialBytesToStrip</b> = \(<b>2</b>\) (= the length of the Length field)
* </pre>
*
* \(<h3>2 bytes length field at offset 0, do not strip header, the length field
* represents the length of the whole message</h3>\)
*
* In most cases, the length field represents the length of the message body
* only, as shown in the previous examples. However, in some protocols, the
* length field represents the length of the whole message, including the
* message header. In such a case, we specify a non-zero
* \(<tt>lengthAdjustment</tt>\). Because the length value in this example message
* is always greater than the body length by \(<tt>2</tt>\), we specify \(<tt>-2</tt>\) as
* \(<tt>lengthAdjustment</tt>\) for compensation.
* <pre>
* lengthFieldOffset = 0
* lengthFieldLength = 2
* \(<b>lengthAdjustment</b> = \(<b>-2</b>\) (= the length of the Length field)
* initialBytesToStrip = 0
* </pre>
*
* \(<h3>2 bytes length field at offset 0, do not strip header, the length field
* represents the length of the whole message</h3>\)
The following message is a simple variation of the first example. An extra header value is prepended to the message. \texttt{lengthAdjustment} is zero again because the decoder always takes the length of the prepended data into account during frame length calculation.

```
lengthFieldOffset = \texttt{2} (= the length of Header 1)
lengthFieldLength = \texttt{3}
lengthAdjustment = 0
initialBytesToStrip = 0
```

```
BEFORE DECODE (17 bytes)                      AFTER DECODE (17 bytes)
+----------+----------+----------------+      +----------+----------+----------------+
| Header 1 |  Length  | Actual Content |----->| Header 1 |  Length  | Actual Content |
|  0xCAFE  | 0x00000C | "HELLO, WORLD" |      |  0xCAFE  | 0x00000C | "HELLO, WORLD" |
+----------+----------+----------------+      +----------+----------+----------------+
```

This is an advanced example that shows the case where there is an extra header between the length field and the message body. You have to specify a positive \texttt{lengthAdjustment} so that the decoder counts the extra header into the frame length calculation.

```
lengthFieldOffset = 0
lengthFieldLength = \texttt{3}
lengthAdjustment = \texttt{2} (= the length of Header 1)
initialBytesToStrip = 0
```

```
BEFORE DECODE (17 bytes)                      AFTER DECODE (17 bytes)
+----------+----------+----------------+      +----------+----------+----------------+
|  Length  | Header 1 | Actual Content |----->|  Length  | Header 1 | Actual Content |
| 0x00000C |  0xCAFE  | "HELLO, WORLD" |      | 0x00000C | 0xCAFE | "HELLO, WORLD" |
+----------+----------+----------------+      +----------+----------+----------------+
```

This is a combination of all the examples above. There are the prepended header before the length field and the extra header after the length field.
* The prepended header affects the `<tt>lengthFieldOffset</tt>` and the extra
* header affects the `<tt>lengthAdjustment</tt>`. We also specified a non-zero
* `<tt>initialBytesToStrip</tt>` to strip the length field and the prepended
* header from the frame. If you don't want to strip the prepended header, you
* could specify `<tt>0</tt>` for `<tt>initialBytesToSkip</tt>`.
* <pre>
* lengthFieldOffset   = 1 (= the length of HDR1)
* lengthFieldLength   = 2
* &lt;b&gt;lengthAdjustment&lt;/b&gt; = &lt;b&gt;1&lt;/b&gt; (= the length of HDR2)
* &lt;b&gt;initialBytesToStrip&lt;/b&gt; = &lt;b&gt;3&lt;/b&gt; (= the length of HDR1 + LEN)
* 
* BEFORE DECODE (16 bytes)                       AFTER DECODE (13 bytes)
* +-------------------------+------------------+
* | HDR1 | Length | HDR2 | Actual Content |----->| HDR2 | Actual Content |
* | 0xCA | 0x000C | 0xFE | "HELLO, WORLD" |      | 0xFE | "HELLO, WORLD" |
* +-------------------------+------------------+
* </pre>

* <h3>2 bytes length field at offset 1 in the middle of 4 bytes header,
* strip the first header field and the length field, the length field
* represents the length of the whole message</h3>

* Let's give another twist to the previous example. The only difference from
* the previous example is that the length field represents the length of the
* whole message instead of the message body, just like the third example.
* We have to count the length of HDR1 and Length into `<tt>lengthAdjustment</tt>`.
* Please note that we don't need to take the length of HDR2 into account
* because the length field already includes the whole header length.
* <pre>
* lengthFieldOffset   = 1
* lengthFieldLength   = 2
* &lt;b&gt;lengthAdjustment&lt;/b&gt; = &lt;b&gt;-3&lt;/b&gt; (= the length of HDR1 + LEN, negative)
* &lt;b&gt;initialBytesToStrip&lt;/b&gt; = &lt;b&gt;3&lt;/b&gt;
* 
* BEFORE DECODE (16 bytes)                       AFTER DECODE (13 bytes)
* +-------------------------+------------------+
* | HDR1 | Length | HDR2 | Actual Content |----->| HDR2 | Actual Content |
* | 0xCA | 0x0010 | 0xFE | "HELLO, WORLD" |      | 0xFE | "HELLO, WORLD" |
* +-------------------------+------------------+
* </pre>

* @see LengthFieldPrepender
*/

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/**
 * Enumeration of supported Base64 dialects.
 * <p>
 * The internal lookup tables in this class has been derived from
 * <a href="http://iharder.sourceforge.net/current/java/base64/">Robert Harder's Public Domain
 * Base64 Encoder/Decoder</a>.
 */

/*

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* jar/io/netty/handler/codec/base64/Base64Dialect.java

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1.977 open-ldap 2.4.57-r1

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# RESTEasy Spring Boot Starter

This Spring Boot starter can be used by any regular Spring Boot application that wants to have REST endpoints and prefers RESTEasy as the JAX-RS implementation.

Also, this RESTEasy Spring Boot starter integrates with Spring as expected, which means every JAX-RS REST resource that is also a Spring bean will be automatically auto-scanned, integrated, and available.
## Features
* Enables RESTEasy for Spring Boot applications
* Supports JAX-RS providers, resources and sub-resources as Spring beans
* Supports automatic discovery and registration of multiple JAX-RS Application](http://docs.oracle.com/javaee/7/api/javax/ws/rs/core/Application.html) classes as Spring beans
* Supports optional registration of JAX-RS Application](http://docs.oracle.com/javaee/7/api/javax/ws/rs/core/Application.html) classes via class-path scanning, or manually, via configuration properties (or YAML) file
* Leverages and supports RESTEasy configuration
* Supports RESTEasy Asynchronous Job Service

*This project has been kindly donated by PayPal. Please refer to https://github.com/paypal/resteasy-spring-boot for old versions.*

## Quick start

### Adding POM dependency
Add the Maven dependency below to your Spring Boot application pom file.

``` xml
<dependency>
    <groupId>org.jboss.resteasy</groupId>
    <artifactId>resteasy-spring-boot-starter</artifactId>
    <version>4.8.1.Final</version>
    <scope>runtime</scope>
</dependency>
```

### Registering JAX-RS application classes
Just define your JAX-RS application class (a subclass of [Application](http://docs.oracle.com/javaee/7/api/javax/ws/rs/core/Application.html)) as a Spring bean, and it will be automatically registered. See the example below.

See section _JAX-RS application registration methods_ in [How to use RESTEasy Spring Boot Starter](mds/USAGE.md) for further information.

``` java
package com.sample.app;

import org.springframework.stereotype.Component;
import javax.ws.rs.ApplicationPath;
import javax.ws.rs.core.Application;

@Component
@ApplicationPath("/sample-app")
public class JaxrsApplication extends Application {
}
```
### Registering JAX-RS resources and providers
Just define them as Spring beans, and they will be automatically registered.
Notice that JAX-RS resources can be singleton or request scoped, while JAX-RS providers must be singletons.

### Further information
See [How to use RESTEasy Spring Boot Starter](mds/USAGE.md).

## Projects
- **sample-app**: A simple Spring Boot application that exposes JAX-RS endpoints as Spring beans using RESTEasy via this RESTEasy Spring Boot starter.
- **resteasy-spring-boot-starter**: The RESTEasy Spring Boot Starter project.
- **resteasy-spring-boot-starter-test**: Integration tests for the RESTEasy Spring Boot Starter project.

## Reporting an issue
Please open an issue using [JIRA](https://issues.jboss.org/browse/RESTEASY) (be sure to set *Spring / Spring Boot* in the *Component/s* field).

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* /opt/ws_local/PERMITS_SQL/1072948687_1595240769.66/0/netty-handler-4-1-51-final-sources-jar/io/netty/handler/traffic/GlobalChannelTrafficShapingHandler.java
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jar/io/netty/handler/address/ResolveAddressHandler.java
* /opt/ws_local/PERMITS_SQL/1072948687_1595240769.66/0/netty-handler-4-1-51-final-sources-
jar/io/netty/handler/logging/ByteBufFormat.java
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[This is the first released version of the Lesser GPL. It also counts
as the successor of the GNU Library Public License, version 2, hence
the version number 2.1.]

Preamble

The licenses for most software are designed to take away your
freedom to share and change it. By contrast, the GNU General Public
Licenses are intended to guarantee your freedom to share and change
free software--to make sure the software is free for all its users.

This license, the Lesser General Public License, applies to some
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can use it too, but we suggest you first think carefully about whether
this license or the ordinary General Public License is the better
strategy to use in any particular case, based on the explanations
below.

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For example, if you distribute copies of the library, whether gratis
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We protect your rights with a two-step method: (1) we copyright the library, and (2) we offer you this license, which gives you legal permission to copy, distribute and/or modify the library.

To protect each distributor, we want to make it very clear that there is no warranty for the free library. Also, if the library is modified by someone else and passed on, the recipients should know that what they have is not the original version, so that the original author's reputation will not be affected by problems that might be introduced by others.

Finally, software patents pose a constant threat to the existence of any free program. We wish to make sure that a company cannot effectively restrict the users of a free program by obtaining a restrictive license from a patent holder. Therefore, we insist that any patent license obtained for a version of the library must be consistent with the full freedom of use specified in this license.

Most GNU software, including some libraries, is covered by the ordinary GNU General Public License. This license, the GNU Lesser General Public License, applies to certain designated libraries, and is quite different from the ordinary General Public License. We use this license for certain libraries in order to permit linking those libraries into non-free programs.

When a program is linked with a library, whether statically or using a shared library, the combination of the two is legally speaking a combined work, a derivative of the original library. The ordinary General Public License therefore permits such linking only if the entire combination fits its criteria of freedom. The Lesser General Public License permits more lax criteria for linking other code with the library.

We call this license the "Lesser" General Public License because it does Less to protect the user's freedom than the ordinary General Public License. It also provides other free software developers Less of an advantage over competing non-free programs. These disadvantages are the reason we use the ordinary General Public License for many libraries. However, the Lesser license provides advantages in certain special circumstances.
For example, on rare occasions, there may be a special need to encourage the widest possible use of a certain library, so that it becomes a de-facto standard. To achieve this, non-free programs must be allowed to use the library. A more frequent case is that a free library does the same job as widely used non-free libraries. In this case, there is little to gain by limiting the free library to free software only, so we use the Lesser General Public License.

In other cases, permission to use a particular library in non-free programs enables a greater number of people to use a large body of free software. For example, permission to use the GNU C Library in non-free programs enables many more people to use the whole GNU operating system, as well as its variant, the GNU/Linux operating system.

Although the Lesser General Public License is less protective of the users' freedom, it does ensure that the user of a program that is linked with the Library has the freedom and the wherewithal to run that program using a modified version of the Library.

The precise terms and conditions for copying, distribution and modification follow. Pay close attention to the difference between a "work based on the library" and a "work that uses the library". The former contains code derived from the library, whereas the latter must be combined with the library in order to run.

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0. This License Agreement applies to any software library or other program which contains a notice placed by the copyright holder or other authorized party saying it may be distributed under the terms of this Lesser General Public License (also called "this License"). Each licensee is addressed as "you".

A "library" means a collection of software functions and/or data prepared so as to be conveniently linked with application programs (which use some of those functions and data) to form executables.

The "Library", below, refers to any such software library or work which has been distributed under these terms. A "work based on the Library" means either the Library or any derivative work under copyright law: that is to say, a work containing the Library or a portion of it, either verbatim or with modifications and/or translated straightforwardly into another language. (Hereinafter, translation is included without limitation in the term "modification".)
"Source code" for a work means the preferred form of the work for making modifications to it. For a library, complete source code means all the source code for all modules it contains, plus any associated interface definition files, plus the scripts used to control compilation and installation of the library.

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You may charge a fee for the physical act of transferring a copy, and you may at your option offer warranty protection in exchange for a fee.

2. You may modify your copy or copies of the Library or any portion of it, thus forming a work based on the Library, and copy and distribute such modifications or work under the terms of Section 1 above, provided that you also meet all of these conditions:

   a) The modified work must itself be a software library.

   b) You must cause the files modified to carry prominent notices stating that you changed the files and the date of any change.

   c) You must cause the whole of the work to be licensed at no charge to all third parties under the terms of this License.

   d) If a facility in the modified Library refers to a function or a table of data to be supplied by an application program that uses the facility, other than as an argument passed when the facility is invoked, then you must make a good faith effort to ensure that, in the event an application does not supply such function or table, the facility still operates, and performs whatever part of its purpose remains meaningful.
(For example, a function in a library to compute square roots has a purpose that is entirely well-defined independent of the application. Therefore, Subsection 2d requires that any application-supplied function or table used by this function must be optional: if the application does not supply it, the square root function must still compute square roots.)

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Thus, it is not the intent of this section to claim rights or contest your rights to work written entirely by you; rather, the intent is to exercise the right to control the distribution of derivative or collective works based on the Library.

In addition, mere aggregation of another work not based on the Library with the Library (or with a work based on the Library) on a volume of a storage or distribution medium does not bring the other work under the scope of this License.

3. You may opt to apply the terms of the ordinary GNU General Public License instead of this License to a given copy of the Library. To do this, you must alter all the notices that refer to this License, so that they refer to the ordinary GNU General Public License, version 2, instead of to this License. (If a newer version than version 2 of the ordinary GNU General Public License has appeared, then you can specify that version instead if you wish.) Do not make any other change in these notices.

^L
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This option is useful when you wish to copy part of the code of the Library into a program that is not a library.

4. You may copy and distribute the Library (or a portion or derivative of it, under Section 2) in object code or executable form under the terms of Sections 1 and 2 above provided that you accompany it with the complete corresponding machine-readable source code, which
must be distributed under the terms of Sections 1 and 2 above on a medium customarily used for software interchange.

If distribution of object code is made by offering access to copy from a designated place, then offering equivalent access to copy the source code from the same place satisfies the requirement to distribute the source code, even though third parties are not compelled to copy the source along with the object code.

5. A program that contains no derivative of any portion of the Library, but is designed to work with the Library by being compiled or linked with it, is called a "work that uses the Library". Such a work, in isolation, is not a derivative work of the Library, and therefore falls outside the scope of this License.

However, linking a "work that uses the Library" with the Library creates an executable that is a derivative of the Library (because it contains portions of the Library), rather than a "work that uses the library". The executable is therefore covered by this License. Section 6 states terms for distribution of such executables.

When a "work that uses the Library" uses material from a header file that is part of the Library, the object code for the work may be a derivative work of the Library even though the source code is not. Whether this is true is especially significant if the work can be linked without the Library, or if the work is itself a library. The threshold for this to be true is not precisely defined by law.

If such an object file uses only numerical parameters, data structure layouts and accessors, and small macros and small inline functions (ten lines or less in length), then the use of the object file is unrestricted, regardless of whether it is legally a derivative work. (Executables containing this object code plus portions of the Library will still fall under Section 6.)

Otherwise, if the work is a derivative of the Library, you may distribute the object code for the work under the terms of Section 6. Any executables containing that work also fall under Section 6, whether or not they are linked directly with the Library itself.

6. As an exception to the Sections above, you may also combine or link a "work that uses the Library" with the Library to produce a work containing portions of the Library, and distribute that work under terms of your choice, provided that the terms permit modification of the work for the customer's own use and reverse engineering for debugging such modifications.

You must give prominent notice with each copy of the work that the
Library is used in it and that the Library and its use are covered by this License. You must supply a copy of this License. If the work during execution displays copyright notices, you must include the copyright notice for the Library among them, as well as a reference directing the user to the copy of this License. Also, you must do one of these things:

a) Accompany the work with the complete corresponding machine-readable source code for the Library including whatever changes were used in the work (which must be distributed under Sections 1 and 2 above); and, if the work is an executable linked with the Library, with the complete machine-readable "work that uses the Library", as object code and/or source code, so that the user can modify the Library and then relink to produce a modified executable containing the modified Library. (It is understood that the user who changes the contents of definitions files in the Library will not necessarily be able to recompile the application to use the modified definitions.)

b) Use a suitable shared library mechanism for linking with the Library. A suitable mechanism is one that (1) uses at run time a copy of the library already present on the user's computer system, rather than copying library functions into the executable, and (2) will operate properly with a modified version of the library, if the user installs one, as long as the modified version is interface-compatible with the version that the work was made with.

c) Accompany the work with a written offer, valid for at least three years, to give the same user the materials specified in Subsection 6a, above, for a charge no more than the cost of performing this distribution.

d) If distribution of the work is made by offering access to copy from a designated place, offer equivalent access to copy the above specified materials from the same place.

e) Verify that the user has already received a copy of these materials or that you have already sent this user a copy.

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   b) Give prominent notice with the combined library of the fact that part of it is a work based on the Library, and explaining where to find the accompanying uncombined form of the same work.

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effectively convey the exclusion of warranty; and each file should
have at least the "copyright" line and a pointer to where the full
notice is found.

<one line to give the library's name and a brief idea of what it
does.>
Copyright (C) <year> <name of author>

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License along with this library; if not, write to the Free Software
Foundation, Inc., 51 Franklin Street, Fifth Floor, Boston, MA 02110-1301 USA

Also add information on how to contact you by electronic and paper
mail.

You should also get your employer (if you work as a programmer) or
your
school, if any, to sign a "copyright disclaimer" for the library, if
necessary. Here is a sample; alter the names:

Yoyodyne, Inc., hereby disclaims all copyright interest in the
library 'Frob' (a library for tweaking knobs) written by James
Random Hacker.

<signature of Ty Coon>, 1 April 1990
Ty Coon, President of Vice

That's all there is to it!

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EFFECTIVE OCT 2008, LICENSE IS BEING CHANGED TO LGPL-2.1 (though not reflected
in released code until Nov 2009 - slow release cycle...)

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Discussion thread from mailing list archive, with approval from everyone actively
involved or holding original licensing rights included.
Re: [Cracklib-devel] cracklib license
From: Mike Frysinger <vapier@ge...> - 2007-10-02 01:16

Attachments: Message as HTML
looks like 2.8.11 is out and marked as "GPL-2" ... releasing libraries unde=

r=20
GPL-2 is not desirable at all ... this is why the LGPL-2.1 exists
=2Dmike

Re: [Cracklib-devel] cracklib license
From: Neulinger, Nathan <nneul@um...> - 2007-10-02 01:18
I understand that, and you're welcome to bring it up with Alec directly
and see if he wants to relicense his code as LGPL... but at this point,
it was enough to just get it consistent and documented as to what it was
released under. This wasn't actually a license change, just a
clarification of the licensing that was already in place.=20

-- Nathan
=20

Nathan Neulinger
EMail: nneul@um...
University of Missouri - Rolla Phone: (573) 341-6679
UMR Information Technology Fax: (573) 341-4216

> -----Original Message-----
> From: cracklib-devel-bounces@li...
> [mailto:cracklib-devel-bounces@li...] On Behalf Of
> Mike Frysinger
> Sent: Monday, October 01, 2007 8:15 PM
> To: cracklib-devel@li...
> Subject: [Cracklib-devel] cracklib license
>=20
> looks like 2.8.11 is out and marked as "GPL-2" ... releasing
> libraries under
> GPL-2 is not desirable at all ... this is why the LGPL-2.1 exists
> -mike

Re: [Cracklib-devel] cracklib license
From: Mike Frysinger <vapier@ge...> - 2007-10-02 01:33

Attachments: Message as HTML
On Monday 01 October 2007, Neulinger, Nathan wrote:
> I understand that, and you're welcome to bring it up with Alec directly
> and see if he wants to relicense his code as LGPL... but at this point,
> it was enough to just get it consistent and documented as to what it was
released under. This wasn't actually a license change, just a clarification of the licensing that was already in place.

the original license (before moving to sourceforge -- aka, 2.7) was not GPL-2 ... it was a modified artistic license ... i didn't notice the license change until it was mentioned in the latest notes.

unlike the old license, GPL-2 prevents people from using cracklib unless their applications are also GPL-2 which imo is just wrong. it isn't the place of a library to dictate to application writes what license they should be using. thus LGPL-2.1 enters to fill this void.

DMike

Re: [Cracklib-devel] cracklib license
From: Neulinger, Nathan <nneul@um...> - 2007-10-02 01:46
Seems like the ideal thing here would be for you and the other distro maintainers to get together with Alec in a conversation and come to a decision as to what licensing scheme y'all want. I haven't really done much other than cleaning up the packaging and patches and a small bit of additional code, so whatever licensing y'all come up with is fine by me.

-- Nathan

Nathan Neulinger EMail: nneul@um...
University of Missouri - Rolla Phone: (573) 341-6679
UMR Information Technology Fax: (573) 341-4216

----Original Message-----
From: cracklib-devel-bounces@li...
[mailto:cracklib-devel-bounces@li...] On Behalf Of Mike Frysinger
Sent: Monday, October 01, 2007 8:33 PM
To: Neulinger, Nathan
Cc: cracklib-devel@li...; Alec Muffett
Subject: Re: [Cracklib-devel] cracklib license

On Monday 01 October 2007, Neulinger, Nathan wrote:
> I understand that, and you're welcome to bring it up with Alec directly
> and see if he wants to relicense his code as LGPL... but at this point,
> it was enough to just get it consistent and documented as to what
> it was
> > released under. This wasn't actually a license change, just a
> > clarification of the licensing that was already in place.
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> > the original license (before moving to sourceforge -- aka, 2.7) was
> > not
> > GPL-2 ... it was a modified artistic license ... i didn't notice the
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> > unlike the old license, GPL-2 prevents people from using cracklib
> > unless their
> > applications are also GPL-2 which imo is just wrong. It isn't the
> > place of a
> > library to dictate to application writes what license they should
> > be using.
> > thus LGPL-2.1 enters to fill this void.
> > -mike

Re: [Cracklib-devel] cracklib license
From: Alec Muffett <alecm@cr...> - 2007-10-02 08:57
> Seems like the ideal thing here would be for you and the other distro
> maintainers to get together with Alec in a conversation and come to a
> decision as to what licensing scheme y'all want. I haven't really done
> much other than cleaning up the packaging and patches and a small
> bit of
> additional code, so whatever licensing y'all come up with is fine
> by me.

I am sympathetic. Guys, what do you reckon?

What I am hearing so far is that LGPL makes sense, since it can be
linked with any code, not just GPL....

-a

Re: [Cracklib-devel] cracklib license
From: Devin Reade <gdr@gn...> - 2007-10-02 15:04
I would like to see it under LGPL as well. I think it is in everyone’s
best interests to have as secure systems as possible, and I think tainting
it via GPL will just make it less likely that the library gets used, and
will not usually cause companies/developers to GPL the dependent code
(where it is not already GPL).

I like GPL, I use it when I can, but I don't think that it's the correct
license in this situation.
Devin
--
If it's sinful, it's more fun.

Re: [Cracklib-devel] cracklib license
From: Nalin Dahyabhai <nalin@re...> - 2008-01-28 16:32
On Tue, Oct 02, 2007 at 09:57:31AM +0100, Alec Muffett wrote:
> > > Seems like the ideal thing here would be for you and the other distro
> > > maintainers to get together with Alec in a conversation and come to a
> > > decision as to what licensing scheme y'all want. I haven't really done
> > > much other than cleaning up the packaging and patches and a small
> > > bit of
> > > additional code, so whatever licensing y'all come up with is fine
> > > by me.
> >
> > I am sympathetic. Guys, what do you reckon?
>
> > What I am hearing so far is that LGPL makes sense, since it can be
> > linked with any code, not just GPL...
>
> My apologies for not chiming in in anything resembling a reasonable
timeframe.

I'd also suggest the LGPL, for the reason you noted above. Alternately,
GPLv2 with the option of using the library under a later version of the
GPL would permit applications which were released under version 3 of the
GPL to use the library, too, which would be sufficient for the packages
which are included in Fedora. FWIW, I'd personally lean toward LGPL.

In any case, I thank you both for working on sorting this out.

Cheers,

Nalin

Re: [Cracklib-devel] cracklib license
From: Mike Frysinger <vapier@ge...> - 2008-10-05 21:27

Attachments: Message as HTML
On Monday 28 January 2008, Nalin Dahyabhai wrote:
> On Tue, Oct 02, 2007 at 09:57:31AM +0100, Alec Muffett wrote:
> > > > Seems like the ideal thing here would be for you and the other distro
> > > > maintainers to get together with Alec in a conversation and come to a
> > > > decision as to what licensing scheme y'all want. I haven't really done
> > > > much other than cleaning up the packaging and patches and a small
> > > bit of
> > > additional code, so whatever licensing y'all come up with is fine
> > > by me.
> > >
> > > I am sympathetic. Guys, what do you reckon?
> > >
> > > What I am hearing so far is that LGPL makes sense, since it can be
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> > >
> > > My apologies for not chiming in in anything resembling a reasonable
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> > >
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> > > which are included in Fedora. FWIW, I'd personally lean toward LGPL.
> > >
> > > In any case, I thank you both for working on sorting this out.

looks like everyone is OK with LGPL-2.1 (GNU Lesser license), so can we make
the change now ?

-mike

Re: [Cracklib-devel] cracklib license
From: Alec Muffett <alecm@cr...> - 2008-10-05 23:18
>> In any case, I thank you both for working on sorting this out.
>
> looks like everyone is OK with LGPL-2.1 (GNU Lesser license), so can we make
> the change now ?

yes. go for it. thanks++

-a

Re: [Cracklib-devel] cracklib license
From: Mike Frysinger <vapier@ge...> - 2008-10-25 22:34

Attachments: Message as HTML
On Sunday 05 October 2008, Alec Muffett wrote:
> >> In any case, I thank you both for working on sorting this out.
> >
> > looks like everyone is OK with LGPL-2.1 (GNU Lesser license), so can we
> > make the change now ?
>>
> yes. go for it. thanks++
Nathan Neulinger is the only one who can actually make said change ...

-mike

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BELOW IS ORIGINAL LICENSING DISCUSSION RE CHANGING TO GPL from Artistic.

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CrackLib was originally licensed with a variant of the Artistic license. In the interests of wider acceptance and more modern licensing, it was switched with the original author's blessing to GPL v2.

This approval was carried out in email discussions in 2005, and has been reconfirmed as of 2007-10-01 with the following email from Alec Muffett.

The below email references nneul@umr.edu address, as that is the address that was used at the time. For any future emails regarding this, please use nneul@neulinger.org.

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From alecm@crypticide.com Mon Oct 1 12:26:03 2007
Received: from umr-exproto2.cc.umr.edu ([131.151.0.192]) by UMR-CMAIL1.umr.edu with Microsoft SMTPSVC (6.0.3790.3959); Mon, 1 Oct 2007 12:26:03 -0500
Received: from scansrv2.srv.mst.edu ([131.151.1.114]) by umr-exproto2.cc.umr.edu with Microsoft SMTPSVC (6.0.3790.3959);
Mon, 1 Oct 2007 12:26:02 -0500
Received: (qmail 8022 invoked from network); 1 Oct 2007 16:59:55 -0000
Received: from smtp1.srv.mst.edu (131.151.1.43) by scanin-ipvs.cc.umr.edu with SMTP; 1 Oct 2007 16:59:55 -0000
Received: from spunkymail-mx8.g.dreamhost.com (mx1.spunky.mail.dreamhost.com [208.97.132.47]) by smtp1.srv.mst.edu (8.13.1/8.13.1) with ESMTP id l91Gxtpr020623 for <nneul@umr.edu>; Mon, 1 Oct 2007 11:59:55 -0500
Received: from rutherford.zen.co.uk (rutherford.zen.co.uk [212.23.3.142]) by spunkymail-mx8.g.dreamhost.com (Postfix) with ESMTP id 2C7734D311 for <nneul@neulinger.org>; Mon, 1 Oct 2007 09:59:50 -0700 (PDT)
Received: from [82.68.43.14] (helo=[192.168.1.3])
by rutherford.zen.co.uk with esmtp (Exim 4.50)
id 1IcOcX-0004Qt-6L
for nneul@neulinger.org; Mon, 01 Oct 2007 16:59:49 +0000
Mime-Version: 1.0 (Apple Message framework v752.2)
In-Reply-To: <1b1b3fd80710010908k11dac0afp1f2dd471059ff9a4@mail.gmail.com>
References: <1190922867.3457.147.camel@localhost.localdomain>
Any chance you could write me a self-contained email stating clearly that the license is being changed to GPL, so I could include that email in the repository and clean up the repository/tarballs? I have all the original discussion, but something succinct and self-contained would be ideal.

The license for my code in the Cracklib distribution is henceforth GPL.

Happy now? :-)
define void @autogen_SD4739(i8*) {
  ; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
  BB:
  %L34 = load i8, i8* %0
  %Cmp56 = icmp sgt i8 undef, %L34
  br label %CF246
CF246:                                            ; preds = %CF246, %BB
  %Sl163 = select i1 %Cmp56, i8 %L34, i8 undef
  br i1 undef, label %CF246, label %CF248
CF248:                                            ; preds = %CF248, %CF246
  store i8 %Sl163, i8* %0
  br label %CF248
}

; NOT: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit,avx512vnni | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; Make sure CPUs default to prefer-256-bit. avx512vnni isn't interesting as it just adds an isel peephole for vpmaddwd+vpadddd
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=avx512vnni -mcpu=cascadelake | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=avx512vnni -mcpu=cooperlake | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=cannonlake | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=avx512vnni -mcpu=icelake-client | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=avx512vnni -mcpu=icelake-server | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
}
define void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="256" { 
; CHECK-LABEL: add256:
; CHECK:    # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpadd 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT: vpadd (%rsi), %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
    %d = load <16 x i32>, <16 x i32>* %a
    %e = load <16 x i32>, <16 x i32>* %b
    %f = add <16 x i32> %d, %e
    store <16 x i32> %f, <16 x i32>* %c
ret void
}

define void @add512(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="512" { 
; CHECK-LABEL: add512:
; CHECK:    # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT: vpadd (%rsi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
    %d = load <16 x i32>, <16 x i32>* %a
    %e = load <16 x i32>, <16 x i32>* %b
    %f = add <16 x i32> %d, %e
    store <16 x i32> %f, <16 x i32>* %c
ret void
}

define void @avg_v64i8_256(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="256" { 
; CHECK-LABEL: avg_v64i8_256:
; CHECK:    # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT: vpavgb (%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpavgb 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT: vmovdqu %ymm1, (%rax)

; This file primarily contains tests for specific places in X86ISelLowering.cpp that needed to be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.
; CHECK-NEXT:  vmovdqu %ymm0, (%rax)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%1 = load <64 x i8>, <64 x i8>* %a
%2 = load <64 x i8>, <64 x i8>* %b
%3 = zext <64 x i8> %1 to <64 x i32>
%4 = zext <64 x i8> %2 to <64 x i32>
%5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
%6 = add nuw nsw <64 x i32> %5, %4
%7 = lshr <64 x i32> %6, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
%8 = trunc <64 x i32> %7 to <64 x i8>
store <64 x i8> %8, <64 x i8>* undef, align 4
ret void

define void @avg_v64i8_512(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="512" {  
; CHECK-LABEL: avg_v64i8_512:
; CHECK:  
; CHECK-NEXT:  vmovdq64 (%rsi), %zmm0
; CHECK-NEXT:  vpavgb (%rdi), %zmm0, %zmm0
; CHECK-NEXT:  vmovdqu64 %zmm0, (%rax)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%1 = load <64 x i8>, <64 x i8>* %a
%2 = load <64 x i8>, <64 x i8>* %b
%3 = zext <64 x i8> %1 to <64 x i32>
%4 = zext <64 x i8> %2 to <64 x i32>
%5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
%6 = add nuw nsw <64 x i32> %5, %4
%7 = lshr <64 x i32> %6, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
%8 = trunc <64 x i32> %7 to <64 x i8>
store <64 x i8> %8, <64 x i8>* undef, align 4
ret void
}
define void @pmaddwd_32_256(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="256" {
; CHECK-LABEL: pmaddwd_32_256:
; CHECK:    # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmaddwd 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT: vpmaddwd (%rsi), %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%A = load <32 x i16>, <32 x i16>* %APtr
%B = load <32 x i16>, <32 x i16>* %BPtr
%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}
}

define void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="512" {
; CHECK-LABEL: pmaddwd_32_512:
; CHECK:    # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT: vpmaddwd (%rsi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%A = load <32 x i16>, <32 x i16>* %APtr
%B = load <32 x i16>, <32 x i16>* %BPtr
%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}
define void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: psubus_64i8_max_256:
  ; CHECK:    # %bb.0:
  ; CHECK-NEXT: vmovdqa (%rdi), %ymm0
  ; CHECK-NEXT: vpsubusb 32(%rsi), %ymm1, %ymm1
  ; CHECK-NEXT: vpsubusb (%rsi), %ymm0, %ymm0
  ; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
  ; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
  ; CHECK-NEXT: vzeroupper
  ; CHECK-NEXT: retq
  %x = load <64 x i8>, <64 x i8>* %xptr
  %y = load <64 x i8>, <64 x i8>* %yptr
  %cmp = icmp ult <64 x i8> %x, %y
  %max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
  %res = sub <64 x i8> %max, %y
  store <64 x i8> %res, <64 x i8>* %zptr
  ret void
}

define void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="512" {
  ; CHECK-LABEL: psubus_64i8_max_512:
  ; CHECK:    # %bb.0:
  ; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
  ; CHECK-NEXT: vpsubusb (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
  ; CHECK-NEXT: vzeroupper
  ; CHECK-NEXT: retq
  %x = load <64 x i8>, <64 x i8>* %xptr
  %y = load <64 x i8>, <64 x i8>* %yptr
  %cmp = icmp ult <64 x i8> %x, %y
  %max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
  %res = sub <64 x i8> %max, %y
  store <64 x i8> %res, <64 x i8>* %zptr
  ret void
}

define i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: _Z9test_charPcS_i_256:
  ; CHECK:    # %bb.0: # %entry
  ; CHECK-NEXT: movl %edx, %eax
  ; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
  ; CHECK-NEXT: xorl %ecx, %ecx
  ; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
}

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; CHECK-NEXT:  vpxor %xmm2, %xmm2, %xmm2
; CHECK-NEXT:  .p2align 4, 0x90
; CHECK-NEXT:  .LBB8_1: # %vector.body
; CHECK-NEXT:  # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:  vpmovsxbw (%rdi,%rcx), %ymm3
; CHECK-NEXT:  vpmovsxbw 16(%rdi,%rcx), %ymm4
; CHECK-NEXT:  vpmaddwd %ymm3, %ymm5, %ymm3
; CHECK-NEXT:  vpaddd %ymm1, %ymm3, %ymm1
; CHECK-NEXT:  vpmovsxbw (%rsi,%rcx), %ymm5
; CHECK-NEXT:  vpmaddwd %ymm3, %ymm5, %ymm3
; CHECK-NEXT:  vpaddd %ymm2, %ymm3, %ymm2
; CHECK-NEXT:  addq $32, %rcx
; CHECK-NEXT:  cmpq %rcx, %rax
; CHECK-NEXT:  jne .LBB8_1
; CHECK-NEXT:  .bb.2: # %middle.block
; CHECK-NEXT:  vpaddd %ymm0, %ymm1, %ymm1
; CHECK-NEXT:  vpaddd %ymm0, %ymm2, %ymm0
; CHECK-NEXT:  vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT:  vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vmovd %xmm0, %eax
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq

entry:
%3 = zext i32 %2 to i64
br label %vector.body

vector.body:
%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %i, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body
%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 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entry:
%.3 = zext i32 %.2 to i64
br label %.vector.body

vector.body:
%.index = phi i64 [ %.index.next, %.vector.body ], [ 0, %.entry ]
%.vec.phi = phi <32 x i32> [ %.11, %.vector.body ], [ zeroinitializer, %.entry ]
%.4 = getelementptr inbounds i8, i8* %.2, i64 %.index
%.5 = bitcast i8* %.4 to <32 x i8>*
%.wide.load = load <32 x i8>, <32 x i8>* %.5, align 1
%.6 = sext <32 x i8> %.wide.load to <32 x i32>
%.7 = getelementptr inbounds i8, i8* %.1, i64 %.index
%.8 = bitcast i8* %.7 to <32 x i8>*
%.wide.load14 = load <32 x i8>, <32 x i8>* %.8, align 1
%.9 = sext <32 x i8> %.wide.load14 to <32 x i32>
%.10 = mul nsw <32 x i32> %.9, %.6
%.11 = add nsw <32 x i32> %.10, %.vec.phi
%.index.next = add i64 %.index, 32
%.12 = icmp eq i64 %.index.next, %.3
br i1 %.12, label %.middle.block, label %.vector.body

middle.block:
%.rdx.shuf1 = shufflevector <32 x i32> %.11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 unde
define i32 @sad_16i8_256() "min-legal-vector-width"="256" {
; CHECK-LABEL: sad_16i8_256:
; CHECK:      # %bb.0: # %entry
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: movq $-1024, %rax # imm = 0xFC00
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB10_1: # %vector.body
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-NEXT: vmovdqu a+1024(%rax), %xmm2
; CHECK-NEXT: vpsadbw b+1024(%rax), %xmm2, %xmm2
; CHECK-NEXT: vpaddd %ymm1, %ymm2, %ymm1
; CHECK-NEXT: vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT: vpaddd %ymm2, %ymm1, %ymm2
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT: vpaddd %ymm1, %ymm0, %ymm0
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT: vpaddd %ymm1, %ymm0, %ymm0
; CHECK-NEXT: vpaddd %ymm1, %ymm0, %ymm0
; CHECK-NEXT: vmovd %ymm0, %eax
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
entry:
br label %vector.body
define i32 @sad_16i8_512() "min-legal-vector-width"="512" {
  ; CHECK-LABEL: sad_16i8_512:
  ; CHECK:    # %bb.0: # %entry
  ; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
  ; CHECK-NEXT:    movq $-1024, %rax # imm = 0xFC00
  ; CHECK-NEXT:    .p2align 4, 0x90

  ; middle.block:
  %.lcssa = phi <16 x i32> [ %10, %vector.body ]
  %rdx.shuf = shufflevector <16 x i32> %.lcssa, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx = add <16 x i32> %.lcssa, %rdx.shuf
  %rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
  %rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
  %rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
  %12 = extractelement <16 x i32> %bin.rdx4, i32 0
  ret i32 %12
}

; CHECK-NEXT:  .LBB11_1: # %vector.body
; CHECK-NEXT:  # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:  vmovdqu a+1024(%rax), %xmm1
; CHECK-NEXT:  vpsadbw b+1024(%rax), %xmm1, %xmm1
; CHECK-NEXT:  vpadd %zmm0, %zmm1, %zmm0
; CHECK-NEXT:  addq $4, %rax
; CHECK-NEXT:  jne .LBB11_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:  vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT:  vpadd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:  vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:  vpadd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:  vpadd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT:  vmovd %xmm0, %eax
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
entry:
  br label %vector.body

vector.body:
  %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
  %vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
  %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
  %1 = bitcast i8* %0 to <16 x i8>*
  %wide.load = load <16 x i8>, <16 x i8>* %1, align 4
  %2 = zext <16 x i8> %wide.load to <16 x i32>
  %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
  %4 = bitcast i8* %3 to <16 x i8>*
  %wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
  %5 = zext <16 x i8> %wide.load1 to <16 x i32>
  %6 = sub nsw <16 x i32> %2, %5
  %7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
  %8 = sub nsw <16 x i32> zeroinitializer, %6
  %9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
  %10 = add nsw <16 x i32> %9, %vec.phi
  %index.next = add i64 %index, 4
  %11 = icmp eq i64 %index.next, 1024
  br i1 %11, label %middle.block, label %vector.body

middle.block:
  %.lcssa = phi <16 x i32> [ %10, %vector.body ]
  %rdx.shuf = shufflevector <16 x i32> %.lcssa, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx = add <16 x i32> %.lcssa, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}
define void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f32_256:
; CHECK:    ; %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    kshiftrw $8, %k0, %k1
; CHECK-NEXT:    vpmovm2d %k1, %ymm0
; CHECK-NEXT:    vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT:    vpmovm2d %k0, %ymm1
; CHECK-NEXT:    vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT:    vmovaps %ymm1, (%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}
define void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK:    ; %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    vpmovm2d %k0, %zmm0
; CHECK-NEXT:    vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT:    vmovaps %zmm0, (%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
define void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f64_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT: vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT: vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT: vmovaps %ymm3, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f64_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm1
; CHECK-NEXT: vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT: vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT: vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f32_256:
; CHECK: # %bb.0:
define void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
    ; CHECK-LABEL: ubto16f32_512:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:    vpmovm2d %k0, %zmm0
    ; CHECK-NEXT:    vpsrld $31, %zmm0, %zmm0
    ; CHECK-NEXT:    vcvtdq2ps %zmm0, %ymm0
    ; CHECK-NEXT:    vcvtdq2ps %zmm0, %ymm0
    ; CHECK-NEXT:    vpmovaps %ymm1, (%rdi)
    ; CHECK-NEXT:    vzeroupper
    retq
    %mask = icmp slt <16 x i16> %a, zeroinitialize
    %l = uito fp <16 x i1> %mask to <16 x float>
    store <16 x float> %l, <16 x float>* %res
    ret void
}

define void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: ubto16f64_256:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vpmovw2m %ymm0, %k0
    ; CHECK-NEXT:    kshiftrw $8, %k0, %k1
    ; CHECK-NEXT:    vpmovm2d %k1, %ymm0
    ; CHECK-NEXT:    vpsrld $31, %ymm0, %ymm0
    ; CHECK-NEXT:    vcvtdq2ps %ymm0, %ymm0
    ; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm0
    ; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm0
    ; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm1
    ; CHECK-NEXT:    vpmovaps %zmm0, (%rdi)
    ; CHECK-NEXT:    vzeroupper
    retq
    %mask = icmp slt <16 x i16> %a, zeroinitialize
    %l = uito fp <16 x i1> %mask to <16 x float>
    store <16 x float> %l, <16 x float>* %res
    ret void
}

define void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {  
  ; CHECK-LABEL: ubto16f64_512:  
  ; CHECK:       # %bb.0:  
  ; CHECK-NEXT:   vpmovw2m %ymm0, %k0  
  ; CHECK-NEXT:   vpmovm2d %k0, %zmm0  
  ; CHECK-NEXT:   vpslld $31, %zmm0, %zmm0  
  ; CHECK-NEXT:   vcvtdq2pd %ymm0, %zmm1  
  ; CHECK-NEXT:   vextracti64x4 $1, %zmm0, %ymm0  
  ; CHECK-NEXT:   vcvtdq2pd %ymm0, %zmm0  
  ; CHECK-NEXT:   vmovaps %zmm0, 64(%rdi)  
  ; CHECK-NEXT:   vmovaps %zmm1, (%rdi)  
  ; CHECK-NEXT:   vzeroupper  
  ; CHECK-NEXT:   retq  
  %mask = icmp slt <16 x i16> %a, zeroinitializer  
  %1 = uitofp <16 x i1> %mask to <16 x double>  
  store <16 x double> %1, <16 x double>* %res  
  ret void  
}  

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {  
  ; CHECK-LABEL: test_16f32toub_256:  
  ; CHECK:       # %bb.0:  
  ; CHECK-NEXT:   vcvttps2dq (%rdi), %ymm1  
  ; CHECK-NEXT:   vpslld $31, %ymm1, %ymm1  
  ; CHECK-NEXT:   vpmovd2m %ymm1, %k0  
  ; CHECK-NEXT:   vcvttps2dq 32(%rdi), %ymm1  
  ; CHECK-NEXT:   vpslld $31, %ymm1, %ymm1  
  ; CHECK-NEXT:   vpmovd2m %ymm1, %k1  
  ; CHECK-NEXT:   kunpckbw %k0, %k1, %k1  
  ; CHECK-NEXT:   vmovdqqu %ymm0, %ymm0 {%k1} [z]  
  ; CHECK-NEXT:   retq  
  %a = load <16 x float>, <16 x float>* %ptr  
  %mask = fptoui <16 x float> %a to <16 x i1>  
  %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer  
}
ret <16 x i16> %select
}

define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {
; CHECK-LABEL: test_16f32toub_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT: vpslld $31, %zmm1, %zmm1
; CHECK-NEXT: vpmovd2m %zmm1, %k1
; CHECK-NEXT: vcmovq16 %ymm0, %ymm0 [%k1] {z}
; CHECK-NEXT: retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {
; CHECK-LABEL: test_16f32tosb_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT: vpmovd2m %ymm1, %k0
; CHECK-NEXT: vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT: vpmovd2m %ymm1, %k1
; CHECK-NEXT: kunpckbw %k0, %k1, %k1
; CHECK-NEXT: vcmovq16 %ymm0, %ymm0 [%k1] {z}
; CHECK-NEXT: retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {
; CHECK-LABEL: test_16f32tosb_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT: vpmovd2m %zmm1, %k1
; CHECK-NEXT: vcmovq16 %ymm0, %ymm0 [%k1] {z}
; CHECK-NEXT: retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}
define void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {
  ; CHECK-AVX512-LABEL: mul256:
  ; CHECK-AVX512:   # %bb.0:
  ; CHECK-AVX512-NEXT:    vmovdqa (%rdi), %ymm0
  ; CHECK-AVX512-NEXT:    vmovdqa 32(%rdi), %ymm1
  ; CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm4 = ymm3[8],ymm0[8],ymm3[9],ymm0[9],ymm3[10],ymm0[10],ymm3[11],ymm0[11],ymm3[12],ymm0[12],ymm3[13],ymm0[13],ymm3[14],ymm0[14],ymm3[15],ymm0[15],ymm3[24],ymm0[24],ymm3[25],ymm0[25],ymm3[26],ymm0[26],ymm3[27],ymm0[27],ymm3[28],ymm0[28],ymm3[29],ymm0[29],ymm3[30],ymm0[30],ymm3[31],ymm0[31]
  ; CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm5 = ymm1[8],ymm0[8],ymm1[9],ymm0[9],ymm1[10],ymm0[10],ymm1[11],ymm0[11],ymm1[12],ymm0[12],ymm1[13],ymm0[13],ymm1[14],ymm0[14],ymm1[15],ymm0[15],ymm1[24],ymm0[24],ymm1[25],ymm0[25],ymm1[26],ymm0[26],ymm1[27],ymm0[27],ymm1[28],ymm0[28],ymm1[29],ymm0[29],ymm1[30],ymm0[30],ymm1[31],ymm0[31]
  ; CHECK-AVX512-NEXT:    vpmullw %ymm4, %ymm5, %ymm4
  ; CHECK-AVX512-NEXT:    vpand %ymm4, %ymm4
  ; CHECK-AVX512-NEXT:    vpunpcklbw {{.*#+}} ymm3 = ymm3[0],ymm0[0],ymm3[1],ymm0[1],ymm3[2],ymm0[2],ymm3[3],ymm0[3],ymm3[4],ymm0[4],ymm3[5],ymm0[5],ymm3[6],ymm0[6],ymm3[7],ymm0[7],ymm3[16],ymm0[16],ymm3[17],ymm0[17],ymm3[18],ymm0[18],ymm3[19],ymm0[19],ymm3[20],ymm0[20],ymm3[21],ymm0[21],ymm3[22],ymm0[22],ymm3[23],ymm0[23]
  ; CHECK-AVX512-NEXT:    vpunpcklbw {{.*#+}} ymm1 = ymm1[0],ymm0[0],ymm1[1],ymm0[1],ymm1[2],ymm0[2],ymm1[3],ymm0[3],ymm1[4],ymm0[4],ymm1[5],ymm0[5],ymm1[6],ymm0[6],ymm1[7],ymm0[7],ymm1[16],ymm0[16],ymm1[17],ymm0[17],ymm1[18],ymm0[18],ymm1[19],ymm0[19],ymm1[20],ymm0[20],ymm1[21],ymm0[21],ymm1[22],ymm0[22],ymm1[23],ymm0[23]
  ; CHECK-AVX512-NEXT:    vpmullw %ymm3, %ymm1, %ymm1
  ; CHECK-AVX512-NEXT:    vpand %ymm5, %ymm1, %ymm1
  ; CHECK-AVX512-NEXT:    vpckuswb %ymm4, %ymm1, %ymm1
  ; CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm3 = ymm2[2],ymm0[2],ymm2[9],ymm0[9],ymm2[10],ymm0[10],ymm2[11],ymm0[11],ymm2[12],ymm0[12],ymm2[13],ymm0[13],ymm2[14],ymm0[14],ymm2[15],ymm0[15],ymm2[24],ymm0[24],ymm2[25],ymm0[25],ymm2[26],ymm0[26],ymm2[27],ymm0[27],ymm2[28],ymm0[28],ymm2[29],ymm0[29],ymm2[30],ymm0[30],ymm2[31],ymm0[31]
  ; CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm4 = ymm0[8,9,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
  ; CHECK-AVX512-NEXT:    vpand %ymm5, %ymm3, %ymm3
  ; CHECK-AVX512-NEXT:    vpand %ymm5, %ymm3, %ymm3
  ; CHECK-AVX512-NEXT:    vpunpcklbw {{.*#+}} ymm2 = ymm2[2],ymm0[2],ymm2[1],ymm0[1],ymm2[2],ymm0[2],ymm2[3],ymm0[3],ymm2[4],ymm0[4],ymm2[5],ymm0[5],ymm2[6],ymm0[6],ymm2[7],ymm0[7],ymm2[16],ymm0[16],ymm2[17],ymm0[17],ymm2[18],ymm0[18],ymm2[19],ymm0[19],ymm2[20],ymm0[20],ymm2[21],ymm0[21],ymm2[22],ymm0[22],ymm2[23],ymm0[23]
  ; CHECK-AVX512-NEXT:    vpunpcklbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,7,7,16,16,17,17,18,18,19,19,19,20,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT:  vpmullw %ymm2, %ymm0, %ymm0
; CHECK-AVX512-NEXT:  vpand %ymm5, %ymm0, %ymm0
; CHECK-AVX512-NEXT:  vpackuswb %ymm3, %ymm0, %ymm0
; CHECK-AVX512-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-AVX512-NEXT:  vmovdqa %ymm1, 32(%rdx)
; CHECK-AVX512-NEXT:  vzeroupper
; CHECK-AVX512-NEXT:  retq
;
; CHECK-VBMI-LABEL:  mul256:
; CHECK-VBMI:       # %bb.0:
; CHECK-VBMI-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-VBMI-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-VBMI-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-VBMI-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm4 =
ymm3[8],ymm0[8],ymm3[9],ymm0[9],ymm3[10],ymm0[10],ymm3[11],ymm0[11],ymm3[12],ymm0[12],ymm3[13 ],ymm0[13],ymm3[14],ymm0[14],ymm3[15],ymm0[15],ymm3[24],ymm0[24],ymm3[25],ymm0[25],ymm3[26],ymm0[26],ymm3[27],ymm0[27],ymm3[28],ymm0[28],ymm3[29],ymm0[29],ymm3[30],ymm0[30],ymm3[31],ymm0[ 31 ]
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm5 =
ymm1[8],ymm0[8],ymm1[9],ymm0[9],ymm1[10],ymm0[10],ymm1[11],ymm0[11],ymm1[12],ymm0[12],ymm1[13 ],ymm0[13],ymm1[14],ymm0[14],ymm1[15],ymm0[15],ymm1[24],ymm0[24],ymm1[25],ymm0[25],ymm1[26],ymm0[26],ymm1[27],ymm0[27],ymm1[28],ymm0[28],ymm1[29],ymm0[29],ymm1[30],ymm0[30],ymm1[31],ymm0[ 31 ]
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm3 =
ymm3[0],ymm0[0],ymm3[1],ymm0[1],ymm3[2],ymm0[2],ymm3[3],ymm0[3],ymm3[4],ymm0[4],ymm3[5],ymm0[ 5],ymm3[6],ymm0[6],ymm3[7],ymm0[7],ymm3[16],ymm0[16],ymm3[17],ymm0[17],ymm3[18],ymm0[18],ymm3[ 19],ymm0[19],ymm3[20],ymm0[20],ymm3[21],ymm0[21],ymm3[22],ymm0[22],ymm3[23],ymm0[23]
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm1 =
ymm1[0],ymm0[0],ymm1[1],ymm0[1],ymm1[2],ymm0[2],ymm1[3],ymm0[3],ymm1[4],ymm0[4],ymm1[5],ymm0[ 5],ymm1[6],ymm0[6],ymm1[7],ymm0[7],ymm1[16],ymm0[16],ymm1[17],ymm0[17],ymm1[18],ymm0[18],ymm1[ 19],ymm0[19],ymm1[20],ymm0[20],ymm1[21],ymm0[21],ymm1[22],ymm0[22],ymm1[23],ymm0[23]
; CHECK-VBMI-NEXT:  vpuinvpckhbw {{.*#+}} ymm3 =
[0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38,40,42,44,46,48,50,52,54,56,58,60,62]
; CHECK-VBMI-NEXT:  vperm2b %ymm3, %ymm4, %ymm3, %ymm1
; CHECK-VBMI-NEXT:  vpuinvpckhbw {{.*#+}} ymm4 =
ymm2[8],ymm0[8],ymm2[9],ymm0[9],ymm2[10],ymm0[10],ymm2[11],ymm0[11],ymm2[12],ymm0[12],ymm2[13 ],ymm0[13],ymm2[14],ymm0[14],ymm2[15],ymm0[15],ymm2[24],ymm0[24],ymm2[25],ymm0[25],ymm2[26],ymm0[26],ymm2[27],ymm0[27],ymm2[28],ymm0[28],ymm2[29],ymm0[29],ymm2[30],ymm0[30],ymm2[31],ymm0[ 31 ]
; CHECK-VBMI-NEXT:  vpuinvpckhbw {{.*#+}} ymm5 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT:  vpuinvpckhbw {{.*#+}} ymm4 =
ymm2[0],ymm0[0],ymm2[1],ymm0[1],ymm2[2],ymm0[2],ymm2[3],ymm0[3],ymm2[4],ymm0[4],ymm2[5],ymm0[ 5],ymm2[6],ymm0[6],ymm2[7],ymm0[7],ymm2[16],ymm0[16],ymm2[17],ymm0[17],ymm2[18],ymm0[18],ymm2[ 18]
define void @mul512(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="512" { ; CHECK-AVX512-LABEL: mul512: ; CHECK-AVX512:   # %bb.0: ; CHECK-AVX512-NEXT:   vmovdqa64 (%rdi), %zmm0 ; CHECK-AVX512-NEXT:   vmovdqa64 (%rsi), %zmm1 ; CHECK-AVX512-NEXT:   vpmulhw {{.*#+}} %zmm2, %zmm0, %zmm0 ; CHECK-AVX512-NEXT:   vpmullw %zmm2, %zmm3, %zmm3 ; CHECK-AVX512-NEXT:   vzeroupper ; CHECK-AVX512-NEXT:   retq
%
%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void
}

19],ymm0[19],ymm2[20],ymm0[20],ymm2[21],ymm0[21],ymm2[22],ymm0[22],ymm2[23],ymm0[23]
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,32,32,33,33,34,34,35,35,36,36,37,37,38,38,39,39,40,40,41,41,42,42,43,43,44,44,45,45,46,46,47,47,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0 ; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0 ; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0 ; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0 ; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0 ; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0 ; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0 ; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0 ; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0 ; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0 ; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0 ; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0 ; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0 ; CHECK-VBI

; CHECK-AVX512-NEXT: vpandq %zmm3, %zmm0, %zmm0
; CHECK-AVX512-NEXT: vpackuswb %zmm2, %zmm0, %zmm0
; CHECK-AVX512-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-AVX512-NEXT: vzeroupper
; CHECK-AVX512-NEXT: retq
;
; CHECK-VBMI-LABEL: mul512:
; CHECK-VBMI:     # %bb:
; CHECK-VBMI-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-VBMI-NEXT: vmovdqa64 (%rsi), %zmm1
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} zmm2 =
    zmm1[8],zmm0[8],zmm1[9],zmm0[9],zmm1[10],zmm0[10],zmm1[11],zmm0[11],zmm1[12],zmm0[12],zmm1[13],
    zmm0[13],zmm1[14],zmm0[14],zmm1[15],zmm0[15],zmm1[24],zmm0[24],zmm1[25],zmm0[25],zmm1[26],zmm0[26],
    zmm1[27],zmm0[27],zmm1[28],zmm0[28],zmm1[29],zmm0[29],zmm1[30],zmm0[30],zmm1[31],zmm0[31],
    zmm1[40],zmm0[40],zmm1[41],zmm0[41],zmm1[42],zmm0[42],zmm1[43],zmm0[43],zmm1[44],zmm0[44],
    zmm1[45],zmm0[45],zmm1[46],zmm0[46],zmm1[47],zmm0[47],zmm1[56],zmm0[56],zmm1[57],zmm0[57],zmm1[58],zmm0[58],zmm1[59],zmm0[59],zmm1[60],zmm0[60],zmm1[61],zmm0[61],zmm1[62],zmm0[62],zmm1[63],zmm0[63]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} zmm3 =
    zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
    2,42,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT: vpmullw %zmm2, %zmm3, %zmm2
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} zmm1 =
    zmm0[0],zmm1[0],zmm0[1],zmm1[1],zmm0[2],zmm1[2],zmm0[3],zmm1[3],zmm0[4],zmm1[4],zmm0[5],
    zmm1[5],zmm0[6],zmm1[6],zmm0[7],zmm1[7],zmm0[16],zmm1[16],zmm0[17],zmm1[17],zmm0[18],zmm1[18],
    zmm0[19],zmm1[19],zmm0[20],zmm1[20],zmm0[21],zmm1[21],zmm0[22],zmm1[22],zmm0[23],zmm1[23],
    zmm0[32],zmm1[32],zmm0[33],zmm1[33],zmm0[34],zmm1[34],zmm0[35],zmm1[35],zmm0[36],zmm1[36],
    zmm0[37],zmm1[37],zmm0[38],zmm1[38],zmm0[39],zmm1[39],zmm0[48],zmm1[48],zmm0[49],zmm1[49],
    zmm0[50],zmm1[50],zmm0[51],zmm1[51],zmm0[52],zmm1[52],zmm0[53],zmm1[53],zmm0[54],zmm1[54],
    zmm0[55],zmm1[55]
; CHECK-VBMI-NEXT: vmovdqa64 {{.*#+}} zmm0 =
    zmm0[0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
    6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-VBMI-NEXT: vmovdqa64 {{.*#+}} zmm1 =
    [0,2,4,6,8,10,12,14,64,66,68,70,72,74,76,78,16,18,20,22,24,26,28,30,80,82,84,86,88,90,92,94,32,34,36,38,40,42,44,
; CHECK-VBMI-NEXT: vpermi2b %zmm2, %zmm0, %zmm1
; CHECK-VBMI-NEXT: vmovdqa64 %[zmm1], (%rdx)
; CHECK-VBMI-NEXT: vzeroupper
; CHECK-VBMI-NEXT: retq
;
%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void
;
; This threw an assertion at one point.
define <4 x i32> @mload_v4i32(<4 x i32> %trigger, <4 x i32>* %addr, <4 x i32> %dst) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: mload_v4i32:
    ; CHECK:    # %bb.0:
    ; CHECK-NEXT: vptestnmd %xmm0, %xmm0, %k1
    ; CHECK-NEXT: vpblendmd (%rdi), %xmm1, %xmm0 {%k1}
    ; CHECK-NEXT: retq
    %mask = icmp eq <4 x i32> %trigger, zeroinitializer
    %res = call <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* %addr, i32 4, <4 x i1> %mask, <4 x i32> %dst)
    ret <4 x i32> %res
}

define <16 x i32> @trunc_v16i64_v16i32(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v16i64_v16i32:
    ; CHECK:    # %bb.0:
    ; CHECK-NEXT: vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
    ; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
    ; CHECK-NEXT: vmovdqa 96(%rdi), %ymm3
    ; CHECK-NEXT: vpmovqd %ymm0, %xmm0
    ; CHECK-NEXT: vpmovqd %ymm1, %xmm1
    ; CHECK-NEXT: vinserti128 $1, %ymm1, %ymm0, %ymm0
    ; CHECK-NEXT: vpmovqd %ymm2, %xmm2
    ; CHECK-NEXT: vpmovqd %ymm3, %xmm3
    ; CHECK-NEXT: vinserti128 $1, %ymm2, %ymm1, %ymm1
    ; CHECK-NEXT: retq
    %a = load <16 x i64>, <16 x i64>* %x
    %b = trunc <16 x i64> %a to <16 x i32>
    ret <16 x i32> %b
}

define <16 x i8> @trunc_v16i64_v16i8(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v16i64_v16i8:
    ; CHECK:    # %bb.0:
    ; CHECK-NEXT: vmovdqa (%rdi), %ymm0
    ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
    ; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
    ; CHECK-NEXT: vmovdqa 96(%rdi), %ymm3
    ; CHECK-NEXT: vpmovqd %ymm0, %xmm0
    ; CHECK-NEXT: vpmovqd %ymm1, %xmm1
    ; CHECK-NEXT: vpmovqd %ymm2, %xmm2
    ; CHECK-NEXT: vpmovqd %ymm3, %xmm3
    ; CHECK-NEXT: vpunpcklqd {{.*#+}} xmm2 = xmm2[0],xmm3[0],xmm2[1],xmm3[1]
    ; CHECK-NEXT: vzeroupper
define <8 x i32> @trunc_v8i64_v8i32_zeroes(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v8i64_v8i32_zeroes:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vpsrlq $48, 32(%rdi), %ymm1
    ; CHECK-NEXT:  vpsrlq $48, (%rdi), %ymm2
    ; CHECK-NEXT:  vmovdqa {{.*#+}} ymm0 = [0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30]
    ; CHECK-NEXT:  vpermi2w %ymm1, %ymm2, %ymm0
    ; CHECK-NEXT:  retq
    %a = load <8 x i64>, <8 x i64>* %x
    %b = lshr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>
    %c = trunc <8 x i64> %b to <8 x i32>
    ret <8 x i32> %c
}

define <16 x i16> @trunc_v16i32_v16i16_zeroes(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: trunc_v16i32_v16i16_zeroes:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:  vmovdqa (%rdi), %ymm1
    ; CHECK-NEXT:  vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]
    ; CHECK-NEXT:  vpermi2w 32(%rdi), %ymm1, %ymm0
    ; CHECK-NEXT:  retq
    %a = load <16 x i32>, <16 x i32>* %x
    %b = lshr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16>
    %c = trunc <16 x i32> %b to <16 x i16>
    ret <16 x i16> %c
}

define <32 x i8> @trunc_v32i16_v32i8_zeroes(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
    ; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_zeroes:
    ; CHECK-AVX512:       # %bb.0:
    ; CHECK-AVX512-NEXT:  vpsrlw $8, 32(%rdi), %ymm0
    ; CHECK-AVX512-NEXT:  vpsrlw $8, (%rdi), %ymm1
    ; CHECK-AVX512-NEXT:  vpackuswb %ymm0, %ymm1, %ymm0
    ; CHECK-AVX512-NEXT:  vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
    ; CHECK-AVX512-NEXT:  retq
    ;
    ; CHECK-VBMI-LABEL: trunc_v32i16_v32i8_zeroes:
    ; CHECK-VBMI:       # %bb.0:
    ; CHECK-VBMI-NEXT:  vmovdqa (%rdi), %ymm1
    ; CHECK-VBMI-NEXT:  vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63]
    ; CHECK-VBMI-NEXT:  vpermi2b 32(%rdi), %ymm1, %ymm0
    ; CHECK-VBMI-NEXT:  retq
    %a = load <32 x i16>, <32 x i16>* %x

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ret <8 x i16> %b
}
%b = lshr <32 x i16> %a, <i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8>
%c = trunc <32 x i16> %b to <32 x i8>
ret <32 x i8> %c
}
define <8 x i32> @trunc_v8i64_v8i32_sign(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i32_sign:
; CHECK: # %bb.0:
; CHECK-NEXT: vpsraq $48, 32(%rdi), %ymm1
; CHECK-NEXT: vpsraq $48, (%rdi), %ymm2
; CHECK-NEXT: vmovdqa {{.*#+}} ymm0 = [0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30]
; CHECK-NEXT: vpermi2w %ymm1, %ymm2, %ymm0
; CHECK-NEXT: retq
%a = load <8 x i64>, <8 x i64>* %x
%b = ashr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>
%c = trunc <8 x i64> %b to <8 x i32>
ret <8 x i32> %c
}
define <16 x i16> @trunc_v16i32_v16i16_sign(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i16_sign:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-NEXT: vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]
; CHECK-NEXT: vpermi2w 32(%rdi), %ymm1, %ymm0
; CHECK-NEXT: retq
%a = load <16 x i32>, <16 x i32>* %x
%b = ashr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16>
%c = trunc <16 x i32> %b to <16 x i16>
ret <16 x i16> %c
}
define <32 x i8> @trunc_v32i16_v32i8_sign(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_sign:
; CHECK-AVX512: # %bb.0:
; CHECK-AVX512-NEXT: vpsraw $8, 32(%rdi), %ymm0
; CHECK-AVX512-NEXT: vpsraw $8, (%rdi), %ymm1
; CHECK-AVX512-NEXT: vpacksswb %ymm0, %ymm1, %ymm0
; CHECK-AVX512-NEXT: vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-AVX512-NEXT: retq
; CHECK-VBMI-LABEL: trunc_v32i16_v32i8_sign:
; CHECK-VBMI: # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-VBMI-NEXT: vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63]
; CHECK-VBMI-NEXT: vpermi2b 32(%rdi), %ymm1, %ymm0  
; CHECK-VBMI-NEXT: retq  
%a = load <32 x i16>, <32 x i16>* %x  
%b = ashr <32 x i16> %a, <i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8>  
%c = trunc <32 x i16> %b to <32 x i8>  
ret <32 x i8> %c  
}  

define void @zext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {  
; CHECK-LABEL: zext_v16i8_v16i64:  
; CHECK: # %bb.0:  
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm1 =  
  xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,  
  xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero  
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm2 =  
  xmm2[0],zero,zero,zero,xmm2[1],zero,zero,zero,xmm2[2],zero,zero,zero,xmm2[3],zero,zero,zero  
; CHECK-NEXT: vextracti128 $1, %ymm1, %xmm1  
; CHECK-NEXT: vpshufd {{.*#+}} xmm3 = xmm1[2,3,0,1]  
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm3 =  
  xmm3[0],zero,zero,zero,xmm3[1],zero,zero,zero,xmm3[2],zero,zero,zero,xmm3[3],zero,zero,zero  
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm1 =  
  xmm1[0],zero,zero,zero,xmm1[1],zero,zero,zero,xmm1[2],zero,zero,zero,xmm1[3],zero,zero,zero  
; CHECK-NEXT: vpmovzxbq {{.*#+}} ymm0 =  
  xmm0[0],zero,zero,zero,xmm0[1],zero,zero,zero,xmm0[2],zero,zero,zero,xmm0[3],zero,zero,zero  
; CHECK-NEXT: vmovdqa %ymm0, (%rdi)  
; CHECK-NEXT: vmovdqa %ymm1, 64(%rdi)  
; CHECK-NEXT: vmovdqa %ymm3, 96(%rdi)  
; CHECK-NEXT: vzeroupper  
; CHECK-NEXT: retq  
%a = zext <16 x i8> %x to <16 x i64>  
store <16 x i64> %a, <16 x i64>* %y  
ret void  
}  

define void @sext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {  
; CHECK-LABEL: sext_v16i8_v16i64:  
; CHECK: # %bb.0:  
; CHECK-NEXT: vpmovsxbw {{.*#+}} ymm1 =  
  xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,  
  xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero  
; CHECK-NEXT: vpshufd {{.*#+}} xmm2 = xmm1[2,3,0,1]  
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm2 =  
  xmm2[0],zero,zero,zero,xmm2[1],zero,zero,zero,xmm2[2],zero,zero,zero,xmm2[3],zero,zero,zero  
; CHECK-NEXT: vextracti128 $1, %ymm1, %xmm1  
; CHECK-NEXT: vpshufd {{.*#+}} xmm3 = xmm1[2,3,0,1]  
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm3 =  
  xmm3[0],zero,zero,zero,xmm3[1],zero,zero,zero,xmm3[2],zero,zero,zero,xmm3[3],zero,zero,zero  
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm1 =  
  xmm1[0],zero,zero,zero,xmm1[1],zero,zero,zero,xmm1[2],zero,zero,zero,xmm1[3],zero,zero,zero  
; CHECK-NEXT: vpmovzxbq {{.*#+}} ymm0 =  
  xmm0[0],zero,zero,zero,xmm0[1],zero,zero,zero,xmm0[2],zero,zero,zero,xmm0[3],zero,zero,zero  
; CHECK-NEXT: vmovdqa %ymm0, (%rdi)  
; CHECK-NEXT: vmovdqa %ymm1, 64(%rdi)  
; CHECK-NEXT: vmovdqa %ymm3, 96(%rdi)  
; CHECK-NEXT: vzeroupper  
; CHECK-NEXT: retq  
%a = zext <16 x i8> %x to <16 x i64>  
store <16 x i64> %a, <16 x i64>* %y  
ret void  
}
define void @vselect_split_v8i16_setcc(<8 x i16> %s, <8 x i16> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: vselect_split_v8i16_setcc:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:   vmovdqa (%rsi), %ymm2
    ; CHECK-NEXT:   vmovdqa 32(%rsi), %ymm3
    ; CHECK-NEXT:   vpcmpeqw %xmm1, %xmm0, %k1
    ; CHECK-NEXT:   kshiftrb $4, %k1, %k2
    ; CHECK-NEXT:   vmovdqa64 32(%rdi), %ymm3 {%k2}
    ; CHECK-NEXT:   vmovdqa64 (%rdi), %ymm2 {%k1}
    ; CHECK-NEXT:   vmovdqa %ymm2, (%rdx)
    ; CHECK-NEXT:   vmovdqa %ymm3, 32(%rdx)
    ; CHECK-NEXT:   vzeroupper
    ; CHECK-NEXT:   retq
    %a = load <8 x i64>, <8 x i64>* %p
    %y = load <8 x i64>, <8 x i64>* %q
    %b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
    store <8 x i64> %b, <8 x i64>* %r
    ret void
}

define void @vselect_split_v8i32_setcc(<8 x i32> %s, <8 x i32> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: vselect_split_v8i32_setcc:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:   vmovdqa (%rsi), %ymm2
    ; CHECK-NEXT:   vmovdqa 32(%rsi), %ymm3
    ; CHECK-NEXT:   vpcmpeqd %ymm1, %ymm0, %k1
    ; CHECK-NEXT:   kshiftrb $4, %k1, %k2
    ; CHECK-NEXT:   vmovdqa64 32(%rdi), %ymm3 {%k2}
    ; CHECK-NEXT:   vmovdqa64 (%rdi), %ymm2 {%k1}
    ; CHECK-NEXT:   vmovdqa %ymm2, (%rdx)
    ; CHECK-NEXT:   vmovdqa %ymm3, 32(%rdx)
    ; CHECK-NEXT:   vzeroupper
    ; CHECK-NEXT:   retq
    %a = load <8 x i64>, <8 x i64>* %p
    %y = load <8 x i64>, <8 x i64>* %q
    %b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
    store <8 x i64> %b, <8 x i64>* %r
    ret void
}
define void @vselect_split_v16i8_setcc(<16 x i8> %s, <16 x i8> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: vselect_split_v16i8_setcc:
    ; CHECK:       # %bb.0:
    ; CHECK-NEXT:    vmovdqa (%rsi), %ymm2
    ; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm3
    ; CHECK-NEXT:    vpcmpeqb %ymm1, %ymm0, %k1
    ; CHECK-NEXT:    kshiftrw $8, %k1, %k2
    ; CHECK-NEXT:    vmovdqa32 32(%rdi), %ymm3 {%k2}
    ; CHECK-NEXT:    vmovdqa32 (%rdi), %ymm2 {%k1}
    ; CHECK-NEXT:    vmovdqa %ymm2, (%rdx)
    ; CHECK-NEXT:    vmovdqa %ymm3, 32(%rdx)
    ; CHECK-NEXT:    vzeroupper
    ; CHECK-NEXT:    retq
    %x = load <16 x i32>, <16 x i32>* %p
    %y = load <16 x i32>, <16 x i32>* %q
    %a = icmp eq <16 x i8> %s, %t
    %b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
    store <16 x i32> %b, <16 x i32>* %r
    ret void
}
define <16 x i8> @trunc_packus_v16i32_v16i8(<16 x i32>* %p) "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_packus_v16i32_v16i8:
; CHECK:    # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vpackusdw 32(%rdi), %ymm0, %ymm0
; CHECK-NEXT:    vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT:    vpmovuswb %ymm0, %xmm0
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
    %a = load <16 x i32>, <16 x i32>* %p
    %b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
    %c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
    %d = icmp sgt <16 x i32> %c, zeroinitializer
    %e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zeroinitializer
    %f = trunc <16 x i32> %e to <16 x i8>
    ret <16 x i8> %f
}
define void @v64i1_shuffle(<64 x i8>* %x, <64 x i8>* %y) "min-legal-vector-width"="256" {
    ; CHECK-LABEL: v64i1_shuffle:
    ; CHECK:       # %bb.0: # %entry
    ; CHECK-NEXT:    vmovdqa (%rdi), %ymm1
    ; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm0
    ; CHECK-NEXT:    vptestnmb %ymm1, %ymm1, %k0
    ; CHECK-NEXT:    kshiftr $1, %k0, %k1
    ; CHECK-NEXT:    movq $-3, %rax
    ; CHECK-NEXT:    kmovq %rax, %k2
    ; CHECK-NEXT:    kandq %k2, %k1, %k1
    ; CHECK-NEXT:    kshiftl $63, %k0, %k2
    ; CHECK-NEXT:    kshiftrq $62, %k2, %k2
    ; CHECK-NEXT:    korq %k2, %k1, %k1
    ; CHECK-NEXT:    movq $-5, %rax
    ; CHECK-NEXT:    kmovq %rax, %k2
    ; CHECK-NEXT:    kandq %k2, %k1, %k1
    ; CHECK-NEXT:    kshiftl $63, %k2, %k2
    ; CHECK-NEXT:    kshiftrq $61, %k2, %k2
    ; CHECK-NEXT:    korq %k2, %k1, %k1
    ; CHECK-NEXT:    movq $-9, %rax
    ; CHECK-NEXT:    kmovq %rax, %k2
    ; CHECK-NEXT:    kandq %k2, %k1, %k1
    ; CHECK-NEXT:    kshiftl $63, %k2, %k2
    ; CHECK-NEXT:    kshiftrq $60, %k2, %k2
    ; CHECK-NEXT:    korq %k2, %k1, %k1
    ; CHECK-NEXT:    movq $-17, %rax
    ; CHECK-NEXT:    kmovq %rax, %k2
    ; CHECK-NEXT:    kandq %k2, %k1, %k1
    ; CHECK-NEXT:    kshiftl $63, %k2, %k2
    ; CHECK-NEXT:    kshiftrq $59, %k2, %k2
    ; CHECK-NEXT:    korq %k2, %k1, %k1
    ; CHECK-NEXT:    movq $-33, %rax
    ; CHECK-NEXT:    kmovq %rax, %k2
    ; CHECK-NEXT:    kandq %k2, %k1, %k1
    ; CHECK-NEXT:    kshiftl $63, %k2, %k2
    ; CHECK-NEXT:    kshiftrq $58, %k2, %k2
    ; CHECK-NEXT:    korq %k2, %k1, %k1
    ; CHECK-NEXT:    movq $-65, %rax
}
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftd $7, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftq $57, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-129, %rax
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftd $6, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftq $56, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-257, %rax # imm = 0xFEFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftd $9, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftq $55, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-513, %rax # imm = 0xFDFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftd $8, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftq $54, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-1025, %rax # imm = 0xFBFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftd $11, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftq $53, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-2049, %rax # imm = 0xF7FF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftd $10, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftq $52, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-4097, %rax # imm = 0xEFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftd $13, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftq $51, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:      movq $-8193, %rax # imm = 0xDFFF
; CHECK-NEXT:      kmovq %rax, %k2
; CHECK-NEXT:      kandq %k2, %k1, %k1
; CHECK-NEXT:      kshiftrd $12, %k0, %k2
; CHECK-NEXT:      kshiftlq $63, %k2, %k2
; CHECK-NEXT:      kshiftrq $50, %k2, %k2
; CHECK-NEXT:      korq %k2, %k1, %k1
; CHECK-NEXT:      movq $-16385, %rax # imm = 0xBFFF
; CHECK-NEXT:      kmovq %rax, %k2
; CHECK-NEXT:      kandq %k2, %k1, %k1
; CHECK-NEXT:      kshiftrd $15, %k0, %k2
; CHECK-NEXT:      kshiftlq $63, %k2, %k2
; CHECK-NEXT:      kshiftrq $49, %k2, %k2
; CHECK-NEXT:      korq %k2, %k1, %k1
; CHECK-NEXT:      movq $-32769, %rax # imm = 0xFFFF7FFF
; CHECK-NEXT:      kmovq %rax, %k2
; CHECK-NEXT:      kandq %k2, %k1, %k1
; CHECK-NEXT:      kshiftrd $14, %k0, %k2
; CHECK-NEXT:      kshiftlq $63, %k2, %k2
; CHECK-NEXT:      kshiftrq $48, %k2, %k2
; CHECK-NEXT:      korq %k2, %k1, %k1
; CHECK-NEXT:      movq $-65537, %rax # imm = 0xFFFEFFFF
; CHECK-NEXT:      kmovq %rax, %k2
; CHECK-NEXT:      kandq %k2, %k1, %k1
; CHECK-NEXT:      kshiftrd $17, %k0, %k2
; CHECK-NEXT:      kshiftlq $63, %k2, %k2
; CHECK-NEXT:      kshiftrq $47, %k2, %k2
; CHECK-NEXT:      korq %k2, %k1, %k1
; CHECK-NEXT:      movq $-131073, %rax # imm = 0xFFF7FFFF
; CHECK-NEXT:      kmovq %rax, %k2
; CHECK-NEXT:      kandq %k2, %k1, %k1
; CHECK-NEXT:      kshiftrd $18, %k0, %k2
; CHECK-NEXT:      kshiftlq $63, %k2, %k2
; CHECK-NEXT:      kshiftrq $46, %k2, %k2
; CHECK-NEXT:      korq %k2, %k1, %k1
; CHECK-NEXT:      movq $-262145, %rax # imm = 0xFFFBF7FFFF
; CHECK-NEXT:      kmovq %rax, %k2
; CHECK-NEXT:      kandq %k2, %k1, %k1
; CHECK-NEXT:      kshiftrd $19, %k0, %k2
; CHECK-NEXT:      kshiftlq $63, %k2, %k2
; CHECK-NEXT:      kshiftrq $45, %k2, %k2
; CHECK-NEXT:      korq %k2, %k1, %k1
; CHECK-NEXT:      movq $-524289, %rax # imm = 0xFFF7FFFF
; CHECK-NEXT:      kmovq %rax, %k2
; CHECK-NEXT:      kandq %k2, %k1, %k1
; CHECK-NEXT:      kshiftrd $18, %k0, %k2
; CHECK-NEXT:      kshiftlq $63, %k2, %k2
; CHECK-NEXT:      kshiftrq $44, %k2, %k2
; CHECK-NEXT:    kshiftrq $43, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-2097153, %rax # imm = 0xFFDFFFFF
; CHECK-NEXT:    kshiftrq $42, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-4194305, %rax # imm = 0xFFBFFFFF
; CHECK-NEXT:    kshiftrq $41, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-8388609, %rax # imm = 0xFF7FFFFF
; CHECK-NEXT:    kshiftrq $40, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-16777217, %rax # imm = 0xFEFFFFFF
; CHECK-NEXT:    kshiftrq $39, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-33554433, %rax # imm = 0xFDFFFFFF
; CHECK-NEXT:    kshiftrq $38, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-67108865, %rax # imm = 0xFBFFFFFF
; CHECK-NEXT:    kshiftrq $37, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-134217729, %rax # imm = 0xF7FFFFFF
; CHECK-NEXT:    kshiftrq $36, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-268435457, %rax # imm = 0xF3FFFFFF
; CHECK-NEXT:    kshiftlq $45, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-536870917, %rax # imm = 0xF1FFFFFF
; CHECK-NEXT:    kshiftlq $44, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-1073741825, %rax # imm = 0xF0800000
; CHECK-NEXT:    kshiftlq $43, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-2147483649, %rax # imm = 0xEFFFFFFF
; CHECK-NEXT:    kshiftlq $42, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-4294967297, %rax # imm = 0xE8000000
; CHECK-NEXT:    kshiftlq $41, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-8589934608, %rax # imm = 0xE0000000
; CHECK-NEXT:    kshiftlq $40, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-17179869184, %rax # imm = 0xE0000000
; CHECK-NEXT:    kshiftlq $39, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-34359738368, %rax # imm = 0xE0000000
; CHECK-NEXT:    kshiftlq $38, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-68719476736, %rax # imm = 0xE0000000
; CHECK-NEXT:    kshiftlq $37, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-137438953472, %rax # imm = 0xE0000000
; CHECK-NEXT:    kshiftlq $36, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-274877906944, %rax # imm = 0xE0000000
; CHECK-NEXT:    kshiftlq $35, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-549755813888, %rax # imm = 0xE0000000
; CHECK-NEXT:    kshiftlq $34, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-1099511627776, %rax # imm = 0xE0000000
; CHECK-NEXT:    kshiftlq $33, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-2199023255552, %rax # imm = 0xE0000000
; CHECK-NEXT:    kshiftlq $32, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-4398046511104, %rax # imm = 0xE0000000
; CHECK-NEXT:    kshiftlq $31, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $.-8796093022208, %rax # imm = 0xE0000000
; CHECK-NEXT:  kshiftrq $37, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-134217729, %rax # imm = 0xF7FFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $26, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $36, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-268435457, %rax # imm = 0xEFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $29, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $35, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-536870913, %rax # imm = 0xDFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $28, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $34, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-1073741825, %rax # imm = 0xBFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $31, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $33, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movabsq $-2147483649, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k2
; CHECK-NEXT:  vptestnmb %ymm0, %ymm0, %k1
; CHECK-NEXT:  kshiftrd $30, %k0, %k0
; CHECK-NEXT:  kshiftlq $63, %k0, %k0
; CHECK-NEXT:  kshiftrq $32, %k0, %k0
; CHECK-NEXT:  korq %k0, %k2, %k0
; CHECK-NEXT:  movabsq $-4294967297, %rax # imm = 0xFFFFFFFFFEFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $1, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $31, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-8589934593, %rax # imm = 0xFFFFFFFFFFFFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $37, %k2, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $36, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
 ; CHECK-NEXT: kandq %k2, %k0, %k0
 ; CHECK-NEXT: kshiftrd $14, %k1, %k2
 ; CHECK-NEXT: kshiftlq $63, %k2, %k2
 ; CHECK-NEXT: kshiftrq $16, %k2, %k2
 ; CHECK-NEXT: korq %k2, %k0, %k0
 ; CHECK-NEXT: movabsq $-281474976710657, %rax # imm = 0xFFEFFFFFFFFFFFF
 ; CHECK-NEXT: kmovq %rax, %k2
 ; CHECK-NEXT: kandq %k2, %k0, %k0
 ; CHECK-NEXT: kshiftrd $17, %k1, %k2
 ; CHECK-NEXT: kshiftlq $63, %k2, %k2
 ; CHECK-NEXT: kshiftrq $14, %k2, %k2
 ; CHECK-NEXT: korq %k2, %k0, %k0
 ; CHECK-NEXT: movabsq $-562949953421313, %rax # imm = 0xFFFFDFFFFFFFFFFFF
 ; CHECK-NEXT: kmovq %rax, %k2
 ; CHECK-NEXT: kandq %k2, %k0, %k0
 ; CHECK-NEXT: kshiftrd $16, %k1, %k2
 ; CHECK-NEXT: kshiftlq $63, %k2, %k2
 ; CHECK-NEXT: kshiftrq $15, %k2, %k2
 ; CHECK-NEXT: korq %k2, %k0, %k0
 ; CHECK-NEXT: movabsq $-1125899906842625, %rax # imm = 0xFFFFBFFFFFFFFFFFFF
 ; CHECK-NEXT: kmovq %rax, %k2
 ; CHECK-NEXT: kandq %k2, %k0, %k0
 ; CHECK-NEXT: kshiftrd $19, %k1, %k2
 ; CHECK-NEXT: kshiftlq $63, %k2, %k2
 ; CHECK-NEXT: kshiftrq $13, %k2, %k2
 ; CHECK-NEXT: korq %k2, %k0, %k0
 ; CHECK-NEXT: movabsq $-2251799813685249, %rax # imm = 0xFFFF7FFFFFFFFFFFF
 ; CHECK-NEXT: kmovq %rax, %k2
 ; CHECK-NEXT: kandq %k2, %k0, %k0
 ; CHECK-NEXT: kshiftrd $18, %k1, %k2
 ; CHECK-NEXT: kshiftlq $63, %k2, %k2
 ; CHECK-NEXT: kshiftrq $12, %k2, %k2
 ; CHECK-NEXT: korq %k2, %k0, %k0
 ; CHECK-NEXT: movabsq $-4503599627370497, %rax # imm = 0xFFEFFFFFFFFFFFF
 ; CHECK-NEXT: kmovq %rax, %k2
 ; CHECK-NEXT: kandq %k2, %k0, %k0
 ; CHECK-NEXT: kshiftrd $21, %k1, %k2
 ; CHECK-NEXT: kshiftlq $63, %k2, %k2
 ; CHECK-NEXT: kshiftrq $11, %k2, %k2
 ; CHECK-NEXT: korq %k2, %k0, %k0
 ; CHECK-NEXT: movabsq $-9007199254740993, %rax # imm = 0xFFDFFFFFFFFFFFF
 ; CHECK-NEXT: kmovq %rax, %k2
 ; CHECK-NEXT: kandq %k2, %k0, %k0
 ; CHECK-NEXT: kshiftrd $20, %k1, %k2
 ; CHECK-NEXT: kshiftlq $63, %k2, %k2
 ; CHECK-NEXT: kshiftrq $10, %k2, %k2
 ; CHECK-NEXT: korq %k2, %k0, %k0
 ; CHECK-NEXT: movabsq $-18014398509481985, %rax # imm = 0xFFBFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $23, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $9, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-36028797018963969, %rax # imm = 0xFFF7FFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $22, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $8, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-72057594037927937, %rax # imm = 0xFEFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $25, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $7, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-144115188075855873, %rax # imm = 0xFDFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $24, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $6, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-288230376151711745, %rax # imm = 0xFBFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $27, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $5, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-576460752303423489, %rax # imm = 0xEFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $26, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $4, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-1152921504606846977, %rax # imm = 0xEFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $29, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $3, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
entry:
%a = load <64 x i8>, <64 x i8>* %x
%b = icmp eq <64 x i8> %a, zeroinitialize
%shuf = shufflevector <64 x i1> %b, undef, <64 x i32> <i32 1, i32 0, i32 2, i32 3, i32 5, i32 4, i32 7, i32 6, i32 9, i32 8, i32 11, i32 10, i32 13, i32 12, i32 15, i32 14, i32 17, i32 16, i32 19, i32 18, i32 21, i32 20, i32 23, i32 22, i32 25, i32 24, i32 27, i32 26, i32 29, i32 28, i32 31, i32 30, i32 33, i32 32, i32 35, i32 34, i32 37, i32 36, i32 39, i32 38, i32 41, i32 40, i32 43, i32 42, i32 45, i32 44, i32 47, i32 46, i32 49, i32 48, i32 51, i32 50, i32 53, i32 52, i32 55, i32 54, i32 57, i32 56, i32 59, i32 58, i32 61, i32 60, i32 63, i32 62>
call void @llvm.masked.store.v64i8.p0v64i8(<64 x i8> %a, <64 x i8>* %y, i32 %shuf)
ret void
}
declare void @llvm.masked.store.v64i8.p0v64i8(<64 x i8>, <64 x i8>*, i32, <64 x i1>)

@mem64_dst = global i64 0, align 8
@mem64_src = global i64 0, align 8
define i32 @v64i1_inline_asm() "min-legal-vector-width"="256" { ; CHECK-LABEL: v64i1_inline_asm:
; CHECK: # %bb.0:
; CHECK-NEXT: kmovq {{.*}}(%rip), %k0
; CHECK-NEXT: #APP
; CHECK-NEXT: #NO_APP
; CHECK-NEXT: kmovq %k0, {{.*}}(%rip)
; CHECK-NEXT: movl -[{{[0-9]+}}](%rsi), %eax
; CHECK-NEXT: retq
%l = alloca i32, align 4
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 */

; NOTE: Assertions have been autogenerated by utils/update_test_checks.py
; UTC_ARGS: --function-signature --scrub-attributes
; RUN: opt -S -argpromotion < %s | FileCheck %s
; RUN: opt -S -passes=argpromotion < %s | FileCheck %s
; Test that we only promote arguments when the caller/callee have compatible
; function attributes.

target triple = "x86_64-unknown-linux-gnu"

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
    ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
    ; CHECK-SAME: (<8 x i64>* \[\[ARG:%.*\]\], <8 x i64> \[\[ARG1_VAL:%.*\]\])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: store <8 x i64> \[\[ARG1_VAL\]\], <8 x i64>* \[\[ARG\]\]
    ; CHECK-NEXT: ret void
open source used in branch migration tool spirit

```asm
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
  ; CHECK-LABEL: define {{[^@]+}} @avx512_legal512_prefer512_call_avx512_legal512_prefer512
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
  ; CHECK-NEXT: bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}
```

```asm
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #1 {
  ; CHECK-LABEL: define {{[^@]+}} @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* [[ARG1_VAL:%.*]])
  ; CHECK-NEXT: bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}
```
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:.]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:.]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:.]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:.]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:.]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
}

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* [[ARG1_VAL:.]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
; bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:.]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:  call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT:  [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT:  call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP_VAL]])

; CHECK-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:  ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #0 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:  store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT:  ret void

; bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:  call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT:  [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT:  call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:  ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
;
; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{[^@]+}} @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
; CHECK-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
; CHECK-NEXT:  ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
;
define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
; CHECK-LABEL: define {{[^@]+}} @avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:  call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT:  call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]])
; CHECK-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:  ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 {    ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
    ; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
    ; CHECK-NEXT: ret void
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {    ; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
    ; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]])
    ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
    ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
    ; CHECK-NEXT: ret void
    bb:
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
    call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #3 {
  ; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* [[ARG1_VAL:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
  ; CHECK-NEXT: ret void
  ;
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
  ; CHECK-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
  ; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
  ; CHECK-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
  ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; CHECK-NEXT: ret void
  ;
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) { /*llvm-ir*/}
define void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256([8 x i64]* [[ARG:%.*]]) #4 {
  ; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* [[ARG1_VAL:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
  ; CHECK-NEXT: ret void
  ;
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
  ; CHECK-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
  ; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
  ; CHECK-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
  ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; CHECK-NEXT: ret void
  ;
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" }

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

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width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512"
"prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256"
"prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }
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; RUN: llc -march=hexagon < %s
; REQUIRES: asserts

; The two loads based on %struct.0, loading two different data types
; cause LSR to assume type "void" for the memory type. This would then
; cause an assert in isLegalAddressingMode. Make sure we no longer crash.

target triple = "hexagon"
%struct.0 = type { i8*, i8, %union.anon.0 }
%union.anon.0 = type { i8* }

define hidden fastcc void @fred() unnamed_addr #0 {
  entry:
  br i1 undef, label %while.end, label %while.body.lr.ph

  while.body.lr.ph: ; preds = %entry
    br label %while.body

  while.body: ; preds = %exit.2, %while.body.lr.ph
    %lsr.iv = phi %struct.0* [%cgep22, %exit.2], [ undef, %while.body.lr.ph ]
    switch i32 undef, label %exit [ i32 1, label %sw.bb.i i32 2, label %sw.bb3.i ]
    sw.bb.i: ; preds = %while.body
      unreachable

    sw.bb3.i: ; preds = %while.body
      unreachable

  exit: ; preds = %while.body
    switch i32 undef, label %exit.2 [ i32 1, label %sw.bb.i17 i32 2, label %sw.bb3.i20 ]
    sw.bb.i17: ; preds = %exit
      %0 = bitcast %struct.0* %lsr.iv to i32*
      %1 = load i32, i32* %0, align 4
      unreachable

    sw.bb3.i20: ; preds = %exit
      %2 = bitcast %struct.0* %lsr.iv to i8**
      %3 = load i8*, i8** %2, align 4
      unreachable

  exit.2: ; preds = %exit
    %cgep22 = getelementptr %struct.0, %struct.0* %lsr.iv, i32 1
    br label %while.body

  while.end: ; preds = %entry
    ret void
}

attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }
define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
    ; CHECK-LABEL: test_sitofp_fixed:
    %flt = sitofp <16 x i32> %in to <16 x double>
    %res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0> 
    ret <16 x double> %res
}

define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
    ; CHECK-LABEL: test_sitofp_fixed_shortish:
    %flt = sitofp <4 x i64> %in to <4 x double>
    %res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0> 
    ret <4 x double> %res
}

define internal void @innerSmall() "min-legal-vector-width"="128" {
ret void
}

define internal void @innerLarge() "min-legal-vector-width"="512" {
    ret void
}

define internal void @innerNoAttribute() {
    ret void
}

; We should not add an attribute during inlining. No attribute means unknown.
; Inlining doesn’t change the fact that we don’t know anything about this
; function.
define void @outerNoAttribute() {
    call void @innerLarge()
    ret void
}

define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
    call void @innerLarge()
    ret void
}

define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
    call void @innerSmall()
    ret void
}

; We should remove the attribute after inlining since the callee’s
; vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
    call void @innerNoAttribute()
    ret void
}

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }
; RUN: opt -consthoist -S -o - %s | FileCheck %s
target triple = "thumbv6m-none--musleabi"

; Check that for i8 type, the maximum legal offset is 31.
; Also check that an constant used as value to be stored rather than
; pointer in a store instruction is hoisted.
define void @foo_i8() {
    entry:
    %0 = load volatile i8, i8* inttoptr (i32 805874688 to i8*)
    %1 = load volatile i8, i8* inttoptr (i32 805874692 to i8*)
    %2 = load volatile i8, i8* inttoptr (i32 805874719 to i8*)
    %3 = load volatile i8, i8* inttoptr (i32 805874720 to i8*)
    %4 = load volatile i8, i8* inttoptr (i32 805874727 to i8*)
    store i8 %4, i8* inttoptr(i32 805873688 to i8*)
    store i8 %3, i8* inttoptr(i32 805873719 to i8*)
    store i8 %2, i8* inttoptr(i32 805873720 to i8*)
    store i8 %1, i8* inttoptr(i32 805873727 to i8*)
    store i8* inttoptr(i32 805874800 to i8*), i8** @goo
    ret void
}
; Check that for i16 type, the maximum legal offset is 62.
; CHECK: foo_i16
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874752 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i16*
; CHECK-NEXT: %1 = load volatile i16, i16* %0, align 2
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i16*
; CHECK-NEXT: %3 = load volatile i16, i16* %2, align 2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 32
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i16*
; CHECK-NEXT: %5 = load volatile i16, i16* %4, align 2
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C2]], 62
; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to i16*
; CHECK-NEXT: %7 = load volatile i16, i16* %6, align 2
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 22
; CHECK-NEXT: %8 = inttoptr i32 %[[M4]] to i16*
; CHECK-NEXT: %9 = load volatile i16, i16* %8, align 2
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i16*
; CHECK-NEXT: %11 = load volatile i16, i16* %10, align 2

define void @foo_i16() {
  entry:
  %0 = load volatile i16, i16* inttoptr (i32 805874688 to i16*), align 2
  %1 = load volatile i16, i16* inttoptr (i32 805874692 to i16*), align 2
  %2 = load volatile i16, i16* inttoptr (i32 805874720 to i16*), align 2
  %3 = load volatile i16, i16* inttoptr (i32 805874750 to i16*), align 2
  %4 = load volatile i16, i16* inttoptr (i32 805874752 to i16*), align 2
  %5 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
  ret void
}

; Check that for i32 type, the maximum legal offset is 124.
; CHECK: foo_i32
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i32*
; CHECK-NEXT: %1 = load volatile i32, i32* %0, align 4
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i32*
; CHECK-NEXT: %3 = load volatile i32, i32* %2, align 4
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 124
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i32*
; CHECK-NEXT: %5 = load volatile i32, i32* %4, align 4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i32*
; CHECK-NEXT: %7 = load volatile i32, i32* %6, align 4
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 8
define void @foo_i32() {
    entry:
    %0 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 4
    %1 = load volatile i32, i32* inttoptr (i32 805874692 to i32*), align 4
    %2 = load volatile i32, i32* inttoptr (i32 805874812 to i32*), align 4
    %3 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
    %4 = load volatile i32, i32* inttoptr (i32 805874824 to i32*), align 4
    %5 = load volatile i32, i32* inttoptr (i32 805874828 to i32*), align 4
    ret void
}
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target triple = "x86_64-unknown-linux-gnu"

; This should promote
define internal fastcall void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* %arg1) #0 {
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}
; CHECK-NEXT:  call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
; CHECK-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:  ret void

; bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {  
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256  
; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
; CHECK-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
; CHECK-NEXT:  ret void

; bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {  
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256  
; CHECK-SAME: (<8 x i64>* nocapture [[ARG:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:  call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT:  call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [%ARG:%.*], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [%ARG1:%.*])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
; CHECK-NEXT: ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void

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%; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
  ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
  ; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64)
  [[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
  ; CHECK-NEXT: bb:
    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
  ; CHECK-NEXT: ret void
  ;
  bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
  ; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
  ; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
  ; CHECK-NEXT: bb:
    [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
  ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; CHECK-NEXT: ret void
  ;
  bb:
    %tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
  ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64)
  [ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [ARG1:%.*])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
  ; CHECK-NEXT: ret void

  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}
define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
  ; CHECK-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* nonnull align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; CHECK-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
  ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; CHECK-NEXT: ret void

  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 {
  ; CHECK-LABEL: define ([[^@]+])@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64)
  [[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT:   [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
  ; CHECK-NEXT:   store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
  ; CHECK-NEXT:   ret void

bb:
%tmp = load <8 x i64>, <8 x i64>* %arg
store <8 x i64> %tmp, <8 x i64>* %arg
ret void

}
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #3 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 32
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
; CHECK-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg)
noalias nocapture nofree nonnull align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull align 32 dereferenceable(64) [[TMP]]
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg)
%tmp
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #4 {
    ; CHECK-LABEL: define [[[^@]+]+]@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
    ; CHECK-SAME: (<8 x i64>* noalias nocaapture nofree nonnull writeonly align 32 dereferenceable(64)
    [[ARG:%.*]], <8 x i64>* noalias nocaapture nofree nonnull readonly align 32 dereferenceable(64) [[ARG1:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: [%tmp:%.*] = load <8 x i64>, <8 x i64>* [[ARG1]], align 32
    ; CHECK-NEXT: store <8 x i64> [%tmp, <8 x i64>* [[ARG]], align 32
    ; CHECK-NEXT: ret void

    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
    ; CHECK-LABEL: define [[[^@]+]+]@avx2_legal512_prefer256_call_avx2_legal256_prefer256
    ; CHECK-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: [%tmp:%.*] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [%tmp2:%.*] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [%tmp3:%.*] = bitcast <8 x i64>* [%tmp] to i8*
    ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
    ; CHECK-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    ; CHECK-NEXT: [%tmp4:%.*] = load <8 x i64>, <8 x i64>* %tmp2, align 32
    ; CHECK-NEXT: store <8 x i64> [%tmp4, <8 x i64>* %arg, align 2
    ; CHECK-NEXT: ret void

    bb:
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
    call void @llvm.memset.p0i8.i64(i8* nocapture nofree nonnull writeonly align 32 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocaapture nofree nonnull readonly align 32 dereferenceable(64) [[TMP]])
    ; CHECK-NEXT: [%tmp4:%.*] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
    ; CHECK-NEXT: store <8 x i64> [%tmp4, <8 x i64>* [[ARG]], align 2
    ; CHECK-NEXT: ret void

    ; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5
attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }

; RUN: llc -O3 -mtriple=powerpc-unknown-linux-gnu -mcpu=e500 -mattr=spe < %s | FileCheck %s

; PowerPC SPE is a rare in-tree target that has the FP_TO_SINT node marked as Legal.

; Verify that fptosi(42.1) isn't simplified when the rounding mode is unknown.
; Verify that no gross errors happen.
; CHECK-LABEL: @f20
; COMMON: cfdctsiz
define i32 @f20(double %a) strictfp {
  entry:
  %result = call i32 @llvm.experimental.constrained.fptosi.i32.f64(double 42.1,
                      metadata !"fpexcept.strict")
    strictfp
  ret i32 %result
}

@llvm.fp.env = thread_local global i8 zeroinitializer, section "llvm.metadata"
declare i32 @llvm.experimental.constrained.fptosi.i32.f64(double, metadata)
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; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s
; D31946
; Check that we dont end up with the "LLVM ERROR: Cannot select" error.
; Additionally ensure that the output code actually put fp128 values in SSE registers.

declare fp128 @llvm.fabs.f128(fp128)
declare fp128 @llvm.copysign.f128(fp128)
declare fp128 @llvm.fabs.f128(fp128)
declare fp128 @llvm.copysign.f128(fp128, fp128)

declare fp128 @TestSelect(fp128 %a, fp128 %b) {
  %cmp = fcmp ogt fp128 %a, %b
  %sub = fsub fp128 %a, %b
  %res = select i1 %cmp, fp128 %sub, fp128 0xL00000000000000000000000000000000
  ret fp128 %res
; CHECK-LABEL: TestSelect:
; CHECK movaps 16(%rsp), %xmm1
; CHECK-NEXT callq __subtf3
; CHECK-NEXT testl %ebx, %ebx
; CHECK-NEXT jg .LBB0_2
; CHECK-NEXT # %bb.1:
define fp128 @TestFabs(fp128 %a) {
  %res = call fp128 @llvm.fabs.f128(fp128 %a)
  ret fp128 %res
}

define fp128 @TestCopysign(fp128 %a, fp128 %b) {
  %res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
  ret fp128 %res
}

define fp128 @TestFneg(fp128 %a) {
  %mul = fmul fp128 %a, %a
  %res = fsub fp128 0xL00000000000000008000000000000000, %mul
  ret fp128 %res
}

define void @zext256() "min-legal-vector-width"="256" {
  ; VEC256-LABEL: 'zext256'
  ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
}
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: ’zext256’
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

; %A = zext <8 x i16> undef to <8 x i64>
%B = zext <8 x i32> undef to <8 x i64>
%C = zext <16 x i8> undef to <16 x i32>
%D = zext <16 x i16> undef to <16 x i32>
%E = zext <32 x i8> undef to <32 x i16>
ret void

} define void @zext512() "min-legal-vector-width"="512" {
; AVX-LABEL: ’zext512’
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: ’zext512’
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
define void @sext256() "min-legal-vector-width"="256" {
    ; VEC256-LABEL: 'sext256'
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x i32>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
    ret void
}
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

; %A = sext <8 x i8> undef to <8 x i64>
; %B = sext <8 x i16> undef to <8 x i64>
; %C = sext <8 x i32> undef to <8 x i64>
; %D = sext <16 x i8> undef to <16 x i32>
; %E = sext <16 x i16> undef to <16 x i32>
; %F = sext <32 x i8> undef to <32 x i16>
ret void
}

define void @sext512() "min-legal-vector-width"="512" { 

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

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* /opt/ws_local/PERMITS_SQL/1068816920_1595472128.15/0/lz4-java-1-7-1-sources-
jar/net/jpountz/lz4/LZ4JNISafeDecompressor.java
* /opt/ws_local/PERMITS_SQL/1068816920_1595472128.15/0/lz4-java-1-7-1-sources-
jar/net/jpountz/lz4/LZ4JNIFastDecompressor.java
* /opt/ws_local/PERMITS_SQL/1068816920_1595472128.15/0/lz4-java-1-7-1-sources-
jar/net/jpountz/xxhash/StreamingXXHash64.java
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jar/net/jpountz/xxhash/XXHash64JNI.java
* /opt/ws_local/PERMITS_SQL/1068816920_1595472128.15/0/lz4-java-1-7-1-sources-
jar/net/jpountz/xxhash/XXHash64.java
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Note: Tuples cannot be directly destructured in method or function parameters.
    Either create a single parameter accepting the Tuple2,
    or consider a pattern matching anonymous function: `
      case (a, b) => ...
    `}
val x: ((Int, Int) => Int) = (((a, b)) => a)
^  
not-a-legal-formal-parameter-tuple.scala:3: error: not a legal formal parameter.
Note: Tuples cannot be directly destructured in method or function parameters.
    Either create a single parameter accepting the Tuple2,
    or consider a pattern matching anonymous function: `
      case (param1, param2) => ...
    `}
val y: ((Int, Int, Int) => Int) = (((a, !)) => a)
^  
not-a-legal-formal-parameter-tuple.scala:4: error: not a legal formal parameter.
Note: Tuples cannot be directly destructured in method or function parameters.
    Either create a single parameter accepting the Tuple3,
    or consider a pattern matching anonymous function: `
      case (param1, ..., param3) => ...
    `}
val z: ((Int, Int, Int) => Int) = (((a, NotAPatternVariableName, c)) => a)
^  
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bzip2/libbzip2 version 1.0.6 of 6 September 2010

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DRuntime: Runtime Library for the D Programming Language

===========================================================================

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Version 3.1, 31 March 2009

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<td>mach_override</td>
<td>lib/interception/mach_override</td>
</tr>
</tbody>
</table>

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+++++++++++++++++

Dean Elsner wrote the original gas for vax. [more details?]

Jay Fenlason maintained gas for a while, adding support for gdb-specific debug information and the 68k series machines, most of the preprocessing pass, and extensive changes in messages.c, input-file.c, write.c.

K. Richard Pixley maintained gas for a while, adding various enhancements and many bug fixes, including merging support for several processors, breaking gas up to handle multiple object file format backends (including heavy rewrite, testing, an integration of the coff and b.out backends), adding configuration including heavy testing and verification of cross assemblers and file splits and renaming, converted gas to strictly ansi C including full prototypes, added support for m680[34]0 & cpu32, considerable work on i960 including a coff port (including considerable amounts of reverse engineering), a sparc opcode file rewrite, decstation, rs6000, and hp300hpux host ports, updated “know” assertions and made them work, much other reorganization, cleanup, and lint.

Ken Raeburn wrote the high-level BFD interface code to replace most of the code in format-specific I/O modules.
The original Vax-VMS support was contributed by David L. Kashtan. Eric Youngdale and Pat Rankin have done much work with it since.

The Intel 80386 machine description was written by Eliot Dresselhaus.

Minh Tran-Le at IntelliCorp contributed some AIX 386 support.

The Motorola 88k machine description was contributed by Devon Bowen of Buffalo University and Torbjorn Granlund of the Swedish Institute of Computer Science.

Keith Knowles at the Open Software Foundation wrote the original MIPS back end (tc-mips.c, tc-mips.h), and contributed Rose format support that hasn't been merged in yet. Ralph Campbell worked with the MIPS code to support a.out format.

Support for the Zilog Z8k and Hitachi H8/300, H8/500 and SH processors (tc-z8k, tc-h8300, tc-h8500, tc-sh), and IEEE 695 object file format (obj-ieee), was written by Steve Chamberlain of Cygnus Solutions. Steve also modified the COFF back end (obj-coffbfd) to use BFD for some low-level operations, for use with the Hitachi, 29k and Zilog targets.

John Gilmore built the AMD 29000 support, added .include support, and simplified the configuration of which versions accept which pseudo-ops. He updated the 68k machine description so that Motorola's opcodes always produced fixed-size instructions (e.g. jsr), while synthetic instructions remained shrinkable (jbsr). John fixed many bugs, including true tested cross-compilation support, and one bug in relaxation that took a week and required the proverbial one-bit fix.

Ian Lance Taylor of Cygnus Solutions merged the Motorola and MIT syntaxes for the 68k, completed support for some COFF targets (68k, i386 SVR3, and SCO Unix), wrote the ECOFF support based on Michael Meissner's mips-tfile program, wrote the PowerPC and RS/6000 support, and made a few other minor patches. He handled the binutils releases for versions 2.7 through 2.9.

David Edelsohn contributed fixes for the PowerPC and AIX support.

Steve Chamberlain made gas able to generate listings.

Support for the HP9000/300 was contributed by Glenn Engel of HP.

Support for ELF format files has been worked on by Mark Eichin of Cygnus Solutions (original, incomplete implementation), Pete Hoogenboom at the University of Utah (PPA mainly), Michael Meissner of the Open Software Foundation (i386 mainly), and Ken Raeburn of...
Cygnus Solutions (sparc, initial 64-bit support).

Several engineers at Cygnus Solutions have also provided many small bug fixes and configuration enhancements.

The initial Alpha support was contributed by Carnegie-Mellon University. Additional work was done by Ken Raeburn of Cygnus Solutions. Richard Henderson then rewrote much of the Alpha support.

Ian Dall updated the support code for the National Semiconductor 32000 series, and added support for Mach 3 and NetBSD running on the PC532.

Klaus Kaempf ported the assembler and the binutils to openVMS/Alpha.

Steve Haworth contributed the support for the Texas Instruction c30 (tms320c30).

H.J. Lu has contributed many patches and much testing.

Alan Modra reworked much of the i386 backend, improving the error checking, updating the code, and improving the 16 bit support, using patches from the work of Martynas Kunigelis and H.J. Lu.

Many others have contributed large or small bugfixes and enhancements. If you've contributed significant work and are not mentioned on this list, and want to be, let us know. Some of the history has been lost; we aren't intentionally leaving anyone out.

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cmd/krb5/kproplog/kproplog.c
cmd/krb5/slave/kpropd_rpc.c
lib/gss_mechs/mech_krb5/et/kdb5_err.c
lib/gss_mechs/mech_spnego/mach/gssapiP_spnego.h
lib/gss_mechs/mech_spnego/mach/spnego_mech.c
lib/krb5/kadm5/kadm_host_srv_names.c
lib/krb5/kdb/kdb_convert.c
lib/krb5/kdb/kdb_hdr.h
lib/krb5/kdb/kdb_log.c
lib/krb5/kdb/kdb_log.h
lib/libgss/g_accept_sec_context.c
lib/libgss/g_acquire_cred.c
lib/libgss/g_canon_name.c
lib/libgss/g_compare_name.c
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lib/libgss/g_delete_sec_context.c
lib/libgss/g_dsp_name.c
lib/libgss/g_dsp_status.c
lib/libgss/g_dup_name.c
lib/libgss/g_exp_sec_context.c
```
lib/libgss/g_export_name.c
lib/libgss/g_glue.c
lib/libgss/g_imp_name.c
lib/libgss/g_imp_sec_context.c
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lib/libgss/g_inquire_context.c
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lib/libgss/g_inquire_names.c
lib/libgss/g_process_context.c
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lib/libgss/g_userok.c
lib/libgss/g_utils.c
lib/libgss/g_verify.c
lib/libgss/gssd_pname_to_uid.c
uts/common/gssapi/include/gssapi_err_generic.h
uts/common/gssapi/include/mechglueP.h

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lib/gssapi/mechglue/g_acquire_cred.c
lib/gssapi/mechglue/g_canon_name.c
lib/gssapi/mechglue/g_compare_name.c
lib/gssapi/mechglue/g_context_time.c
lib/gssapi/mechglue/g_delete_sec_context.c
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lib/gssapi/mechglue/g_dsp_status.c
lib/gssapi/mechglue/g_dup_name.c
lib/gssapi/mechglue/g_exp_sec_context.c
lib/gssapi/mechglue/g_export_name.c
lib/gssapi/mechglue/g_glue.c
lib/gssapi/mechglue/g_imp_name.c
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kadmin/server/ipropd_svc.c
lib/kdb/iprop.x
lib/kdb/kdb_convert.c
lib/kdb/kdb_log.c
lib/kdb/kdb_log.h
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### xwd v1.0.7

### xwd utility

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<td>Khronos</td>
</tr>
<tr>
<td></td>
<td>GL/wglext.h</td>
<td>Khronos</td>
</tr>
<tr>
<td></td>
<td>KHR/khrplatform.h</td>
<td>Khronos</td>
</tr>
</tbody>
</table>

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include/GL/glx.h :

Mesa 3-D graphics library

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*****************************************************************************

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include/GL/glxext.h
include/GL/wglxext.h :

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* /opt/cola/permits/1170785299_1622700563.86/0/python-excel-xlrd-1-1-0-0-ge1930e4-1-tar-gz/python-excel-xlrd-e1930e4/scripts/runxlrd.py
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Found in path(s):
* /opt/cola/permits/1170785299_1622700563.86/0/python-excel-xlrd-1-1-0-0-ge1930e4-1-tar-gz/python-excel-xlrd-e1930e4/tests/test_formulas.py
* /opt/cola/permits/1170785299_1622700563.86/0/python-excel-xlrd-1-1-0-0-ge1930e4-1-tar-gz/python-excel-xlrd-e1930e4/tests/test_cell.py
* /opt/cola/permits/1170785299_1622700563.86/0/python-excel-xlrd-1-1-0-0-ge1930e4-1-tar-gz/python-excel-xlrd-e1930e4/tests/test_formats.py
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* /opt/cola/permits/1170785299_1622700563.86/0/python-excel-xlrd-1-1-0-0-ge1930e4-1.tar.gz/python-excel-xlrd-e1930e4/xlrd/sheet.py
* /opt/cola/permits/1170785299_1622700563.86/0/python-excel-xlrd-1-1-0-0-ge1930e4-1.tar.gz/python-excel-xlrd-e1930e4/xlrd/xldate.py
* /opt/cola/permits/1170785299_1622700563.86/0/python-excel-xlrd-1-1-0-0-ge1930e4-1.tar.gz/python-excel-xlrd-e1930e4/xlrd/formula.py
* /opt/cola/permits/1170785299_1622700563.86/0/python-excel-xlrd-1-1-0-0-ge1930e4-1.tar.gz/python-excel-xlrd-e1930e4/xlrd/formatting.py
* /opt/cola/permits/1170785299_1622700563.86/0/python-excel-xlrd-1-1-0-0-ge1930e4-1.tar.gz/python-excel-xlrd-e1930e4/xlrd/compdoc.py
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* /opt/cola/permits/1170785299_1622700563.86/0/python-excel-xlrd-1-1-0-0-ge1930e4-1-tar-gz/python-excel-xlrd-e1930e4/tests/test_xldate.py

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Found in path(s):
* /opt/cola/permits/1170785299_1622700563.86/0/python-excel-xlrd-1-1-0-0-ge1930e4-1-tar-gz/python-excel-xlrd-e1930e4/xlrd/timemachine.py
* /opt/cola/permits/1170785299_1622700563.86/0/python-excel-xlrd-1-1-0-0-ge1930e4-1-tar-gz/python-excel-xlrd-e1930e4/xlrd/examples/xlrdnameAPIdemo.py

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* /opt/cola/permits/1170785299_1622700563.86/0/python-excel-xlrd-1-1-0-0-ge1930e4-1-tar-gz/python-excel-xlrd-e1930e4/setup.py
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1.1068 wildfly-elytron-sasl 1.13.1.Final

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1.1069 keycloak-saml-core-public 12.0.2

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*/
/**
* Encodes and decodes to and from Base64 notation.
* 
* Change Log:
* </p>
* <ul>
* <li>v2.1 - Cleaned up javadoc comments and unused variables and methods. Added some convenience methods
* for reading
* and
* writing to and from files.</li>
* <li>v2.0.2 - Now specifies UTF-8 encoding in places where the code fails on systems with other encodings (like
* EBCDIC).</li>
* <li>v2.0.1 - Fixed an error when decoding a single byte, that is, when the encoded data was a single byte.</li>
* <li>v2.0 - I got rid of methods that used booleans to set options. Now everything is more consolidated and cleaner.
* The code
* now detects when data that's being decoded is gzip-compressed and will decompress it automatically. Generally
* things
* are cleaner. You'll probably have to change some method calls that you were making to support the new options
* format (not int that you "OR" together).</li>
* <li>v1.5.1 - Fixed bug when decompressing and decoding to a byte[] using decode (String s, boolean
* gzipCompressed

*/
* Added the ability to “suspend” encoding in the Output Stream so you can turn on and off the encoding if you need to.
* embed
* base64 data in an otherwise “normal” stream (like an XML file).
* Added the ability to “suspend” encoding in the Output Stream so you can turn on and off the encoding if you need to.
* embed
* base64 data in an otherwise “normal” stream (like an XML file).
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* base64 data in an otherwise “normal” stream (like an XML file).
* Added the ability to “suspend” encoding in the Output Stream so you can turn on and off the encoding if you need to.
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* embed
* base64 data in an otherwise “normal” stream (like an XML file).

- v1.5 - Output stream pases on flush() command but doesn't do anything itself. This helps when using GZIP streams.
- Added the ability to GZip-compress objects before encoding them.
- v1.4 - Added helper methods to read/write files.
- v1.3.6 - Fixed OutputStream.flush() so that 'position' is reset.
- v1.3.5 - Added flag to turn on and off line breaks. Fixed bug in input stream where last buffer being read, if not completely full, was not returned.
- v1.3.4 - Fixed when "improperly padded stream" error was thrown at the wrong time.
- v1.3.3 - Fixed I/O streams which were totally messed up.
- </ul>

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* </p>

* @author Robert Harder
  * @author rob@iharder.net
  * @version 2.1
*/

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* /opt/cola/permits/1130030965_1612433589.69/0/keycloak-saml-core-public-12-0-2-sources.jar/org/keycloak/saml/common/util/Base64.java
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1.1070 e2fsprogs 1.44.5 1+deb10u3

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were written by Theodore Ts'o <tytso@mit.edu> and Remy Card
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+++ tdbsa/tdb.c
@@ -4,11 +4,11 @@
Last Changed Date: 2007-06-06 20:14:06 -0400 (Wed, 06 Jun 2007)
*/
/*
- Unix SMB/CIFS implementation.
+ trivial database library - standalone version

- trivial database library - private includes
-
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Theodore Ts'o
23-June-2007

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The reason we have a separate public license for some libraries is that they blur the distinction we usually make between modifying or adding to a program and simply using it. Linking a program with a library, without changing the library, is in some sense simply using the library, and is analogous to running a utility program or application program. However, in a textual and legal sense, the linked executable is a combined work, a derivative of the original library, and the ordinary General Public License treats it as such.

Because of this blurred distinction, using the ordinary General Public License for libraries did not effectively promote software sharing, because most developers did not use the libraries. We concluded that weaker conditions might promote sharing better.

However, unrestricted linking of non-free programs would deprive the users of those programs of all benefit from the free status of the libraries themselves. This Library General Public License is intended to permit developers of non-free programs to use free libraries, while preserving your freedom as a user of such programs to change the free libraries that are incorporated in them. (We have not seen how to achieve this as regards changes in header files, but we have achieved it as regards changes in the actual functions of the Library.) The hope is that this will lead to faster development of free libraries.

The precise terms and conditions for copying, distribution and modification follow. Pay close attention to the difference between a "work based on the library" and a "work that uses the library". The former contains code derived from the library, while the latter only works together with the library.

Note that it is possible for a library to be covered by the ordinary General Public License rather than by this special one.

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A "library" means a collection of software functions and/or data prepared so as to be conveniently linked with application programs (which use some of those functions and data) to form executables.

The "Library", below, refers to any such software library or work
which has been distributed under these terms. A "work based on the Library" means either the Library or any derivative work under copyright law: that is to say, a work containing the Library or a portion of it, either verbatim or with modifications and/or translated straightforwardly into another language. (Hereinafter, translation is included without limitation in the term "modification").

"Source code" for a work means the preferred form of the work for making modifications to it. For a library, complete source code means all the source code for all modules it contains, plus any associated interface definition files, plus the scripts used to control compilation and installation of the library.

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the facility, other than as an argument passed when the facility is invoked, then you must make a good faith effort to ensure that, in the event an application does not supply such function or table, the facility still operates, and performs whatever part of its purpose remains meaningful.

(For example, a function in a library to compute square roots has a purpose that is entirely well-defined independent of the application. Therefore, Subsection 2d requires that any application-supplied function or table used by this function must be optional: if the application does not supply it, the square root function must still compute square roots.)

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Thus, it is not the intent of this section to claim rights or contest your rights to work written entirely by you; rather, the intent is to exercise the right to control the distribution of derivative or collective works based on the Library.

In addition, mere aggregation of another work not based on the Library with the Library (or with a work based on the Library) on a volume of a storage or distribution medium does not bring the other work under the scope of this License.

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This option is useful when you wish to copy part of the code of
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must be distributed under the terms of Sections 1 and 2 above on a
medium customarily used for software interchange.

If distribution of object code is made by offering access to copy
from a designated place, then offering equivalent access to copy the
source code from the same place satisfies the requirement to
distribute the source code, even though third parties are not
compelled to copy the source along with the object code.

5. A program that contains no derivative of any portion of the
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therefore falls outside the scope of this License.

However, linking a "work that uses the Library" with the Library
creates an executable that is a derivative of the Library (because it
contains portions of the Library), rather than a "work that uses the
library". The executable is therefore covered by this License.
Section 6 states terms for distribution of such executables.

When a "work that uses the Library" uses material from a header file
that is part of the Library, the object code for the work may be a
derivative work of the Library even though the source code is not.
Whether this is true is especially significant if the work can be
linked without the Library, or if the work is itself a library. The
threshold for this to be true is not precisely defined by law.

If such an object file uses only numerical parameters, data
structure layouts and accessors, and small macros and small inline
functions (ten lines or less in length), then the use of the object
file is unrestricted, regardless of whether it is legally a derivative
work. (Executables containing this object code plus portions of the
Library will still fall under Section 6.)

Otherwise, if the work is a derivative of the Library, you may
distribute the object code for the work under the terms of Section 6.
Any executables containing that work also fall under Section 6,
whether or not they are linked directly with the Library itself.

6. As an exception to the Sections above, you may also compile or
link a "work that uses the Library" with the Library to produce a
work containing portions of the Library, and distribute that work under terms of your choice, provided that the terms permit modification of the work for the customer's own use and reverse engineering for debugging such modifications.

You must give prominent notice with each copy of the work that the Library is used in it and that the Library and its use are covered by this License. You must supply a copy of this License. If the work during execution displays copyright notices, you must include the copyright notice for the Library among them, as well as a reference directing the user to the copy of this License. Also, you must do one of these things:

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b) Accompany the work with a written offer, valid for at least three years, to give the same user the materials specified in Subsection 6a, above, for a charge no more than the cost of performing this distribution.

c) If distribution of the work is made by offering access to copy from a designated place, offer equivalent access to copy the above specified materials from the same place.

d) Verify that the user has already received a copy of these materials or that you have already sent this user a copy.

For an executable, the required form of the "work that uses the Library" must include any data and utility programs needed for reproducing the executable from it. However, as a special exception, the source code distributed need not include anything that is normally distributed (in either source or binary form) with the major components (compiler, kernel, and so on) of the operating system on which the executable runs, unless that component itself accompanies the executable.

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<signature of Ty Coon>, 1 April 1990
Ty Coon, President of Vice

That's all there is to it!
This package was added to the e2fsprogs debian source package by Theodore Ts'o <tytso@mit.edu> on Sat Mar 15 15:33:37 EST 2003

It is part of the main e2fsprogs distribution, which can be found at:

http://sourceforge.net/projects/e2fsprogs

Upstream Author: Theodore Ts'o <tytso@mit.edu>

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This is the Debian GNU/Linux prepackaged version of the ss command-line interface parsing library. It is currently distributed together with the EXT2 file system utilities, which are otherwise packaged as "e2fsprogs".

This package was put together by Yann Dirson <dirson@debian.org>, from sources obtained from a mirror of:
tsx-11.mit.edu:/pub/linux/packages/ext2fs/

From the original distribution:

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# This is a Makefile stub which handles the creation of BSD shared libraries.
# In order to use this stub, the following makefile variables must be defined.

# BSDLIB_VERSION = 1.0
# BSDLIB_IMAGE = libce
# BSDLIB_MYDIR = et
# BSDLIB_INSTALL_DIR = $(SHLIBDIR)

all:: image

real-subdirs:: Makefile
@echo "MKDIR pic"
@mkdir -p pic

BSD_LIB = $(BSDLIB_IMAGE).so.$(BSDLIB_VERSION)
BSDLIB_PIC_FLAG = -fpic

image::$(BSD_LIB)

$(BSD_LIB): $(OBJS)
(cd pic; ld -Bshareable -o $(BSD_LIB) $(LDFLAGS_SHLIB) $(OBJS))
$(MV) pic/$(BSD_LIB) .
$(RM) -f ../$(BSD_LIB)
(cd ..; $(LN) $(LINK_BUILD_FLAGS) `echo $(my_dir) | sed -e 's;lib/;;'`/$(BSD_LIB) $(BSD_LIB))

install-shlibs install:: $(BSD_LIB)
@echo "INSTALL_PROGRAM $(BSDLIB_INSTALL_DIR)/$(BSD_LIB)"
@$(INSTALL_PROGRAM) $(BSD_LIB) \ $(DESTDIR)$BSDLIB_INSTALL_DIR/$BSDLIB_LIB\ @-$(LDCONFIG)

install-strip: install

install-shlibs-strip: install-shlibs

uninstall-shlibs uninstall::
$(RM) -f $(DESTDIR)$BSDLIB_INSTALL_DIR/$BSDLIB_LIB

clean::
$(RM) -rf pic
$(RM) -f $(BSD_LIB)
$(RM) -f ../$(BSD_LIB)

This is the Debian GNU/Linux prepackaged version of the Common Error Description library. It is currently distributed together with the EXT2 file system utilities, which are otherwise packaged as "e2fsprogs".
This package was put together by Yann Dirson <dirson@debian.org>, from sources obtained from a mirror of:
tsx-11.mit.edu:/pub/linux/packages/ext2fs/

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Gadi Oxman, August 1995

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c) If the modified program normally reads commands interactively when run, you must cause it, when started running for such interactive use in the most ordinary way, to print or display an announcement including an appropriate copyright notice and a notice that there is no warranty (or else, saying that you provide a warranty) and that users may redistribute the program under these conditions, and telling the user how to view a copy of this License. (Exception: if the Program itself is interactive but does not normally print such an announcement, your work based on the Program is not required to print an announcement.)

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c) Accompany it with the information you received as to the offer
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allowed only for noncommercial distribution and only if you
received the program in object code or executable form with such
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The source code for a work means the preferred form of the work for
making modifications to it. For an executable work, complete source
code means all the source code for all modules it contains, plus any
associated interface definition files, plus the scripts used to
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1.1071 pyrsistent 0.18.0
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1.1072 pcre 8.42-4.el8

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End
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----------

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THE BASIC LIBRARY FUNCTIONS
-----------------------------

Written by: Philip Hazel
Email local part: ph10
Email domain: cam.ac.uk

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* /opt/cola/permits/1130029659_1612433580.39/0/wildfly-elytron-auth-server-http-1-13-1-final-sources-
  jar/org/wildfly/security/auth/server/http/ElytronMessages.java
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  jar/org/wildfly/security/auth/server/HttpAuthenticationFactory.java

1.1074 click 6.7

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"Source code" for a work means the preferred form of the work for making modifications to it. For a library, complete source code means all the source code for all modules it contains, plus any associated interface definition files, plus the scripts used to control compilation and installation of the library.

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in the event an application does not supply such function or
table, the facility still operates, and performs whatever part of
its purpose remains meaningful.

(For example, a function in a library to compute square roots has
a purpose that is entirely well-defined independent of the
application. Therefore, Subsection 2d requires that any
application-supplied function or table used by this function must
be optional: if the application does not supply it, the square
root function must still compute square roots.)

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If distribution of object code is made by offering access to copy
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creates an executable that is a derivative of the Library (because it
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If such an object file uses only numerical parameters, data
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Otherwise, if the work is a derivative of the Library, you may
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Ty Coon, President of Vice

That's all there is to it!

1.1080 orm-core 5.3.20.Final
1.1080.1 Available under license:

# The main CI of Hibernate ORM is https://ci.hibernate.org/job/hibernate-orm-6.0-h2-main/.
# However, Hibernate ORM builds run on GitHub actions regularly
# to check that it still works and can be used in GitHub forks.
# See https://docs.github.com/en/free-pro-team@latest/actions
# for more information about GitHub actions.

name: Hibernate ORM build
on:
push:
  branches:
  - 'main'
  - 'wip/6.0'
pull_request:
  branches:
  - 'main'
  - 'wip/6.0'
jobs:
build:
  name: Java 8
  runs-on: ubuntu-latest
  # We want to know the test results of all matrix entries
  continue-on-error: true
  strategy:
    fail-fast: false
  matrix:
    # When GitHub Actions supports it: https://github.com/actions/toolkit/issues/399
    # We will use the experimental flag as indicator whether a failure should cause a workflow failure
    include:
      - rdbms: h2
        experimental: false
      - rdbms: derby
        experimental: true
      - rdbms: mariadb
        experimental: true
      - rdbms: postgresql
        experimental: true
      - rdbms: oracle
        experimental: true
      - rdbms: db2
        experimental: true
      - rdbms: mssql
        experimental: true
    # Running with HANA requires at least 8GB memory just for the database, which we don't have on GH Actions runners
    #       - rdbms: hana
    #       experimental: true
  steps:
    - uses: actions/checkout@v2
    with:
      persist-credentials: false
    - name: Reclaim Disk Space
      run: .github/ci-prerequisites.sh
    - name: Start database
      env:
- name: Set up Java 8
  uses: actions/setup-java@v1
  with:
    java-version: 1.8
- name: Get year/month for cache key
  id: get-date
  run: |
    echo "::set-output name=yearmonth::$(/bin/date -u "+%Y-%m")"
  shell: bash
- name: Cache Maven local repository
  uses: actions/cache@v2
  id: cache-maven
  with:
    path: |
      ~/.m2/repository
      ~/.gradle/caches/
      ~/.gradle/wrapper/
    # refresh cache every month to avoid unlimited growth
    key: maven-localrepo-${{ steps.get-date.outputs.yearmonth }}
- name: Run build script
  env:
    RDBMS: ${{ matrix.rdbms }}
  run: ./ci/build-github.sh
  shell: bash
- name: Upload test reports (if Gradle failed)
  uses: actions/upload-artifact@v2
  if: failure()
  with:
    name: test-reports-java8-${{ matrix.rdbms }}
    path: |
      ./**/target/reports/tests/
      ./**/target/reports/checkstyle/
- name: Omit produced artifacts from build cache
  run: ./ci/before-cache.sh

build11:
  name: Java 11
  runs-on: ubuntu-latest
  # We want to know the test results of all matrix entries
  continue-on-error: true
  steps:
    - uses: actions/checkout@v2
      with:
        persist-credentials: false
    - name: Set up Java 11
      uses: actions/setup-java@v1
      with:
java-version: 11
- name: Get year/month for cache key
  id: get-date
  run: |
    echo '::set-output name=yearmonth::$(/bin/date -u "+%Y-%m")'
  shell: bash
- name: Cache Maven local repository
  uses: actions/cache@v2
  id: cache-maven
  with:
    path: |
      ~/.m2/repository
      ~/.gradle/caches/
      ~/.gradle/wrapper/
    # refresh cache every month to avoid unlimited growth
    key: maven-localrepo-$
    
- name: Run build script
  run: ./ci/build-github.sh
  shell: bash
- name: Upload test reports (if Gradle failed)
  uses: actions/upload-artifact@v2
  if: failure()
  with:
    name: test-reports-java11
    path: |
      /**/target/reports/tests/
      /**/target/reports/checkstyle/

- name: Omit produced artifacts from build cache
  run: ./ci/before-cache.sh

This file is part of Hibernate Spatial, an extension to the hibernate ORM solution for spatial (geographic) data.

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(For example, a function in a library to compute square roots has a purpose that is entirely well-defined independent of the application. Therefore, Subsection 2d requires that any application-supplied function or table used by this function must be optional: if the application does not supply it, the square root function must still compute square roots.)

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If distribution of object code is made by offering access to copy from a designated place, then offering equivalent access to copy the source code from the same place satisfies the requirement to distribute the source code, even though third parties are not compelled to copy the source along with the object code.
5. A program that contains no derivative of any portion of the Library, but is designed to work with the Library by being compiled or linked with it, is called a "work that uses the Library". Such a work, in isolation, is not a derivative work of the Library, and therefore falls outside the scope of this License.

However, linking a "work that uses the Library" with the Library creates an executable that is a derivative of the Library (because it contains portions of the Library), rather than a "work that uses the library". The executable is therefore covered by this License. Section 6 states terms for distribution of such executables.

When a "work that uses the Library" uses material from a header file that is part of the Library, the object code for the work may be a derivative work of the Library even though the source code is not. Whether this is true is especially significant if the work can be linked without the Library, or if the work is itself a library. The threshold for this to be true is not precisely defined by law.

If such an object file uses only numerical parameters, data structure layouts and accessors, and small macros and small inline functions (ten lines or less in length), then the use of the object file is unrestricted, regardless of whether it is legally a derivative work. (Executables containing this object code plus portions of the Library will still fall under Section 6.)

Otherwise, if the work is a derivative of the Library, you may distribute the object code for the work under the terms of Section 6. Any executables containing that work also fall under Section 6, whether or not they are linked directly with the Library itself.

6. As an exception to the Sections above, you may also combine or link a "work that uses the Library" with the Library to produce a work containing portions of the Library, and distribute that work under terms of your choice, provided that the terms permit modification of the work for the customer's own use and reverse engineering for debugging such modifications.

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b) Use a suitable shared library mechanism for linking with the Library. A suitable mechanism is one that (1) uses at run time a copy of the library already present on the user's computer system, rather than copying library functions into the executable, and (2) will operate properly with a modified version of the library, if the user installs one, as long as the modified version is interface-compatible with the version that the work was made with.

c) Accompany the work with a written offer, valid for at least three years, to give the same user the materials specified in Subsection 6a, above, for a charge no more than the cost of performing this distribution.

d) If distribution of the work is made by offering access to copy from a designated place, offer equivalent access to copy the above specified materials from the same place.

e) Verify that the user has already received a copy of these materials or that you have already sent this user a copy.

For an executable, the required form of the "work that uses the Library" must include any data and utility programs needed for reproducing the executable from it. However, as a special exception, the materials to be distributed need not include anything that is normally distributed (in either source or binary form) with the major components (compiler, kernel, and so on) of the operating system on which the executable runs, unless that component itself accompanies the executable.

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4. You may copy and distribute the Library (or a portion or derivative of it, under Section 2) in object code or executable form under the terms of Sections 1 and 2 above provided that you accompany it with the complete corresponding machine-readable source code, which must be distributed under the terms of Sections 1 and 2 above on a medium customarily used for software interchange.

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dns.c - Recursive, Reentrant DNS Resolver.

--*--

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Otherwise, if the work is a derivative of the Library, you may distribute the object code for the work under the terms of Section 6. Any executables containing that work also fall under Section 6, whether or not they are linked directly with the Library itself.

6. As an exception to the Sections above, you may also combine or link a "work that uses the Library" with the Library to produce a work containing portions of the Library, and distribute that work under terms of your choice, provided that the terms permit modification of the work for the customer’s own use and reverse engineering for debugging such modifications.

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b) Use a suitable shared library mechanism for linking with the Library. A suitable mechanism is one that (1) uses at run time a copy of the library already present on the user's computer system, rather than copying library functions into the executable, and (2) will operate properly with a modified version of the library, if the user installs one, as long as the modified version is interface-compatible with the version that the work was made with.

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For an executable, the required form of the "work that uses the Library" must include any data and utility programs needed for reproducing the executable from it. However, as a special exception, the materials to be distributed need not include anything that is normally distributed (in either source or binary form) with the major components (compiler, kernel, and so on) of the operating system on which the executable runs, unless that component itself accompanies the executable.

It may happen that this requirement contradicts the license restrictions of other proprietary libraries that do not normally accompany the operating system. Such a contradiction means you cannot use both them and the Library together in an executable that you distribute.

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=aarch64-- | FileCheck %s

; A shuffle mask with all undef elements is always legal.

define <4 x i32> @PR41535(<2 x i32> %p1, <2 x i32> %p2) {
    ; CHECK-LABEL: PR41535:
    ; CHECK:       // %bb.0:
    ; CHECK-NEXT:  ext v0.8b, v0.8b, v1.8b, #4
    ; CHECK-NEXT:  mov v0.d[1], v0.d[0]
    ; CHECK-NEXT:  ret
    %cat1 = shufflevector <2 x i32> %p1, <2 x i32> undef, <4 x i32> <i32 undef, i32 1, i32 undef, i32 undef>
    %cat2 = shufflevector <2 x i32> %p2, <2 x i32> undef, <4 x i32> <i32 0, i32 undef, i32 undef, i32 undef>
%r = shufflevector <4 x i32> %cat1, <4 x i32> %cat2, <4 x i32> <i32 undef, i32 undef, i32 1, i32 4>
ret <4 x i32> %r
}
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;
; Test that early if conversion produces LOCR with operands of the right register classes.

define void @autogen_SD4739(i8*) {
 ; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
 BB:
  %L34 = load i8, i8* %0
  %Cmp56 = icmp sgt i8 undef, %L34

br label %CF246

CF246: ; preds = %CF246, %BB
%Sl163 = select i1 %Cmp56, i8 %L34, i8 undef
br i1 undef, label %CF246, label %CF248

CF248: ; preds = %CF248, %CF246
store i8 %Sl163, i8* %0
br label %CF248
}

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define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
    ; CHECK-LABEL: test_sitofp_fixed:
    ; First, extend each i32 to i64
    ; CHECK-DAG: sshll2.2d [[BLOCK0_HI:v[0-9]+]], v0, #0
    ; CHECK-DAG: sshll2.2d [[BLOCK1_HI:v[0-9]+]], v1, #0
    ; CHECK-DAG: sshll2.2d [[BLOCK2_HI:v[0-9]+]], v2, #0
    ; CHECK-DAG: sshll2.2d [[BLOCK3_HI:v[0-9]+]], v3, #0
    ; CHECK-DAG: sshll.2d [[BLOCK0_LO:v[0-9]+]], v0, #0
    ; CHECK-DAG: sshll.2d [[BLOCK1_LO:v[0-9]+]], v1, #0
    ; CHECK-DAG: sshll.2d [[BLOCK2_LO:v[0-9]+]], v2, #0
    ; CHECK-DAG: sshll.2d [[BLOCK3_LO:v[0-9]+]], v3, #0
    ; Next, convert each to double.
    ; CHECK-DAG: scvtf.2d v0, [[BLOCK0_LO]]
    ; CHECK-DAG: scvtf.2d v1, [[BLOCK0_HI]]
    ; CHECK-DAG: scvtf.2d v2, [[BLOCK1_LO]]
    ; CHECK-DAG: scvtf.2d v3, [[BLOCK1_HI]]
    ; CHECK-DAG: scvtf.2d v4, [[BLOCK2_LO]]
    ; CHECK-DAG: scvtf.2d v5, [[BLOCK2_HI]]
    ; CHECK-DAG: scvtf.2d v6, [[BLOCK3_LO]]
    ; CHECK-DAG: scvtf.2d v7, [[BLOCK3_HI]]
    ; CHECK: ret
    %flt = sitofp <16 x i32> %in to <16 x double>
    %res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0>
    ret <16 x double> %res
}

; This one is small enough to satisfy isSimple, but still illegally large.
define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
    ; CHECK-LABEL: test_sitofp_fixed_shortish:
    ; CHECK-DAG: scvtf.2d v0, v0
    ; CHECK-DAG: scvtf.2d v1, v1
    ; CHECK: ret
    %flt = sitofp <4 x i64> %in to <4 x double>
    %res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
    ret <4 x double> %res
}

; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking %s
; D31946
; Check that we dont end up with the "LLVM ERROR: Cannot select" error.

; Additionally ensure that the output code actually put fp128 values in SSE registers.

declare fp128 @llvm.fabs.f128(fp128)
declare fp128 @llvm.copysign.f128(fp128, fp128)

define fp128 @TestSelect(fp128 %a, fp128 %b) {
  ; CHECK-LABEL: TestSelect:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT: pushq %rbx 
  ; CHECK-NEXT: .cfi_def_cfa_offset 16
  ; CHECK-NEXT: subq $32, %rsp
  ; CHECK-NEXT: .cfi_def_cfa_offset 48
  ; CHECK-NEXT: .cfi_offset %rbx, -16
  ; CHECK-NEXT: movaps %xmm1, {{[[-9]+]}(%r{{[sb]}}p)} # 16-byte Spill
  ; CHECK-NEXT: movaps %xmm0, (%r{sb}) # 16-byte Spill
  ; CHECK-NEXT: callq __gttf2
  ; CHECK-NEXT: movl %eax, %ebx
  ; CHECK-NEXT: movaps (%r{sb}), %xmm1 # 16-byte Reload
  ; CHECK-NEXT: callq __subtf3
  ; CHECK-NEXT: testl %ebx, %ebx
  ; CHECK-NEXT: jg .LBB0_2
  ; CHECK-NEXT: xorps %xmm0, %xmm0
  ; CHECK-NEXT: .LBB0_2:
  ; CHECK-NEXT: addq $32, %rsp
  ; CHECK-NEXT: .cfi_def_cfa_offset 16
  ; CHECK-NEXT: popq %rbx
  ; CHECK-NEXT: .cfi_def_cfa_offset 8
  ; CHECK-NEXT: retq
  %cmp = fcmp ogt fp128 %a, %b
  %sub = fsub fp128 %a, %b
  %res = select i1 %cmp, fp128 %sub, fp128 0x00000000000000000000000000000000
  ret fp128 %res
}

define fp128 @TestFabs(fp128 %a) {
  ; CHECK-LABEL: TestFabs:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT: andps {{.*}}(%rip), %xmm0
  ; CHECK-NEXT: retq
  %res = call fp128 @llvm.fabs.f128(fp128 %a)
  ret fp128 %res
}

define fp128 @TestCopysign(fp128 %a, fp128 %b) {
  ; CHECK-LABEL: TestCopysign:
  ; CHECK:       # %bb.0:
; CHECK-NEXT:  andps {{.*}}(%rip), %xmm1
; CHECK-NEXT:  andps {{.*}}(%rip), %xmm0
; CHECK-NEXT:  orps %xmm1, %xmm0
; CHECK-NEXT:  retq
%res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
ret fp128 %res
}
define fp128 @TestFneg(fp128 %a) {
; CHECK-LABEL: TestFneg:
; CHECK:  # %bb.0:
; CHECK-NEXT:  pushq %rax
; CHECK-NEXT:  .cfi_def_cfa_offset 16
; CHECK-NEXT:  movaps %xmm0, %xmm1
; CHECK-NEXT:  callq __multf3
; CHECK-NEXT:  xorps {{.*}}(%rip), %xmm0
; CHECK-NEXT:  popq %rax
; CHECK-NEXT:  .cfi_def_cfa_offset 8
; CHECK-NEXT:  retq
%mul = fmul fp128 %a, %a
%res = fsub fp128 0xL00000000000000008000000000000000, %mul
ret fp128 %res
}

; RUN: opt %s -inline -S | FileCheck %s
define internal void @innerSmall() "min-legal-vector-width"="128" {
ret void
}
define internal void @innerLarge() "min-legal-vector-width"="512" {
ret void
}
define internal void @innerNoAttribute() {
ret void
}

; We should not add an attribute during inlining. No attribute means unknown.
; Inlining doesn't change the fact that we don't know anything about this
; function.
define void @outerNoAttribute() {
call void @innerLarge()
ret void
}
define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
call void @innerLarge()
ret void
define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
    call void @innerSmall()
    ret void
}

; We should remove the attribute after inlining since the callee's
; vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
    call void @innerNoAttribute()
    ret void
}

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }

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; Check that for i8 type, the maximum legal offset is 31.
; Also check that an constant used as value to be stored rather than
; pointer in a store instruction is hoisted.
; CHECK: foo_i8
; CHECK-DAG: %[[C1:const[0-9]?]]= bitcast i32 805874720 to i32
; CHECK-DAG: %[[C2:const[0-9]?]]= bitcast i32 805874688 to i32
; CHECK-DAG: %[[C3:const[0-9]?]]= bitcast i32 805873720 to i32
; CHECK-DAG: %[[C4:const[0-9]?]]= bitcast i32 805873668 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i8*
; CHECK-NEXT: %1 = load volatile i8, i8* %0
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i8*
; CHECK-NEXT: %3 = load volatile i8, i8* %2
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i8*
; CHECK-NEXT: %5 = load volatile i8, i8* %4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i8*
; CHECK-NEXT: %7 = load volatile i8, i8* %6
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i8*
; CHECK-NEXT: %9 = load volatile i8, i8* %8
; CHECK-NEXT: %10 = inttoptr i32 %[[C4]] to i8*
; CHECK-NEXT: store i8 %9, i8* %10
; CHECK-NEXT: %11 = inttoptr i32 %[[M4]] to i8*
; CHECK-NEXT: store i8 %7, i8* %11
; CHECK-NEXT: %12 = inttoptr i32 %[[C3]] to i8*
; CHECK-NEXT: store i8 %5, i8* %12
; CHECK-NEXT: %13 = inttoptr i32 %[[M5]] to i8*
; CHECK-NEXT: store i8 %3, i8* %13
; CHECK-NEXT: %14 = inttoptr i32 %[[M6]] to i8*
; CHECK-NEXT: store i8* %14, i8** @goo

@goo = global i8* undef

define void @foo_i8() {
  entry:
  %0 = load volatile i8, i8* inttopr (i32 805874688 to i8*)
  %1 = load volatile i8, i8* inttopr (i32 805874692 to i8*)
  %2 = load volatile i8, i8* inttopr (i32 805874719 to i8*)
  %3 = load volatile i8, i8* inttopr (i32 805874720 to i8*)
  %4 = load volatile i8, i8* inttopr (i32 805874727 to i8*)
}
store i8 %4, i8* inttoptr(i32 805873688 to i8*)
store i8 %3, i8* inttoptr(i32 805873719 to i8*)
store i8 %2, i8* inttoptr(i32 805873720 to i8*)
store i8 %1, i8* inttoptr(i32 805873727 to i8*)
store i8* inttoptr(i32 805874800 to i8*), i8** @goo
ret void
}

; Check that for i16 type, the maximum legal offset is 62.
; CHECK: foo_i16
; CHECK-DAG: %[[C1:const[0-9]?:]] = bitcast i32 805874752 to i32
; CHECK-DAG: %[[C2:const[0-9]?:]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttopr i32 %[[C2]] to i16*
; CHECK-NEXT: %1 = load volatile i16, i16* %0, align 2
; CHECK-NEXT: %[[M1:const_mat[0-9]?:]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = load volatile i16, i16* %1, align 2
; CHECK-NEXT: %[[M2:const_mat[0-9]?:]] = add i32 %[[C2]], 32
; CHECK-NEXT: %3 = load volatile i16, i16* %2, align 2
; CHECK-NEXT: %[[M3:const_mat[0-9]?:]] = add i32 %[[C2]], 62
; CHECK-NEXT: %4 = load volatile i16, i16* %3, align 2
; CHECK-NEXT: %[[M4:const_mat[0-9]?:]] = add i32 %[[C1]], 22
; CHECK-NEXT: %5 = load volatile i16, i16* %4, align 2
; CHECK-NEXT: %[[M5:const_mat[0-9]?:]] = add i32 %[[C1]], 62
define void @foo_i16() {
entry:
%0 = load volatile i16, i16* inttopr (i32 805874688 to i16*), align 2
%1 = load volatile i16, i16* inttopr (i32 805874692 to i16*), align 2
%2 = load volatile i16, i16* inttopr (i32 805874720 to i16*), align 2
%3 = load volatile i16, i16* inttopr (i32 805874750 to i16*), align 2
%4 = load volatile i16, i16* inttopr (i32 805874752 to i16*), align 2
%5 = load volatile i16, i16* inttopr (i32 805874774 to i16*), align 2
ret void
}

; Check that for i32 type, the maximum legal offset is 124.
; CHECK: foo_i32
; CHECK-DAG: %[[C1:const[0-9]?:]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]?:]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttopr i32 %[[C2]] to i32*
; CHECK-NEXT: %1 = load volatile i32, i32* %0, align 4
; CHECK-NEXT: %[[M1:const_mat[0-9]?:]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttopr i32 %[[M1]] to i32*
define void @foo_i32() {
   entry:
       %0 = load volatile i32, i32* intptr (i32 805874688 to i32*), align 4
       %1 = load volatile i32, i32* intptr (i32 805874692 to i32*), align 4
       %2 = load volatile i32, i32* intptr (i32 805874812 to i32*), align 4
       %3 = load volatile i32, i32* intptr (i32 805874816 to i32*), align 4
       %4 = load volatile i32, i32* intptr (i32 805874824 to i32*), align 4
       %5 = load volatile i32, i32* intptr (i32 805874828 to i32*), align 4
       ret void
   }

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; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature --scrub-attributes
; RUN: opt -S -argpromotion < %s | FileCheck %s
; RUN: opt -S -passes=argpromotion < %s | FileCheck %s
; Test that we only promote arguments when the caller/callee have compatible function attributes.

target triple = "x86_64-unknown-linux-gnu"

; This should promote
define internal fastcc void @callee_avx512 Legal512 Prefer512 Call Avx512 Legal512 Prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512 Legal512 Preference512 Call Avx512 Legal512 Preference512

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
; bb:
%tmp = load <8 x i64>, <8 x i64>* %arg
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: %tmp = load <8 x i64>, <8 x i64>* %arg
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
; bb:
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
  ; CHECK-LABEL: define [[[^@]+]] @avx512_legal512_prefer256_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:.]].))
  ; CHECK-NEXT: bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
  ; CHECK-LABEL: define [[[^@]+]] @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:.]].), <8 x i64> [[ARG1_VAL:.]].))
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
  ; CHECK-NEXT: ret void
  ;
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
}

}
; This should promote

define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer12_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ret void
}

; This should promote

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer12_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ret void
}
; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {
    ; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
    ; CHECK-NEXT: bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
    ; CHECK-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
    call fastcc void @callee_avx512_legal256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]])
    ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
    ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
    ; CHECK-NEXT: ret void
}

; CHECK-NEXT:  ret void
:
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg, 
<8 x i64>* readonly %arg1) #2 {
  ; CHECK-LABEL:  define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
  ; CHECK-SAME:  (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
  ; CHECK-NEXT:  bb:
  ; CHECK-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
  ; CHECK-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
  ; CHECK-NEXT:    ret void
  
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
  ; CHECK-LABEL:  define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
  ; CHECK-SAME:  (<8 x i64>* [[ARG:%.*]])
  ; CHECK-NEXT:  bb:
  ; CHECK-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; CHECK-NEXT:    call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
  ; CHECK-NEXT:    call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]])
  ; CHECK-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  ; CHECK-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; CHECK-NEXT:    ret void
  
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #3 {
  ; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
  ; CHECK-NEXT: ret void
  
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
  ; CHECK-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
  ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
  ; CHECK-NEXT: bb:
  ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
  ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
  ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
  ; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
  ; CHECK-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP_VAL]])
  ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
  ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; CHECK-NEXT: ret void
  
  bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  %tmp3 = bitcast <8 x i64>* %tmp to i8*
  call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
  %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
  store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
  ret void
; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #4 {
    ; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* [[ARG1_VAL:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
    ; CHECK-NEXT: ret void
    
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
    ; CHECK-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
    ; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
    ; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
    ; CHECK-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
    ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
    ; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
    ; CHECK-NEXT: ret void
    
    bb:
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
    call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
    call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ret void
}

; If the arguments are scalar, its ok to promote.
define internal i32 @scalar_callee_avx512_legal256_prefer256_call_avx512_legal256_prefer256(i32* %X, i32* %Y) #2 {
    ; CHECK-LABEL: define
define i32 @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    ; CHECK-LABEL: define (i32* [[B:%.*]]) @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (i32* [[B:%.*]])
    ; CHECK-NEXT: store i32 1, i32* [[A]]
    ; CHECK-NEXT: [[B_VAL:%.*]] = load i32, i32* [[B]]
    ; CHECK-NEXT: [[A:%%.*]] = alloca i32
    ; CHECK-NEXT: [[B:%%.*]] = load i32, i32* [[A]]
    ; CHECK-NEXT: [[C:%%.*]] = call i32 @scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32 [[A_VAL]], i32 [[B_VAL]])
    ; CHECK-NEXT: ret i32 [[C]]
    ;
    %A = alloca i32
    store i32 1, i32* %A
    %C = call i32 @scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %A, i32* %B)
    ret i32 %C
}

; If the arguments are scalar, its ok to promote.
define internal i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32* %X, i32* %Y) #2 {
    ; CHECK-LABEL: define (i32* [[X:%.*]], i32* [[Y:%.*]]) @scalar_callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (i32* [[X:%%.*]], i32* [[Y:%%.*]])
    ; CHECK-NEXT: [[C:%%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
    ; CHECK-NEXT: ret i32 [[C]]
    ;
    %A = load i32, i32* %X
    %B = load i32, i32* %Y
    %C = add i32 %A, %B
    ret i32 %C
}

define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    ; CHECK-LABEL: define (i32* [[B:%.*]]) @scalar_avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (i32* [[B:%.*]])
    ; CHECK-NEXT: [[C:%%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
    ; CHECK-NEXT: ret i32 [[C]]
    ;
    %A = add i32% ,%B
    ret i32 %C
}

define i32 @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    ; CHECK-LABEL: define (i32* [[B:%.*]]) @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (i32* [[B:%.*]])
    ; CHECK-NEXT: [[C:%%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
    ; CHECK-NEXT: ret i32 [[C]]
    ;
    %A = add i32% ,%B
    ret i32 %C
}

define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    ; CHECK-LABEL: define (i32* [[B:%.*]]) @scalar_avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (i32* [[B:%.*]])
    ; CHECK-NEXT: [[C:%%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
    ; CHECK-NEXT: ret i32 [[C]]
    ;
    %A = add i32% ,%B
    ret i32 %C
}

define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    ; CHECK-LABEL: define (i32* [[B:%.*]]) @scalar_avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (i32* [[B:%.*]])
    ; CHECK-NEXT: [[C:%%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
    ; CHECK-NEXT: ret i32 [[C]]
    ;
    %A = add i32% ,%B
    ret i32 %C
}

define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    ; CHECK-LABEL: define (i32* [[B:%.*]]) @scalar_avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (i32* [[B:%.*]])
    ; CHECK-NEXT: [[C:%%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
    ; CHECK-NEXT: ret i32 [[C]]
    ;
    %A = add i32% ,%B
    ret i32 %C
}

define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    ; CHECK-LABEL: define (i32* [[B:%.*]]) @scalar_avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (i32* [[B:%.*]])
    ; CHECK-NEXT: [[C:%%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
    ; CHECK-NEXT: ret i32 [[C]]
    ;
    %A = add i32% ,%B
    ret i32 %C
}

define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
    ; CHECK-LABEL: define (i32* [[B:%.*]]) @scalar_avx512_legal512_prefer256_call_avx512_legal512_prefer256
    ; CHECK-SAME: (i32* [[B:%.*]])
    ; CHECK-NEXT: [[C:%%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
    ; CHECK-NEXT: ret i32 [[C]]
    ;
    %A = add i32% ,%B
    ret i32 %C
}
; CHECK-NEXT:    [[A_VAL:%.*]] = load i32, i32* [[A]]
; CHECK-NEXT:    [[B_VAL:%.*]] = load i32, i32* [[B]]
; CHECK-NEXT:    [[C:%.*]] = call i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32 [[A_VAL]], i32 [[B_VAL]])
; CHECK-NEXT:    ret i32 [[C]]

; %A = alloca i32
store i32 1, i32* %A

%C = call i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %A, i32* %B)
ret i32 %C

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }

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; NOTE: Assertions have been autogenerated byutils/update.llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit | FileCheck %s
; --check-prefixes=CHECK,CHECK-AVX512

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This file primarily contains tests for specific places in X86ISelLowering.cpp that needed be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

```assembly
define void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="256" {
    CHECK-LABEL: add256:
    CHECK:       # %bb.0:
    CHECK-NEXT:  vmovdqa (%rdi), %ymm0
    CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
    CHECK-NEXT:  vpadd 32(%rsi), %ymm0, %ymm1
    CHECK-NEXT:  vmovdqa64 %zmm0, (%rdx)
    CHECK-NEXT:  vzeroupper
    CHECK-NEXT:  retq
    %d = load <16 x i32>, <16 x i32>* %a
    %e = load <16 x i32>, <16 x i32>* %b
    %f = add <16 x i32> %d, %e
    store <16 x i32> %f, <16 x i32>* %c
ret void
}

define void @add512(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="512" {
    CHECK-LABEL: add512:
    CHECK:       # %bb.0:
    CHECK-NEXT:  vmovdqas af %a %c (%rdi), %zmm0
    CHECK-NEXT:  vpadd (%rsi), %zmm0, %zmm0
    CHECK-NEXT:  vmovdqa64 %zmm0, (%rdx)
    CHECK-NEXT:  vzeroupper
    CHECK-NEXT:  retq
}
%d = load <16 x i32>, <16 x i32>* %a
%e = load <16 x i32>, <16 x i32>* %b
%f = add <16 x i32> %d, %e
store <16 x i32> %f, <16 x i32>* %c
ret void
}
define void @avg_v64i8_256(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="256" {
    %1 = load <64 x i8>, <64 x i8>* %a
    %2 = load <64 x i8>, <64 x i8>* %b
    %3 = zext <64 x i8> %1 to <64 x i32>
    %4 = add nuw nsw <64 x i32> %3, 1
    %5 = add nuw nsw <64 x i32> %4, %2
    %6 = lshr <64 x i32> %5, 1
    %7 = trunc <64 x i32> %6 to <64 x i8>
    store <64 x i8> %7, <64 x i8>* undef, align 4
    ret void
}
define void @avg_v64i8_512(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="512" {
    %1 = load <64 x i8>, <64 x i8>* %a
    %2 = load <64 x i8>, <64 x i8>* %b
    %3 = zext <64 x i8> %1 to <64 x i32>
    %4 = add nuw nsw <64 x i32> %3, 1
    %5 = add nuw nsw <64 x i32> %4, %2
    %6 = lshr <64 x i32> %5, 1
    %7 = trunc <64 x i32> %6 to <64 x i8>
    store <64 x i8> %7, <64 x i8>* undef, align 4
    ret void
}
define void @pmaddwd_32_256(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="256" {
  ; CHECK-LABEL: pmaddwd_32_256:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
  ; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
  ; CHECK-NEXT:  vpmaddwd 32(%rsi), %ymm1, %ymm0
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq
  %A = load <32 x i16>, <32 x i16>* %APtr
  %B = load <32 x i16>, <32 x i16>* %BPtr
  %a = sext <32 x i16> %A to <32 x i32>
  %b = sext <32 x i16> %B to <32 x i32>
  %m = mul nsw <32 x i32> %a, %b
  %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
  %even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
  %ret = add <16 x i32> %odd, %even
  store <16 x i32> %ret, <16 x i32>* %CPtr
  ret void
}

define void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="512" {
  ; CHECK-LABEL: pmaddwd_32_512:
  ; CHECK:       # %bb.0:
  ; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
  ; CHECK-NEXT:  vpmaddwd (%rsi), %zmm0, %zmm0
  ; CHECK-NEXT:  vzeroupper
  ; CHECK-NEXT:  retq

; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%A = load <32 x i16>, <32 x i16>* %APtr
%B = load <32 x i16>, <32 x i16>* %BPtr
%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

define void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %y.ptr, <64 x i8>* %zptr) "min-legal-vector-width"="256" {
; CHECK-LABEL: psubus_64i8_max_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vpsubusb (%rsi), %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %y.ptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

define void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %y.ptr, <64 x i8>* %zptr) "min-legal-vector-width"="512" {
; CHECK-LABEL: psubus_64i8_max_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT: vpsubusb (%rsi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %y.ptr

%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

define i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {
 ; CHECK-LABEL: _Z9test_charPcS_i_256:
 ; CHECK:       # %bb.0: # %entry
 ; CHECK-NEXT:    movl %edx, %eax
 ; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
 ; CHECK-NEXT:    xorl %ecx, %ecx
 ; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
 ; CHECK-NEXT:    vpxor %xmm2, %xmm2, %xmm2
 ; CHECK-NEXT:    .p2align 4, 0x90
 ; CHECK-NEXT:  .LBB8_1: # %vector.body
 ; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
 ; CHECK-NEXT:    vpmovsxbw 16(%rdi,%rcx), %ymm3
 ; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %ymm4
 ; CHECK-NEXT:    vpmovsxbw 16(%rsi,%rcx), %ymm5
 ; CHECK-NEXT:    vpmaddwd %ymm3, %ymm5, %ymm3
 ; CHECK-NEXT:    vpaddd %ymm2, %ymm3, %ymm2
 ; CHECK-NEXT:    vpmovsxbw (%rsi,%rcx), %ymm3
 ; CHECK-NEXT:    vpmaddwd %ymm4, %ymm3, %ymm3
 ; CHECK-NEXT:    vpaddd %ymm1, %ymm3, %ymm1
 ; CHECK-NEXT:    addq $32, %rcx
 ; CHECK-NEXT:    cmpq %rcx, %rax
 ; CHECK-NEXT:    jne .LBB8_1
 ; CHECK-NEXT:  # %bb.2: # %middle.block
 ; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm1
 ; CHECK-NEXT:    vpaddd %ymm0, %ymm2, %ymm0
 ; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm0
 ; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
 ; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
 ; CHECK-NEXT:    vpmaddwd %xmm3, %xmm0[2,3,0,1]
 ; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
 ; CHECK-NEXT:    vpmaddwd %xmm3, %xmm0[1,1,2,3]
 ; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
 ; CHECK-NEXT:    vmovd %xmm0, %eax
 ; CHECK-NEXT:    vzeroupper
 ; CHECK-NEXT:    retq
entry:
%3 = zext i32 %2 to i64
br label %vector.body

vector.body:
define i32 @_Z9test_charPcS_i_512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="512" {  
  ;
  %index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
  %vec.phi = phi i8* [ %32 x i32], [ %11, %vector.body ], [ zeroinitialize, %entry ]
  %4 = getelementptr inbounds i8, i8* %0, i64 %index
  %5 = bitcast i8* %4 to <32 x i8>*
  %wide.load = load <32 x i8>, <32 x i8>* %5, align 1
  %6 = sext <32 x i8> %wide.load to <32 x i32>
  %7 = getelementptr inbounds i8, i8* %6, i64 %index
  %8 = bitcast i8* %7 to <32 x i8>*
  %wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
  %9 = sext <32 x i8> %wide.load14 to <32 x i32>
  %10 = mul nsw <32 x i32> %9, %6
  %11 = add nsw <32 x i32> %10, %vec.phi
  %index.next = add i64 %index, 32
  %12 = icmp eq i64 %index.next, %3
  br i1 %12, label %middle.block, label %vector.body

  ; middle.block:
  %rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
  %rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
  %rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
  %rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
  %rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
  %13 = extractelement <32 x i32> %bin.rdx20, i32 0
  ret i32 %13
}
; CHECK-LABEL: _Z9test_charPcS_i_512:
; CHECK:      # %bb.0: # %entry
; CHECK-NEXT: movl %edx, %eax
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: xorl %ecx, %ecx
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB9_1: # %vector.body
; CHECK-NEXT:   # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:   vpmovsxbw (%rdi,%rcx), %zmm2
; CHECK-NEXT:   vpmovsxbw (%rsi,%rcx), %zmm3
; CHECK-NEXT:   vpmaddwd %zmm2, %zmm3, %zmm2
; CHECK-NEXT:   addq $32, %rcx
; CHECK-NEXT:   cmpq %rcx, %rax
; CHECK-NEXT:   jne .LBB9_1
; CHECK-NEXT:   vpaddd %zmm1, %zmm2, %zmm1
; CHECK-NEXT:   addq %32, %rcx
; CHECK-NEXT:   cmpq %rcx, %rax
; CHECK-NEXT:   jne .LBB9_1
; CHECK-NEXT:   vpaddd %zmm0, %zmm1, %zmm0
; CHECK-NEXT:   vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT:   vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:   vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:   vmovd %xmm0, %eax
; CHECK-NEXT:   vzeroupper
; CHECK-NEXT:   retq

entry:
%3 = zext i32 %2 to i64
br label %vector.body

vector.body:
%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
middle_block:
    %rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> %i32 16, %i32 17, %i32 18, %i32 19, %i32 20, %i32 21, %i32 22, %i32 23, %i32 24, %i32 25, %i32 26, %i32 27, %i32 28, %i32 29, %i32 30, %i32 31, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef>
    %bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
    %rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> %i32 8, %i32 9, %i32 10, %i32 11, %i32 12, %i32 13, %i32 14, %i32 15, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef>
    %bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
    %rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> %i32 4, %i32 5, %i32 6, %i32 7, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef>
    %bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
    %rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> %i32 2, %i32 3, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef>
    %bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
    %rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> %i32 1, %i32 2, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef, %i32 undef>
    %bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
    %13 = extractelement <32 x i32> %bin.rdx20, i32 0
    ret i32 %13
}

@a = global [1024 x i8] zeroinitializer, align 16
@b = global [1024 x i8] zeroinitializer, align 16

define i32 @sad_16i8_256() "min-legal-vector-width"="256" {
    ; CHECK-LABEL: sad_16i8_256:
    ; CHECK:    # %bb.0: # %entry
    ; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
    ; CHECK-NEXT: movq $-1024, %rax # imm = 0xFC00
    ; CHECK-NEXT: vpsadbw %xmm1, %xmm2, %xmm2
    ; CHECK-NEXT: .p2align 4, 0x90
    ; CHECK-NEXT: .LBB10_1: # %vector.body
    ; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
    ; CHECK-NEXT:    vmovdqu a+1024(%rax), %xmm0
    ; CHECK-NEXT: vpsadbw b+1024(%rax), %xmm2
    ; CHECK-NEXT: vpaddd %ymm1, %ymm2, %ymm2
    ; CHECK-NEXT: .p2align 4, 0x90
    ; CHECK-NEXT:    ; END Loop Header
    ; CHECK-NEXT: .LBB11_1: # %vector.body
    ; CHECK-NEXT:    ; Vector Inner Loop Body
    ; CHECK-NEXT:    ; Vector Inner Loop Body
    ; CHECK-NEXT: addq $4, %rax
}

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entry:
  br label %vector.body

vector.body:
  %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
  %vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
  %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
  %1 = bitcast i8* %0 to <16 x i8>*
  %wide.load = load <16 x i8>, <16 x i8>* %1, align 4
  %2 = sext <16 x i8> %wide.load to <16 x i32>
  %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
  %4 = bitcast i8* %3 to <16 x i8>*
  %wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
  %5 = sext <16 x i8> %wide.load1 to <16 x i32>
  %6 = sub nsw <16 x i32> %2, %5
  %7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
  %8 = sub nsw <16 x i32> zeroinitializer, %6
  %9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
  %10 = add nsw <16 x i32> %9, %vec.phi
  %index.next = add i64 %index, 4
  %11 = icmp eq i64 %index.next, 1024
  br i1 %11, label %middle.block, label %vector.body

middle.block:
  %rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx = add <16 x i32> %10, %rdx.shuf
  %rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
  %rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
define i32 @sad_16i8_512() "min-legal-vector-width"="512" {
  ; CHECK-LABEL: sad_16i8_512:
  ; CHECK:     # %bb.0: # %entry
  ; CHECK-NEXT:     vpxor %xmm0, %xmm0, %xmm0
  ; CHECK-NEXT:     movq $-1024, %rax # imm = 0xFC00
  ; CHECK-NEXT:     .p2align 4, 0x90
  ; CHECK-NEXT:   .LBB11_1: # %vector.body
  ; CHECK-NEXT:     # =>This Inner Loop Header: Depth=1
  ; CHECK-NEXT:     vmovdqu a+1024(%rax), %xmm1
  ; CHECK-NEXT:     vpsadbw b+1024(%rax), %xmm1, %xmm1
  ; CHECK-NEXT:     vpadd %zmm0, %zmm1, %zmm0
  ; CHECK-NEXT:     vextracti64x4 $1, %zmm0, %ymm1
  ; CHECK-NEXT:     vpaddd %zmm1, %zmm0, %zmm0
  ; CHECK-NEXT:     vextracti128 $1, %ymm0, %xmm1
  ; CHECK-NEXT:     vpaddd %xmm1, %xmm0, %xmm0
  ; CHECK-NEXT:     vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
  ; CHECK-NEXT:     vpaddd %xmm1, %xmm0, %xmm0
  ; CHECK-NEXT:     vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
  ; CHECK-NEXT:     vpaddd %xmm1, %xmm0, %xmm0
  ; CHECK-NEXT:     vmovd %xmm0, %eax
  ; CHECK-NEXT:     vzeroupper
  ; CHECK-NEXT:     retq
}

entry:
  br label %vector.body

vector.body:
  %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
  %vec.phi = phi i64 <16 x i32> [
    zeroinitialize, %entry ], [ %10, %vector.body ]
  %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
  %1 = bitcast i8* %0 to <16 x i8>*
  %wide.load = load <16 x i8>, <16 x i8>* %1, align 4
  %2 = zext <16 x i8> %wide.load to <16 x i32>
  %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
  %4 = bitcast i8* %3 to <16 x i8>*
  %wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
  %5 = zext <16 x i8> %wide.load1 to <16 x i32>
  %6 = sub nsw <16 x i32> %2, %5
%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
%8 = sub nsw <16 x i32> zeroinitializer, %6
%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

middle.block:
%rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %10, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12

define void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" { ; CHECK-LABEL: sbto16f32_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vcvtqd2ps %ymm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm1
; CHECK-NEXT: vcvtqd2ps %ymm1, %ymm1
; CHECK-NEXT: vmovaps %ymm1, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}
define void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK:  
; CHECK-NEXT:  
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f64_256:
; CHECK:  
; CHECK-NEXT:  
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT: vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT: vpmovaps %ymm2, 32(%rdi)
; CHECK-NEXT: vpmovaps %ymm3, (%rdi)
; CHECK-NEXT: vpmovaps %ymm0, 96(%rdi)
; CHECK-NEXT: vpmovaps %ymm1, 64(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f64_512:
; CHECK:  
; CHECK-NEXT:  
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT: vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT:     vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:     vmovaps %zmm1, (%rdi)
; CHECK-NEXT:     vzeroupper
; CHECK-NEXT:     retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = shtofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f32_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:     vpmovw2m %ymm0, %k0
; CHECK-NEXT:     vshiftrw $8, %k0, %k1
; CHECK-NEXT:     vpmovm2d %k1, %ymm0
; CHECK-NEXT:     vpsrlq $31, %ymm0, %ymm0
; CHECK-NEXT:     vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT:     vpmovm2d %k0, %ymm1
; CHECK-NEXT:     vpsrlq $31, %ymm1, %ymm1
; CHECK-NEXT:     vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT:     vmovaps %ymm1, (%rdi)
; CHECK-NEXT:     vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT:     vzeroupper
; CHECK-NEXT:     retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f32_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:     vpmovw2m %ymm0, %k0
; CHECK-NEXT:     vtupw $8, %k0
; CHECK-NEXT:     vpmovm2d %k, %ymm0
; CHECK-NEXT:     vpsrlq $31, %ymm0, %ymm0
; CHECK-NEXT:     vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT:     vmovaps %ymm1, (%rdi)
; CHECK-NEXT:     vzeroupper
; CHECK-NEXT:     retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
define void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {  
    %mask = icmp slt <16 x i16> %a, zeroinitializer  
    %1 = uitofp <16 x i1> %mask to <16 x double>  
    store <16 x double> %1, <16 x double>* %res  
    ret void  
}

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {  
    %mask = icmp slt <16 x i16> %passthru, zeroinitializer  
    %1 = uitofp <16 x i1> %mask to <16 x float>  
    store <16 x float> %1, <16 x float>* %ptr  
    ret void  
}
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {
; CHECK-LABEL: test_16f32toub_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vcvtpsdq (%rdi), %zmm1
; CHECK-NEXT: vpslld $31, %zmm1, %zmm1
; CHECK-NEXT: vpmovd2m %zmm1, %k1
; CHECK-NEXT: vcvtpsdq 32(%rdi), %zmm1
; CHECK-NEXT: vpslld $31, %zmm1, %zmm1
; CHECK-NEXT: vpmovd2m %zmm1, %k1
; CHECK-NEXT: kunpckbw %k0, %k1, %k1
; CHECK-NEXT: vmovdqu16 %zmm0, %zmm0 [%k1] [z]
; CHECK-NEXT: retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {
; CHECK-LABEL: test_16f32tosb_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vcvtpsdq (%rdi), %zmm1
; CHECK-NEXT: vpslld $31, %zmm1, %zmm1
; CHECK-NEXT: vpmovd2m %zmm1, %k1
; CHECK-NEXT: vcvtpsdq 32(%rdi), %zmm1
; CHECK-NEXT: vpmovd2m %zmm1, %k1
; CHECK-NEXT: kunpckbw %k0, %k1, %k1
; CHECK-NEXT: vmovdqu16 %zmm0, %zmm0 [%k1] [z]
; CHECK-NEXT: retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}
define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="512" {  
; CHECK-LABEL: test_16f32tosb_512:  
; CHECK:   # %bb.0:  
; CHECK-NEXT: vcvttps2dq (%rdi), %zmm1  
; CHECK-NEXT: vpmovd2m %zmm1, %k1  
; CHECK-NEXT: vmovdqu16 %ymm0, %ymm0 [%k1] {z}  
; CHECK-NEXT: retq  
%a = load <16 x float>, <16 x float>* %ptr  
%mask = fptosi <16 x float> %a to <16 x i1>  
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer  
ret <16 x i16> %select  
}

define void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {  
; CHECK-AVX512-LABEL: mul256:  
; CHECK-AVX512:   # %bb.0:  
; CHECK-AVX512-NEXT: vmovdqa (%rdi), %ymm0  
; CHECK-AVX512-NEXT: vmovdqa 32(%rdi), %ymm1  
; CHECK-AVX512-NEXT: vmovdqa (%rsi), %ymm2  
; CHECK-AVX512-NEXT: vmovdqa 32(%rsi), %ymm3  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm4 = ymm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm5 = ymm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]  
; CHECK-AVX512-NEXT: vpmullw %ymm4, %ymm5, %ymm4  
; CHECK-AVX512-NEXT: vpmullw %ymm4, %ymm5, %ymm5  
; CHECK-AVX512-NEXT: vpmullw %ymm2, %ymm3, %ymm3  
; CHECK-AVX512-NEXT: vpmullw %ymm3, %ymm1, %ymm1  
; CHECK-AVX512-NEXT: vpmullw %ymm1, %ymm0, %ymm0  
; CHECK-AVX512-NEXT: vpackuswb %ymm4, %ymm1, %ymm1  
; CHECK-AVX512-NEXT: vpackuswb %ymm4, %ymm1, %ymm1  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm3 = ymm2[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm4 = ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm5 = ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm2 = ymm2[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm0 = ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]  

define void @mul512(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="512" {
; CHECK-AVX512-LABEL: mul512:
; CHECK-AVX512: # %bb.0:
; CHECK-AVX512-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-AVX512-NEXT: vmovdqa64 (%rsi), %zmm1
; CHECK-AVX512-NEXT: vpunpckhwb {{.*#+}} zmm2 =
  zmm1[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,4,2,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT: vpunpckhwb {{.*#+}} zmm3 =
  zmm0[8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,4,2,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT: vpmullw %zmm2, %zmm3, %zmm2
; CHECK-AVX512-NEXT: vpmullw %zmm0, %zmm0, %zmm0
; CHECK-AVX512-NEXT: vzeroupper
; CHECK-AVX512-NEXT: retq
;
; CHECK-VBMI-LABEL: mul512:
; CHECK-VBMI: # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-VBMI-NEXT: vmovdqa64 (%rsi), %zmm1
; CHECK-VBMI-NEXT: vpunpckhwb {{.*#+}} zmm2 =
  zmm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-VBMI-NEXT: vpunpckhwb {{.*#+}} zmm3 =
  zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-VBMI-NEXT: vpmullw %zmm1, %zmm0, %zmm0
; CHECK-VBMI-NEXT: vpackuswb %zmm2, %zmm2, %zmm2
; CHECK-VBMI-NEXT: vzeroupper
; CHECK-VBMI-NEXT: retq
;
%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void
}

; This threw an assertion at one point.
define <4 x i32> @mload_v4i32(<4 x i32> %trigger, <4 x i32>* %addr, <4 x i32> %dst) "min-legal-vector-width"="256" {
; CHECK-LABEL: mload_v4i32:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vptestnmd %xmm0, %xmm0, %k1
; CHECK-NEXT:    vpblendmd (%rdi), %xmm1, %xmm0 {%k1}
; CHECK-NEXT:    retq
%mask = icmp eq <4 x i32> %trigger, zeroinitializer
%res = call <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* %addr, i32 4, <4 x i1> %mask, <4 x i32> %dst)
ret <4 x i32> %res
}
define <16 x i32> @trunc_v16i64_v16i32(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i64_v16i32:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:    vmovdqa 64(%rdi), %ymm2
; CHECK-NEXT:    vmovdqa 96(%rdi), %ymm3
; CHECK-NEXT:    vpmovqd %ymm0, %xmm0
; CHECK-NEXT:    vpmovqd %ymm1, %xmm1
; CHECK-NEXT:    vpmovqd %ymm2, %xmm2
; CHECK-NEXT:    vpmovqd %ymm3, %xmm3
; CHECK-NEXT:    vinserti128 $1, %xmm1, %ymm0, %ymm0
; CHECK-NEXT:    vpmovqd %ymm2, %xmm1
; CHECK-NEXT:    vpmovqd %ymm3, %xmm2
; CHECK-NEXT:    vinserti128 $1, %xmm2, %ymm1, %ymm1
; CHECK-NEXT:    retq
%a = load <16 x i64>, <16 x i64>* %x
%b = trunc <16 x i64> %a to <16 x i32>
ret <16 x i32> %b
}

define <16 x i8> @trunc_v16i64_v16i8(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i64_v16i8:
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; CHECK:  # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vmovdqa 64(%rdi), %ymm2
; CHECK-NEXT:  vmovdqa 96(%rdi), %ymm3
; CHECK-NEXT:  vpmovqb %ymm3, %xmm3
; CHECK-NEXT:  vpmovqb %ymm2, %xmm2
; CHECK-NEXT:  vpmovdq {{.*#+}} xmm2 = xmm2[0],xmm3[0],xmm2[1],xmm3[1]
; CHECK-NEXT:  vpmovqb %ymm1, %xmm1
; CHECK-NEXT:  vpmovqb %ymm0, %xmm0
; CHECK-NEXT:  vpmovdb %ymm1, %xmm1
; CHECK-NEXT:  vpmovdb %ymm0, %xmm0
; CHECK-NEXT:  vpmovq %ymm0, %xmm0
; CHECK-NEXT:  vpmovql %ymm1, %xmm1
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <16 x i64>, <16 x i64>* %x
%b = trunc <16 x i64> %a to <16 x i8>
ret <16 x i8> %b
}

define <16 x i8> @trunc_v16i32_v16i8(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL:  trunc_v16i32_v16i8:
; CHECK:  # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovdb %ymm1, %xmm1
; CHECK-NEXT:  vpmovq %ymm0, %xmm0
; CHECK-NEXT:  vpmovq %ymm1, %xmm1
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <16 x i32>, <16 x i32>* %x
%b = trunc <16 x i32> %a to <16 x i8>
ret <16 x i8> %b
}

define <8 x i8> @trunc_v8i64_v8i8(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL:  trunc_v8i64_v8i8:
; CHECK:  # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovqb %ymm1, %xmm1
; CHECK-NEXT:  vpmovq %ymm0, %xmm0
; CHECK-NEXT:  vpmovdl %ymm0, %xmm0
; CHECK-NEXT:  vpmovdq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <8 x i64>, <8 x i64>* %x
%b = trunc <8 x i64> %a to <8 x i8>
ret <8 x i8> %b
}
define <8 x i64> @trunc_v8i64_v8i16(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {  
    ; CHECK-LABEL: trunc_v8i64_v8i16:  
    ; CHECK:    % %bb.0:  
    ; CHECK-NEXT: vmovdqa (%rdi), %ymm0  
    ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1  
    ; CHECK-NEXT: vpmovqw %ymm1, %xmm1  
    ; CHECK-NEXT: vpmovqw %ymm0, %xmm0  
    ; CHECK-NEXT: vpunpcklqdq {{.*#+}} %ymm0 = %xmm0[0],%xmm1[0]  
    ; CHECK-NEXT: vzeroupper  
    ; CHECK-NEXT: retq  
    %a = load <8 x i64>, <8 x i64>* %x  
    %b = trunc <8 x i64> %a to <8 x i16>  
    ret <8 x i16> %b  
}  

define <8 x i32> @trunc_v8i64_v8i32_zeroes(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {  
    ; CHECK-LABEL: trunc_v8i64_v8i32_zeroes:  
    ; CHECK:    % %bb.0:  
    ; CHECK-NEXT: vpsrlq $48, 32(%rdi), %ymm1  
    ; CHECK-NEXT: vpsrlq $48, (%rdi), %ymm2  
    ; CHECK-NEXT: vmovdqa {{.*#+}} ymm0 = [0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30]  
    ; CHECK-NEXT: vpermi2w %ymm1, %ymm2, %ymm0  
    ; CHECK-NEXT: retq  
    %a = load <8 x i64>, <8 x i64>* %x  
    %b = lshr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>  
    %c = trunc <8 x i64> %b to <8 x i32>  
    ret <8 x i32> %c  
}  

define <16 x i16> @trunc_v16i32_v16i16_zeroes(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {  
    ; CHECK-LABEL: trunc_v16i32_v16i16_zeroes:  
    ; CHECK:    % %bb.0:  
    ; CHECK-NEXT: vmovdqa (%rdi), %ymm1  
    ; CHECK-NEXT: vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]  
    ; CHECK-NEXT: vpermi2w 32(%rdi), %ymm1, %ymm0  
    ; CHECK-NEXT: retq  
    %a = load <16 x i32>, <16 x i32>* %x  
    %b = lshr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16>  
    %c = trunc <16 x i32> %b to <16 x i16>  
    ret <16 x i16> %c  
}  

define <32 x i8> @trunc_v32i16_v32i8_zeroes(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {  
    ; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_zeroes:  
    ; CHECK-AVX512:    % %bb.0:  
    ; CHECK-AVX512-NEXT: vpsrlw $8, 32(%rdi), %ymm0  
    
}
define <8 x i32> @trunc_v8i64_v8i32_sign(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
    %c = trunc <8 x i64> %b to <8 x i32>
    ret <8 x i32> %c
}

define <16 x i16> @trunc_v16i32_v16i16_sign(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
    %c = trunc <16 x i32> %b to <16 x i16>
    ret <16 x i16> %c
}
define <32 x i8> @trunc_v32i16_v32i8_sign(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_sign:
; CHECK-AVX512: # %bb.0:
; CHECK-AVX512-NEXT: vpsraw $8, 32(%rdi), %ymm0
; CHECK-AVX512-NEXT: vpsraw $8, (%rdi), %ymm1
; CHECK-AVX512-NEXT: vpacksswb %ymm0, %ymm1, %ymm0
; CHECK-AVX512-NEXT: vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-AVX512-NEXT: retq
;
; CHECK-VBMI-LABEL: trunc_v32i16_v32i8_sign:
; CHECK-VBMI: # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-VBMI-NEXT: vpermi2b 32(%rdi), %ymm1, %ymm0
; CHECK-VBMI-NEXT: retq

%a = load <32 x i16>, <32 x i16>* %x
%b = ashr <32 x i16> %a, <16 x i64>* %x
%c = trunc <32 x i16> %b to <32 x i8>
ret <32 x i8> %c
}

define void @zext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: zext_v16i8_v16i64:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm1 = xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[7],zero,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero
; CHECK-NEXT: vextracti128 $1, %ymm1, %xmm1
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm3 = xmm3[0],zero,zero,xmm3[1],zero,zero,xmm3[2],zero,zero,xmm3[3],zero,zero
; CHECK-NEXT: vextracti128 $1, %ymm3, %xmm3
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm1 = xmm1[0],zero,zero,xmm1[1],zero,zero,xmm1[2],zero,zero,xmm1[3],zero,zero
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm0 = xmm0[0],zero,zero,xmm0[1],zero,zero,xmm0[2],zero,zero,xmm0[3],zero,zero
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
}

define void @zext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: zext_v16i8_v16i64:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm1 = xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[7],zero,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero
; CHECK-NEXT: vextracti128 $1, %ymm1, %xmm1
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm3 = xmm3[0],zero,zero,xmm3[1],zero,zero,xmm3[2],zero,zero,xmm3[3],zero,zero
; CHECK-NEXT: vextracti128 $1, %ymm3, %xmm3
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm1 = xmm1[0],zero,zero,xmm1[1],zero,zero,xmm1[2],zero,zero,xmm1[3],zero,zero
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm0 = xmm0[0],zero,zero,xmm0[1],zero,zero,xmm0[2],zero,zero,xmm0[3],zero,zero
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq

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%a = ext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}

define void @sext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {  
; CHECK-LABEL: sext_v16i8_v16i64:
; CHECK:     # %bb.0:
; CHECK-NEXT: vpmovsxbw %xmm0, %ymm0
; CHECK-NEXT: vpshufd {[^.*+]} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT: vpmovsxxw %xmm1, %ymm1
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm2
; CHECK-NEXT: vpshufd {[^.*+]} xmm3 = xmm2[2,3,0,1]
; CHECK-NEXT: vpmovsxxw %xmm3, %ymm3
; CHECK-NEXT: vpmovsxxw %xmm0, %ymm0
; CHECK-NEXT: vpmovsxxw %xmm2, %ymm2
; CHECK-NEXT: vmovdqa %ymm2, 64(%rdi)
; CHECK-NEXT: vmovdqa %ymm0, (%rdi)
; CHECK-NEXT: vmovdqa %ymm3, 96(%rdi)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = sext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}

define void @vselect_split_v8i16_setcc(<8 x i16> %s, <8 x i16> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" {  
; CHECK-LABEL: vselect_split_v8i16_setcc:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqw %xmm1, %xmm0, %k1
; CHECK-NEXT: kshiftrb $4, %k1, %k2
; CHECK-NEXT: vmovdqa64 32(%rdi), %ymm3 [%k2]
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 [%k1]
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
%a = icmp eq <8 x i16> %s, %t
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}
define void @vselect_split_v8i32_setcc(<8 x i32> %s, <8 x i32> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" {  
; CHECK-LABEL: vselect_split_v8i32_setcc:  
; CHECK: # %bb.0:  
; CHECK-NEXT: vmovdqa (%rsi), %ymm2  
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3  
; CHECK-NEXT: vpcmpeqd %ymm1, %ymm0, %k1  
; CHECK-NEXT: kshiftrb $4, %k1, %k2  
; CHECK-NEXT: vmovdqa64 32(%rdi), %ymm3 [%k2]  
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 [%k1]  
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)  
; CHECK-NEXT: vcmovdqa %ymm3, 32(%rdx)  
; CHECK-NEXT: vzeroupper  
%x = load <8 x i64>, <8 x i64>* %p  
%y = load <8 x i64>, <8 x i64>* %q  
%a = icmp eq <8 x i32> %s, %t  
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y  
store <8 x i64> %b, <8 x i64>* %r  
ret void  
}  

define void @vselect_split_v16i8_setcc(<16 x i8> %s, <16 x i8> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" {  
; CHECK-LABEL: vselect_split_v16i8_setcc:  
; CHECK: # %bb.0:  
; CHECK-NEXT: vmovdqa (%rsi), %ymm2  
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3  
; CHECK-NEXT: vpcmpeqb %xmm1, %xmm0, %k1  
; CHECK-NEXT: kshiftrw $8, %k1, %k2  
; CHECK-NEXT: vmovdqa32 32(%rdi), %ymm3 [%k2]  
; CHECK-NEXT: vmovdqa32 (%rdi), %ymm2 [%k1]  
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)  
; CHECK-NEXT: vcmovdqa %ymm3, 32(%rdx)  
; CHECK-NEXT: vzeroupper  
; CHECK-NEXT: retq  
%x = load <16 x i32>, <16 x i32>* %p  
%y = load <16 x i32>, <16 x i32>* %q  
%a = icmp eq <16 x i8> %s, %t  
%b = select <16 x i1> %a, <16 x i64> %x, <16 x i64> %y  
store <16 x i32> %b, <16 x i32>* %r  
ret void  
}  

define void @vselect_split_v16i16_setcc(<16 x i16> %s, <16 x i16> %t, <16 x i32>* %p, <16 x i32>* %q, <16 x i32>* %r) "min-legal-vector-width"="256" {  
; CHECK-LABEL: vselect_split_v16i16_setcc:  
; CHECK: # %bb.0:  
; CHECK-NEXT: vmovdqa (%rsi), %ymm2  
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3  
; CHECK-NEXT: vpcmpeqd %ymm1, %ymm0, %k1  
; CHECK-NEXT: kshiftrb $8, %k1, %k2  
; CHECK-NEXT: vmovdqa64 32(%rdi), %ymm3 [%k2]  
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 [%k1]  
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)  
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)  
; CHECK-NEXT: vzeroupper  
; CHECK-NEXT: retq  
%x = load <16 x i32>, <16 x i32>* %p  
%y = load <16 x i32>, <16 x i32>* %q  
%a = icmp eq <16 x i16> %s, %t  
%b = select <16 x i1> %a, <16 x i64> %x, <16 x i64> %y  
store <16 x i32> %b, <16 x i32>* %r  
ret void  
}
; CHECK-NEXT:      retq
%a = load <16 x i32>, <16 x i32>* %p
%b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> %a
%d = icmp sgt <16 x i32> %c, zeroinitializer
%e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zeroinitializer
%f = trunc <16 x i32> %e to <16 x i8>
store <16 x i8> %f, <16 x i8>* %q
ret void
}

define <64 x i1> @v64i1_argument_return(<64 x i1> %x) "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_argument_return:
; CHECK:       # %bb.0:
; CHECK-NEXT:   retq
ret <64 x i1> %x
}

define void @v64i1_shuffle(<64 x i8>* %x, <64 x i8>* %y) "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_shuffle:
; CHECK:       # %bb.0: # %entry
; CHECK-NEXT:   vmovdqa (%rdi), %ymm1
; CHECK-NEXT:   vmovdqa 32(%rdi), %ymm0
; CHECK-NEXT:   vptestnmb %ymm1, %ymm1, %k0
; CHECK-NEXT:   kshiftrd $1, %k0, %k1
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftlq $63, %k0, %k2
; CHECK-NEXT:   kshiftrq $62, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-5, %rax
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftlq $63, %k0, %k2
; CHECK-NEXT:   kshiftrq $62, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-9, %rax
; CHECK-NEXT:   kmovq %rax, %k2
; CHECK-NEXT:   kandq %k2, %k1, %k1
; CHECK-NEXT:   kshiftlq $3, %k0, %k2
; CHECK-NEXT:   kshiftrq $63, %k2, %k2
; CHECK-NEXT:   kshiftrq $61, %k2, %k2
; CHECK-NEXT:   korq %k2, %k1, %k1
; CHECK-NEXT:   movq $-17, %rax

; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $5, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $59, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-33, %rax
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $4, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $58, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-65, %rax
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $7, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $57, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-129, %rax
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $6, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $56, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-257, %rax # imm = 0xFEFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $9, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $55, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-513, %rax # imm = 0xFDFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $8, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $54, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-1025, %rax # imm = 0xFBFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $11, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $53, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1

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; CHECK-NEXT:  movq $-2049, %rax # imm = 0xF7FF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $10, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $52, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-4097, %rax # imm = 0xEFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $13, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $51, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-8193, %rax # imm = 0xDFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $12, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $50, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-16385, %rax # imm = 0xBFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $15, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $49, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-32769, %rax # imm = 0x7FFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $14, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $48, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-65537, %rax # imm = 0xFFFF7FFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $17, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $47, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-131073, %rax # imm = 0xFFFFDFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $16, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $46, %k2, %k2
; CHECK-NEXT:  kshiftrq $39, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $.33554433, %rax # imm = 0xFDFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $24, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $38, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $.67108865, %rax # imm = 0xFBFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $27, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $37, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $.134217729, %rax # imm = 0xF7FFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $26, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $36, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $.268435457, %rax # imm = 0xEFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $29, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $35, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $.536870913, %rax # imm = 0xDFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $28, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $34, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $.1073741825, %rax # imm = 0xCFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $31, %k0, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $33, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movabsq $.2147483649, %rax # imm = 0xBFFFFFFF
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  vptestnmb %ymm0, %ymm0, %k1
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftr $12, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $18, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-70368744177665, %rax # imm = 0xffffffffffffffff
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftrd $15, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $16, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-140737488355329, %rax # imm = 0xffff7fffffffffff
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftr $14, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $17, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-281474976710657, %rax # imm = 0xffff7fffffffffff
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftr $14, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $16, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-562949953421313, %rax # imm = 0xffff7fffffffffff
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftr $15, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $15, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-1125899906842625, %rax # imm = 0xffff7fffffffffff
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftr $16, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $14, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-2251799813685249, %rax # imm = 0xffff7fffffffffff
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k0, %k0
; CHECK-NEXT:  kshiftr $19, %k1, %k2
; CHECK-NEXT:  kshiftlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $13, %k2, %k2
; CHECK-NEXT:  korq %k2, %k0, %k0
; CHECK-NEXT:  movabsq $-4503599627370497, %rax # imm = 0xffeffffffffffff
entry:
%a = load <64 x i8>, <64 x i8>* %x
%b = icmp eq <64 x i8> %a, zeroinitializer
%shuf = shufflevector <64 x i1> %b, <64 x i1> undef, <64 x i12> %i132 1, i32 0, i32 3, i32 2, i32 5, i32 4, i32 7, i32 6, i32 9, i32 8, i32 11, i32 10, i32 13, i32 12, i32 15, i32 14, i32 17, i32 16, i32 19, i32 18, i32 21, i32 20, i32 23, i32 22, i32 25, i32 24, i32 27, i32 26, i32 29, i32 28, i32 31, i32 30, i32 33, i32 32, i32 35, i32 34, i32 37, i32 36, i32 39, i32 38, i32 41, i32 40, i32 43, i32 42, i32 45, i32 44, i32 47, i32 46, i32 49, i32 48, i32 51, i32 50, i32 53, i32 52, i32 55, i32 54, i32 57, i32 56, i32 59, i32 58, i32 61, i32 60, i32 63, i32 62>
call void @llvm.masked.store.v64i8.p0v64i8(<64 x i8> %a, <64 x i8>* %y, <64 x i1> %shuf)
ret void
def cmp_v8i64_zext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-vector-width"="256" {  
    ; CHECK-LABEL: cmp_v8i64_zext:  
    ; CHECK:               # %bb.0:  
    ; CHECK-NEXT:        vmovdqa (%rsi), %ymm0  
    ; CHECK-NEXT:        vmovdqa 32(%rsi), %ymm1  
    ; CHECK-NEXT:        vpcmpgtq 32(%rdi), %ymm1, %ymm1  
    ; CHECK-NEXT:        vpcmpgtq (%rdi), %ymm0, %ymm0  
    ; CHECK-NEXT:        vmovdqa %ymm0, %ymm0  
    ; CHECK-NEXT:        vmovdqa %ymm1, 32(%rdx)  
    ; CHECK-NEXT:        vzeroupper  
    ; CHECK-NEXT:        retq  
    ; CHECK-NEXT:        retq  
    ; CHECK-NEXT:        retq  
    ; CHECK-NEXT:        %x = load <8 x i64>, <8 x i64>* %xptr  
    ; CHECK-NEXT:        %y = load <8 x i64>, <8 x i64>* %yptr  
    ; CHECK-NEXT:        %cmp = icmp slt <8 x i64> %x, %y  
    ; CHECK-NEXT:        %ext = sext <8 x i1> %cmp to <8 x i64>  
    ; CHECK-NEXT:        store <8 x i64> %ext, <8 x i64>* %zptr  
    ; CHECK-NEXT:        ret void  
    }
; CHECK-NEXT: vcpmpgtq (%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpsrlq $63, %ymm1, %ymm1
; CHECK-NEXT: vpsrlq $63, %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %xptr
%y = load <8 x i64>, <8 x i64>* %y.ptr
%cmp = icmp slt <8 x i64> %x, %y
%ext = zext <8 x i1> %cmp to <8 x i64>
save <8 x i64> %ext, <8 x i64>* %zptr
ret void

define <16 x i8> @var_rotate_v16i8(<16 x i8> %a, <16 x i8> %b) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: var_rotate_v16i8:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa [8,8,8,8,8,8,8,8,8,8,8,8,8,8,8,8] xmm2 = xmm1[0],zero,xmm1[1],zero,xmm1[2],zero,xmm1[3],zero,xmm1[4],zero,xmm1[5],zero,xmm1[6],zero,xmm1[7],zero,xmm1[8],zero,xmm1[9],zero,xmm1[10],zero,xmm1[11],zero,xmm1[12],zero,xmm1[13],zero,xmm1[14],zero,xmm1[15],zero
; CHECK-NEXT: vpmovzxbw xmm0 = xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero
; CHECK-NEXT: vpsllvw %ymm1, %ymm0, %ymm2
; CHECK-NEXT: vpor %ymm0, %ymm1, %ymm2
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%b8 = sub <16 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %b
%shl = shl <16 x i8> %a, %b
%lsr = lshr <16 x i8> %a, %b8
%or = or <16 x i8> %shl, %lsr
ret <16 x i8> %or
}

define <32 x i8> @var_rotate_v32i8(<32 x i8> %a, <32 x i8> %b) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: var_rotate_v32i8:
; CHECK: # %bb.0:
; CHECK-NEXT:  vpsllw $4, %ymm0, %ymm2
; CHECK-NEXT:  vpsrlw $4, %ymm0, %ymm3
; CHECK-NEXT:  vpternlogq $216, {{.*}}(%rip), %ymm2, %ymm3
; CHECK-NEXT:  vpsllw $5, %ymm1, %ymm1
; CHECK-NEXT:  vpblendvb %ymm1, %ymm3, %ymm0, %ymm0
; CHECK-NEXT:  vpsllw $2, %ymm0, %ymm2
; CHECK-NEXT:  vpsrlw $6, %ymm0, %ymm3
; CHECK-NEXT:  vpternlogq $216, {{.*}}(%rip), %ymm2, %ymm3
; CHECK-NEXT:  vpaddb %ymm1, %ymm1, %ymm0
; CHECK-NEXT:  vpsllw $5, %ymm1, %ymm1
; CHECK-NEXT:  vpblendvb %ymm1, %ymm3, %ymm0, %ymm0
; CHECK-NEXT:  vpternlogq $248, {{.*}}(%rip), %ymm2, %ymm3
; CHECK-NEXT:  vpaddb %ymm1, %ymm1, %ymm0
; CHECK-NEXT:  retq

%b8 = sub <32 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %b
%shl = shl <32 x i8> %a, %b
%lshr = lshr <32 x i8> %a, %b8
%or = or <32 x i8> %shl, %lshr
ret <32 x i8> %or

}
%splat8 = sub <32 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %splat
%shl = shl <32 x i8> %a, %splat
%lshr = lshr <32 x i8> %a, %splat8
%or = or <32 x i8> %shl, %lshr
ret <32 x i8> %or
}

define <32 x i8> @constant_rotate_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
 ; CHECK-AVX512-LABEL: constant_rotate_v32i8:
 ; CHECK-AVX512: # %bb.0:
 ; CHECK-AVX512-NEXT: vpsllw $4, %ymm0, %ymm1
 ; CHECK-AVX512-NEXT: vpand {{.*}}(%rip), %ymm1, %ymm1
 ; CHECK-AVX512-NEXT: vbroadcasti128 {{.*#+}} ymm2 = [8192,24640,41088,57536,57344,41152,24704,8256,8192,24640,41088,57536,57344,41152,24704,8256]
 ; CHECK-AVX512-NEXT: # ymm2 = mem[0,1,0,1]
 ; CHECK-AVX512-NEXT: vpsllw %2, %ymm1, %ymm3
 ; CHECK-AVX512-NEXT: vpand {{.*}}(%rip), %ymm3, %ymm3
 ; CHECK-AVX512-NEXT: vpackuswb %ymm3, %ymm0, %ymm0
 ; CHECK-AVX512-NEXT: vpor %ymm0, %ymm1, %ymm0
 ; CHECK-AVX512-NEXT: retq
 ; CHECK-VBMI-LABEL: constant_rotate_v32i8:
 ; CHECK-VBMI: # %bb.0:
 ; CHECK-VBMI-NEXT: vpsllw %4, %ymm0, %ymm1
 ; CHECK-VBMI-NEXT: vpand {{.*}}(%rip), %ymm1, %ymm1
 ; CHECK-VBMI-NEXT: vbroadcasti128 {{.*#+}} ymm2 = [8192,24640,41088,57536,57344,41152,24704,8256,8192,24640,41088,57536,57344,41152,24704,8256]
 ; CHECK-VBMI-NEXT: # ymm2 = mem[0,1,0,1]
 ; CHECK-VBMI-NEXT: vpsllw %2, %ymm1, %ymm3
 ; CHECK-VBMI-NEXT: vpand {{.*}}(%rip), %ymm3, %ymm3
 ; CHECK-VBMI-NEXT: vpackuswb %ymm3, %ymm0, %ymm0
 ; CHECK-VBMI-NEXT: vpor %ymm0, %ymm1, %ymm0
 ; CHECK-VBMI-NEXT: retq
 ;
 ; CHECK-VPBMI-LABEL: constant_rotate_v32i8:
 ; CHECK-VPBMI: # %bb.0:
 ; CHECK-VPBMI-NEXT: vpsllw %4, %ymm0, %ymm1
 ; CHECK-VPBMI-NEXT: vpand {{.*}}(%rip), %ymm1, %ymm1
 ; CHECK-VPBMI-NEXT: vbroadcasti128 {{.*#+}} ymm2 = [8192,24640,41088,57536,57344,41152,24704,8256,8192,24640,41088,57536,57344,41152,24704,8256]
 ;

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define <32 x i8> @splatconstant_rotate_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
  ret <32 x i8> %or
}

; CHECK-LABEL: splatconstant_rotate_v32i8:
; CHECK: # %bb.0:
; CHECK-NEXT: vpsllw $4, %ymm0, %ymm1
; CHECK-NEXT: vpshl $4, %ymm0, %ymm0
; CHECK-NEXT: vpternlogq $216, {%.*}(%rip), %ymm1, %ymm0
; CHECK-NEXT: retq

%shl = shl <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 9, i8 10, i8 11, i8 12, i8 13, i8 14, i8 15, i8 16, i8 17, i8 18, i8 19, i8 20, i8 21, i8 22, i8 23, i8 24, i8 25, i8 26, i8 27, i8 28, i8 29, i8 30, i8 31, i8 32>
%lshr = lshr <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 9, i8 10, i8 11, i8 12, i8 13, i8 14, i8 15, i8 16, i8 17, i8 18, i8 19, i8 20, i8 21, i8 22, i8 23, i8 24, i8 25, i8 26, i8 27, i8 28, i8 29, i8 30, i8 31, i8 32>
%or = or <32 x i8> %shl, %lshr
ret <32 x i8> %or
define <32 x i8> @splatconstant_rotate_mask_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
    ; CHECK-LABEL: splatconstant_rotate_mask_v32i8:
    ; CHECK:    # %bb.0:
    ; CHECK-NEXT:  vpsllw $4, %ymm0, %ymm1
    ; CHECK-NEXT:  vpsrlw $4, %ymm0, %ymm0
    ; CHECK-NEXT:  vpternlogq $216, {{.*}}(%rip), %ymm1, %ymm0
    ; CHECK-NEXT:  vpand {{.*}}(%rip), %ymm0, %ymm0
    ; CHECK-NEXT:  retq
    %shl = shl <32 x i8> %a, <i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4>
    %lshr = lshr <32 x i8> %a, <i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4>
    %rmask = and <32 x i8> %lshr, <i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55>
    %lmask = and <32 x i8> %shl, <i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33>
    %or = or <32 x i8> %lmask, %rmask
    ret <32 x i8> %or
}

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add_lldb_library(lldbPluginObjectContainerBSDArchive PLUGIN
 ObjectContainerBSDArchive.cpp

LINK_LIBS
 lldbCore
 lldbHost
 lldbSymbol

LINK_COMPONENTS
 Support

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The two loads based on `%struct.0`, loading two different data types
cause LSR to assume type "void" for the memory type. This would then
cause an assert in isLegalAddressingMode. Make sure we no longer crash.

target triple = "hexagon"

%struct.0 = type { i8*, i8, %union.anon.0 }
%union.anon.0 = type { i8* }
define hidden fastcc void @fred() unnamed_addr #0 {
    entry:
    br i1 undef, label %while.end, label %while.body.lr.ph

    while.body.lr.ph: ; preds = %entry
    br label %while.body

    while.body: ; preds = %exit.2, %while.body.lr.ph
    %lsr.iv = phi %struct.0* [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
    switch i32 undef, label %exit [
        i32 1, label %sw.bb.i
        i32 2, label %sw.bb3.i
    ]

    sw.bb.i: ; preds = %while.body
    unreachable

    sw.bb3.i: ; preds = %while.body
    unreachable

    exit: ; preds = %while.body
    switch i32 undef, label %exit.2 [
        i32 1, label %sw.bb.i17
        i32 2, label %sw.bb3.i20
    ]

    sw.bb.i17: ; preds = %.exit
    %0 = bitcast %struct.0* %lsr.iv to i32*
    %1 = load i32, i32* %0, align 4
    unreachable

    sw.bb3.i20: ; preds = %exit
    %2 = bitcast %struct.0* %lsr.iv to i8**
    %3 = load i8*, i8** %2, align 4
    unreachable

    exit.2: ; preds = %exit
    %cgep22 = getelementptr %struct.0, %struct.0* %lsr.iv, i32 1
    br label %while.body

    while.end: ; preds = %entry
    ret void
}

attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }
; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature --scrub-attributes
; RUN: opt -attributor -attributor-manifest-internal -attributor-max-iterations-verify -attributor-annotate-decl-cs -
target triple = "x86_64-unknown-linux-gnu"

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
  ;
  ; NOT_TUNIT_NPM-LABEL: define
  ({{[^@]+}}) @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
  ; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
  ; NOT_TUNIT_NPM-NEXT: bb:
  ; NOT_TUNIT_NPM-NEXT:    [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
  ; NOT_TUNIT_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
  ; NOT_TUNIT_NPM-NEXT:    [[ARG:%.*]] = load <8 x i64>, <8 x i64>* [[ARG]], align 64
  ; NOT_TUNIT_NPM-NEXT:    ret void
  ;
  ; IS__TUNIT_NPM-LABEL: define
  ({{[^@]+}}) @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
  ; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]])
  ; IS__TUNIT_NPM-NEXT: bb:
  ; IS__TUNIT_NPM-NEXT:    [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
  ; IS__TUNIT_NPM-NEXT:    store <8 x i64> [[ARG1_PRIV]], <8 x i64>* [[ARG]], align 64
  ; IS__TUNIT_NPM-NEXT:    ret void
  ;
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
    ; IS__UNIT_OPM-LABEL: define [{[^@]+}] @avx512_legal512_prefer512_call_avx512_legal512_prefer512
    ; IS__UNIT_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
    ; IS__UNIT_OPM-NEXT: bb:
    ; IS__UNIT_OPM-NEXT: [[TMP:.%]] = alloca <8 x i64>, align 32
    ; IS__UNIT_OPM-NEXT: [[TMP2:.%]] = alloca <8 x i64>, align 32
    ; IS__UNIT_OPM-NEXT: [[TMP3:.%]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; IS__UNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
    ; IS__UNIT_OPM-NEXT: call fastcc void
    @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* nocapture nofree nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64
dereferenceable(64) [[TMP]])
    ; IS__UNIT_OPM-NEXT: [[TMP4:.%]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
    ; IS__UNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
    ; IS__UNIT_OPM-NEXT: ret void
    ;
    ; IS__UNIT_NPM-LABEL: define [{[^@]+}] @avx512_legal512_prefer512_call_avx512_legal512_prefer512
    ; IS__UNIT_NPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
    ; IS__UNIT_NPM-NEXT: bb:
    ; IS__UNIT_NPM-NEXT: [[TMP:.%]] = alloca <8 x i64>, align 32
    ; IS__UNIT_NPM-NEXT: [[TMP2:.%]] = alloca <8 x i64>, align 32
    ; IS__UNIT_NPM-NEXT: [[TMP3:.%]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; IS__UNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
    ; IS__UNIT_NPM-NEXT: call fastcc void
    @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64
dereferenceable(64) [[TMP0]])
    ; IS__UNIT_NPM-NEXT: [[TMP4:.%]] = load <8 x i64>, <8 x i64>* [[TMP0]], align 64
    ; IS__UNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
    ; IS__UNIT_NPM-NEXT: ret void
    ;
    ; IS__CGSCC_OPM-LABEL: define [{[^@]+}] @avx512_legal512_prefer512_call_avx512_legal512_prefer512
    ; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
    ; IS__CGSCC_OPM-NEXT: bb:
    ; IS__CGSCC_OPM-NEXT: [[TMP:.%]] = alloca <8 x i64>, align 32
    ; IS__CGSCC_OPM-NEXT: [[TMP2:.%]] = alloca <8 x i64>, align 32
    ; IS__CGSCC_OPM-NEXT: [[TMP3:.%]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
    ; IS__CGSCC_OPM-NEXT: call fastcc void
    @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* nocapture nofree nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64
dereferenceable(64) [[TMP]])
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #1 {
    bb:
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
    call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
    call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #1 {
    bb:
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>, align 32
    %tmp3 = bitcast <8 x i64>* %tmp to i8*
    call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
    call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
    %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
    store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
    ret void
}
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {  
  ; %tmp = load <8 x i64>, <8 x i64>* %arg 
  store <8 x i64> %tmp, <8 x i64>* %arg 
  ret void 
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {  
  ; %tmp = load <8 x i64>, <8 x i64>* %arg 
  store <8 x i64> %tmp, <8 x i64>* %arg 
  ret void 
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {  
  ; %tmp = load <8 x i64>, <8 x i64>* %arg 
  store <8 x i64> %tmp, <8 x i64>* %arg 
  ret void 
}
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; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT:  [[TMP:%.%]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:  [[TMP2:%.%]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:  [[TMP3:%.%]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT:  call fastcc void
@calleee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_OPM-NEXT:  [[TMP4:%.%]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT:  ret void
;
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT:  [[TMP:%.%]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:  [[TMP2:%.%]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:  [[TMP3:%.%]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT:  call fastcc void
@calleee_avx512_legal512_prefer56_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_NPM-NEXT:  [[TMP4:%.%]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT:  ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @calleee_avx512_legal512_prefer56_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @calleee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #1 {

;
; NOT_TUNIT_NPM-LABEL: define
([[@*]+]) @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; NOT_TUNIT_NPM-NEXT: bb:
; NOT_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: ret void
;
; IS__TUNIT_NPM-LABEL: define
([[@*]+]) @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64> [[TMP0:%.*]])
; IS__TUNIT_NPM-NEXT: bb:
%tmp = load <8 x i64>, <8 x i64>* %arg
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
;
; IS__TUNIT_OPM-LABEL: define ([[@*]+]) @avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_OPM-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

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; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapturenonnull writeonlyalign 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* nocapturenonnull writeonlyalign 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]])
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapturenonnull writeonlyalign 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapturenonnull writeonlyalign 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* nocapturenonnull writeonlyalign 64 dereferenceable(64) [[TMP2]], <8 x i64> [[ARG]])
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void
;
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapturenonnull writeonlyalign 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapturenonnull writeonlyalign 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* nocapturenonnull writeonlyalign 64 dereferenceable(64) [[TMP2]], <8 x i64> [[ARG]])
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
  
  NOT_TUNIT_NPM-LABEL: define {
    }@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
  NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
  NOT_TUNIT_NPM-NEXT: bb:
    NOT_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
    NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
    NOT_TUNIT_NPM-NEXT: ret void
    
  IS__TUNIT_NPM-LABEL: define {
    }@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
  IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]])
  IS__TUNIT_NPM-NEXT: bb:
    IS__TUNIT_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
    IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
    IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
    IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
    IS__TUNIT_NPM-NEXT: ret void
    
  bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
  
  IS__TUNIT_OPM-LABEL: define {
    }@avx512_legal512_prefer256_call_avx512_legal512_prefer512
  IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
  IS__TUNIT_OPM-NEXT: bb:
    IS__TUNIT_OPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
    IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
    IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
    IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
    IS__TUNIT_OPM-NEXT: ret void
    
  bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
  }
: IS__TUNIT_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
: IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
: IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
: IS__TUNIT_OPM-NEXT: ret void

: IS__TUNIT_NPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal512_prefer512
: IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
: IS__TUNIT_NPM-NEXT: bb:
: IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloc <8 x i64>, align 32
: IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloc <8 x i64>, align 32
: IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
: IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
: IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
: IS__TUNIT_NPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* [[TMP0]])
: IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
: IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
: IS__TUNIT_NPM-NEXT: ret void

: IS__CGSCC_OPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal512_prefer512
: IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
: IS__CGSCC_OPM-NEXT: bb:
: IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloc <8 x i64>, align 32
: IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloc <8 x i64>, align 32
: IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
: IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
: IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
: IS__CGSCC_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
: IS__CGSCC_OPM-NEXT: bb:
: IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloc <8 x i64>, align 32
: IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloc <8 x i64>, align 32
: IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
: IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
: IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
: IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
: IS__CGSCC_OPM-NEXT: ret void

: IS__CGSCC_NPM-LABEL: define {{[^@]+}} @avx512_legal512_prefer256_call_avx512_legal512_prefer512
: IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
: IS__CGSCC_NPM-NEXT: bb:
: IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloc <8 x i64>, align 32
: IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloc <8 x i64>, align 32
: IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
: IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; This should not promote

define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
(8 x i64)* %arg, %8 x i64)*%arg1)
{
    bb:
        %tmp = alloca <8 x i64>, align 32
        %tmp2 = alloca <8 x i64>, align 32
        %tmp3 = bitcast <8 x i64>* %tmp to i8*
        call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
        call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
(8 x i64)*%tmp2, %8 x i64)* %tmp)
        %tmp4 = load <8 x i64>, %tmp2, align 32
        store <8 x i64> %tmp4, %arg, align 2
        ret void
}

; This should not promote

define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
(8 x i64)* %arg, %8 x i64)*%arg1)
{
    bb:
        %tmp = alloca <8 x i64>, align 32
        %tmp2 = alloca <8 x i64>, align 32
        %tmp3 = bitcast <8 x i64>* %tmp to i8*
        call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
        call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
(8 x i64)*%tmp2, %8 x i64)* %tmp)
        %tmp4 = load <8 x i64>, %tmp2, align 32
        store <8 x i64> %tmp4, %arg, align 2
        ret void
}

; This should not promote

define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
(8 x i64)* %arg, %8 x i64)*%arg1)
{
    bb:
        %tmp = alloca <8 x i64>, align 32
        %tmp2 = alloca <8 x i64>, align 32
        %tmp3 = bitcast <8 x i64>* %tmp to i8*
        call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
        call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
(8 x i64)*%tmp2, %8 x i64)* %tmp)
        %tmp4 = load <8 x i64>, %tmp2, align 32
        store <8 x i64> %tmp4, %arg, align 2
        ret void
}
define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
  ; IS__TUNIT_OPM-LABEL: define {{[^@]+}} @avx512_legal256_prefer256_call_avx512_legal512_prefer256
  ; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
  ; IS__TUNIT_OPM-NEXT: bb:
    ; IS__TUNIT_OPM-NEXT: [[TMP:.%.*]] = alloca <8 x i64>, align 32
    ; IS__TUNIT_OPM-NEXT: [[TMP2:.%.*]] = alloca <8 x i64>, align 32
    ; IS__TUNIT_OPM-NEXT: [[TMP3:.%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; IS__TUNIT_OPM-NEXT: call fastcc void
  @ callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nofree nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree nonnull readonly align 64
dereferenceable(64) [[TMP]])
  ; IS__TUNIT_OPM-NEXT: [[TMP4:.%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
  ; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; IS__TUNIT_OPM-NEXT: ret void
  ; IS__TUNIT_NPM-LABEL: define {{[^@]+}} @avx512_legal256_prefer256_call_avx512_legal512_prefer256
  ; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
  ; IS__TUNIT_NPM-NEXT: bb:
    ; IS__TUNIT_NPM-NEXT: [[TMP:.%.*]] = alloca <8 x i64>, align 32
    ; IS__TUNIT_NPM-NEXT: [[TMP2:.%.*]] = alloca <8 x i64>, align 32
    ; IS__TUNIT_NPM-NEXT: [[TMP3:.%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; IS__TUNIT_NPM-NEXT: call fastcc void
  @ callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64
dereferenceable(64) [[TMP]])
  ; IS__TUNIT_NPM-NEXT: [[TMP4:.%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
  ; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; IS__TUNIT_NPM-NEXT: ret void
  ; IS__CGSCC_OPM-LABEL: define {{[^@]+}} @avx512_legal256_prefer256_call_avx512_legal512_prefer256
  ; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
  ; IS__CGSCC_OPM-NEXT: bb:
    ; IS__CGSCC_OPM-NEXT: [[TMP:.%.*]] = alloca <8 x i64>, align 32
    ; IS__CGSCC_OPM-NEXT: [[TMP2:.%.*]] = alloca <8 x i64>, align 32
    ; IS__CGSCC_OPM-NEXT: [[TMP3:.%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
    ; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
  ; IS__CGSCC_OPM-NEXT: call fastcc void
  @ callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64
dereferenceable(64) [[TMP]])
  ; IS__CGSCC_OPM-NEXT: [[TMP4:.%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
  ; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
  ; IS__CGSCC_OPM-NEXT: ret void
  ; IS__CGSCC_OPM-LABEL: define {{[^@]+}} @avx512_legal256_prefer256_call_avx512Legal512_prefer256
  ; IS__CGSCC_OPM-SAME: (<8 x i64>* %arg) #2
}
; IS__CGSCC_OPM-NEXT: ret void

; IS__CGSCC_NPM-LABEL: define {{[^@]+}} @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
; IS__CGSCC_NPM-NEXT: bb:

; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__CGSCC_NPM-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[TMP]])
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 {

; NOT_TUNIT_NPM-LABEL: define {{[^@]+}} @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; NOT_TUNIT_NPM-NEXT: bb:

; NOT_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: ret void

; IS__TUNIT_NPM-LABEL: define {{[^@]+}} @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; IS__TUNIT_NPM-NEXT: bb:
define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 { 
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 { 
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 { 
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 { 
    bb:
    %tmp = load <8 x i64>, <8 x i64>* %arg1
    store <8 x i64> %tmp, <8 x i64>* %arg
    ret void
}
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; is__cgsccl_omp-next: [[tmp2:%.*]] = alloca <8 x i64>, align 32
; is__cgsccl_omp-next: [[tmp3:%.*]] = bitcast <8 x i64>* [[tmp2]] to i8*
; is__cgsccl_omp-next: call void @llvm.memset.p0i8.i64(i8* no capture nonnull writeonly align 64
dereferenceable(64) [[tmp3]], i8 0, i64 32, i1 false)
; is__cgsccl_omp-next: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* no capture nofree
nonnull writeonly align 64 dereferenceable(64) [[tmp2]], <8 x i64>* no capture nofree nonnull readonly align 64
dereferenceable(64) [[tmp3]])
; is__cgsccl_omp-next: [[tmp4:%.*]] = load <8 x i64>, <8 x i64>* [[tmp3]], align 64
; is__cgsccl_omp-next: store <8 x i64> [[tmp4]], <8 x i64>* [[arg]], align 2
; is__cgsccl_omp-next: ret void

; is__cgsccl_npm-label: define ([[@*+]])@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; is__cgsccl_npm-same: (<8 x i64>* no capture nonnull writeonly align 2 dereferenceable(64) [[arg:%.*]])
; is__cgsccl_npm-next: bb:
; is__cgsccl_npm-next: [[tmp:%.*]] = alloca <8 x i64>, align 32
; is__cgsccl_npm-next: [[tmp2:%.*]] = alloca <8 x i64>, align 32
; is__cgsccl_npm-next: [[tmp3:%.*]] = bitcast <8 x i64>* [[tmp]] to i8*
; is__cgsccl_npm-next: call void @llvm.memset.p0i8.i64(i8* align 32 [[tmp3]], i8 0, i64 32, i1 false)
; is__cgsccl_npm-next: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* noalias nofree nonnull
writeonly align 64 dereferenceable(64) [[tmp2]], <8 x i64>* noalias nofree nonnull readonly align 64
dereferenceable(64) [[tmp3]])
; is__cgsccl_npm-next: [[tmp4:%.*]] = load <8 x i64>, <8 x i64>* [[tmp3]], align 64
; is__cgsccl_npm-next: store <8 x i64> [[tmp4]], <8 x i64>* [[arg]], align 2
; is__cgsccl_npm-next: ret void

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8
x i64>* readily %arg1) #3 {

; NOT_TUNIT_NPM-LABEL: define
([[@*+]])@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; NOT_TUNIT_NPM-SAME: (<8 x i64>* no capture nofree nonnull writeonly align 64 dereferenceable(64)
[[arg:%.*]], <8 x i64>* no capture nofree nonnull readonly align 64 dereferenceable(64) [[arg1:%.*]])
define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg!
  store <8 x i64> %tmp, <8 x i64>* %arg!
  ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg!
  store <8 x i64> %tmp, <8 x i64>* %arg!
  ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg!
  store <8 x i64> %tmp, <8 x i64>* %arg!
  ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
  bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg!
  store <8 x i64> %tmp, <8 x i64>* %arg!
  ret void
}
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
void trie

; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8 x i64>* %arg1) #4 {

; NOT_TUNIT_NPM-LABEL: define
{[^@]+}@callee_avx2_legal512_prefer256_call_avx2_legal512_prefer256
; NOT_TUNIT_NPM-SAME: (<8 x i64>* nocapture noreturn noreturn noreturn align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* noreturn noreturn noreturn readonly align 64 dereferenceable(64) [[ARG1:%.*]])
; NOT_TUNIT_NPM-NEXT: bb:
; NOT_TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; NOT_TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; NOT_TUNIT_NPM-NEXT: ret void

; IS__TUNIT_NPM-LABEL: define {[^@]+}@callee_avx2_legal512_prefer256_call_avx2_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias noreturn noreturn noreturn align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]])
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT: ret void

bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void

define void @avx2_legal512_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #3 {

; IS__TUNIT_OPM-LABEL: define {[^@]+}@avx2_legal512_prefer256_call_avx2_legal512_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* noreturn writeonly [[ARG:%.*]])
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32 dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
; IS__TUNIT_OPM-NEXT: call fastcc void
@callee_avx2_legal512_prefer256_call_avx2_legal512_prefer256(<8 x i64>* noreturn noreturn noreturn align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noreturn noreturn noreturn readonly align 64 dereferenceable(64) [[TMP]])
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
: IS__UNIT_OPM-NEXT: ret void

: IS__UNIT_NPM-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
: IS__UNIT_NPM-SAME: (<8 x i64>* nocapture writeonly [[ARG:%.*]])
: IS__UNIT_NPM-NEXT: bb:
: IS__UNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
: IS__UNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
: IS__UNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
: IS__UNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 32
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
: IS__UNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
: IS__UNIT_NPM-NEXT: call fastcc void
@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nofree nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]])
: IS__UNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
: IS__UNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
: IS__UNIT_NPM-NEXT: ret void

: IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
: IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
: IS__CGSCC_OPM-NEXT: bb:
: IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
: IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
: IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
: IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
: IS__CGSCC_OPM-NEXT: call fastcc void
@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nofree nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64
dereferenceable(64) [[TMP2]])
: IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
: IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
: IS__CGSCC_OPM-NEXT: ret void

: IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
: IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
: IS__CGSCC_NPM-NEXT: bb:
: IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
: IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
: IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
: IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nonnull writeonly align 64
dereferenceable(64) [[TMP3]], i8 0, i64 32, i1 false)
: IS__CGSCC_NPM-NEXT: call fastcc void
@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nofree nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree nonnull readonly align 64
dereferenceable(64) [[TMP2]])
: IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
: IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT:    ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }

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; RUN: llc -O3 -mtriple=powerpc-unknown-linux-gnu -mcpu=e500 -mattr=spe < %s | FileCheck %s

; PowerPC SPE is a rare in-tree target that has the FP_TO_SINT node marked as Legal.

; Verify that fptosi(42.1) isn't simplified when the rounding mode is unknown.
; Verify that no gross errors happen.
; CHECK-LABEL: @f20
; COMMON: cfdctsiz

define i32 @f20(double %a) strictfp {
  entry:
  %result = call i32 @llvm.experimental.constrained.fptosi.i32.f64(double 42.1,
                       metadata !"fpexcept.strict")
    strictfp
  ret i32 %result
}

@llvm.fp.env = thread_local global i8 zeroinitializer, section "llvm.metadata"
declare i32 @llvm.experimental.constrained.fptosi.i32.f64(double, metadata)

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; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC256,SKX256
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define void @zext256() "min-legal-vector-width"="256" {
    ; VEC256-LABEL: 'zext256'
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    ; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

    ; AVX512VL512-LABEL: 'zext256'
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

    ; SKX512-LABEL: 'zext256'
    ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>

define void @zext512() "min-legal-vector-width"="512" {
    ; AVX-LABEL: 'zext512'
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    ret void
}

define void @zext512() "min-legal-vector-width"="512" {
    ; AVX512VL256-LABEL: 'zext512'
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
}

define void @zext512() "min-legal-vector-width"="512" {
    ; AVX512VL512-LABEL: 'zext512'
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
}

define void @zext512() "min-legal-vector-width"="512" {
    ; SKX256-LABEL: 'zext512'
    ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
    ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
    ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
    ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
    ; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
    ; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
}
define void @sext256() "min-legal-vector-width"="256" { 
 ; VEC256-LABEL: 'sext256'
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = sext <16 x i8> undef to <16 x i32>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void 
}

define void @sext256() "min-legal-vector-width"="256" { 
 ; VEC256-LABEL: 'sext256'
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = sext <16 x i8> undef to <16 x i32>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void 
}

define void @sext256() "min-legal-vector-width"="256" { 
 ; VEC256-LABEL: 'sext256'
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = sext <16 x i8> undef to <16 x i32>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void 
}

define void @sext256() "min-legal-vector-width"="256" { 
 ; VEC256-LABEL: 'sext256'
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = sext <16 x i8> undef to <16 x i32>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
 ; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void 
}
define void @sext512() "min-legal-vector-width"="512" {
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
    ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    ;
    ; SKX512-LABEL: 'sext256'
    ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
    ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
    ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
    ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
    ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
    ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
    ; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    ;
    ;
    ; AVX5-LABEL: 'sext512'
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = sext <8 x i8> undef to <8 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = sext <8 x i16> undef to <8 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
    ;
    ; AVX512VL256-LABEL: 'sext512'
}
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: AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
: AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
: AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
: AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
: AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
: AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
: AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

: AVX512VL512-LABEL: 'sext512'
: AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
: AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
: AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
: AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
: AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
: AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
: AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

: SKX256-LABEL: 'sext512'
: SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
: SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
: SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
: SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
: SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
: SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
: SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

: SKX512-LABEL: 'sext512'
: SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
: SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
: SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

define void @trunc256() "min-legal-vector-width"="256" {
; AVX-LABEL: 'trunc256'
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL256-LABEL: 'trunc256'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'trunc256'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = trunc <8 x i64> undef to
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

; SKX256-LABEL: 'trunc256'
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

; SKX512-LABEL: 'trunc256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

%A = trunc <8 x i64> undef to <8 x i32>
%B = trunc <8 x i64> undef to <8 x i16>
%C = trunc <8 x i64> undef to <8 x i8>
%D = trunc <16 x i32> undef to <16 x i16>
%E = trunc <16 x i32> undef to <16 x i8>
%F = trunc <32 x i16> undef to <32 x i8>
ret void
define i32 @zext256_vXi1() "min-legal-vector-width"="256" {
  ; AVX-LABEL: 'zext256_vXi1'
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
  ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
  ;
  ; AVX512VL256-LABEL: 'zext256_vXi1'
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
  ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 12 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 12 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 25 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; AVX512VL512-LABEL: 'zext256_vXi1'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i64 = zext <16 x i1> undef to <16 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i16 = zext <4 x i1> undef
to <4 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 19 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX256-LABEL: 'zext256_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX512-LABEL: 'zext256_vXi1'
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
%V2i64 = zext <2 x i1> undef to <2 x i64>
%V4i64 = zext <4 x i1> undef to <4 x i64>
%V8i64 = zext <8 x i1> undef to <8 x i64>

%V2i32 = zext <2 x i1> undef to <2 x i32>
%V4i32 = zext <4 x i1> undef to <4 x i32>
%V8i32 = zext <8 x i1> undef to <8 x i32>
%V16i32 = zext <16 x i1> undef to <16 x i32>

%V2i16 = zext <2 x i1> undef to <2 x i16>
%V4i16 = zext <4 x i1> undef to <4 x i16>
%V8i16 = zext <8 x i1> undef to <8 x i16>
%V16i16 = zext <16 x i1> undef to <16 x i16>
%V32i16 = zext <32 x i1> undef to <32 x i16>

%V2i8 = zext <2 x i1> undef to <2 x i8>
%V4i8 = zext <4 x i1> undef to <4 x i8>
%V8i8 = zext <8 x i1> undef to <8 x i8>
%V16i8 = zext <16 x i1> undef to <16 x i8>
%V32i8 = zext <32 x i1> undef to <32 x i8>
%V64i8 = zext <64 x i1> undef to <64 x i8>

ret i32 undef
}

define i32 @sext256_vXi1() "min-legal-vector-width"="256" {
 ; AVX-LABEL: 'sext256_vXi1'
 ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
 ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
 ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
 ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
 ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = sext <2 x i1> undef to <2 x
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 5 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 5 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 5 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 10 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 21 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 42 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL512-LABEL: 'sext256_vXi1'
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V16i64 = sext <16 x i1> undef to <16 x i64>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V32i64 = sext <32 x i1> undef to <32 x i64>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V64i64 = sext <64 x i1> undef to <64 x i64>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V32i32 = sext <32 x i1> undef to <32 x i32>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V64i32 = sext <64 x i1> undef to <64 x i32>
<4 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 15 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX256-LABEL: 'sext256_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; %I64 = sext i1 undef to i64
%V2i64 = sext <2 x i1> undef to <2 x i64>
%V4i64 = sext <4 x i1> undef to <4 x i64>
%V8i64 = sext <8 x i1> undef to <8 x i64>

%I32 = sext i1 undef to i32
%V2i32 = sext <2 x i1> undef to <2 x i32>
%V4i32 = sext <4 x i1> undef to <4 x i32>
%V8i32 = sext <8 x i1> undef to <8 x i32>
%V16i32 = sext <16 x i1> undef to <16 x i32>

%I16 = sext i1 undef to i16
%V2i16 = sext <2 x i1> undef to <2 x i16>
%V4i16 = sext <4 x i1> undef to <4 x i16>
%V8i16 = sext <8 x i1> undef to <8 x i16>
%V16i16 = sext <16 x i1> undef to <16 x i16>
%V32i16 = sext <32 x i1> undef to <32 x i16>

%I8 = sext i1 undef to i8
%V2i8 = sext <2 x i1> undef to <2 x i8>
%V4i8 = sext <4 x i1> undef to <4 x i8>
%V8i8 = sext <8 x i1> undef to <8 x i8>
%V16i8 = sext <16 x i1> undef to <16 x i8>
%V32i8 = sext <32 x i1> undef to <32 x i8>
%V64i8 = sext <64 x i1> undef to <64 x i8>

ret i32 undef
}

define i32 @trunc_vXi1() "min-legal-vector-width"="256" {
    ; AVX-LABEL: 'trunc_vXi1'
    ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 46 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>
    ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>

    ret i32 undef
}
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 22 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 18 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; AVX512VL256-LABEL: 'trunc_vXi1'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 22 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 44 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 20 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 16 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 32 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 17 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 34 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; AVX512VL512-LABEL: 'trunc_vXi1'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 22 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 44 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 14 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 15 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

; SKX256-LABEL: 'trunc_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>
<table>
<thead>
<tr>
<th>Instruction</th>
<th>Cost Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>%V32i64 = trunc &lt;32 x i64&gt; undef to &lt;32 x i1&gt;</td>
<td></td>
</tr>
<tr>
<td>%V64i64 = trunc &lt;64 x i64&gt; undef to &lt;64 x i1&gt;</td>
<td></td>
</tr>
<tr>
<td>%V2i32 = trunc &lt;2 x i32&gt; undef to &lt;2 x i1&gt;</td>
<td></td>
</tr>
<tr>
<td>%V4i32 = trunc &lt;4 x i32&gt; undef to &lt;4 x i1&gt;</td>
<td></td>
</tr>
<tr>
<td>%V8i32 = trunc &lt;8 x i32&gt; undef to &lt;8 x i1&gt;</td>
<td></td>
</tr>
<tr>
<td>%V16i32 = trunc &lt;16 x i32&gt; undef to &lt;16 x i1&gt;</td>
<td></td>
</tr>
<tr>
<td>%V32i32 = trunc &lt;32 x i32&gt; undef to &lt;32 x i1&gt;</td>
<td></td>
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<tr>
<td>%V64i32 = trunc &lt;64 x i32&gt; undef to &lt;64 x i1&gt;</td>
<td></td>
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<tr>
<td>%V2i16 = trunc &lt;2 x i16&gt; undef to &lt;2 x i1&gt;</td>
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<tr>
<td>%V4i16 = trunc &lt;4 x i16&gt; undef to &lt;4 x i1&gt;</td>
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<td>%V8i16 = trunc &lt;8 x i16&gt; undef to &lt;8 x i1&gt;</td>
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<td>%V16i16 = trunc &lt;16 x i16&gt; undef to &lt;16 x i1&gt;</td>
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<td>%V32i16 = trunc &lt;32 x i16&gt; undef to &lt;32 x i1&gt;</td>
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<td>%V64i16 = trunc &lt;64 x i16&gt; undef to &lt;64 x i1&gt;</td>
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<tr>
<td>%V2i8 = trunc &lt;2 x i8&gt; undef to &lt;2 x i1&gt;</td>
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<td>%V4i8 = trunc &lt;4 x i8&gt; undef to &lt;4 x i1&gt;</td>
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<td>%V32i8 = trunc &lt;32 x i8&gt; undef to &lt;32 x i1&gt;</td>
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<tr>
<td>%V64i8 = trunc &lt;64 x i8&gt; undef to &lt;64 x i1&gt;</td>
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<tr>
<td>%V32i64 = trunc &lt;32 x i64&gt; undef to &lt;32 x i1&gt;</td>
<td></td>
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<tr>
<td>%V16i64 = trunc &lt;16 x i64&gt; undef to &lt;16 x i1&gt;</td>
<td></td>
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<td>%V32i64 = trunc &lt;32 x i64&gt; undef to &lt;32 x i1&gt;</td>
<td></td>
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</tbody>
</table>

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* /opt/cola/permits/1130029928_1612433355.79/0/wildfly-elytron-jacc-1-13-1-final-sources.jar/org/wildfly/security/authz/jacc/ElytronPolicyConfiguration.java
* /opt/cola/permits/1130029928_1612433355.79/0/wildfly-elytron-jacc-1-13-1-final-sources.jar/org/wildfly/security/authz/jacc/JaccDelegatingPolicy.java
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* /opt/cola/permits/1130029928_1612433355.79/0/wildfly-elytron-jacc-1-13-1-final-sources-
  jar/org/wildfly/security/authz/jacc/package-info.java
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  jar/org/wildfly/security/authz/jacc/ElytronMessages.java

1.1090 opensaml-profile-api 3.3.1
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/**
 * A predicate implementation that indicates whether the message channel does
 * <strong>NOT</strong> support confidentiality end-to-end.
 *
 * Typically but not exclusively used as a predicate for whether to encrypt something.</p>
 */

Found in path(s):
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-
* jar/org/opensaml/profile/logic/NoConfidentialityMessageChannelPredicate.java

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* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/logic/PredicateAccessControl.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/context/navigate/package-info.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/logic/BrowserProfilePredicate.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/context/AccessControlContext.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/action/package-info.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/action/EventIds.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/logic/ProfileIdPredicate.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/logic/IPRangePredicate.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/context/package-info.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/context/navigate/OutboundMessageContextLookup.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/context/package-info.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/action/EventException.java
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* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/logic/MessageContextPredicateAdapter.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/context/package-info.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/logic/package-info.java
* /opt/cola/permits/1111302142_1606896640.05/0/opensaml-profile-api-3-3-1-sources-1-jar/org/opensaml/profile/action/AbstractConditionalProfileAction.java
1.1091 connect-file 2.7.0

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Zstd-jni: JNI bindings to Zstd Library

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1.1094 python-setuptools 57.0.0

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1.1095 zlib 1.2.11

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/* zlib.h -- interface of the 'zlib' general purpose compression library
version 1.2.11, January 15th, 2017

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1.1096 jackson-databind 2.10.3
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1.1097 sysv-init 2.93 9

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## libressl

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## c-ares

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## zlib

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## libssh2

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Class, field, and method level annotations for describing thread-safety policies.

Three class-level annotations describe the intended thread-safety promises of a class: `@Immutable`, `@ThreadSafe`, and `@NotThreadSafe`. `@Immutable` means that the class is immutable, and implies `@ThreadSafe`. `@NotThreadSafe` is optional; if a class is not annotated as thread-safe, it should be presumed not to be thread-safe, but if you want to make it extra clear, use `@NotThreadSafe`.

These annotations are relatively unintrusive and are beneficial to both users and maintainers. Users can see immediately whether a class is thread-safe, and maintainers can see immediately whether thread-safety guarantees must be preserved. Annotations are also useful to a third constituency: tools. Static code-analysis tools may be able to verify that the code complies with the contract indicated by the annotation, such as verifying that a class annotated with `@Immutable` actually is immutable.
Classes that use locking should document which state variables are guarded with which locks, and which locks are used to guard those variables. A common source of inadvertent non-thread-safety is when a thread-safe class consistently uses locking to guard its state, but is later modified to add either new state variables that are not adequately guarded by locking, or new methods that do not use locking properly to guard the existing state variables. Documenting which variables are guarded by which locks can help prevent both types of omissions.

The `<code>@GuardedBy(lock)</code>` annotation documents that a field or method should be accessed only with a specific lock held.

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<?xml version="1.0"?>
<xsl:stylesheet version="1.0"

xmlns:xsl="http://www.w3.org/1999/XSL/Transform">

<xsl:output method="html" encoding="utf-8" standalone="no" media-type="text/html" />
<xsl:param name="product"/>
<xsl:param name="version"/>
<xsl:variable name="lowercase" select="'abcdefghijklmnopqrstuvwxyz'" />
<xsl:variable name="uppercase" select="'ABCDEFGHIJKLMNOPQRSTUVWXYZ'" />

<xsl:template match="/"

<html>
<head>
<meta http-equiv="Content-Type" content="text/html; charset=utf-8" />
<link rel="stylesheet" type="text/css" href="licenses.css"/>
</head>
<body>
<p>The following material has been provided for informational purposes only, and should not be relied
upon or construed as a legal opinion or legal advice.</p>
<!-- Read matching templates -->
<table>
<tr>
<th>Package</th>
<th>Package Artifact</th>
<th>Package Version</th>
<th>Remote Licenses</th>
<th>Local Licenses</th>
</tr>
<xsl:for-each select="licenseSummary/dependencies/dependency">
<xsl:sort select="concat(groupId, '.', artifactId)"/>
<tr>
<td><xsl:value-of select="concat(groupId, packageName)"/></td>
<td><xsl:value-of select="artifactId"/></td>
<td><xsl:value-of select="version"/></td>
<td>
<xsl:for-each select="licenses/license"/>
</td>
</tr>
</xsl:for-each>
</table>
<xsl:template name="remap-local-filename">
  <xsl:param name="filename"/>
  <xsl:choose>
    <xsl:when test="contains($filename, 'bsd') and contains($filename, '2-clause')">
      <xsl:text>bsd-2-clause.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'bsd') and contains($filename, '3-clause')">
      <xsl:text>bsd-3-clause.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'apache') and contains($filename, '1.1')">
      <xsl:text>apache-1.1.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'apache') and contains($filename, '2.0')">
      <xsl:text>apache license 2.0.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'jsr-000107')">
      <xsl:text>apache license 2.0.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'cddl') and contains($filename, 'gplv2')">
      <xsl:text>cddl-gplv2-classpath.txt</xsl:text>
    </xsl:when>
    <xsl:when test="contains($filename, 'common public license')">
      <xsl:text>common public license 1.0.txt</xsl:text>
    </xsl:when>
    <xsl:when test="$filename = 'gnu library general public license, version 2 - lgpl-2.0.txt'">
      <xsl:text>gnu library general public license, version 2.txt</xsl:text>
    </xsl:when>
    <xsl:when test="$filename = 'lgpl.txt'">
      <xsl:text>gnu library general public license, version 2.txt</xsl:text>
    </xsl:when>
    <xsl:when test="$filename = 'the dom4j license - license'">
      <xsl:text>the dom4j license.txt</xsl:text>
    </xsl:when>
    <xsl:when test="$filename = 'creative commons attribution 2.5 - legalcode'">
      <xsl:text>creative commons attribution 2.5.html</xsl:text>
    </xsl:when>
  </xsl:choose>
</xsl:template>
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Version 2.1, February 1999

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    at assemblers) written by James Hacker.

    <signature of Ty Coon>, 1 April 1989
    Ty Coon, President of Vice

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* /opt/ws_local/PERMITS_SQL/1094801243_1601320735.8/0/microprofile-rest-client-api-1-4-0-sources-
jar/org/eclipse/microprofile/rest/client/ext/AsyncInvocationInterceptorFactory.java
* /opt/ws_local/PERMITS_SQL/1094801243_1601320735.8/0/microprofile-rest-client-api-1-4-0-sources-
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  jar/org/eclipse/microprofile/rest/client/ext/ResponseExceptionMapper.java
* /opt/ws_local/PERMITS_SQL/1094801243_1601320735.8/0/microprofile-rest-client-api-1-4-0-sources-
  jar/org/eclipse/microprofile/rest/client/annotation/RegisterProvider.java
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1.1112 libverto 0.3.1-r1

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Metadata-Version: 1.1
Name: jtextfsm
Version: 0.3.1
Summary: UNKNOWN
Home-page: https://github.com/jonathanslenders/textfsm
Author: Google; Jonathan Slenders
1.1114 nghttp2 1.36.0-2+deb10u1

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set yrange [0:]
set terminal pngcairo font 'Sans, 8' lw 1 size 1400,1024
set xtics rotate by -45
set style histogram errorbars gap 2 lw 1
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1.1119 cxf-tools-wsdlto-databinding-jaxb

3.3.7

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1.1120 typing-extensions 3.10.0.0

1.1120.1 Available under license :

A. HISTORY OF THE SOFTWARE

Python was created in the early 1990s by Guido van Rossum at Stichting
Mathematisch Centrum (CWI, see http://www.cwi.nl) in the Netherlands
as a successor of a language called ABC. Guido remains Python's
principal author, although it includes many contributions from others.

In 1995, Guido continued his work on Python at the Corporation for
National Research Initiatives (CNRI, see http://www.cnri.reston.va.us)
in Reston, Virginia where he released several versions of the
software.

In May 2000, Guido and the Python core development team moved to
BeOpen.com to form the BeOpen PythonLabs team. In October of the same
year, the PythonLabs team moved to Digital Creations (now Zope
Corporation, see http://www.zope.com). In 2001, the Python Software
Foundation (PSF, see http://www.python.org/psf/) was formed, a
non-profit organization created specifically to own Python-related
Intellectual Property. Zope Corporation is a sponsoring member of
the PSF.

All Python releases are Open Source (see http://www.opensource.org for
the Open Source Definition). Historically, most, but not all, Python
releases have also been GPL-compatible; the table below summarizes
the various releases.

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1.1121 wss4j-ws-security-dom 2.2.5

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# Contributions to the urllib3 project

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In chronological order:

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  * HTTPS patch (which inspired HTTPSConnectionPool)

* erikcederstrand <http://code.google.com/u/erikcederstrand/>
  * NTLM-authenticated HTTPSConnectionPool
  * Basic-authenticated HTTPSConnectionPool (merged into make_headers)

* niphlod <niphlod@gmail.com>
  * Client-verified SSL certificates for HTTPSConnectionPool
  * Response gzip and deflate encoding support
  * Better unicode support for filepost using StringIO buffers

* btoconnor <brian@btoconnor.net>
  * Non-multipart encoding for POST requests

* p.dobrogost <http://code.google.com/u/@WBRSRIBZDhBFXQB6/>
  * Code review, PEP8 compliance, benchmark fix

* kennethreitz <me@kennethreitz.com>
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* georgemarshall <https://github.com/georgemarshall>
  * Bugfixes, Improvements and Test coverage

* Thomas Kluyver <thomas@kluyver.me.uk>
* Python 3 support

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  * Design review, bugfixes, test coverage.

* studer <theo.studer@gmail.com>
  * IPv6 url support and test coverage

* Shivaram Lingamneni <slingamn@cs.stanford.edu>
  * Support for explicitly closing pooled connections

* hartator <hartator@gmail.com>
  * Corrected multipart behavior for params

* Thomas Weischuh <thomas@t-8ch.de>
  * Support for TLS SNI
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  * Bugfixes in testsuite

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  * Correct six.moves conflict
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* Boris Figovsky <boris.figovsky@ravellosystems.com>
  * Allowed to skip SSL hostname verification

* Cory Benfield <https://lukasa.co.uk/about/>
  * Stream method for Response objects.
  * Return native strings in header values.
  * Generate 'Host' header when using proxies.

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  * Add missing WrappedSocket.fileno method in PyOpenSSL

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  * Fixed a race condition

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  * Added HTTPS (CONNECT) proxy support

* Stephen Holsapple <sholsapp@gmail.com>
* Added abstraction for granular control of request fields

* Martin von Gagern <Martin.vGagern@gmx.net>
* Support for non-ASCII header parameters

* Kevin Burke <kev@inburke.com> and Pavel Kirichenko <juanych@yandex-team.ru>
* Support for separate connect and request timeouts

* Peter Waller <p@pwaller.net>
* HTTPResponse.tell() for determining amount received over the wire

* Nipunn Koorapati <nipunn1313@gmail.com>
* Ignore default ports when comparing hosts for equality

* Danilo @dbrgn <https://dbrgn.ch/>
* Disabled TLS compression by default on Python 3.2+
* Disabled TLS compression in pyopenssl contrib module
* Configurable cipher suites in pyopenssl contrib module

* Roman Bogorodskiy <roman.bogorodskiy@ericsson.com>
* Account retries on proxy errors

* Nicolas Delaby <nicolas.delaby@ezeep.com>
* Use the platform-specific CA certificate locations

* Josh Schneier <https://github.com/jschneier>
* HTTPHeaderDict and associated tests and docs
* Bugfixes, docs, test coverage

* Tahia Khan <http://tahia.tk/>
* Added Timeout examples in docs

* Arthur Grunseid <https://grunseid.com>
* source_address support and tests (with https://github.com/bui)

* Ian Cordasco <graaffatcolmingov@gmail.com>
* PEP8 Compliance and Linting
* Add ability to pass socket options to an HTTP Connection

* Erik Tollerud <erik.tollerud@gmail.com>
* Support for standard library io module.

* Krishna Prasad <kprasad.iitd@gmail.com>
* Google App Engine documentation

* Aaron Meurer <asmeurer@gmail.com>
* Added Url.url, which unparses a Url
* Evgeny Kapun <abacabadabacaba@gmail.com>
  * Bugfixes

* Benjamen Meyer <bm_witness@yahoo.com>
  * Security Warning Documentation update for proper capture

* Shivan Sornarajah <github@sornars.com>
  * Support for using ConnectionPool and PoolManager as context managers.

* Alex Gaynor <alex.gaynor@gmail.com>
  * Updates to the default SSL configuration

* Tomas Tomecek <ttomecek@redhat.com>
  * Implemented generator for getting chunks from chunked responses.

* tlynn <https://github.com/tlynn>
  * Respect the warning preferences at import.

* David D. Riddle <ddriddle@illinois.edu>
  * IPv6 bugfixes in testsuite

* Thea Flowers <magicalgirl@google.com>
  * App Engine environment tests.
  * Documentation re-write.

* John Krauss <https://github.com/talos>
  * Clues to debugging problems with `cryptography` dependency in docs

* Disassem <https://github.com/Disassem>
  * Fix pool-default headers not applying for url-encoded requests like GET.

* James Atherfold <jlatherfold@hotmail.com>
  * Bugfixes relating to cleanup of connections during errors.

* Christian Pedersen <https://github.com/chripede>
  * IPv6 HTTPS proxy bugfix

* Jordan Moldow <https://github.com/jmoldow>
  * Fix low-level exceptions leaking from `HTTPResponse.stream()`.
  * Bugfix for `ConnectionPool.urlopen(release_conn=False)`.
  * Creation of `HTTPConnectionPool.ResponseCls`.

* Predrag Gruevski <https://github.com/obi1kenobi>
  * Made cert digest comparison use a constant-time algorithm.

* Adam Talsma <https://github.com/a-tal>
  * Bugfix to ca_cert file paths.
* Evan Meagher <https://evanmeagher.net>
  * Bugfix related to \texttt{memoryview}\ usage in PyOpenSSL adapter

* John Vandenberg <jayvdb@gmail.com>
  * Python 2.6 fixes; pyflakes and pep8 compliance

* Andy Caldwell <andy.m.caldwell@googlemail.com>
  * Bugfix related to reusing connections in indeterminate states.

* Ville Skytt <ville.skytta@iki.fi>
  * Logging efficiency improvements, spelling fixes, Travis config.

* Shige Takeda <smtakeda@gmail.com>
  * Started Recipes documentation and added a recipe about handling concatenated gzip data in HTTP response

* Jess Shapiro <jesse@jesseshapiro.net>
  * Various character-encoding fixes/tweaks
  * Disabling IPv6 DNS when IPv6 connections not supported

* David Foster <http://dafoster.net/>
  * Ensure order of request and response headers are preserved.

* Jeremy Cline <jeremy@jcline.org>
  * Added connection pool keys by scheme

* Aviv Palivoda <palaviv@gmail.com>
  * History list to Retry object.
  * HTTPResponse contains the last Retry object.

* Nate Prewitt <nate.prewitt@gmail.com>
  * Ensure timeouts are not booleans and greater than zero.
  * Fixed infinite loop in \texttt{``stream``} when \texttt{amt=None}.
  * Added \texttt{length\_remaining} to determine remaining data to be read.
  * Added \texttt{enforce\_content\_length} to raise exception when incorrect \texttt{content\_length} received.

* Seth Michael Larson <sethmichaellarson@protonmail.com>
  * Created selectors backport that supports PEP 475.

* Alexandre Dias <alex.dias@smarkets.com>
  * Don't retry on timeout if method not in whitelist

* Moinuddin Quadri <moin18@gmail.com>
  * Lazily load idna package

* Tom White <s6yg1ez3@mail2tor.com>
  * Made SOCKS handler differentiate socks5h from socks5 and socks4a from socks4.

* Tim Burke <tim.burke@gmail.com>
* Stop buffering entire deflate-encoded responses.

* Tuukka Mustonen <tuukka.mustonen@gmail.com>
  * Add counter for status_forcelist retries.

* Erik Rose <erik@mozilla.com>
  * Bugfix to pyopenssl vending

* Wolfgang Richter <wolfgang.richter@gmail.com>
  * Bugfix related to loading full certificate chains with PyOpenSSL backend.

* Mike Miller <github@mikeage.net>
  * Logging improvements to include the HTTP(S) port when opening a new connection

* Ioannis Tziakos <mail@itziakos.gr>
  * Fix `util.selectors._fileobj_to_fd` to accept `long`.
  * Update appveyor tox setup to use the 64bit python.

* Akamai (through Jess Shapiro) <jshapiro@akamai.com>
  * Ongoing maintenance; 2017-2018

* Dominique Leuenberger <dimstar@opensuse.org>
  * Minor fixes in the test suite

* Will Bond <will@wbond.net>
  * Add Python 2.6 support to `contrib.securetransport`

* Aleksei Alekseev <alekseev.yeskela@gmail.com>
  * using auth info for socks proxy

* Chris Wilcox <git@crwilcox.com>
  * Improve contribution guide
  * Add `HTTPResponse.geturl` method to provide `urllib2.urlopen().geturl()` behavior

* Bruce Merry <https://www.brucemerry.org.za>
  * Fix leaking exceptions when system calls are interrupted with zero timeout

* Hugo van Kemenade <https://github.com/hugovk>
  * Drop support for EOL Python 2.6

* Tim Bell <https://github.com/timb07>
  * Bugfix for responses with Content-Type: message/* logging warnings

* Justin Bramley <https://github.com/jbramleycl>
  * Add ability to handle multiple Content-Encodings

* Katsuhiko YOSHIDA <https://github.com/kyoshidajp>
  * Remove Authorization header regardless of case when redirecting to cross-site
* James Meickle (<https://permadeath.com/>)
  * Improve handling of Retry-After header

* Chris Jerdonek (<chris.jerdonek@gmail.com>)
  * Remove a spurious TypeError from the exception chain inside HTTPConnectionPool._make_request(), also for BaseExceptions.

* Jorge Lopez Silva (<https://github.com/jalopezsilva>)
  * Added support for forwarding requests through HTTPS proxies.

* Benno Rice (<benno@jeamland.net>)
  * Allow cadata parameter to be passed to underlying `SSLContext.load_verify_locations()`.

* Keiichi Kobayashi (<abok.1k@gmail.com>)
  * Rename VerifiedHTTPSConnection to HTTPSConnection

* Himanshu Garg (<garg_himanshu@outlook.com>)
  * DOC & LICENSE Update

* Hod Bin Noon (<bin.noon.hod@gmail.com>)
  * Test improvements

* Chris Olufson (<tycarac@gmail.com>)
  * Fix for connection not being released on HTTP redirect and response not preloaded

* [Bastiaan Bakker] (<https://github.com/bastiaanb>)
  * Support for logging session keys via environment variable `SSLKEYLOGFILE` (Python 3.8+)

* [Ezzeri Esa] (<https://github.com/savarin>)
  * Ports and extends on types from typeshed

* [Your name or handle] (<[email or website]>)
  * [Brief summary of your changes]

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 * Rob Earhart
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1.1140 wildfly-webservices-server-integration

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1.1142 wildfly-microprofile-health-smallrye

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* org.eclipse.jetty.orbit:org.eclipse.jdt.core

The following artifacts are EPL and ASL2.
* org.eclipse.jetty.orbit:javax.security.auth.message

The following artifacts are EPL and CDDL 1.0.
* org.eclipse.jetty.orbit:javax.mail.glassfish
Oracle

The following artifacts are CDDL + GPLv2 with classpath exception. https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

* javax.servlet:javax.servlet-api
* javax.annotation:javax.annotation-api
* javax.transaction:javax.transaction-api
* javax.websocket:javax.websocket-api

Oracle OpenJDK

If ALPN is used to negotiate HTTP/2 connections, then the following artifacts may be included in the distribution or downloaded when ALPN module is selected.

* java.sun.security.ssl

These artifacts replace/modify OpenJDK classes. The modifications are hosted at github and both modified and original are under GPL v2 with classpath exceptions. http://openjdk.java.net/legal/gplv2+ce.html

OW2

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org.ow2.asm:asm-commons
org.ow2.asm:asm

Apache

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org.apache.taglibs:taglibs-standard-spec
org.apache.taglibs:taglibs-standard-impl
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org.mortbay.jasper:apache-jsp
org.apache.tomcat:tomcat-jasper
org.apache.tomcat:tomcat-juli
org.apache.tomcat:tomcat-jsp-api
org.apache.tomcat:tomcat-el-api
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-api
org.apache.tomcat:tomcat-util-scan
org.apache.tomcat:tomcat-util

org.mortbay.jasper:apache-el
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-el-api

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The following artifacts are CDDL + GPLv2 with classpath exception.

https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

org.eclipse.jetty.toolchain:jetty-schemas

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Assorted

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1.1159 resteasy-json-binding-provider

3.13.2.Final

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## The Unicode Standard, Unicode Character Database, Version 13.0.0

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<tr>
<td>Main Mesa code</td>
<td>src/mesa/</td>
<td>MIT</td>
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<tr>
<td>Device drivers</td>
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<td>MIT, generally</td>
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Gallium code    src/gallium/    MIT

Ext headers    GL/glext.h    Khronos
                GL/xext.h    Khronos
                GL/wglexxt.h    Khronos
                KHR/khrplatform.h    Khronos

***************************************************************************

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include/GL/g1.h :

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include/GL/xlext.h
include/GL/wglexxt.h :

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1.1171 jopt-simple 5.0.4

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1.1172 debian-archive-keyring

2019.1+deb10u1

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Version: 1.3.3
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You must pass in the refresh token and authenticate the client if it is not public.

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#
org.keycloak.exportimport.KeycloakClientDescriptionConverter
org.keycloak.protocol.oidc.OIDCClientDescriptionConverterFactory
org.keycloak.protocol.saml.EntityDescriptorDescriptionConverter

Found in path(s):
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/META-INF/services/org.keycloak.exportimport.ClientDescriptionConverterFactory
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#
org.keycloak.executors.DefaultExecutorsProviderFactory

Found in path(s):
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources.jar/META-INF/services/org.keycloak.executors.ExecutorsProviderFactory

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org.keycloak.locale.DefaultLocaleUpdaterProviderFactory
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#
org.keycloak.protocol.oidc.installation.KeycloakOIDCClientInstallation
org.keycloak.protocol.oidc.installation.KeycloakOIDCJbossSubsystemClientCliInstallation
org.keycloak.protocol.oidc.installation.KeycloakOIDCJbossSubsystemClientInstallation
org.keycloak.protocol.oidc.installation.KeycloakOIDCJbossSubsystemInstallation
org.keycloak.protocol.saml.installation.KeycloakSamlClientInstallation
org.keycloak.protocol.saml.installation.KeycloakSamlSubsystemClientInstallation
org.keycloak.protocol.saml.installation.KeycloakSamlSubsystemInstallation
org.keycloak.protocol.docker.installation.DockerVariableOverrideInstallationProvider
org.keycloak.protocol.docker.installation.DockerRegistryConfigFileInstallationProvider
org.keycloak.protocol.docker.installation.DockerComposeYamlInstallationProvider

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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
jar/org/keycloak/crypto/ES512ClientSignatureVerifierProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
jar/org/keycloak/services/resources/admin/AdminEventBuilder.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
jar/org/keycloak/crypto/AsymmetricClientSignatureVerifierProvider.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
jar/org/keycloak/crypto/RS256ClientSignatureVerifierProviderFactory.java
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jar/org/keycloak/broker/oidc/mappers/ExternalKeycloakRoleToRoleMapper.java
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jar/org/keycloak/protocol/oidc/endpoints/LoginStatusIframeEndpoint.java
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jar/org/keycloak/protocol/openshift/OpenShiftTokenReviewEndpoint.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
jar/org/keycloak/services/DefaultKeycloakSessionFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
jar/org/keycloak/services/ErrorResponse.java
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jar/org/keycloak/theme/beans/AdvancedMessageFormatterMethod.java
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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/email/DefaultEmailSenderProviderFactory.java
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org.keycloak.timer.basic.BasicTimerProviderFactory

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#
org.keycloak.keys.GeneratedHmacKeyProviderFactory
org.keycloak.keys.GeneratedAesKeyProviderFactory
org.keycloak.keys.GeneratedRsaKeyProviderFactory
org.keycloak.keys.JavaKeystoreKeyProviderFactory
org.keycloak.keys.ImportedRsaKeyProviderFactory
org.keycloak.keys.GeneratedEcdsaKeyProviderFactory

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org.keycloak.authentication.forms.RegistrationPage

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#

org.keycloak.forms.login.freemarker.FreeMarkerLoginFormsProviderFactory

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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/META-INF/services/org.keycloak.forms.login.LoginFormsProviderFactory
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org.keycloak.exportimport.dir.DirExportProviderFactory
org.keycloak.exportimport.singlefile.SingleFileExportProviderFactory

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org.keycloak.storage.openshiftOpenshiftClientStorageProviderFactory

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org.keycloak.events.email.EmailEventListenerProviderFactory
org.keycloak.events.log.JBossLoggingEventListenerProviderFactory

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org.keycloak.truststore.FileTruststoreProviderFactory

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org.keycloak.services.managers.DefaultBruteForceProtectorFactory

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#
org.keycloak.forms.account.freemarker.FreeMarkerAccountProviderFactory

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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak/services-12-0-2-sources-jar/org/keycloak/authorization/protection/introspect/RPTIntrospectionProvider.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak/services-12-0-2-sources-jar/org/keycloak/authorization/protection/introspect/RPTIntrospectionProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak/services-12-0-2-sources-jar/org/keycloak/protocol/oidc/AccessTokenIntrospectionProvider.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak/services-12-0-2-sources-jar/org/keycloak/protocol/oidc/AccessTokenIntrospectionProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak/services-12-0-2-sources-jar/org/keycloak/protocol/oidc/RefreshTokenIntrospectionProvider.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak/services-12-0-2-sources-jar/org/keycloak/protocol/oidc/RefreshTokenIntrospectionProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak/services-12-0-2-sources-jar/org/keycloak/protocol/oidc/RefreshTokenIntrospectionProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak/services-12-0-2-sources-jar/org/keycloak/protocol/oidc/AccessTokenIntrospectionProvider.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak/services-12-0-2-sources-jar/org/keycloak/protocol/oidc/AccessTokenIntrospectionProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak/services-12-0-2-sources-jar/org/keycloak/authorization/config/UmaWellKnownProviderFactory.java

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org.keycloak.email.freemarker.FreeMarkerEmailTemplateProviderFactory

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org.keycloak.locale.DefaultLocaleSelectorProviderFactory

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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/credential/AttestationStatementConverter.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authentication/requiredactions/WebAuthnRegister.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/credential/AAGUIDConverter.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/credential/WebAuthnCredentialProvider.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/credential/WebAuthnCredentialProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authentication/authenticators/browser/WebAuthnAuthenticator.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/credential/AttestationStatementSerializationContainer.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/credential/WebAuthnCredentialModelInput.java
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org.keycloak.broker.provider.HardcodedRoleMapper
org.keycloak.broker.provider.HardcodedAttributeMapper
org.keycloak.broker.provider.HardcodedUserSessionAttributeMapper
org.keycloak.broker.oidc.mappers.ClaimToRoleMapper
org.keycloak.broker.oidc.mappers.AdvancedClaimToRoleMapper
org.keycloak.broker.oidc.mappers.ExternalKeycloakRoleToRoleMapper
org.keycloak.broker.oidc.mappers.UserAttributeMapper
org.keycloak.broker.oidc.mappers.UsernameTemplateMapper
org.keycloak.broker.saml.mappers.AdvancedAttributeToRoleMapper
org.keycloak.broker.saml.mappers.AttributeToRoleMapper
org.keycloak.broker.saml.mappers.UserAttributeMapper
org.keycloak.broker.saml.mappers.UsernameTemplateMapper
org.keycloak.social.facebook.FacebookUserAttributeMapper
org.keycloak.social.github.GitHubUserAttributeMapper
org.keycloak.social.paypal.PayPalUserAttributeMapper
org.keycloak.social.google.GoogleUserAttributeMapper
org.keycloak.social.linkedin.LinkedInUserAttributeMapper
org.keycloak.social.stackoverflow.StackoverflowUserAttributeMapper
org.keycloak.social.microsoft.MicrosoftUserAttributeMapper
org.keycloak.social.instagram.InstagramUserAttributeMapper

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org.keycloak.protocol.oidc.OIDCLoginProtocolFactory
org.keycloak.protocol.saml.SamlProtocolFactory
org.keycloak.protocol.docker.DockerAuthV2ProtocolFactory

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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/validation/DefaultClientValidationProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/vault/DefaultVaultCharSecret.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/protocol/oidc/mappers/DeployedScriptOIDCProtocolMapper.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/services/util/JsonConfigProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/vault/VaultNotFoundException.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/provider/DeploymentProviderLoader.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/crypto/PS384ClientSignatureVerifierProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/platform/PlatformProvider.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/config/ConfigProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/platform/Platform.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/crypto/PS256SignatureProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/crypto/PS256ClientSignatureVerifierProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/crypto/PS384SignatureProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/vault/AbstractVaultProvider.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/vault/AbstractVaultProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/protocol/saml/mappers/SAMLAudienceResolveProtocolMapper.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/crypto/PS512SignatureProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/vault/AbstractVaultProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authentication/authenticators/browser/DeployedScriptAuthenticatorFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/protocol/saml/mappers/SAMLAudienceProtocolMapper.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/vault/VaultConfigurationException.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/vault/DefaultVaultTranscriber.java
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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/services/scheduled/ClearExpiredClientInitialAccessTokens.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/utils/RoleResolveUtil.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/keys/GeneratedAesKeyProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/crypto/JavaAlgorithmHashProvider.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/connections/httpclient/ProxyMappings.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/services/resources/admin/ClientScopeEvaluateScopeMappingsResource.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/services/managers/AuthSessionId.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/protocol/oidc/utils/OAuth2Code.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/keys/AbstractGeneratedSecretKeyProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/services/managers/UserSessionCrossDCManager.java
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org.keycloak.authentication.authenticators.browser.CookieAuthenticatorFactory
org.keycloak.authentication.authenticators.browser.UsernamePasswordFormFactory
org.keycloak.authentication.authenticators.browser.UsernameFormFactory
org.keycloak.authentication.authenticators.browser.PasswordFormFactory
org.keycloak.authentication.authenticators.browser.OTPFormAuthenticatorFactory
org.keycloak.authentication.authenticators.browser.ScriptBasedAuthenticatorFactory
org.keycloak.authentication.authenticators.browser.SpnegoAuthenticatorFactory
org.keycloak.authentication.authenticators.browser.IdentityProviderAuthenticatorFactory
org.keycloak.authentication.authenticators.conditional.ConditionalRoleAuthenticatorFactory
org.keycloak.authentication.authenticators.conditional.ConditionalUserConfiguredAuthenticatorFactory
org.keycloak.authentication.authenticators.directgrant.ValidateOTP
org.keycloak.authentication.authenticators.directgrant.ValidatePassword
org.keycloak.authentication.authenticators.directgrant.ValidateUsername
org.keycloak.authentication.authenticators.resetcred.ResetCredentialChooseUser
org.keycloak.authentication.authenticators.resetcred.ResetCredentialEmail
org.keycloak.authentication.authenticators.resetcred.ResetOTP
org.keycloak.authentication.authenticators.directgrant.ValidateUsername
org.keycloak.authentication.authenticators.broker.IdpReviewProfileAuthenticatorFactory
org.keycloak.authentication.authenticators.broker.IdpCreateUserIfUniqueAuthenticatorFactory
org.keycloak.authentication.authenticators.broker.IdpConfirmLinkAuthenticatorFactory
org.keycloak.authentication.authenticators.broker.IdpEmailVerificationAuthenticatorFactory
org.keycloak.authentication.authenticators.broker.IdpUsernamePasswordFormFactory
org.keycloak.authentication.authenticators.broker.IdpAutoLinkAuthenticatorFactory
org.keycloak.authentication.authenticators.browser.ConditionalOtpFormAuthenticatorFactory
org.keycloak.protocol.saml.profile.ecp.authenticator.HttpBasicAuthenticatorFactory
org.keycloak.authentication.authenticators.x509.X509ClientCertificateAuthenticatorFactory
org.keycloak.authentication.authenticators.x509.ValidateX509CertificateUsernameFactory
org.keycloak.protocol.docker.DockerAuthenticatorFactory
org.keycloak.authentication.authenticators.console.ConsoleUsernamePasswordAuthenticatorFactory
org.keycloak.authentication.authenticators.challenge.BasicAuthOTPAuthenticatorFactory
org.keycloak.authentication.authenticators.challenge.NoCookieFlowRedirectAuthenticatorFactory
org.keycloak.authentication.authenticators.browser.WebAuthnAuthenticatorFactory
org.keycloak.authentication.authenticators.browser.WebAuthnPasswordlessAuthenticatorFactory

Found in path(s):
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/META-INF/services/org.keycloak.authentication.AuthenticatorFactory
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org.keycloak.services.x509.DefaultClientCertificateLookupFactory
org.keycloak.services.x509.HaProxySslClientCertificateLookupFactory
org.keycloak.services.x509.ApacheProxySslClientCertificateLookupFactory
org.keycloak.services.x509.NginxProxySslClientCertificateLookupFactory

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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/META-INF/services/org.keycloak.services.x509.X509ClientCertificateLookupFactory
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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/services/x509/ApacheProxySslClientCertificateLookupFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/services/x509/DefaultClientCertificateLookup.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/services/x509/X509ClientCertificateLookupFactory.java

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org.keycloak.authorization.DefaultAuthorizationProviderFactory

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#
org.keycloak.authentication.authenticators.client.ClientIdAndSecretAuthenticator
org.keycloak.authentication.authenticators.client.JWTClientAuthenticator
org.keycloak.authentication.authenticators.client.JWTClientSecretAuthenticator
org.keycloak.authentication.authenticators.client.X509ClientAuthenticator

Found in path(s):
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/META-INF/services/org.keycloak.authentication.ClientAuthenticatorFactory

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#
org.keycloak.protocol.oidc.mappers.UserAttributeMapper
org.keycloak.protocol.oidc.mappers.FullNameMapper
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org.keycloak.provider.DefaultProviderLoaderFactory
org.keycloak.provider.FileSystemProviderLoaderFactory

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#
org.keycloak.broker.oidc.OIDCIdentityProviderFactory
org.keycloak.broker.oidc.KeycloakOIDCIdentityProviderFactory
org.keycloak.broker.saml.SAMLIdentityProviderFactory

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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/META-INF/services/org.keycloak.broker.identityprovider.IdentityProviderFactory
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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/protection/ProtectionService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/PolicyEvaluationService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/ResourceServerService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/DefaultEvaluationContext.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/PermissionService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/ResourceSetService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/PolicyService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/ScopeService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/AuthorizationService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/ErrorCodes.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/DefaultAuthorizationProviderFactory.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/PermissionTicketService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/AuthorizationService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/ScopeService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/AuthorizationService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/ScopeService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/Policy/services/UserManagedPermissionService.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/authorization/admin/ScopeService.java

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org.keycloak.social.facebook.FacebookIdentityProviderFactory
org.keycloak.social.paypal.PayPalIdentityProviderFactory
org.keycloak.social.github.GitHubIdentityProviderFactory
org.keycloak.social.google.GoogleIdentityProviderFactory
org.keycloak.social.linkedin.LinkedInIdentityProviderFactory
org.keycloak.social.stackoverflow.StackoverflowIdentityProviderFactory
org.keycloak.social.twitter.TwitterIdentityProviderFactory
org.keycloak.social.microsoft.MicrosoftIdentityProviderFactory
org.keycloak.social.openshift.OpenShiftV3IdentityProviderFactory
org.keycloak.social.openshift.OpenShiftV4IdentityProviderFactory
org.keycloak.social.gitlab.GitLabIdentityProviderFactory
org.keycloak.social.bitbucket.BitbucketIdentityProviderFactory
org.keycloak.social.instagram.InstagramIdentityProviderFactory

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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
ar/jar/org/keycloak/authentication/actiontoken/resetcred/ResetCredentialsActionToken.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
ar/jar/org/keycloak/authentication/actiontoken/DefaultActionTokenKey.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
ar/jar/org/keycloak/services/resources/LoginActionsServiceChecks.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
ar/jar/org/keycloak/authentication/actiontoken/DefaultActionToken.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
ar/jar/org/keycloak/authentication/actiontoken/TokenUtils.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
ar/jar/org/keycloak/authentication/actiontoken/ExplainedTokenVerificationException.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
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ar/jar/org/keycloak/authentication/actiontoken/IdpVerifyAccountLinkActionToken.java
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ar/jar/org/keycloak/services/resources/LoginActionsServiceException.java
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ar/jar/org/keycloak/services/resources/LoginActionsServiceException.java
* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-
ar/jar/org/keycloak/services/resources/LoginActionsServiceException.java

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#
org.keycloak.authentication.requiredactions.UpdatePassword
org.keycloak.authentication.requiredactions.UpdateProfile
org.keycloak.authentication.requiredactions.UpdateTotp
org.keycloak.authentication.requiredactions.VerifyEmail
org.keycloak.authentication.requiredactions.TermsAndConditions
org.keycloak.authentication.requiredactions.WebAuthnRegisterFactory
org.keycloak.authentication.requiredactions.WebAuthnPasswordlessRegisterFactory
org.keycloak.authentication.requiredactions.UpdateUserLocaleAction
org.keycloak.authentication.requiredactions.DeleteAccount

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org.keycloak.services.clientregistration.policy.impl.TrustedHostClientRegistrationPolicyFactory
org.keycloak.services.clientregistration.policy.impl.ConsentRequiredClientRegistrationPolicyFactory
org.keycloak.services.clientregistration.policy.impl.ProtocolMappersClientRegistrationPolicyFactory
org.keycloak.services.clientregistration.policy.impl.ClientScopesClientRegistrationPolicyFactory
org.keycloak.services.clientregistration.policy.impl.ScopeClientRegistrationPolicyFactory
org.keycloak.services.clientregistration.policy.impl.ClientDisabledClientRegistrationPolicyFactory
org.keycloak.services.clientregistration.policy.impl.MaxClientsClientRegistrationPolicyFactory

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#
org.keycloak.connections.httpclient.DefaultHttpClientFactory

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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/META-INF/services/org.keycloak.connections.httpclient.HttpClientFactory
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org.keycloak.authentication.forms.RegistrationProfile
org.keycloak.authentication.forms.RegistrationUserCreation
org.keycloak.authentication.forms.RegistrationRecaptcha

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org.keycloak.exportimport.ClientDescriptionConverterSpi
org.keycloak.wellknown.WellKnownSpi
org.keycloak.services.clientregistration.ClientRegistrationSpi
org.keycloak.services.clientregistration.policy.ClientRegistrationPolicySpi
org.keycloak.authentication.actiontoken.ActionTokenHandlerSpi
org.keycloak.services.x509.X509CertificateLookupSpi
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org.keycloak.protocol.saml.preprocessor.SamlAuthenticationPreprocessorSpi
org.keycloak.encoding.ResourceEncodingSpi

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#
org.keycloak.theme.JarThemeProviderFactory
org.keycloak.theme.FolderThemeProviderFactory

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org.keycloak.userprofile.LegacyUserProfileProviderFactory

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* /opt/cola/permits/1130030773_1612433060.44/0/keycloak-services-12-0-2-sources-jar/org/keycloak/crypto/Aes128GcmContentEncryptionProviderFactory.java
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#
org.keycloak.protocol.oidc.OIDCWellKnownProviderFactory

org.keycloak.authorization.config.UmaWellKnownProviderFactory

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org.keycloak.crypto.SHA256HashProviderFactory
org.keycloak.crypto.SHA384HashProviderFactory
org.keycloak.crypto.SHA512HashProviderFactory

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PCRE LICENCE

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PCRE is a library of functions to support regular expressions whose syntax and semantics are as close as possible to those of the Perl 5 language.

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The basic library functions are written in C and are freestanding. Also included in the distribution is a set of C++ wrapper functions, and a just-in-time compiler that can be used to optimize pattern matching. These are both optional features that can be omitted when the library is built.

THE BASIC LIBRARY FUNCTIONS

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PCRE JUST-IN-TIME COMPILATION SUPPORT
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numbered 2 because it goes with version 2 of the ordinary GPL.]

Preamble

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1.1192 wildfly-mod-cluster-extension

21.0.2.Final

1.1192.1 Available under license:

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1.1193 wildfly-client-all 21.0.2.Final

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Found in path(s):
* /opt/cola/permits/1136416130_1613765682.8/0/jakarta-enterprise-cdi-api-2-0-2-2-jar/beans_1_0.xsd
* /opt/cola/permits/1136416130_1613765682.8/0/jakarta-enterprise-cdi-api-2-0-2-2-jar/beans_1_1.xsd
No license file was found, but licenses were detected in source scan.

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* /opt/cola/permits/1136416130_1613765682.8/0/jakarta-enterprise-cdi-api-2.0-2.2.jar/META-INF/maven/jakarta.enterprise/jakarta.enterprise.cdi-api/pom.xml
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Manifest-Version: 1.0
Bundle-Description: APIs for Jakarta CDI (Contexts and Dependency Injection)
Bundle-License: https://repository.jboss.org/licenses/apache-2.0.txt
Bundle-SymbolicName: jakarta.enterprise.cdi-api
Archiver-Version: Plexus Archiver
Built-By: default
Bnd-LastModified: 1565451400486
Bundle-ManifestVersion: 2
Bundle-Document: https://jakarta.ee
Bundle-Vendor: Eclipse Foundation
Import-Package: javax.el;version="2.2",javax.inject,javax.interceptor;
version="[1.2,2)"
Require-Capability: osgi.ee;filter="(&(osgi.ee=JavaSE)(version=1.8))"
Tool: Bnd-2.4.1.201501161923
Export-Package: javax.decorator;version="2.0",uses:="javax.enterprise.
inject",javax.enterprise.context;version="2.0",uses:="javax.enterpris
e.util",javax.inject",javax.enterprise.context.control;version="2.0",u
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1.1195 picketbox 5.0.3.Final-redhat-00006
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1.1206 musl 1.1.20-r4

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import io
import re

from setuptools import setup

with io.open("README.rst", "rt", encoding="utf8") as f:
    readme = f.read()

with io.open("flask_sqlalchemy/__init__.py", "rt", encoding="utf8") as f:
    version = re.search(r'^__version__ = "(.*)"', f.read(), re.M).group(1)

setup(
    name="Flask-SQLAlchemy",
    version=version,
    url="https://github.com/pallets/flask-sqlalchemy",
    project_urls={
        "Documentation": "https://flask-sqlalchemy.palletsprojects.com/",
        "Issue tracker": "https://github.com/pallets/flask-sqlalchemy/issues",
    },
    license="BSD-3-Clause",
    author="Armin Ronacher",
    author_email="armin.ronacher@active-4.com",
    maintainer="Pallets",
    maintainer_email="contact@palletsprojects.com",
    description="adds SQLAlchemy support to your Flask application.",
    long_description=readme,
    packages=['flask_sqlalchemy'],
    include_package_data=True,
    python_requires=">= 2.7, != 3.0.*, != 3.1.*, != 3.2.*, != 3.3.*",
    install_requires=['Flask>=0.10', 'SQLAlchemy>=0.8.0'],
    classifiers=[
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        "Environment :: Web Environment",
        "Intended Audience :: Developers",
        "License :: OSI Approved :: BSD License",
        "Operating System :: OS Independent",
        "Programming Language :: Python",
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        "Programming Language :: Python :: 3.7",
        "Programming Language :: Python :: Implementation :: CPython",
        "Programming Language :: Python :: Implementation :: PyPy",
        "Topic :: Internet :: WWW/HTTP :: Dynamic Content",
        ]
)
Declaring Models
=============

Generally Flask-SQLAlchemy behaves like a properly configured declarative base from the :mod:`sqlalchemy.ext.declarative` extension. As such we recommend reading the SQLAlchemy docs for a full reference. However the most common use cases are also documented here.

Things to keep in mind:

- The baseclass for all your models is called `db.Model`. It's stored on the SQLAlchemy instance you have to create. See :ref:`quickstart` for more details.
- Some parts that are required in SQLAlchemy are optional in Flask-SQLAlchemy. For instance the table name is automatically set for you unless overridden. It's derived from the class name converted to lowercase and with “CamelCase” converted to “camel_case”. To override the table name, set the `__tablename__` class attribute.

Simple Example
-----------

A very simple example:

```python
class User(db.Model):
    id = db.Column(db.Integer, primary_key=True)
    username = db.Column(db.String(80), unique=True, nullable=False)
    email = db.Column(db.String(120), unique=True, nullable=False)

    def __repr__(self):
        return '<User %r>' % self.username
```

Use `class:`~sqlalchemy.schema.Column` to define a column. The name of the column is the name you assign it to. If you want to use a different name in the table you can provide an optional first argument which is a string.
with the desired column name. Primary keys are marked with `primary_key=True`. Multiple keys can be marked as primary keys in which case they become a compound primary key.

The types of the column are the first argument to :class:`~sqlalchemy.schema.Column`. You can either provide them directly or call them to further specify them (like providing a length). The following types are the most common:

```
========================================================================================================
<table>
<thead>
<tr>
<th>Class</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>~sqlalchemy.types.Integer</td>
<td>an integer</td>
</tr>
<tr>
<td>~sqlalchemy.types.String(size)</td>
<td>a string with a maximum length (optional in some databases, e.g. PostgreSQL)</td>
</tr>
<tr>
<td>~sqlalchemy.types.Text</td>
<td>some longer unicode text</td>
</tr>
<tr>
<td>~sqlalchemy.types.DateTime</td>
<td>date and time expressed as Python :class:<code>~datetime.datetime</code> object.</td>
</tr>
<tr>
<td>~sqlalchemy.types.Float</td>
<td>stores floating point values</td>
</tr>
<tr>
<td>~sqlalchemy.types.Boolean</td>
<td>stores a boolean value</td>
</tr>
<tr>
<td>~sqlalchemy.types.PickleType</td>
<td>stores a pickled Python object</td>
</tr>
<tr>
<td>~sqlalchemy.types.LargeBinary</td>
<td>stores large arbitrary binary data</td>
</tr>
</tbody>
</table>
```

One-to-Many Relationships
-------------------------

The most common relationships are one-to-many relationships. Because relationships are declared before they are established you can use strings to refer to classes that are not created yet (for instance if `Person` defines a relationship to `Address` which is declared later in the file).

Relationships are expressed with the :func:`~sqlalchemy.orm.relationship` function. However the foreign key has to be separately declared with the :class:`~sqlalchemy.schema.ForeignKey` class::

```python
class Person(db.Model):
    id = db.Column(db.Integer, primary_key=True)
    name = db.Column(db.String(50), nullable=False)
    addresses = db.relationship('Address', backref='person', lazy=True)

class Address(db.Model):
    id = db.Column(db.Integer, primary_key=True)
    email = db.Column(db.String(120), nullable=False)
    person_id = db.Column(db.Integer, db.ForeignKey('person.id'), nullable=False)
```
What does :func:`db.relationship() <sqlalchemy.orm.relationship>` do? That function returns a new property that can do multiple things. In this case we told it to point to the `Address` class and load multiple of those. How does it know that this will return more than one address? Because SQLAlchemy guesses a useful default from your declaration. If you would want to have a one-to-one relationship you can pass `uselist=False` to :func:`~sqlalchemy.orm.relationship`.

Since a person with no name or an email address with no address associated makes no sense, `nullable=False` tells SQLAlchemy to create the column as `NOT NULL`. This is implied for primary key columns, but it's a good idea to specify it for all other columns to make it clear to other people working on your code that you did actually want a nullable column and did not just forget to add it.

So what do `backref` and `lazy` mean? `backref` is a simple way to also declare a new property on the `Address` class. You can then also use `my_address.person` to get to the person at that address. `lazy` defines when SQLAlchemy will load the data from the database:

- ``'select'`` / ``True`` (which is the default, but explicit is better than implicit) means that SQLAlchemy will load the data as necessary in one go using a standard select statement.
- ``'joined'`` / ``False`` tells SQLAlchemy to load the relationship in the same query as the parent using a ``JOIN`` statement.
- ``'subquery'`` works like ``'joined'`` but instead SQLAlchemy will use a subquery.
- ``'dynamic'`` is special and can be useful if you have many items and always want to apply additional SQL filters to them. Instead of loading the items SQLAlchemy will return another query object which you can further refine before loading the items. Note that this cannot be turned into a different loading strategy when querying so it's often a good idea to avoid using this in favor of ``'lazy=True'``. A query object equivalent to a dynamic `user.addresses` relationship can be created using :meth:`Address.query.with_parent(user)` while still being able to use lazy or eager loading on the relationship itself as necessary.

How do you define the lazy status for backrefs? By using the :func:`~sqlalchemy.orm.backref` function:

```python
class Person(db.Model):
    id = db.Column(db.Integer, primary_key=True)
    name = db.Column(db.String(50), nullable=False)
    addresses = db.relationship('Address', lazy='select',
                               backref=db.backref('person', lazy='joined'))
```
Many-to-Many Relationships

If you want to use many-to-many relationships you will need to define a helper table that is used for the relationship. For this helper table it is strongly recommended to *not* use a model but an actual table::

```python
tags = db.Table('tags',
    db.Column('tag_id', db.Integer, db.ForeignKey('tag.id'), primary_key=True),
    db.Column('page_id', db.Integer, db.ForeignKey('page.id'), primary_key=True)
)
```

```python
class Page(db.Model):
    id = db.Column(db.Integer, primary_key=True)
    tags = db.relationship('Tag', secondary=tags, lazy='subquery',
                           backref=db.backref('pages', lazy=True))

class Tag(db.Model):
    id = db.Column(db.Integer, primary_key=True)
```

Here we configured `Page.tags` to be loaded immediately after loading a Page, but using a separate query. This always results in two queries when retrieving a Page, but when querying for multiple pages you will not get additional queries.

The list of pages for a tag on the other hand is something that's rarely needed. For example, you won't need that list when retrieving the tags for a specific page. Therefore, the backref is set to be lazy-loaded so that accessing it for the first time will trigger a query to get the list of pages for that tag. If you need to apply further query options on that list, you could either switch to the ``'dynamic'`` strategy - with the drawbacks mentioned above - or get a query object using :meth:`Page.query.with_parent(some_tag)` which allows you to apply further query options.

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Schema for XML Signatures
http://www.w3.org/2000/09/xmldsig#
$Revision: 1.1 $ on $Date: 2002/02/08 20:32:26 $ by $Author: reagle $

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* /opt/cola/permits/1130029681_1612432768.57/0/keycloak-saml-core-12-0-2-sources-jar/org/keycloak/saml/processing/core/parsers/saml/xmldsig/AbstractStaxXmlDSigParser.java

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* /opt/cola/permits/1130029681_1612432768.57/0/keycloak-saml-core-12-0-2-sources-jar/org/keycloak/saml/common/parsers/AbstractStaxParser.java

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1.1211 cxf-rt-transports-http-hc 3.3.7

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Python was created in the early 1990s by Guido van Rossum at Stichting Mathematisch Centrum (CWI, see http://www.cwi.nl) in the Netherlands as a successor of a language called ABC. Guido remains Python's principal author, although it includes many contributions from others.

In 1995, Guido continued his work on Python at the Corporation for National Research Initiatives (CNRI, see http://www.cnri.reston.va.us) in Reston, Virginia where he released several versions of the software.

In May 2000, Guido and the Python core development team moved to BeOpen.com to form the BeOpen PythonLabs team. In October of the same year, the PythonLabs team moved to Digital Creations (now Zope Corporation, see http://www.zope.com). In 2001, the Python Software Foundation (PSF, see http://www.python.org/psf/) was formed, a non-profit organization created specifically to own Python-related Intellectual Property. Zope Corporation is a sponsoring member of the PSF.

All Python releases are Open Source (see http://www.opensource.org for the Open Source Definition). Historically, most, but not all, Python releases have also been GPL-compatible; the table below summarizes the various releases.

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Python was created in the early 1990s by Guido van Rossum at Stichting
Mathematisch Centrum (CWI, see http://www.cwi.nl) in the Netherlands
as a successor of a language called ABC. Guido remains Python's
principal author, although it includes many contributions from others.

In 1995, Guido continued his work on Python at the Corporation for
National Research Initiatives (CNRI, see http://www.cnri.reston.va.us)
in Reston, Virginia where he released several versions of the
software.

In May 2000, Guido and the Python core development team moved to
BeOpen.com to form the BeOpen PythonLabs team. In October of the same
year, the PythonLabs team moved to Digital Creations (now Zope
Corporation, see http://www.zope.com). In 2001, the Python Software
Foundation (PSF, see http://www.python.org/psf/) was formed, a
non-profit organization created specifically to own Python-related
Intellectual Property. Zope Corporation is a sponsoring member of
the PSF.

All Python releases are Open Source (see http://www.opensource.org for
the Open Source Definition). Historically, most, but not all, Python
releases have also been GPL-compatible; the table below summarizes
the various releases.

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c-a-bundle.crt -- Bundle of CA Root Certificates
Certificate data from Mozilla as of: Thu Nov  3 19:04:19 2011#
This is a bundle of X.509 certificates of public Certificate Authorities (CA). These were automatically extracted from Mozilla's root certificates file (certdata.txt). This file can be found in the mozilla source tree:
It contains the certificates in PEM format and therefore can be directly used with curl / libcurl / php_curl, or with an Apache+mod_ssl webserver for SSL client authentication.
Just configure this file as the SSLCACertificateFile.#

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@(#) $RCSfile: certdata.txt,v $ $Revision: 1.80 $ $Date: 2011/11/03 15:11:58 $
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History
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1.1217 e2fsprogs 1.45.7-r0

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This is the Debian GNU/Linux prepackaged version of the static EXT2 file system consistency checker (e2fsck.static). The EXT2 utilities were written by Theodore Ts'o <tytso@mit.edu> and Remy Card <card@masi.ibp.fr>.

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#
# This is a Makefile stub which handles the creation of BSD shared
# libraries.
#
# In order to use this stub, the following makefile variables must be defined.
#
# BSDLIB_VERSION = 1.0
# BSDLIB_IMAGE = libce
# BSDLIB_MYDIR = et
# BSDLIB_INSTALL_DIR = $(SHLIBDIR)
#
all:: image

real-subdirs:: Makefile
@echo "MKDIR pic"
@mkdir -p pic

BSD_LIB = $(BSDLIB_IMAGE).so.$(BSDLIB_VERSION)
BSDLIB_PIC_FLAG = -fpic

image:$(BSDLIB_LIB)

$(BSDLIB_LIB): $(OBJ)
(cd pic; ld -Bshareable -o $(BSDLIB_LIB) $(LDFLAGS_SHLIB) $(OBJ))
$(MV) pic/$(BSDLIB_LIB) .
$(RM) -f $(BSDLIB_LIB)
(cd ..; $(LN) $(LINK_BUILD_FLAGS) \ `echo $(my_dir) | sed -e \'s;lib/;;\'"/$(BSDLIB_LIB) $(BSDLIB_LIB))

install-shlibs install:: $(BSDLIB_LIB)
    @echo "INSTALL_PROGRAM $(BSDLIB_INSTALL_DIR)/$(BSDLIB_LIB)"
    @$(INSTALL_PROGRAM) $(BSDLIB_LIB) $(DESTDIR)$(BSDLIB_INSTALL_DIR)/$(BSDLIB_LIB)
    @-$(LDCONFIG)

install-strip: install

install-shlibs-strip:: install-shlibs

uninstall-shlibs uninstall::
    $(RM) -f $(DESTDIR)$(BSDLIB_INSTALL_DIR)/$(BSDLIB_LIB)

clean::
    $(RM) -rf pic
    $(RM) -f $(BSDLIB_LIB)
    $(RM) -f ../*$(BSDLIB_LIB)

This package was added to the e2fsprogs debian source package by Theodore Ts'o <tytso@mit.edu> on Sat Mar 15 15:33:37 EST 2003

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===================================================================
--- tdbsa.orig/tdb.c
+++ tdbsa/tdb.c
@@ -4,11 +4,11 @@ Rev: 23371
Last Changed Date: 2007-06-06 20:14:06 -0400 (Wed, 06 Jun 2007)

- Unix SMB/CIFS implementation.
+ trivial database library - standalone version

- trivial database library - private includes

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Theodore Ts'o
23-June-2007

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* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/connections/jpa/updater/liquibase/LiquibaseJpaUpdaterProviderFactory.java
* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/models/jpa/PersistenceExceptionConverter.java
* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/models/jpa/entities/UserRoleMappingEntity.java
* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/connections/jpa/updater liquibase/conn/LiquibaseConnectionProvider.java
* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/storage/jpa/entity/FederatedUserAttributeEntity.java
* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/connections/jpa/updater liquibase/conn/DefaultLiquibaseConnectionProvider.java
* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/models/jpa/entities/RoleEntity.java
* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/events/jpa/JPaEventStoreProvider.java
* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/models/jpa/session/PersistentClientSessionEntity.java
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* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/authorization/jpa/store/ScopeAdapter.java
* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/models/jpa/entities/GroupEntity.java
* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/authorization/jpa/store/ResourceServerAdapter.java
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* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/models/jpa/entities/GroupAttributeEntity.java
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org.keycloak.connections.jpa.updater.liquibase.lock.LiquibaseDBLockProviderFactory

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org.keycloak.events.jpa.JpaEventStoreProviderFactory

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* /opt/cola/permits/1130030284_1612433026.09/0/keycloak-model-jpa-12-0-2-sources-jar/org/keycloak/authorization/jpa/entities/PolicyEntity.java

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org.keycloak.models.jpa.JpaClientProviderFactory

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org.keycloak.connections.jpa.updater.liquibase.conn.DefaultLiquibaseConnectionProvider

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org.keycloak.connections.jpa.JpaConnectionSpi
org.keycloak.connections.jpa.updater.JpaUpdaterSpi
org.keycloak.connections.jpa.updater.liquibase.conn.LiquibaseConnectionSpi
org.keycloak.connections.jpa.entityprovider.JpaEntitySpi

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org.keycloak.models.jpa.JpaRoleProviderFactory

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org.keycloak.models.jpa.JpaUserProviderFactory

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org.keycloak.models.jpa.JpaGroupProviderFactory

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org.keycloak.connections.jpa.updater.liquibase.LiquibaseJpaUpdaterProviderFactory

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1.1224 jboss-ejb-client 4.0.33.Final
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1.1225 jctools-core 3.0.0

1.1225.1 Available under license:

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Build-Jdk: 1.8.0_232
Built-By: yak
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Bundle-License: http://www.apache.org/licenses/LICENSE-2.0.txt
Bundle-ManifestVersion: 2
Bundle-Name: Java Concurrency Tools Core Library
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Bundle-Version: 3.0.0
Created-By: Apache Maven Bundle Plugin
Export-Package: org.jctools.maps;version="3.0.0",org.jctools.util;version="3.0.0",org.jctools.queues;version="3.0.0";uses:"sun.misc",org.jctools.queues.spec;version="3.0.0",org.jctools.queues.spec;version="3.0.0";uses:"org.jctools.queues.org.jctools.queues.spec"
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This option is useful when you wish to copy part of the code of the Library into a program that is not a library.

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Whether this is true is especially significant if the work can be
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threshold for this to be true is not precisely defined by law.

If such an object file uses only numerical parameters, data
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functions (ten lines or less in length), then the use of the object
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user can modify the Library and then relink to produce a modified
executable containing the modified Library. (It is understood
that the user who changes the contents of definitions files in the
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to use the modified definitions.)

b) Use a suitable shared library mechanism for linking with the
Library. A suitable mechanism is one that (1) uses at run time a
copy of the library already present on the user's computer system,
rather than copying library functions into the executable, and (2) will operate properly with a modified version of the library, if the user installs one, as long as the modified version is interface-compatible with the version that the work was made with.

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* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/MpscArrayQueue.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/NonBlockingArrayQueue.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/MpscArrayBlockingQueue.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/NonBlockingArrayBlockingQueue.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/NonBlockingArrayBlockingQueueUtil.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/NonBlockingArrayQueueUtil.java
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* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/MessagePassingQueueUtil.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/spec/Ordering.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/maps/NonBlockingIdentityHashMap.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/MpscLinkedQueue.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/atomic/LinkedQueueAtomicNode.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/SpscUnboundedArrayQueue.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/BaseLinkedQueue.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/SpncChunkedArrayQueue.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/ConcurrentSequencedCircularArrayQueue.java
* /opt/cola/permits/1140962761_1614910158.25/0/jctools-core-2-1-2-sources-2-jar/org/jctools/queues/package-info.java
1.1233 taglibs-standard-spec 1.2.6-RC1

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Local-Date: Fri, 06 Jun 2003 13:18:52 -0400
Date: Fri, 6 Jun 2003 10:18:52 -0700
From: Juan Gomez <juang@us.ibm.com>
To: Stephen Frost <sfrost@debian.org>
X-Mailer: Lotus Notes Release 5.0.2a (Intl) 23 November 1999
Subject: Re: Juan C. Gomez license in OpenLDAP Source

Stephen,

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Regards, Juan

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MA

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Date: Thu, 5 Jun 2003 16:53:32 -0400 (EDT)
From: Mark Adamson <adamson@andrew.cmu.edu>
To: Stephen Frost <sfrost@debian.org>
Subject: Re: Mark Adamson license in OpenLDAP source

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---
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* To: Stephen Frost <sfrost@snowman.net>
* Subject: Re: OpenLDAP Licenseing issues
* From: "Kurt D. Zeilenga" <Kurt@OpenLDAP.org>
* Date: Wed, 28 May 2003 10:55:44 -0700
* Cc: Steve Langasek <vorlon@netexpress.net>,debian-legal@lists.debian.org, openldap-devel@OpenLDAP.org
* In-reply-to: <20030528162613.GB8524@ns.snowman.net>
* Message-id: <5.2.0.9.0.20030528094229.02924780@127.0.0.1>
* Old-return-path: <Kurt@OpenLDAP.org>

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Regards, Kurt

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1.1235 xz 5.2.4-3.el8

1.1235.1 Available under license:

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* /opt/cola/permits/1130030731_1612433546.08/0/wildfly-elytron-sasl-scram-1-13-1-final-sources-jar/org/wildfly/security/sasl/scram/ScramSaslServer.java

1.1240 jetty-client 9.4.33.v20201020
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* org.eclipse.jetty.orbit:org.eclipse.jdt.core

The following artifacts are EPL and ASL2.
* org.eclipse.jetty.orbit:javax.security.auth.message

The following artifacts are EPL and CDDL 1.0.
* org.eclipse.jetty.orbit:javax.mail.glassfish
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Oracle

The following artifacts are CDDL + GPLv2 with classpath exception.
https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

* javax.servlet:javax.servlet-api
* javax.annotation:javax.annotation-api
* javax.transaction:javax.transaction-api
* javax.websocket:javax.websocket-api

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Oracle OpenJDK

If ALPN is used to negotiate HTTP/2 connections, then the following
artifacts may be included in the distribution or downloaded when ALPN
module is selected.

* java.sun.security.ssl

These artifacts replace/modify OpenJDK classes. The modifications
are hosted at github and both modified and original are under GPL v2 with
classpath exceptions.
http://openjdk.java.net/legal/gplv2+ce.html

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OW2

The following artifacts are licensed by the OW2 Foundation according to the
terms of http://asm.ow2.org/license.html

org.ow2.asm:asm-commons
org.ow2.asm:asm

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Apache

The following artifacts are ASL2 licensed.

org.apache.taglibs:taglibs-standard-spec
org.apache.taglibs:taglibs-standard-impl

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org.mortbay.jasper:apache-jsp
org.apache.tomcat:tomcat-jasper
org.apache.tomcat:tomcat-juli
org.apache.tomcat:tomcat-jsp-api
org.apache.tomcat:tomcat-el-api
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-api
org.apache.tomcat:tomcat-util-scan
org.apache.tomcat:tomcat-util

org.mortbay.jasper:apache-el
org.apache.tomcat:tomcat-jasper-el
org.apache.tomcat:tomcat-el-api

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https://glassfish.dev.java.net/nonav/public/CDDL+GPL.html

org.eclipse.jetty.toolchain:jetty-schemas

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Assorted

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### 1.1251 wildfly-elytron-tool 1.13.1.Final

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* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources-
jar/org/wildfly/security/auth/callback/CredentialCallback.java
* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources-
jar/org/wildfly/security/auth/callback/_private/ElytronMessages.java
* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources-
jar/org/wildfly/security/auth/callback/SocketAddressQueryCallbackHandler.java
* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources-
jar/org/wildfly/security/auth/callback/ChannelBindingCallback.java
* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources-
jar/org/wildfly/security/auth/callback/FastUnsupportedCallbackException.java
* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources-
jar/org/wildfly/security/auth/server/RealmIdentity.java
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* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1.13.1-final-sources.jar/org/wildfly/security/auth/callback/EvidenceDecoder.java
* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1.13.1-final-sources.jar/org/wildfly/security/auth/server/event/SecurityRealmUnavailableEvent.java
* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1.13.1-final-sources.jar/org/wildfly/security/authz/RegexRoleMapper.java
* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1.13.1-final-sources.jar/org/wildfly/security/authz/SourceAddressRoleDecoder.java
* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1.13.1-final-sources.jar/org/wildfly/security/authz/SourceAddressRoleDecoder.java
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* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources-jar/org/wildfly/security/auth/callback/AbstractCredentialCallback.java
* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources-jar/org/wildfly/security/auth/server/Scoped.java
* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources-jar/org/wildfly/security/auth/server/event/SecurityDefiniteOutcomeEvent.java
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* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources-jar/org/wildfly/security/auth/server/event/SecurityAuthenticationSuccessfulEvent.java
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* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources-jar/org/wildfly/security/authz/DisjunctionRoles.java
* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources-jar/org/wildfly/security/auth/callback/package-info.java
* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources-jar/org/wildfly/security/auth/callback/ServerCredentialCallback.java
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* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources.jar/org/wildfly/security/authz/Attributes.java
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* /opt/cola/permits/1130030716_1612433565.05/0/wildfly-elytron-auth-server-1-13-1-final-sources.jar/org/wildfly/security/authz/AuthorizationException.java
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* /opt/cola/permits/1130029393_1612432976.98/0/wildfly-elytron-password-impl-1-13-1-final-sources-jar/org/wildfly/security/password/impl/UnixMD5CryptPasswordImpl.java
* /opt/cola/permits/1130029393_1612432976.98/0/wildfly-elytron-password-impl-1-13-1-final-sources-jar/org/wildfly/security/password/impl/SunUnixMD5CryptPasswordImpl.java
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jar/org/wildfly/security/password/impl/SaltedPasswordAlgorithmParametersSpiImpl.java
* /opt/cola/permits/1130029393_1612432976.98/0/wildfly-elytron-password-impl-1-13-1-final-sources-
jar/org/wildfly/security/password/impl/DigestPasswordAlgorithmParametersSpiImpl.java
* /opt/cola/permits/1130029393_1612432976.98/0/wildfly-elytron-password-impl-1-13-1-final-sources-
jar/org/wildfly/security/password/impl/MaskedPasswordImpl.java
* /opt/cola/permits/1130029393_1612432976.98/0/wildfly-elytron-password-impl-1-13-1-final-sources-
jar/org/wildfly/security/password/impl/DigestUtil.java
* /opt/cola/permits/1130029393_1612432976.98/0/wildfly-elytron-password-impl-1-13-1-final-sources-
jar/org/wildfly/security/password/impl/OneTimePasswordAlgorithmParametersSpiImpl.java
* /opt/cola/permits/1130029393_1612432976.98/0/wildfly-elytron-password-impl-1-13-1-final-sources-
jar/org/wildfly/security/password/impl/IteratedPasswordAlgorithmParametersSpiImpl.java
* /opt/cola/permits/1130029393_1612432976.98/0/wildfly-elytron-password-impl-1-13-1-final-sources-
jar/org/wildfly/security/password/impl/IteratedSaltedPasswordAlgorithmParametersSpiImpl.java
* /opt/cola/permits/1130029393_1612432976.98/0/wildfly-elytron-password-impl-1-13-1-final-sources-
jar/org/wildfly/security/password/impl/MaskedPasswordAlgorithmParametersSpiImpl.java

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* /opt/cola/permits/1130029393_1612432976.98/0/wildfly-elytron-password-impl-1-13-1-final-sources-jar/org/wildfly/security/password/impl/OneTimePasswordImpl.java

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1.1270 wildfly-http-transaction-client

1.1.2.Final

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org.wildfly.httpclient.transaction.HttpRemoteTransactionProvider

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1.1271 jboss-metadata-ejb 13.0.0.Final

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* /opt/cola/permits/1130031223_1612432923.19/0/wildfly-http-ejb-client-1-1-2-final-sources.jar/org/wildfly/httpclient/ejb/HttpInvocationHandler.java
* /opt/cola/permits/1130031223_1612432923.19/0/wildfly-http-ejb-client-1-1-2-final-sources.jar/org/wildfly/httpclient/ejb/HttpProtocolV1ObjectTable.java
* /opt/cola/permits/1130031223_1612432923.19/0/wildfly-http-ejb-client-1-1-2-final-sources.jar/org/wildfly/httpclient/ejb/HttpEJBInvocationBuilder.java
* /opt/cola/permits/1130031223_1612432923.19/0/wildfly-http-ejb-client-1-1-2-final-sources.jar/org/wildfly/httpclient/ejb/HttpCancelHandler.java
* /opt/cola/permits/1130031223_1612432923.19/0/wildfly-http-ejb-client-1-1-2-final-sources.jar/org/wildfly/httpclient/ejb/HttpSessionOpenHandler.java
* /opt/cola/permits/1130031223_1612432923.19/0/wildfly-http-ejb-client-1-1-2-final-sources.jar/org/wildfly/httpclient/ejb/ModuleIdentifier.java
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* /opt/cola/permits/1130031223_1612432923.19/0/wildfly-http-ejb-client-1-1-2-final-sources.jar/org/wildfly/httpclient/ejb/EjbHttpService.java
* /opt/cola/permits/1130031223_1612432923.19/0/wildfly-http-ejb-client-1-1-2-final-sources.jar/org/wildfly/httpclient/ejb/EJBMarshallingCompatibilityHelper.java
* /opt/cola/permits/1130031223_1612432923.19/0/wildfly-http-ejb-client-1-1-2-final-sources.jar/org/wildfly/httpclient/ejb/HttpClientProvider.java
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org.wildfly.httpclient.ejb.EJBMarshallingCompatibilityHelper

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* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
  jar/org/keycloak/authorization/attribute/Attributes.java
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  jar/org/keycloak/authorization/AuthorizationProviderFactory.java
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  jar/org/keycloak/authorization/permission/evaluator/IterablePermissionEvaluator.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
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  jar/org/keycloak/authorization/model/Resource.java
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  jar/org/keycloak/authorization/model/ResourceServer.java
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* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
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* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/userprofile/UserProfileContext.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/userprofile/validation/UserUpdateEvent.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/storage/group/GroupStorageProviderSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/headers/SecurityHeadersSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/userprofile/UserProfileAttributes.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/GroupProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/utils/StreamsUtil.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/services/clientpolicy/ClientPolicySpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/userprofile/UserProfile.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/validation/DefaultValidationContext.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/GroupSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/RoleSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/validation/Validator.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/validation/ClientValidationContext.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/services/clientpolicy/condition/ClientPolicyConditionProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/ClientProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/RoleProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/headers/SecurityHeadersProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/policy/NotEmailPasswordPolicyProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/validation/ValidationErrorResponse.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/migration/migrators/MigrateTo12_0_0.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/events/EventListenerTransaction.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/headers/SecurityHeadersOptions.java

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* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/authorization/UserManagedPermissionUtil.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/authorization/policy/evaluation/DecisionPermissionCollector.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/crypto/CekManagementSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/crypto/ContentEncryptionSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/migration/migrators/MigrateTo4_2_0.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/crypto/CekManagementProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/storage/client/AbstractReadOnlyClientScopeAdapter.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/authorization/policy/evaluation/AbstractDecisionCollector.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/authorization/policy/evaluation/Realm.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/crypto/ContentEncryptionProvider.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/authorization/model/AbstractAuthorizationModel.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/crypto/CekManagementProvider.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/scripting/ScriptCompilationException.java
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* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/ActionTokenStoreSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/ActionTokenStoreProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/ActionTokenStoreProvider.java

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#

org.keycloak.policy.DigitsPasswordPolicyProviderFactory
org.keycloak.policy.ForceExpiredPasswordPolicyProviderFactory
org.keycloak.policy.HashAlgorithmPasswordPolicyProviderFactory
org.keycloak.policy.HashIterationsPasswordPolicyProviderFactory
org.keycloak.policy.HistoryPasswordPolicyProviderFactory
org.keycloak.policy.LengthPasswordPolicyProviderFactory
org.keycloak.policy.LowerCasePasswordPolicyProviderFactory
org.keycloak.policy.NotUsernamePasswordPolicyProviderFactory
org.keycloak.policy.RegexPatternsPasswordPolicyProviderFactory
org.keycloak.policy.SpecialCharsPasswordPolicyProviderFactory
org.keycloak.policy.UpperCasePasswordPolicyProviderFactory
org.keycloak.policy.BlacklistPasswordPolicyProviderFactory
org.keycloak.policy.NotEmailPasswordPolicyProviderFactory

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* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/META-INF/services/org.keycloak.policy.PasswordPolicyProviderFactory
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* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/SingleUseTokenStoreProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/migration/migrators/MigrateTo4_0_0.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/executors/ExecutorsSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/crypto/HashProvider.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/crypto/HashProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/utils/SessionTimeoutHelper.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/utils/ResetTimeOffsetEvent.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/SingleUseTokenStoreProvider.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/executor/ExecutorsProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/CodeToTokenStoreSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/CodeToTokenStoreProvider.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/crypto/HashSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/authorization/model/PermissionTicket.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/authorization/store/PermissionTicketStore.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/migration/migrators/MigrateTo3_4_0.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/DefaultClientScopes.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/policy/BlacklistPasswordPolicyProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/CodeToTokenStoreProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/authorization/policy/evaluation/PermissionTicketAwareDecisionResultCollector.java

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* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/storage/adapter/UpdateOnlyChangeUserModelDelegate.java
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* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/protocol/oidc/TokenIntrospectionProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/protocol/oidc/TokenIntrospectionSpi.java
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org.keycloak.provider.ExceptionConverterSpi
org.keycloak.storage.UserStorageProviderSpi
org.keycloak.storage.federated.UserFederatedStorageProviderSpi
org.keycloak.models.ClientSpi
org.keycloak.models.GroupSpi
org.keycloak.models.RealmSpi
org.keycloak.models.RoleSpi
org.keycloak.models.ActionTokenStoreSpi
org.keycloak.models.CodeToTokenStoreSpi
org.keycloak.models.SingleUseTokenStoreSpi
org.keycloak.models.TokenRevocationStoreSpi
org.keycloak.models.UserSessionSpi
org.keycloak.models.UserSpi
org.keycloak.models.models.Session.UserSessionPersisterSpi
org.keycloak.models.dblock.DBlockSpi
org.keycloak.migration.MigrationSpi
org.keycloak.events.EventListenerSpi
org.keycloak.events.EventStoreSpi
org.keycloak.exportimport.ExportSpi
org.keycloak.exportimport.ImportSpi
org.keycloak.timer.TimerSpi
org.keycloak.scripting.ScriptingSpi
org.keycloak.services.managers.BruteForceProtectorSpi
org.keycloak.services.resource.RealmResourceSPI
org.keycloak.sessions.AuthenticationSessionSpi
org.keycloak.sessions.StickySessionEncoderSpi
org.keycloak.protocol.ClientInstallationSpi
org.keycloak.protocol.LoginProtocolSpi
org.keycloak.protocol.ProtocolMapperSpi
org.keycloak.broker.provider.IdentityProviderSpi
org.keycloak.broker.provider.IdentityProviderMapperSpi
org.keycloak.broker.social.SocialProviderSpi
org.keycloak.forms.account.AccountSpi
org.keycloak.forms.login.LoginFormsSpi
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org.keycloak.email.EmailTemplateSpi
org.keycloak.executors.ExecutorsSpi
org.keycloak.theme.ThemeSpi
org.keycloak.truststore.TruststoreSpi
org.keycloak.connections.httpclient.HttpClientSpi
org.keycloak.models.cache.CacheRealmProviderSpi
org.keycloak.models.cache.CacheUserProviderSpi
org.keycloak.authentication.AuthenticatorSpi
org.keycloak.authentication.ClientAuthenticatorSpi
org.keycloak.authentication.RequiredActionSpi
org.keycloak.authentication.FormAuthenticatorSpi
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org.keycloak.cluster.ClusterSpi
org.keycloak.authorization.policy.provider.PolicySpi
org.keycloak.authorization.store.StoreFactorySpi
org.keycloak.authorization.AuthorizationSpi
org.keycloak.models.cache.authorization.CachedStoreFactorySpi
org.keycloak.protocol.oidc.TokenIntrospectionSpi
org.keycloak.policy.PasswordPolicySpi
org.keycloak.policy.PasswordPolicyManagerSpi
org.keycloak.transaction.TransactionManagerLookupSpi
org.keycloak.credential.hash.PasswordHashSpi
org.keycloak.credential.CredentialSpi
org.keycloak.keys.PublicKeyStorageSpi
org.keycloak.keys.KeySpi
org.keycloak.storage.client.ClientStorageProviderSpi
org.keycloak.storage.role.RoleStorageProviderSpi
org.keycloak.storage.group.GroupStorageProviderSpi
org.keycloak.crypto.SignatureSpi
org.keycloak.crypto.ClientSignatureVerifierSpi
org.keycloak.crypto.HashSpi
org.keycloak.vault.VaultSpi
org.keycloak.crypto.CekManagementSpi
org.keycloak.crypto.ContentEncryptionSpi
org.keycloak.validation.ClientValidationSPI
org.keycloak.headers.SecurityHeadersSpi
org.keycloak.services.clientpolicy.ClientPolicySpi
org.keycloak.services.clientpolicy.condition.ClientPolicyConditionSpi
org.keycloak.services.clientpolicy.executor.ClientPolicyExecutorSpi
org.keycloak.userprofile.UserProfileSpi

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#
org.keycloak.policy.DefaultPasswordPolicyManagerProviderFactory

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* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/TokenRevocationStoreProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/models/TokenRevocationStoreSpi.java

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/**
 * This class encapsulates a proprietary HTTP challenge protocol designed by keycloak team which is used by text-based console
 * clients to dynamically render and prompt for information in a textual manner. The class is a builder which can
 * build the challenge response (the header and response body).
 */
When doing code to token flow in OAuth, server could respond with

401
WWW-Authenticate: X-Text-Form-Challenge callback="http://localhost/..."
param="username" label="Username: " mask=false
param="password" label="Password: " mask=true
Content-Type: text/plain

Please login with your username and password

The client receives this challenge. It first outputs whatever the text body of the message contains. It will then prompt for username and password using the label values as prompt messages for each parameter.

After the input has been entered by the user, the client does a form POST to the callback url with the values of the input parameters entered.

The server can challenge with 401 as many times as it wants. The client will look for 302 responses. It will follow all redirects unless the Location url has an OAuth "code" parameter. If there is a code parameter, then the client will stop and finish the OAuth flow to obtain a token. Any other response code other than 401 or 302 the client should abort with an error message.

Found in path(s):
/opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/authentication/ConsoleDisplayMode.java

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*/
jar/org/keycloak/keys/PublicKeyStorageSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/theme/ThemeProvider.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/broker/provider/ExchangeTokenToIdentityProviderToken.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/authentication/RequiredActionFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/events/admin/AuthDetails.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/migration/migrators/MigrateTo2_0_0.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/cluster/ClusterEvent.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/policy/HashIterationsPasswordPolicyProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/models/ClaimMask.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/migration/migrators/MigrateTo1_9_0.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/truststore/TruststoreSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/protocol/ClientInstallationProvider.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/events/admin/OperationType.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/models/utils/CredentialValidation.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/email/EmailTemplateProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/migration/migrators/MigrateTo2_2_0.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/cluster/ClusterProvider.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/authentication/FlowStatus.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/transaction/TransactionManagerLookupSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/models/RealmProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/models/utils/reflection/PropertyQueries.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/models/UserSessionProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/org/keycloak/broker/provider/IdentityProviderSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/org/keycloak/broker/provider/util/IdentityBrokerState.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/org/keycloak/protocol/ProtocolMapperConfigException.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/keycloak/storage/client/AbstractReadOnlyClientStorageAdapter.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/keycloak/broker/provider/util/IdentityBrokerState.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/keycloak/keys/PublicKeyLoader.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/keycloak/forms/login/LoginFormsSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/keycloak/migration/migrators/MigrateTo3_0_0.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/keycloak/policy/PasswordPolicyProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/keycloak/policy/LengthPasswordPolicyProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/keycloak/accounts/auth/FormAuthenticator.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/keycloak/sessions/AuthenticationSessionSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/keycloak/protocol/LoginProtocolSpi.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/keycloak/protocol/DigitsPasswordPolicyProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/keycloak/protocol/authentication/FormAuthenticator.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources.jar/keycloak/credential/hash/Pbkdf2PasswordHashProvider.java

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* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/META-INF/maven/org.keycloak/keycloak-server-spi-private/pom.xml
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#
org.keycloak.models.session.DisabledUserSessionPersisterProvider

Found in path(s):
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/META-INF/services/org.keycloak.models.session.UserSessionPersisterProviderFactory
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* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/migration/migrators/MigrateTo9_0_0.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/validation/ClientValidationProvider.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/validation/ClientValidationProviderFactory.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/authentication/InitiatedActionSupport.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/device/DeviceActivityManager.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/validation/ClientValidationSPI.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/migration/migrators/MigrateTo8_0_0.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/validation/ValidationUtil.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/cluster/ManagedCacheManagerProvider.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/migration/migrators/MigrateTo6_0_0.java
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-
jar/org/keycloak/validation/ValidationContext.java

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*/
/**
*
* Called when a user event occurs e.g. log in, register.
* <p/>
* Note this method should not do any action that cannot be rolled back, see { @link EventListenerProvider} javadoc
* for more details.
*
* @param event to be triggered
*/

Found in path(s):
* /opt/cola/permits/1130030606_1612432933.35/0/keycloak-server-spi-private-12-0-2-sources-jar/org/keycloak/events/EventListenerProvider.java

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Boolean configPropertySupportsDynamicUpdates, Boolean configPropertyConfidential, String configPropertyConfidentialId) this.configPropertyConfidential = configPropertyConfidential; this.configPropertyConfidentialId = configPropertyConfidentialId; public Boolean get configurablePropertyConfidential() return configPropertyConfidential; public String get-configPropertyConfidentialId() return
configPropertyConfidentialId; configPropertyConfidential, CopyUtil.cloneString(id), mandatory,
CopyUtil.cloneString(configPropertyConfidentialId)); result = prime * result + ((configPropertyConfidential ==
null) ? 0 : configPropertyConfidential.hashCode()); result = prime * result + ((configPropertyConfidentialId == null)
? 0 : configPropertyConfidentialId.hashCode()); if (configPropertyConfidential == null) if
(other.configPropertyConfidential != null) else if
(!other.configPropertyConfidential.equals(configPropertyConfidential)) if (configPropertyConfidentialId == null)
else if (!configPropertyConfidentialId.equals(other.configPropertyConfidentialId)) if (configPropertyConfidential != null)
else if (other.configPropertyConfidential == null) else if (!configPropertyConfidential.equals(other.configPropertyConfidential)) sb.append("</").append(XML.ConfigPropertyTag.CONFIGPROPERTYCONFIDENTIAL).append(">");
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configPropertyConfidential = null; configPropertyConfidential, id, false, null, case
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configPropertyConfidential = configPropertyAnnotation.confidential(); configPropertyConfidential, null, false,
c.getConfigPropertyConfidential(), c.getId(), c.getConfigPropertyConfidentialId());
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CONFIGPROPERTYCONFIDENTIAL: { configPropertyConfidential = elementAsBoolean(reader);}
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configPropertyConfidential = configPropertyAnnotation.confidential(); configPropertyConfidential, null, false,
c.getConfigPropertyConfidential(), c.getId(), c.getConfigPropertyConfidentialId());
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* /opt/cola/permits/1130031031_1612433078.07/0/wildfly-elytron-x500-cert-1-13-1-final-sources-jar/org/wildfly/security/x500/cert/CertUtil.java
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public DomainCommandBuilder setInterProcessHostControllerPort(final int port) 
public DomainCommandBuilder setMasterAddressHint(final String address) 
public DomainCommandBuilder setMasterPortHint(final String port) 
public DomainCommandBuilder setProcessControllerAddress(final String address) 
public DomainCommandBuilder setProcessControllerPort(final String port) 
public DomainCommandBuilder setBaseDirectory(final String baseDir) 
public DomainCommandBuilder setInterProcessHostControllerPort(final int port) 
public DomainCommandBuilder setMasterAddressHint(final String address) 
public DomainCommandBuilder setMasterPortHint(final String port) 
public DomainCommandBuilder setProcessControllerAddress(final String address) 
public DomainCommandBuilder setProcessControllerPort(final String port) 
public DomainCommandBuilder setBaseDirectory(final String baseDir) 
public DomainCommandBuilder setInterProcessHostControllerPort(final int port) 

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1.1309 simpleclient-common 0.6.0

1.1310 cryptography 3.4.7
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1.1311 jansi-osx 1.7

Open Source Used In Branch Migration Tool Spirit 11318
Python was created in the early 1990s by Guido van Rossum at Stichting Mathematisch Centrum (CWI, see http://www.cwi.nl) in the Netherlands as a successor of a language called ABC. Guido remains Python’s principal author, although it includes many contributions from others.

In 1995, Guido continued his work on Python at the Corporation for National Research Initiatives (CNRI, see http://www.cnri.reston.va.us) in Reston, Virginia where he released several versions of the software.

In May 2000, Guido and the Python core development team moved to BeOpen.com to form the BeOpen PythonLabs team. In October of the same year, the PythonLabs team moved to Digital Creations (now Zope Corporation, see http://www.zope.com). In 2001, the Python Software Foundation (PSF, see http://www.python.org/psf/) was formed, a non-profit organization created specifically to own Python-related Intellectual Property. Zope Corporation is a sponsoring member of the PSF.

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1.1313 jinja2 3.0.1
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Metadata-Version: 2.1
Name: Jinja2
Version: 3.0.1
Summary: A very fast and expressive template engine.
Home-page: https://palletsprojects.com/p/jinja/
Author: Armin Ronacher
Author-email: armin.ronacher@active-4.com
Maintainer: Pallets
Maintainer-email: contact@palletsprojects.com
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Project-URL: Changes, https://jinja.palletsprojects.com/changes/
Project-URL: Twitter, https://twitter.com/PalletsTeam
Project-URL: Chat, https://discord.gg/pallets
Description: Jinja

Description: Jinja

Jinja is a fast, expressive, extensible templating engine. Special
placeholders in the template allow writing code similar to Python
syntax. Then the template is passed data to render the final document.
It includes:

- Template inheritance and inclusion.
- Define and import macros within templates.
- HTML templates can use autoescaping to prevent XSS from untrusted user input.
- A sandboxed environment can safely render untrusted templates.
- AsyncIO support for generating templates and calling async functions.
- I18N support with Babel.
- Templates are compiled to optimized Python code just-in-time and cached, or can be compiled ahead-of-time.
- Exceptions point to the correct line in templates to make debugging easier.
- Extensible filters, tests, functions, and even syntax.

Jinja's philosophy is that while application logic belongs in Python if possible, it shouldn't make the template designer's job difficult by restricting functionality too much.

Installing
----------

Install and update using `pip`:

.. code-block:: text

   $ pip install -U Jinja2


In A Nutshell
-------------

.. code-block:: jinja

   {% extends "base.html" %}
   {% block title %}Members{% endblock %}
   {% block content %}
   <ul>
   {% for user in users %}
   <li><a href="{{ user.url }}">{{ user.username }}</a></li>
   {% endfor %}
   </ul>
   {% endblock %}
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- Documentation: https://jinja.palletsprojects.com/
- Changes: https://jinja.palletsprojects.com/changes/
- PyPI Releases: https://pypi.org/project/Jinja2/
- Source Code: https://github.com/pallets/jinja/
- Issue Tracker: https://github.com/pallets/jinja/issues/
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Platform: UNKNOWN
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Classifier: Operating System :: OS Independent
Classifier: Programming Language :: Python
Classifier: Topic :: Internet :: WWW/HTTP :: Dynamic Content
Classifier: Topic :: Text Processing :: Markup :: HTML
Requires-Python: >=3.6
Description-Content-Type: text/x-rst
Provides-Extra: i18n

Found in path(s):
* /opt/cola/permits/1166437412_1621420347.71/0/jinja2-3.0-1.tar.gz/Jinja2-3.0.1/PKG-INFO

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[metadata]
name = Jinja2
version = attr: jinja2.__version__
url = https://palletsprojects.com/p/jinja/
project_urls =
  Donate = https://palletsprojects.com/donate
  Documentation = https://jinja.palletsprojects.com/
  Changes = https://jinja.palletsprojects.com/changes/
  Source Code = https://github.com/pallets/jinja/
  Issue Tracker = https://github.com/pallets/jinja/issues/
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license = BSD-3-Clause
license_files = LICENSE.rst
author = Armin Ronacher
author_email = armin.ronacher@active-4.com
maintainer = Pallets
maintainer_email = contact@palletsprojects.com
description = A very fast and expressive template engine.
long_description = file: README.rst
long_description_content_type = text/x-rst
classifiers =
  Development Status :: 5 - Production/Stable
  Environment :: Web Environment
  Intended Audience :: Developers
  License :: OSI Approved :: BSD License
  Operating System :: OS Independent
  Programming Language :: Python
  Topic :: Internet :: WWW/HTTP :: Dynamic Content
  Topic :: Text Processing :: Markup :: HTML

[options]
packages = find:
  package_dir = src
  include_package_data = true
  python_requires = >= 3.6

[options.packages.find]
where = src

[options.entry_points]
babel.extractors =
  jinja2 = jinja2.ext:babel_extract[i18n]

[tool:pytest]
testpaths = tests
  filterwarnings =
    error

[coverage:run]
branch = True
source =
  jinja2
tests

[coverage:paths]
source =
  src
  */site-packages

[flake8]
select = B, E, F, W, B9, ISC
ignore =
  E203
  E501
  E722
  W503
max-line-length = 80
per-file-ignores =
src/jinja2/__init__.py: F401

[mypy]
files = src/jinja2
python_version = 3.6
disallow_subclassing_any = True
disallow_untyped_calls = True
disallow_untyped_defs = True
disallow_incomplete_defs = True
no_implicit_optional = True
local_partial_types = True
no_implicit_reexport = True
strict_equality = True
warn_redundant_casts = True
warn_unused_configs = True
warn_unused_ignores = True
warn_return_any = True
warn_unreachable = True

[mypy-jinja2.defaults]
no_implicit_reexport = False

[mypy-markupsafe]
no_implicit_reexport = False

[egg_info]
tag_build =
tag_date = 0

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* /opt/cola/permits/1166437412_1621420347.71/0/jinja2-3-0-1-tar-gz/Jinja2-3.0.1/setup.cfg

1.1314 lz4-java 1.7.1
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1.1315 wildfly-elytron-provider-util
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* /opt/cola/permits/1130030884_1612433244.43/0/wildfly-elytron-provider-util-1-13-1-final-sources-jar/org/wildfly/security/provider/util/ProviderUtil.java

1.1316 wildfly-platform-mbean 13.0.3.Final

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1.1317 netty-transport-native-unix-common

4.1.51.Final

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* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/io/netty/channel/unix/UnixChannelOption.java
* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/io/netty/channel/unix/package-info.java

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* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/io/netty/channel/unix/Buffer.java
* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/netty_unix_buffer.c
* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/netty_unix_buffer.h

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* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/io/netty/channel/unix/UnixChannelUtil.java
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* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/netty_unix_socket.c
* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/io/netty/channel/unix/NativeInetAddress.java
* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/netty_unix_filedescriptor.h
* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/netty_unix_filedescriptor.c
* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/io/netty/channel/unix/DatagramSocketAddress.java
* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/netty_unix_socket.h
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* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/netty_unix_limits.h
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* /opt/ws_local/PERMITS_SQL/1075084034_1596044782.67/0/netty-transport-native-unix-common-4-1-51-final-sources-jar/io/netty/channel/unix/Limits.java
1.1318 flask-restful 0.3.8

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1.1319 resteasy-multipart-provider

3.13.2.Final

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* /opt/cola/permits/1110676238_1606843959.02/0/hornetq-commons-2-4-7-final-sources-1.jar/org/hornetq/utils/ByteUtil.java

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 */
/**
 * <p>Encodes and decodes to and from Base64 notation.</p>
The `<tt>options</tt>` parameter, which appears in a few places, is used to pass several pieces of information to the encoder. In the "higher level" methods such as `encodeBytes( bytes, options )` the options parameter can be used to indicate such things as first gzipping the bytes before encoding them, not inserting linefeeds (though that breaks strict Base64 compatibility), and encoding using the URL-safe and Ordered dialects.

The constants defined in Base64 can be OR-ed together to combine options, so you might make a call like this:

```java
String encoded = Base64.encodeBytes( mybytes, Base64.GZIP | Base64.DONT_BREAK_LINES );
```

to compress the data before encoding it and then making the output have no newline characters.

Change Log:

- v2.2.2 - Fixed `encodeFileToFile` and `decodeFileToFile` to use the Base64.InputStream class to encode and decode on the fly which uses less memory than encoding/decoding an entire file into memory before writing.
- v2.2.1 - Fixed bug using URL_SAFE and ORDERED encodings. Fixed bug when using very small files (~< 40 bytes).
- v2.2 - Added some helper methods for encoding/decoding directly from one file to the next. Also added a main() method to support command line encoding/decoding from one file to the next. Also added these Base64 dialects:
  - The default is RFC3548 format.
  - Calling `Base64.setFormat(Base64.BASE64_FORMAT.URLSAFE_FORMAT)` generates URL and file name friendly format as described in Section 4 of RFC3548.
  - Calling `Base64.setFormat(Base64.BASE64_FORMAT.ORDERED_FORMAT)` generates URL and file name friendly format that preserves lexical ordering as described in http://www.faqs.org/qa/rfcc-1940.html
  - Special thanks to Jim Kellerman at http://www.powerset.com/ for contributing the new Base64 dialects.
  - v2.1 - Cleaned up javadoc comments and unused variables and methods. Added some convenience methods for reading and writing to and from files.
  - v2.0.2 - Now specifies UTF-8 encoding in places where the code fails on systems with other encodings (like EBCDIC).
  - v2.0.1 - Fixed an error when decoding a single byte, that is, when the encoded data was a single byte.
  - v2.0 - I got rid of methods that used booleans to set options.
    - Now everything is more consolidated and cleaner. The code now detects when data that's being decoded is gzip-compressed and will decompress it automatically. Generally things are cleaner. You'll probably have to...
* change some method calls that you were making to support the new
* options format (<tt>int</tt>s that you “OR” together).
* <li>v1.5.1 - Fixed bug when decompressing and decoding to a
* byte[] using <tt>decode( String s, boolean gzipCompressed )</tt>.
* Added the ability to "suspend" encoding in the Output Stream so
* you can turn on and off the encoding if you need to embed base64
* data in an otherwise "normal" stream (like an XML file).
* <li>v1.5 - Output stream passes on flush() command but doesn't do anything itself.
* This helps when using GZIP streams.
* Added the ability to GZip-compress objects before encoding them.</li>
* <li>v1.4 - Added helper methods to read/write files.
* <li>v1.3.6 - Fixed OutputStream.flush() so that 'position' is reset.</li>
* <li>v1.3.5 - Added flag to turn on and off line breaks. Fixed bug in input stream
* where last buffer being read, if not completely full, was not returned.</li>
* <li>v1.3.4 - Fixed when "improperly padded stream" error was thrown at the wrong time.</li>
* <li>v1.3.3 - Fixed I/O streams which were totally messed up.</li>
* </ul>

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* plenty of well-wishing instead!
* Please visit <a href="http://iharder.net/base64">http://iharder.net/base64</a>
* periodically to check for updates or to contribute improvements.
* </p>

* @author Robert Harder
* @author rob@iharder.net
* @version 2.2.2
*/

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* /opt/cola/permits/1110676238_1606843959.02/0/hornetq-commons-2-4-7-final-sources-1-
jar/org/hornetq/utils/Base64.java
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1.1329 findutils 4.6.0+git+20190209 2

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It was downloaded from ftp://ftp.gnu.org/gnu/findutils

Debian maintainer history: The original package was put together by Ian Murdock <imurdock@debian.org>, afterwards Kevin Dalley <kevind@rahul.net> took over. 2003-07 Andreas Metzler <ametzler@debian.org> followed.

Upstream Authors:

* GNU find was written by Eric Decker <cire@cisco.com>, with enhancements by David MacKenzie <djm@gnu.org>, Jay Plett <jay@silence.princeton.nj.us>, and Tim Wood <axolotl!tim@toad.com>. The idea for -print0 and xargs -0 came from Dan Bernstein <brnstdnd@kramden.acf.nyu.edu>. Improvements have been made by James Youngman <jay@gnu.org>.

* GNU xargs was originally written by Mike Rendell, with enhancements by David MacKenzie. Modifications by James Youngman Dmitry V. Levin

* GNU locate and its associated utilities were originally written by James Woods, with enhancements by David MacKenzie, James Youngman and Bas van Gompel.

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   Eric B. Decker
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1.1330 glib 2.66.8-r0

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