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```
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scriptversion=2009-04-28.21; # UTC

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Author: Christopher Olah <colah@xelerance.com>

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""" Easy DNS (including DNSSEC) via ldns.

Ldns is a great library. It is a powerfull tool for working with DNS. python-ldns it is a straight up clone of the C interface, however that is not a very good interface for python. Its documentation is incomplete and some functions don't work as described. And some objects don't have a full python API.

ldnsx aims to fix this. It wraps around the ldns python bindings, working around its limitations and providing a well-documented, more pythonistic interface.

/*

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```
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Gnomovision comes with ABSOLUTELY NO WARRANTY; for details type `show w'.
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The hypothetical commands `show
w' and `show c' should show the appropriate
parts of the General Public License. Of course, the commands you use may
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```
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<signature of Ty Coon>, 1 April 1989
Ty Coon, President of Vice
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```
@ignore
@c Set file name and title for man page.
@setfilename gpl
@settitle GNU General Public License
@c man begin SEEALSO
gfdl(7), fsf-funding(7).
@c man end
@c man begin COPYRIGHT
Copyright @copyright{} 2007 Free Software Foundation, Inc.
```

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```
@c man end
```

@end ignore
@node Copying
@c man begin DESCRIPTION
@unnumbered GNU General Public License
@center Version 3, 29 June 2007

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@smallexample

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```
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This is free software, and you are welcome to redistribute it
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```

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@c man end

GCC RUNTIME LIBRARY EXCEPTION

Version 3.1, 31 March 2009

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Version 2.1, February 1999

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This is an attempt to acknowledge early contributions to the garbage collector. Later contributions should instead be mentioned in README.changes.

HISTORY -

Early versions of this collector were developed as a part of research

projects supported in part by the National Science Foundation and the Defense Advance Research Projects Agency.

The garbage collector originated as part of the run-time system for the Russell programming language implementation. The first version of the garbage collector was written primarily by Al Demers. It was then refined and mostly rewritten, primarily by Hans-J. Boehm, at Cornell U., the University of Washington, Rice University (where it was first used for C and assembly code), Xerox PARC, SGI, and HP Labs. However, significant contributions have also been made by many others.

Some other contributors:

More recent contributors are mentioned in the modification history in README.changes. My apologies for any omissions.

The SPARC specific code was originally contributed by Mark Weiser.

The Encore Multimax modifications were supplied by Kevin Kenny (kenny@m.cs.uiuc.edu). The adaptation to the IBM PC/RT is largely due to Vernon Lee, on machines made available to Rice by IBM.

Much of the HP specific code and a number of good suggestions for improving the generic code are due to Walter Underwood.

Robert Brazile (brazile@diamond.bbn.com) originally supplied the ULTRIX code. Al Dosser (dosser@src.dec.com) and Regis Cridlig (Regis.Cridlig@cl.cam.ac.uk) subsequently provided updates and information on variation between ULTRIX systems. Parag Patel (parag@netcom.com) supplied the A/UX code.

Jesper Peterson(jep@mtiame.mtia.oz.au), Michel Schinz, and Martin Tauchmann (martintauchmann@bigfoot.com) supplied the Amiga port. Thomas Funke (thf@zelator.in-berlin.de(?)) and

Brian D.Carlstrom (bdc@clark.lcs.mit.edu) supplied the NeXT ports.

Douglas Steel (doug@wg.icl.co.uk) provided ICL DRS6000 code.

Bill Janssen (janssen@parc.xerox.com) supplied the SunOS dynamic loader

specific code. Manuel Serrano (serrano@cornas.inria.fr) supplied linux and Sony News specific code. Al Dosser provided Alpha/OSF/1 code. He and

Dave Detlefs(detlefs@src.dec.com) also provided several generic bug fixes.

Alistair G. Crooks(agc@uts.amdahl.com) supplied the NetBSD and 386BSD ports.

Jeffrey Hsu (hsu@soda.berkeley.edu) provided the FreeBSD port.

Brent Benson (brent@jade.ssd.csd.harris.com) ported the collector to a Motorola 88K processor running CX/UX (Harris NightHawk).

Ari Huttunen (Ari.Huttunen@hut.fi) generalized the OS/2 port to nonIBM development environments (a nontrivial task).

Patrick Beard (beard@cs.ucdavis.edu) provided the initial MacOS port.

David Chase, then at Olivetti Research, suggested several improvements.

Scott Schwartz (schwartz@groucho.cse.psu.edu) supplied some of the code to save and print call stacks for leak detection on a SPARC.

Jesse Hull and John Ellis supplied the C++ interface code.

Zhong Shao performed much of the experimentation that led to the current typed allocation facility. (His dynamic type inference code hasn't made it into the released version of the collector, yet.)
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Version 2.1, February 1999

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If such an object file uses only numerical parameters, data structure layouts and accessors, and small macros and small inline functions (ten lines or less in length), then the use of the object file is unrestricted, regardless of whether it is legally a derivative work. (Executables containing this object code plus portions of the Library will still fall under Section 6.)

Otherwise, if the work is a derivative of the Library, you may

distribute

the object code for the work under the terms of Section 6.

Any executables containing that work also fall under Section 6, whether or not they are linked directly with the Library itself.

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Program	Directory

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mach_override	lib/interception/mach_override
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@cindex LGPL, Lesser General Public License
@center Version 2.1, February 1999

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@appendixsubsec Preamble

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@heading END OF TERMS AND CONDITIONS

@end iftex

@ifinfo

@center END OF TERMS AND CONDITIONS

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@page

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@var{signature of Ty Coon}, 1 April 1990

Ty Coon, President of Vice

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@ignore

@c Set file name and title for man page.

@setfilename gfdl

@settitle GNU Free Documentation License

@c man begin SEEALSO

gpl(7), fsf-funding(7).

@c man end

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@c hence no sectioning command or @node.

@c man end

@end ignore

@c Special handling for inclusion in the install manual.

@ifset gfdlhtml

@ifnohtml

@comment node-name, next, previous, up

@node GNU Free Documentation License, Concept Index, Old, Top

@end ifnohtml

@html

<h1 align="center">Installing GCC: GNU Free Documentation License</h1>

@end html

@ifnohtml

@unnumbered GNU Free Documentation License

@end ifnohtml

@end ifset

@c man begin DESCRIPTION

@ifclear gfdlhtml

@node GNU Free Documentation License

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This is an attempt to acknowledge early contributions to the garbage collector. Later contributions should instead be mentioned in README.changes.

HISTORY -

Early versions of this collector were developed as a part of research projects supported in part by the National Science Foundation and the Defense Advance Research Projects Agency.

The garbage collector originated as part of the run-time system for the Russell programming language implementation. The first version of the garbage collector was written primarily by Al Demers. It was then refined and mostly rewritten, primarily by Hans-J. Boehm, at Cornell U., the University of Washington, Rice University (where it was first used for C and assembly code), Xerox PARC, SGI, and HP Labs. However, significant contributions have also been made by many others.

Some other contributors:

More recent contributors are mentioned in the modification history in README.changes. My apologies for any omissions.

The SPARC specific code was
originally contributed by Mark Weiser.

The Encore Multimax modifications were supplied by
Kevin Kenny (kenny@m.cs.uiuc.edu). The adaptation to the IBM PC/RT is largely
due to Vernon Lee, on machines made available to Rice by IBM.

Much of the HP specific code and a number of good suggestions for improving the
generic code are due to Walter Underwood.

Robert Brazile (brazile@diamond.bbn.com) originally supplied the ULTRIX code.
Al Dosser (dosser@src.dec.com) and Regis Cridlig (Regis.Cridlig@cl.cam.ac.uk)
subsequently provided updates and information on variation between ULTRIX
systems. Parag Patel (parag@netcom.com) supplied the A/UX code.

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Martin Tauchmann (martintauchmann@bigfoot.com) supplied the Amiga port.

Thomas Funke (thf@zelator.in-berlin.de(?)) and
Brian D.Carlstrom (bdc@clark.lcs.mit.edu) supplied the NeXT ports.

Douglas Steel (doug@wg.icl.co.uk) provided ICL DRS6000 code.

Bill Janssen (janssen@parc.xerox.com) supplied
the SunOS dynamic loader

specific code. Manuel Serrano (serrano@cornas.inria.fr) supplied linux and
Sony News specific code. Al Dosser provided Alpha/OSF/1 code. He and
Dave Detlefs(detlefs@src.dec.com) also provided several generic bug fixes.

Alistair G. Crooks(agc@uts.amdahl.com) supplied the NetBSD and 386BSD ports.

Jeffrey Hsu (hsu@soda.berkeley.edu) provided the FreeBSD port.

Brent Benson (brent@jade.ssd.csd.harris.com) ported the collector to
a Motorola 88K processor running CX/UX (Harris NightHawk).

Ari Huttunen (Ari.Huttunen@hut.fi) generalized the OS/2 port to
nonIBM development environments (a nontrivial task).

Patrick Beard (beard@cs.ucdavis.edu) provided the initial MacOS port.

David Chase, then at Olivetti Research, suggested several improvements.

Scott Schwartz (schwartz@groucho.cse.psu.edu) supplied some of the
code to save and print call stacks for leak detection on a SPARC.

Jesse Hull and John Ellis supplied the C++ interface code.

Zhong Shao performed much of the
experimentation that led to the
current typed allocation facility. (His dynamic type inference code hasn't
made it into the released version of the collector, yet.)

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<?xml version="1.0" encoding="UTF-8"?>

<!DOCTYPE article PUBLIC "-//Boost//DTD BoostBook XML V1.0//EN"

```
"http://www.boost.org/tools/boostbook/dtd/boostbook.dtd">
<article id="copyright_test" last-revision="DEBUG MODE Date: 2000/12/20 12:00:00 $"
xmlns:xi="http://www.w3.org/2001/XInclude">
<title>Copyright Test</title>
<articleinfo>
<copyright>
<year>1963</year> <year>1964</year> <year>1965</year> <holder>Jane Doe</holder>
</copyright>
<copyright>
<year>2018</year> <holder>Joe Blow, John Coe</holder>
</copyright>
<copyright>
<year>1977</year> <year>1985</year> <holder>Someone else</holder>
</copyright>
</articleinfo>
</article>
```

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////

[#mpl]

MPL Support, <boost/mp11/mpl.hpp>

:toc:

:toc-title:

:idprefix:

The header `<boost/mp11/mpl.hpp>`, when included, defines the
necessary support infrastructure for `mp_list` and `std::tuple`
to be valid link:../../../../libs/mpl[MPL] sequences.

NOTE: `mpl.hpp` is not included by `<boost/mp11.hpp>`.

1.5 libgpg-error 1.2

1.5.1 Available under license :

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Version 1.0

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1.9 thrift 0.13.0

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1.10 linenoise 1.0.0

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```
/* linenoise.h -- guerrilla line editing library against the idea that a
 * line editing lib needs to be 20,000 lines of C code.
 *
 * See linenoise.c for more information.
 *
 * -----
 *
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 */
```

Found in path(s):

* /brick-lang-linenoise-ml-1-0-0-0-g923ca3c-tar-gz/brick-lang-linenoise-ml-923ca3c/linenoise_c/linenoise.h

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```
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 *
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```

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*/

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* /brick-lang-linenoise-ml-1-0-0-0-g923ca3c-tar-gz/brick-lang-linenoise-ml-923ca3c/headers/raw_pointer.h

* /brick-lang-linenoise-ml-1-0-0-0-g923ca3c-tar-gz/brick-lang-linenoise-ml-923ca3c/headers/complex_stubs.h

* /brick-lang-linenoise-ml-1-0-0-0-g923ca3c-tar-gz/brick-lang-linenoise-ml-923ca3c/headers/primitives.h

* /brick-lang-linenoise-ml-1-0-0-0-g923ca3c-tar-gz/brick-lang-linenoise-ml-923ca3c/headers/type_info_stubs.h

* /brick-lang-linenoise-ml-1-0-0-0-g923ca3c-tar-gz/brick-lang-linenoise-ml-923ca3c/headers/managed_buffer_stubs.h

* /brick-lang-linenoise-ml-1-0-0-0-g923ca3c-tar-gz/brick-lang-linenoise-ml-923ca3c/headers/unsigned_stubs.h

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/* linenoise.c -- guerrilla line editing library against the idea that a

* line editing lib needs to be 20,000 lines of C code.

*

* You can find the latest source code at:

*

* <http://github.com/antirez/linenoise>

*

* Does a number of crazy assumptions that happen to be true in 99.9999% of

* the 2010 UNIX computers around.

*

* -----

*

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* -----

*

* References:

* - <http://invisible-island.net/xterm/ctlseqs/ctlseqs.html>

* - <http://www.3waylabs.com/nw/WWW/products/wizcon/vt220.html>

*

* Todo list:

* - Filter bogus Ctrl+<char> combinations.

* - Win32 support

*

* Bloat:

* - History search like Ctrl+r in readline?

*

* List of escape sequences used by this program, we do everything just

* with three sequences. In order to be so cheap we may have some

* flickering effect with some slow terminal, but the lesser sequences

* the more compatible.

*

* CHA (Cursor Horizontal Absolute)

* Sequence: ESC [n G

* Effect: moves cursor to column n

*

* EL (Erase Line)

* Sequence: ESC [n K

* Effect: if n is 0 or missing, clear from cursor to end of line

* Effect: if n is 1, clear from beginning of line to cursor

* Effect: if n is 2, clear entire line

*

* CUF (CUrsor Forward)

* Sequence: ESC [n C

* Effect: moves cursor forward of n

chars

*

* When multi line mode is enabled, we also use an additional escape

* sequence. However multi line editing is disabled by default.

*

* CUU (CUrsor Up)

* Sequence: ESC [n A

* Effect: moves cursor up of n chars.

*

* CUD (CUrsor Down)

* Sequence: ESC [n B

- * Effect: moves cursor down of n chars.
- *
- * The following are used to clear the screen: ESC [H ESC [2 J
- * This is actually composed of two sequences:
- *
- * cursorhome
- * Sequence: ESC [H
- * Effect: moves the cursor to upper left corner
- *
- * ED2 (Clear entire screen)
- * Sequence: ESC [2 J
- * Effect: clear the whole screen
- *
- */

Found in path(s):

- * /brick-lang-linenoise-ml-1-0-0-0-g923ca3c-tar-gz/brick-lang-linenoise-ml-923ca3c/linenoise_c/linenoise.c

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OASISFormat: 0.4

Name: linenoise

Version: 0.1

Synopsis: A small readline replacement

Authors: Katherine Whitlock

License: BSD-3-clause

Plugins: META(0.4)

Library linenoise

Path: .

BuildTools: ocamlbuild

CSources: linenoise_stubs.c, linenoise_c/linenoise.c, linenoise_c/linenoise.h, headers/complex_stubs.h, headers/cstubs_internals.h, headers/managed_buffer_stubs.h, headers/primitives.h, headers/raw_pointer.h, headers/type_info_stubs.h, headers/unsigned_stubs.h

BuildDepends: ctypes.foreign, ctypes.stubs, core, threads

Modules: Linenoise_bindings, Linenoise

Install: true

SourceRepository head

Type: git

Location: <https://github.com/brick-lang/linenoise-ml>

Browser: <https://github.com/brick-lang/linenoise-ml>

Found in path(s):

- * /brick-lang-linenoise-ml-1-0-0-0-g923ca3c-tar-gz/brick-lang-linenoise-ml-923ca3c/_oasis

1.11 Iz4 1.8.1

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Upstream-Name: liblz4

Upstream-Contact: Yann Collet <Cyan4973@github.com>

Source: <https://github.com/lz4/lz4>

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1.12 rapidxml 1.13

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1.15 Iz4 1.9.3

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Upstream-Name: liblz4

Upstream-Contact: Yann Collet <Cyan4973@github.com>

Source: <https://github.com/lz4/lz4>

Files: *

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1.16 log4net 1.2

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1.21 json-cpp 1.9.5

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1.22 libcxxabi 9.0.1

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1.23 libcxx 9.0.1

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1.24 rocksdb 6.22.1

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1.25 libarchive 3.6.1

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1.26 llvm 2.16.840

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=aarch64-- | FileCheck %s

; A shuffle mask with all undef elements is always legal.

```
define <4 x i32> @PR41535(<2 x i32> %p1, <2 x i32> %p2) {  
; CHECK-LABEL: PR41535:  
; CHECK:      // %bb.0:  
; CHECK-NEXT:  ext v0.8b, v0.8b, v1.8b, #4  
; CHECK-NEXT:  mov v0.d[1], v0.d[0]
```

```
; CHECK-NEXT:  ret
%cat1 = shufflevector <2 x i32> %p1, <2 x i32> undef, <4 x i32> <i32 undef, i32 1, i32 undef, i32 undef>
%cat2 = shufflevector <2 x i32> %p2, <2 x i32> undef, <4 x i32> <i32 0, i32 undef, i32 undef, i32 undef>
%r = shufflevector <4 x i32> %cat1, <4 x i32> %cat2, <4 x i32> <i32 undef, i32 undef, i32 1, i32 4>
ret <4 x i32> %r
}
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=amdgc -mcpu=fiji < %s | FileCheck -enable-var-scope --check-prefixes=GCN,GCN-
SAFE,VI,VI-SAFE %s
; RUN: llc -enable-no-signed-zeros-fp-math -mtriple=amdgc -mcpu=fiji < %s | FileCheck -enable-var-scope --
check-prefixes=GCN,GCN-NSZ,VI,VI-NSZ %s
```

```
; -----
; rcp tests
; -----
```

```
define half @v_fneg_rcp_f16(half %a) #0 {
; GCN-LABEL: v_fneg_rcp_f16:
; GCN:      ; %bb.0:
; GCN-NEXT:  s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; GCN-NEXT:  v_rcp_f16_e64 v0, -v0
; GCN-NEXT:  s_setpc_b64 s[30:31]
%rcp = call half @llvm.amdgc.rcp.f16(half %a)
%fneg = fneg half %rcp
ret half %fneg
}
```

```
define half @v_fneg_rcp_fneg_f16(half %a) #0 {
; GCN-LABEL: v_fneg_rcp_fneg_f16:
; GCN:      ; %bb.0:
; GCN-NEXT:  s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; GCN-NEXT:
    v_rcp_f16_e32 v0, v0
; GCN-NEXT:  s_setpc_b64 s[30:31]
%fneg.a = fneg half %a
%rcp = call half @llvm.amdgc.rcp.f16(half %fneg.a)
%fneg = fneg half %rcp
ret half %fneg
}
```

```
define { half, half } @v_fneg_rcp_store_use_fneg_f16(half %a) #0 {
; GCN-LABEL: v_fneg_rcp_store_use_fneg_f16:
; GCN:      ; %bb.0:
; GCN-NEXT:  s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; GCN-NEXT:  v_rcp_f16_e32 v2, v0
; GCN-NEXT:  v_xor_b32_e32 v1, 0x8000, v0
; GCN-NEXT:  v_mov_b32_e32 v0, v2
; GCN-NEXT:  s_setpc_b64 s[30:31]
```

```

%fneg.a = fneg half %a
%rcp = call half @llvm.amdgcn.rcp.f16(half %fneg.a)
%fneg = fneg half %rcp
%insert.0 = insertvalue { half, half } poison, half %fneg, 0
%insert.1 = insertvalue { half, half } %insert.0, half %fneg.a, 1
ret { half, half } %insert.1
}

define { half, half } @v_fneg_rcp_multi_use_fneg_f16(half %a, half %c) #0 {
; GCN-LABEL: v_fneg_rcp_multi_use_fneg_f16:
; GCN:      ; %bb.0:
; GCN-NEXT:  s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; GCN-NEXT:
    v_rcp_f16_e32 v2, v0
; GCN-NEXT:  v_mul_f16_e64 v1, -v0, v1
; GCN-NEXT:  v_mov_b32_e32 v0, v2
; GCN-NEXT:  s_setpc_b64 s[30:31]
%fneg.a = fneg half %a
%rcp = call half @llvm.amdgcn.rcp.f16(half %fneg.a)
%fneg = fneg half %rcp
%use1 = fmul half %fneg.a, %c
%insert.0 = insertvalue { half, half } poison, half %fneg, 0
%insert.1 = insertvalue { half, half } %insert.0, half %use1, 1
ret { half, half } %insert.1
}

; -----
; sin tests
; -----

define half @v_fneg_amdgcn_sin_f16(half %a) #0 {
; GCN-LABEL: v_fneg_amdgcn_sin_f16:
; GCN:      ; %bb.0:
; GCN-NEXT:  s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; GCN-NEXT:  v_sin_f16_e64 v0, -v0
; GCN-NEXT:  s_setpc_b64 s[30:31]
%sin = call half @llvm.amdgcn.sin.f16(half %a)
%fneg = fneg half %sin
ret half %fneg
}

; -----
;
; vintrp tests
; -----

define { float, float } @v_fneg_interp_p1_f16(float %a, float %b) #0 {
; GCN-LABEL: v_fneg_interp_p1_f16:

```

```

; GCN:      ; %bb.0:
; GCN-NEXT:  s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; GCN-NEXT:  v_mul_f32_e64 v1, v0, -v1
; GCN-NEXT:  s_mov_b32 m0, 0
; GCN-NEXT:  s_setreg_imm32_b32 hwreg(HW_REG_MODE, 2, 2), 3
; GCN-NEXT:  v_interp_p1ll_f16 v0, v1, attr0.x
; GCN-NEXT:  v_interp_p1ll_f16 v1, v1, attr0.y
; GCN-NEXT:  s_setpc_b64 s[30:31]
%mul = fmul float %a, %b
%fneg = fneg float %mul
%intrap0 = call float @llvm.amdgcn.interp.p1.f16(float %fneg, i32 0, i32 0, i1 false, i32 0)
%intrap1 = call float @llvm.amdgcn.interp.p1.f16(float %fneg, i32 1, i32 0, i1 false, i32 0)
%insert.0 = insertvalue { float, float } poison, float %intrap0, 0
%insert.1 = insertvalue { float, float } %insert.0, float %intrap1, 1
ret { float, float } %insert.1
}

define
{ half, half } @v_fneg_interp_p2_f16(float %a, float %b) #0 {
; GCN-LABEL: v_fneg_interp_p2_f16:
; GCN:      ; %bb.0:
; GCN-NEXT:  s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; GCN-NEXT:  v_mul_f32_e64 v1, v0, -v1
; GCN-NEXT:  v_mov_b32_e32 v2, 4.0
; GCN-NEXT:  s_mov_b32 m0, 0
; GCN-NEXT:  s_setreg_imm32_b32 hwreg(HW_REG_MODE, 2, 2), 3
; GCN-NEXT:  v_interp_p2_f16 v0, v1, attr0.x, v2
; GCN-NEXT:  v_interp_p2_f16 v1, v1, attr0.y, v2
; GCN-NEXT:  s_setpc_b64 s[30:31]
%mul = fmul float %a, %b
%fneg = fneg float %mul
%intrap0 = call half @llvm.amdgcn.interp.p2.f16(float 4.0, float %fneg, i32 0, i32 0, i1 false, i32 0)
%intrap1 = call half @llvm.amdgcn.interp.p2.f16(float 4.0, float %fneg, i32 1, i32 0, i1 false, i32 0)
%insert.0 = insertvalue { half, half } poison, half %intrap0, 0
%insert.1 = insertvalue { half, half } %insert.0, half %intrap1, 1
ret { half, half } %insert.1
}

; -----
;
; arithmetic.fence tests
; -----

; FIXME: Legalization/promote is broken
define half @v_fneg_arithmetic_fence_f16(half %a) #0 {
; GCN-LABEL: v_fneg_arithmetic_fence_f16:
; GCN:      ; %bb.0:
; GCN-NEXT:  ; ARITH_FENCE

```

```

; GCN-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; GCN-NEXT: v_xor_b32_e32 v0, 0x8000, v0
; GCN-NEXT: s_setpc_b64 s[30:31]
%fence = call half @llvm.arithmetic.fence.f16(half %a)
%fneg = fneg half %fence
ret half %fneg
}

define half @v_fneg_arithmetic_fence_fmuls_f16(half %a, half %b) #0 {
; GCN-LABEL: v_fneg_arithmetic_fence_fmuls_f16:
; GCN:      ; %bb.0:
; GCN-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; GCN-NEXT: v_mul_f16_e32 v0, v0, v1
; GCN-NEXT: ;ARITH_FENCE
; GCN-NEXT: v_xor_b32_e32 v0, 0x8000, v0
; GCN-NEXT: s_setpc_b64 s[30:31]
%mul = fmul half %a, %b
%fence = call half @llvm.arithmetic.fence.f16(half %mul)
%fneg = fneg half %fence
ret half
%fneg
}

declare half @llvm.amdgcn.rcp.f16(half) #1
declare half @llvm.amdgcn.sin.f16(half) #1
declare half @llvm.arithmetic.fence.f16(half) #1
declare float @llvm.amdgcn.interp.p1.f16(float, i32, i32, i1, i32) #0
declare half @llvm.amdgcn.interp.p2.f16(float, float, i32, i32, i1, i32) #0

attributes #0 = { nounwind "denormal-fp-math-f32"="preserve-sign,preserve-sign" }
attributes #1 = { nounwind readnone }
attributes #2 = { nounwind "unsafe-fp-math"="true" }
attributes #3 = { nounwind "no-signed-zeros-fp-math"="true" }
attributes #4 = { nounwind "amdgpu-ieee"="false" "denormal-fp-math-f32"="preserve-sign,preserve-sign" }
;; NOTE: These prefixes are unused and the list is autogenerated. Do not add tests below this line:
; GCN-NSZ: {{.*}}
; GCN-SAFE: {{.*}}
; VI: {{.*}}
; VI-NSZ: {{.*}}
; VI-SAFE: {{.*}}
; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature --
check-attributes --check-globals
; RUN: opt -aa-pipeline=basic-aa -passes=attributor -attributor-manifest-internal -attributor-annotate-decl-cs -S <
%$ | FileCheck %$ --check-prefixes=CHECK,TUNIT
; RUN: opt -aa-pipeline=basic-aa -passes=attributor-cgscs -attributor-manifest-internal -attributor-annotate-decl-cs -
S < %$ | FileCheck %$ --check-prefixes=CHECK,CGSCC
; Test that we only promote arguments when the caller/callee have compatible
; function attributes.

```

target triple = "x86_64-unknown-linux-gnu"

; This should promote

define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr %arg, ptr
readonly %arg1) #0 {

;

; CHECK: Function Attrs: inlinehint mustprogress nofree norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable

; CHECK-LABEL: define {{{^@}+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512

; CHECK-SAME:

(ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>
[[TMP0:%.*]]) #[[ATTR0:[0-9]+]] {

; CHECK-NEXT: bb:

; CHECK-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64

; CHECK-NEXT: store <8 x i64> [[TMP0]], ptr [[ARG1_PRIV]], align 64

; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1_PRIV]], align 64

; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64

; CHECK-NEXT: ret void

;

bb:

%tmp = load <8 x i64>, ptr %arg1

store <8 x i64> %tmp, ptr %arg

ret void

}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr %arg) #0 {

;

; TUNIT: Function Attrs: inlinehint mustprogress nofree norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable

; TUNIT-LABEL: define {{{^@}+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512

; TUNIT-SAME: (ptr nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR0]] {

; TUNIT-NEXT: bb:

; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align

32

; TUNIT-NEXT: [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32

; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 32
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5:[0-9]+]]

; TUNIT-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64

; TUNIT-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr
noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], <8 x i64>
[[TMP0]]) #[[ATTR6:[0-9]+]]

; TUNIT-NEXT: [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64

; TUNIT-NEXT: store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2

; TUNIT-NEXT: ret void

;

; CGSCC: Function Attrs: inlinehint mustprogress nofree norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable

```

; CGSCC-LABEL: define {{^[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
; CGSCC-SAME: (ptr nocapture
  nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]]) #[[ATTR0]] {
; CGSCC-NEXT: bb:
; CGSCC-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5:[0-9]+]]
; CGSCC-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; CGSCC-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr
noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], <8 x i64>
[[TMP0]]) #[[ATTR6:[0-9]+]]
; CGSCC-NEXT: [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; CGSCC-NEXT: store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; CGSCC-NEXT: ret void
;
bb:
  %tmp = alloca <8 x i64>, align 32
  %tmp2 = alloca <8 x i64>, align 32
  call void
  @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
  call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr %tmp2, ptr %tmp)
  %tmp4 = load <8 x i64>, ptr %tmp2, align 32
  store <8 x i64> %tmp4, ptr %arg, align 2
  ret void
}

```

; This should promote

```

define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr %arg, ptr
readonly %arg1) #1 {
;

```

```

; CHECK: Function Attrs: inlinehint mustprogress nofree norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable

```

```

; CHECK-LABEL: define {{^[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256

```

```

; CHECK-SAME: (ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)

```

```

[[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR1:[0-9]+]] {

```

```

; CHECK-NEXT: bb:

```

```

; CHECK-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64

```

```

; CHECK-NEXT: store <8 x i64> [[TMP0]], ptr [[ARG1_PRIV]], align 64

```

```

; CHECK-NEXT: [[TMP:%.*]] = load <8 x

```

```

i64>, ptr [[ARG1_PRIV]], align 64

```

```

; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64

```

```

; CHECK-NEXT: ret void
;

```

```

;

```

```

bb:

```

```

  %tmp = load <8 x i64>, ptr %arg1

```

```

  store <8 x i64> %tmp, ptr %arg

```

```

  ret void

```

```

}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr %arg) #1 {
;
; TUNIT: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; TUNIT-LABEL: define {{{^@+}}} @avx512_legal512_prefer256_call_avx512_legal512_prefer256
; TUNIT-SAME: (ptr nocapture norecurse writeonly [[ARG:%.*]]) #[[ATTR1]] {
; TUNIT-NEXT: bb:
; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture norecurse noundef nonnull writeonly align 32
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; TUNIT-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; TUNIT-NEXT:
    call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr noalias nocapture
norecurse noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], <8 x i64> [[TMP0]]) #[[ATTR6]]
; TUNIT-NEXT: [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; TUNIT-NEXT: store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; TUNIT-NEXT: ret void
;
; CGSCC: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; CGSCC-LABEL: define {{{^@+}}} @avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CGSCC-SAME: (ptr nocapture norecurse noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
#[[ATTR1]] {
; CGSCC-NEXT: bb:
; CGSCC-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture norecurse noundef nonnull writeonly align 64
dereferenceable(64)
[[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; CGSCC-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; CGSCC-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr
noalias nocapture norecurse noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], <8 x i64>
[[TMP0]]) #[[ATTR6]]
; CGSCC-NEXT: [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; CGSCC-NEXT: store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; CGSCC-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void

```



```

}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr
%arg, ptr readonly %arg1) #1 {
;
; CHECK: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr noalias nocapture norecurse noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR1]] {
; CHECK-NEXT: bb:
; CHECK-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; CHECK-NEXT: store <8 x i64> [[TMP0]], ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr %arg) #0 {
;
; TUNIT: Function Attrs: inlinehint mustprogress norecurse nosync nounwind
willreturn memory(argmem: readwrite) uwtable
; TUNIT-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; TUNIT-SAME: (ptr nocapture norecurse writeonly [[ARG:%.*]]) #[[ATTR0]] {
; TUNIT-NEXT: bb:
; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture norecurse noundef nonnull writeonly align 32
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; TUNIT-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; TUNIT-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr
noalias nocapture norecurse noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], <8 x i64>
[[TMP0]]) #[[ATTR6]]
; TUNIT-NEXT: [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; TUNIT-NEXT: store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; TUNIT-NEXT:
ret void
;
; CGSCC: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; CGSCC-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CGSCC-SAME: (ptr nocapture norecurse noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])

```

```

#[[ATTR0]] {
; CGSCC-NEXT: bb:
; CGSCC-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT:  [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT:  call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; CGSCC-NEXT:  [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; CGSCC-NEXT:  call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr
noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], <8 x i64>
[[TMP0]]) #[[ATTR6]]
; CGSCC-NEXT:
    [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; CGSCC-NEXT:  store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; CGSCC-NEXT:  ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr %arg, ptr
readonly %arg1) #0 {
;
; CHECK: Function Attrs: inlinehint mustprogress nofree norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; CHECK-LABEL: define { {^@}+ } @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]],
<8 x i64> [[TMP0:%.*]]) #[[ATTR0]] {
; CHECK-NEXT: bb:
; CHECK-NEXT:  [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; CHECK-NEXT:  store <8 x i64> [[TMP0]], ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT:  [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT:  store <8 x i64> [[TMP]], ptr [[ARG]], align 64
; CHECK-NEXT:  ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
}

```

```

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr %arg) #1 {
;
; TUNIT: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; TUNIT-LABEL: define {{^@+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; TUNIT-SAME: (ptr nocapture norecurse writeonly [[ARG:%.*]]) #[[ATTR1]] {
; TUNIT-NEXT: bb:
; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr
noalias nocapture norecurse noundef nonnull writeonly align 32 dereferenceable(64) [[TMP]], i8 noundef 0, i64
noundef 32, i1 noundef false) #[[ATTR5]]
; TUNIT-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; TUNIT-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr
noalias nocapture norecurse noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], <8 x i64>
[[TMP0]]) #[[ATTR6]]
; TUNIT-NEXT: [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; TUNIT-NEXT: store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; TUNIT-NEXT: ret void
;
; CGSCC: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; CGSCC-LABEL: define {{^@+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CGSCC-SAME: (ptr nocapture norecurse noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
#[[ATTR1]] {
; CGSCC-NEXT: bb:
; CGSCC-NEXT:
[[TMP:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture norecurse noundef nonnull writeonly align 64
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; CGSCC-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; CGSCC-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr
noalias nocapture norecurse noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], <8 x i64>
[[TMP0]]) #[[ATTR6]]
; CGSCC-NEXT: [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; CGSCC-NEXT: store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; CGSCC-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr
%tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void

```

```

}

; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr %arg, ptr
readonly %arg1) #1 {
;
; CHECK: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; CHECK-LABEL: define {{{^@+}}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr noalias nocapture norecurse noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], ptr noalias nocapture norecurse noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR1]] {
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1]], align 64
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr %arg) #2 {
;
; TUNIT: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; TUNIT-LABEL: define {{{^@+}}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; TUNIT-SAME: (ptr nocapture norecurse writeonly [[ARG:%.*]]) #[[ATTR2:[0-9]+]] {
; TUNIT-NEXT: bb:
; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture norecurse noundef nonnull writeonly align 32
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; TUNIT-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr
noalias nocapture norecurse noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], ptr noalias
nocapture norecurse noundef nonnull readonly align 64 dereferenceable(64)
[[TMP]]) #[[ATTR6]]
; TUNIT-NEXT: [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; TUNIT-NEXT: store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; TUNIT-NEXT: ret void
;
; CGSCC: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; CGSCC-LABEL: define {{{^@+}}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CGSCC-SAME: (ptr nocapture norecurse noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
#[[ATTR2:[0-9]+]] {
; CGSCC-NEXT: bb:

```

```

; CGSCC-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture norecurse nosync nounwind willreturn memory(argmem:
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; CGSCC-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal256_prefer256(ptr
noalias
nocapture norecurse noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], ptr noalias nocapture
norecurse noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR6]]
; CGSCC-NEXT: [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; CGSCC-NEXT: store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; CGSCC-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal256_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal256_prefer256(ptr %arg, ptr
readonly %arg1) #2 {
;
; CHECK: Function Attrs: inlinehint mustprogress norecurse norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
;
CHECK-LABEL: define {{^[^@]+}}@callee_avx512_legal256_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (ptr noalias nocapture norecurse noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], ptr noalias nocapture norecurse noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR2:[0-9]+]] {
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1]], align 64
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal256_prefer256(ptr %arg) #1 {
;
; TUNIT: Function Attrs: inlinehint mustprogress norecurse norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable

```

```

; TUNIT-LABEL: define {{^(^@)+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; TUNIT-SAME: (ptr nocapture norelease writeonly [[ARG:%.*]]) #[[ATTR1]] {
; TUNIT-NEXT: bb:
; TUNIT-NEXT:
    [[TMP:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT:  [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT:  call void @llvm.memset.p0.i64(ptr noalias nocapture norelease noundef nonnull writeonly align 32
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; TUNIT-NEXT:  call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr
noalias nocapture norelease noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], ptr noalias
nocapture norelease noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR6]]
; TUNIT-NEXT:  [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; TUNIT-NEXT:  store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; TUNIT-NEXT:  ret void
;
; CGSCC: Function Attrs: inlinehint mustprogress norelease norecure nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; CGSCC-LABEL: define {{^(^@)+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
;
    CGSCC-SAME: (ptr nocapture norelease noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
#[[ATTR1]] {
; CGSCC-NEXT: bb:
; CGSCC-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT:  [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT:  call void @llvm.memset.p0.i64(ptr noalias nocapture norelease noundef nonnull writeonly align 64
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; CGSCC-NEXT:  call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr
noalias nocapture norelease noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], ptr noalias
nocapture norelease noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR6]]
; CGSCC-NEXT:  [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; CGSCC-NEXT:  store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; CGSCC-NEXT:  ret void
;
bb:
    %tmp = alloca <8 x i64>, align 32
    %tmp2 = alloca <8 x i64>,
    align 32
    call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
    call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr %tmp2, ptr %tmp)
    %tmp4 = load <8 x i64>, ptr %tmp2, align 32
    store <8 x i64> %tmp4, ptr %arg, align 2
    ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr %arg, ptr readonly
%arg1) #3 {
;

```

```

; CHECK: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; CHECK-LABEL: define {{^(^@)+}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (ptr noalias nocapture norecurse noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR3:[0-9]+]] {
; CHECK-NEXT: bb:
; CHECK-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; CHECK-NEXT: store <8 x i64> [[TMP0]], ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT: [[TMP:%.*]]
= load <8 x i64>, ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr %arg) #4 {
;
; TUNIT: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; TUNIT-LABEL: define {{^(^@)+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; TUNIT-SAME: (ptr nocapture norecurse writeonly [[ARG:%.*]]) #[[ATTR3]] {
; TUNIT-NEXT: bb:
; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture norecurse noundef nonnull writeonly align 32
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; TUNIT-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
;
TUNIT-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr noalias
nocapture norecurse noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], <8 x i64> [[TMP0]])
#[[ATTR6]]
; TUNIT-NEXT: [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; TUNIT-NEXT: store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; TUNIT-NEXT: ret void
;
; CGSCC: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; CGSCC-LABEL: define {{^(^@)+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CGSCC-SAME: (ptr nocapture norecurse noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
#[[ATTR3]] {
; CGSCC-NEXT: bb:
; CGSCC-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture norecurse noundef nonnull writeonly align 64

```

```

dereferenceable(64) [[TMP]],
i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; CGSCC-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; CGSCC-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr noalias
nocapture norefree noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], <8 x i64> [[TMP0]])
#[[ATTR6]]
; CGSCC-NEXT: [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; CGSCC-NEXT: store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; CGSCC-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr
%arg, ptr readonly %arg1) #4 {
;
; CHECK: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; CHECK-LABEL: define {{^(^@)+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (ptr noalias nocapture norefree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR3]] {
; CHECK-NEXT: bb:
; CHECK-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; CHECK-NEXT: store <8 x i64> [[TMP0]], ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr %arg) #3 {
;
; TUNIT: Function Attrs: inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; TUNIT-LABEL: define {{^(^@)+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; TUNIT-SAME: (ptr nocapture norefree writeonly [[ARG:%.*]]) #[[ATTR3]] {

```



```

; TUNIT-NEXT: bb:
; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture norecurse noundef nonnull writeonly align 32
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; TUNIT-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; TUNIT-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr noalias
nocapture norecurse noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], <8 x i64> [[TMP0]])
#[[ATTR6]]
; TUNIT-NEXT: [[TRUETMP4:%.*]] = load <8 x i64>, ptr [[TRUETMP2]], align 64
; TUNIT-NEXT: store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; TUNIT-NEXT: ret void
;
; CGSCC: Function
Attrs: inlinehint mustprogress norecurse norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable
; CGSCC-LABEL: define { {^@}+ } @avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CGSCC-SAME: (ptr nocapture norecurse noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
#[[ATTR3]] {
; CGSCC-NEXT: bb:
; CGSCC-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: [[TRUETMP2:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture norecurse noundef nonnull writeonly align 64
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; CGSCC-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; CGSCC-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr noalias
nocapture norecurse noundef nonnull writeonly align 64 dereferenceable(64) [[TRUETMP2]], <8 x i64> [[TMP0]])
#[[ATTR6]]
; CGSCC-NEXT: [[TRUETMP4:%.*]] = load <8 x i64>,
ptr [[TRUETMP2]], align 64
; CGSCC-NEXT: store <8 x i64> [[TRUETMP4]], ptr [[ARG]], align 2
; CGSCC-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0.i64(ptr nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-

```

```

width="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="256"
"prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512"
"prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256"
"prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }
;
; TUNIT: attributes #[[ATTR0]] = { inlinehint mustprogress norecurse nosync nounwind willreturn
memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="512" "target-
features"="+avx512vl" }
; TUNIT: attributes #[[ATTR1]] = { inlinehint mustprogress norecurse nosync nounwind willreturn
memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-
features"="+avx512vl" }
; TUNIT: attributes #[[ATTR2]] = { inlinehint mustprogress norecurse nosync nounwind willreturn
memory(argmem: readwrite) uwtable "min-legal-vector-width"="256" "prefer-vector-width"="256"
"target-features"="+avx512vl" }
; TUNIT: attributes #[[ATTR3]] = { inlinehint mustprogress norecurse nosync nounwind willreturn
memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-
features"="+avx2" }
; TUNIT: attributes #[[ATTR4:[0-9]+]] = { norecurse norecurse nosync nounwind willreturn memory(argmem: write) }
; TUNIT: attributes #[[ATTR5]] = { norecurse willreturn memory(write) }
; TUNIT: attributes #[[ATTR6]] = { norecurse nosync nounwind willreturn }
;
; CGSCC: attributes #[[ATTR0]] = { inlinehint mustprogress norecurse nosync nounwind willreturn
memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="512" "target-
features"="+avx512vl" }
; CGSCC: attributes #[[ATTR1]] = { inlinehint mustprogress norecurse nosync nounwind willreturn
memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-
features"="+avx512vl" }
; CGSCC: attributes #[[ATTR2]]
= { inlinehint mustprogress norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable
"min-legal-vector-width"="256" "prefer-vector-width"="256" "target-features"="+avx512vl" }
; CGSCC: attributes #[[ATTR3]] = { inlinehint mustprogress norecurse nosync nounwind willreturn
memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-
features"="+avx2" }
; CGSCC: attributes #[[ATTR4:[0-9]+]] = { norecurse norecurse nosync nounwind willreturn memory(argmem: write) }
; CGSCC: attributes #[[ATTR5]] = { norecurse willreturn memory(write) }
; CGSCC: attributes #[[ATTR6]] = { norecurse nounwind willreturn }
;
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefix=RV64I
; RUN: llc -mtriple=riscv64 -mattr=+zbb -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefix=RV64ZBB

```

```
declare i32 @llvmctl.i32(i32, i1)
```

```
define signext i32 @ctlz_i32(i32 signext %a) nounwind {  
; RV64I-LABEL: ctlz_i32:  
; RV64I:      # %bb.0:  
; RV64I-NEXT: beqz a0, .LBB0_2  
; RV64I-NEXT: # %bb.1: # %cond.false  
; RV64I-NEXT: addi sp, sp, -16  
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill  
; RV64I-NEXT: srliw a1, a0, 1  
; RV64I-NEXT: or a0, a0, a1  
; RV64I-NEXT: srliw a1, a0, 2  
; RV64I-NEXT: or a0, a0, a1  
; RV64I-NEXT: srliw a1, a0, 4  
; RV64I-NEXT: or a0, a0, a1  
; RV64I-NEXT: srliw a1, a0, 8  
; RV64I-NEXT: or a0, a0, a1  
; RV64I-NEXT: srliw a1, a0, 16  
; RV64I-NEXT: or a0, a0, a1  
; RV64I-NEXT:  
    not a0, a0  
; RV64I-NEXT: srliw a1, a0, 1  
; RV64I-NEXT: lui a2, 349525  
; RV64I-NEXT: addi a2, a2, 1365  
; RV64I-NEXT: and a1, a1, a2  
; RV64I-NEXT: subw a0, a0, a1  
; RV64I-NEXT: lui a1, 209715  
; RV64I-NEXT: addi a1, a1, 819  
; RV64I-NEXT: and a2, a0, a1  
; RV64I-NEXT: srliw a0, a0, 2  
; RV64I-NEXT: and a0, a0, a1  
; RV64I-NEXT: add a0, a2, a0  
; RV64I-NEXT: srliw a1, a0, 4  
; RV64I-NEXT: addw a0, a0, a1  
; RV64I-NEXT: lui a1, 61681  
; RV64I-NEXT: addiw a1, a1, -241  
; RV64I-NEXT: and a0, a0, a1  
; RV64I-NEXT: lui a1, 4112  
; RV64I-NEXT: addiw a1, a1, 257  
; RV64I-NEXT: call __muldi3  
; RV64I-NEXT: srliw a0, a0, 24  
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload  
; RV64I-NEXT: addi sp, sp, 16  
; RV64I-NEXT: ret  
; RV64I-NEXT: .LBB0_2:  
; RV64I-NEXT: li a0, 32  
; RV64I-NEXT: ret  
;
```

```

; RV64ZBB-LABEL: ctlz_i32:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  clzw a0, a0
; RV64ZBB-NEXT:  ret
%1 = call i32 @llvm.ctlz.i32(i32 %a, i1 false)
ret i32 %1
}

```

```

define signext i32 @log2_i32(i32 signext %a) nounwind {
; RV64I-LABEL: log2_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  beqz a0, .LBB1_2
; RV64I-NEXT:  # %bb.1: # %cond.false
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  srliw a1, a0, 1
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 2
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 4
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 8
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 16
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  not a0, a0
; RV64I-NEXT:  srliw a1, a0, 1
; RV64I-NEXT:  lui a2, 349525
; RV64I-NEXT:  addi a2, a2, 1365
; RV64I-NEXT:  and a1, a1, a2
; RV64I-NEXT:  subw a0, a0, a1
; RV64I-NEXT:  lui a1, 209715
; RV64I-NEXT:  addi a1, a1, 819
; RV64I-NEXT:  and a2, a0, a1
; RV64I-NEXT:  srliw a0, a0, 2
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  add a0, a2, a0
; RV64I-NEXT:
    srliw a1, a0, 4
; RV64I-NEXT:  addw a0, a0, a1
; RV64I-NEXT:  lui a1, 61681
; RV64I-NEXT:  addiw a1, a1, -241
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  lui a1, 4112
; RV64I-NEXT:  addiw a1, a1, 257
; RV64I-NEXT:  call __muldi3
; RV64I-NEXT:  srliw a0, a0, 24
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload

```

```

; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  j .LBB1_3
; RV64I-NEXT:  .LBB1_2:
; RV64I-NEXT:  li a0, 32
; RV64I-NEXT:  .LBB1_3: # %cond.end
; RV64I-NEXT:  li a1, 31
; RV64I-NEXT:  subw a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: log2_i32:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  clzw a0, a0
; RV64ZBB-NEXT:  li a1, 31
; RV64ZBB-NEXT:  subw a0, a1, a0
; RV64ZBB-NEXT:  ret
%1 = call i32 @llvmctlz.i32(i32 %a, i1 false)
%2 = sub i32 31, %1
ret i32 %2
}

define signext i32 @log2_ceil_i32(i32 signext %a) nounwind {
; RV64I-LABEL: log2_ceil_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra,
; RV64I-NEXT:  8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  sd s0, 0(sp) # 8-byte Folded Spill
; RV64I-NEXT:  addiw a0, a0, -1
; RV64I-NEXT:  li s0, 32
; RV64I-NEXT:  li a1, 32
; RV64I-NEXT:  beqz a0, .LBB2_2
; RV64I-NEXT:  # %bb.1: # %cond.false
; RV64I-NEXT:  srliw a1, a0, 1
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 2
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 4
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 8
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 16
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  not a0, a0
; RV64I-NEXT:  srliw a1, a0, 1
; RV64I-NEXT:  lui a2, 349525
; RV64I-NEXT:  addi a2, a2, 1365
; RV64I-NEXT:  and a1, a1, a2
; RV64I-NEXT:  subw a0, a0, a1

```

```

; RV64I-NEXT: lui a1, 209715
; RV64I-NEXT: addi a1, a1, 819
; RV64I-NEXT: and a2, a0, a1
; RV64I-NEXT: srliw a0, a0, 2
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: add a0, a2, a0
; RV64I-NEXT: srliw a1, a0, 4
; RV64I-NEXT:
    addw a0, a0, a1
; RV64I-NEXT: lui a1, 61681
; RV64I-NEXT: addiw a1, a1, -241
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: lui a1, 4112
; RV64I-NEXT: addiw a1, a1, 257
; RV64I-NEXT: call __muldi3
; RV64I-NEXT: srliw a1, a0, 24
; RV64I-NEXT: .LBB2_2: # %cond.end
; RV64I-NEXT: subw a0, s0, a1
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: ld s0, 0(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
;
; RV64ZBB-LABEL: log2_ceil_i32:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT: addi a0, a0, -1
; RV64ZBB-NEXT: clzw a0, a0
; RV64ZBB-NEXT: li a1, 32
; RV64ZBB-NEXT: subw a0, a1, a0
; RV64ZBB-NEXT: ret
%1 = sub i32 %a, 1
%2 = call i32 @llvmctlz.i32(i32 %1, i1 false)
%3 = sub i32 32, %2
ret i32 %3
}

define signext i32 @findLastSet_i32(i32 signext %a) nounwind {
; RV64I-LABEL: findLastSet_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
;
    RV64I-NEXT: sd s0, 0(sp) # 8-byte Folded Spill
; RV64I-NEXT: mv s0, a0
; RV64I-NEXT: srliw a0, a0, 1
; RV64I-NEXT: or a0, s0, a0
; RV64I-NEXT: srliw a1, a0, 2
; RV64I-NEXT: or a0, a0, a1

```

```

; RV64I-NEXT: srliw a1, a0, 4
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srliw a1, a0, 8
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srliw a1, a0, 16
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: not a0, a0
; RV64I-NEXT: srliw a1, a0, 1
; RV64I-NEXT: lui a2, 349525
; RV64I-NEXT: addi a2, a2, 1365
; RV64I-NEXT: and a1, a1, a2
; RV64I-NEXT: subw a0, a0, a1
; RV64I-NEXT: lui a1, 209715
; RV64I-NEXT: addi a1, a1, 819
; RV64I-NEXT: and a2, a0, a1
; RV64I-NEXT: srliw a0, a0, 2
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: add a0, a2, a0
; RV64I-NEXT: srliw a1, a0, 4
; RV64I-NEXT: addw a0, a0, a1
; RV64I-NEXT: lui a1, 61681
; RV64I-NEXT: addiw a1, a1, -241
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: lui a1, 4112
; RV64I-NEXT:
    addiw a1, a1, 257
; RV64I-NEXT: call __muldi3
; RV64I-NEXT: srliw a0, a0, 24
; RV64I-NEXT: xori a0, a0, 31
; RV64I-NEXT: snez a1, s0
; RV64I-NEXT: addiw a1, a1, -1
; RV64I-NEXT: or a0, a1, a0
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: ld s0, 0(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
;
; RV64ZBB-LABEL: findLastSet_i32:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT: clzw a1, a0
; RV64ZBB-NEXT: xori a1, a1, 31
; RV64ZBB-NEXT: snez a0, a0
; RV64ZBB-NEXT: addiw a0, a0, -1
; RV64ZBB-NEXT: or a0, a0, a1
; RV64ZBB-NEXT: ret
%1 = call i32 @llvm.ctlz.i32(i32 %a, i1 true)
%2 = xor i32 31, %1
%3 = icmp eq i32 %a, 0

```

```

%4 = select i1 %3, i32 -1, i32 %2
ret i32 %4
}

```

```

define i32 @ctlz_lshr_i32(i32 signext %a) {
; RV64I-LABEL: ctlz_lshr_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srlw a0, a0, 1
; RV64I-NEXT:  beqz a0, .LBB4_2
; RV64I-NEXT:  # %bb.1: # %cond.false
; RV64I-NEXT:  addi sp, sp,
-16
; RV64I-NEXT:  .cfi_def_cfa_offset 16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  .cfi_offset ra, -8
; RV64I-NEXT:  srlw a1, a0, 1
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srlw a1, a0, 2
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srlw a1, a0, 4
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srlw a1, a0, 8
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srlw a1, a0, 16
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  not a0, a0
; RV64I-NEXT:  srlw a1, a0, 1
; RV64I-NEXT:  lui a2, 349525
; RV64I-NEXT:  addi a2, a2, 1365
; RV64I-NEXT:  and a1, a1, a2
; RV64I-NEXT:  subw a0, a0, a1
; RV64I-NEXT:  lui a1, 209715
; RV64I-NEXT:  addi a1, a1, 819
; RV64I-NEXT:  and a2, a0, a1
; RV64I-NEXT:  srlw a0, a0, 2
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  add a0, a2, a0
; RV64I-NEXT:  srlw a1, a0, 4
; RV64I-NEXT:  addw a0, a0, a1
; RV64I-NEXT:  lui a1, 61681
; RV64I-NEXT:  addiw a1, a1, -241
; RV64I-NEXT:  and a0,
a0, a1
; RV64I-NEXT:  lui a1, 4112
; RV64I-NEXT:  addiw a1, a1, 257
; RV64I-NEXT:  call __muldi3
; RV64I-NEXT:  srlw a0, a0, 24
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload

```



```

; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
; RV64I-NEXT:  .LBB4_2:
; RV64I-NEXT:  li a0, 32
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: ctlz_lshr_i32:
; RV64ZBB:     # %bb.0:
; RV64ZBB-NEXT:  srliw a0, a0, 1
; RV64ZBB-NEXT:  clzw a0, a0
; RV64ZBB-NEXT:  ret
%1 = lshr i32 %a, 1
%2 = call i32 @llvm.ctlz.i32(i32 %1, i1 false)
ret i32 %2
}

```

```

declare i64 @llvm.ctlz.i64(i64, i1)

```

```

define i64 @ctlz_i64(i64 %a) nounwind {
; RV64I-LABEL: ctlz_i64:
; RV64I:     # %bb.0:
; RV64I-NEXT:  beqz a0, .LBB5_2
; RV64I-NEXT:  # %bb.1: # %cond.false
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  srli a1, a0, 1
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srli a1, a0, 2
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srli a1, a0, 4
; RV64I-NEXT:
    or a0, a0, a1
; RV64I-NEXT:  srli a1, a0, 8
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srli a1, a0, 16
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srli a1, a0, 32
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  not a0, a0
; RV64I-NEXT:  srli a1, a0, 1
; RV64I-NEXT:  lui a2, 349525
; RV64I-NEXT:  addiw a2, a2, 1365
; RV64I-NEXT:  slli a3, a2, 32
; RV64I-NEXT:  add a2, a2, a3
; RV64I-NEXT:  and a1, a1, a2
; RV64I-NEXT:  sub a0, a0, a1
; RV64I-NEXT:  lui a1, 209715
; RV64I-NEXT:  addiw a1, a1, 819

```

```

; RV64I-NEXT: slli a2, a1, 32
; RV64I-NEXT: add a1, a1, a2
; RV64I-NEXT: and a2, a0, a1
; RV64I-NEXT: srli a0, a0, 2
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: add a0, a2, a0
; RV64I-NEXT: srli a1, a0, 4
; RV64I-NEXT: add a0, a0, a1
; RV64I-NEXT: lui a1, 61681
; RV64I-NEXT: addiw a1, a1, -241
; RV64I-NEXT: slli a2, a1, 32
; RV64I-NEXT: add a1, a1, a2
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: lui a1, 4112
; RV64I-NEXT:
    addiw a1, a1, 257
; RV64I-NEXT: slli a2, a1, 32
; RV64I-NEXT: add a1, a1, a2
; RV64I-NEXT: call __muldi3
; RV64I-NEXT: srli a0, a0, 56
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
; RV64I-NEXT: .LBB5_2:
; RV64I-NEXT: li a0, 64
; RV64I-NEXT: ret
;
; RV64ZBB-LABEL: ctlz_i64:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT: clz a0, a0
; RV64ZBB-NEXT: ret
%1 = call i64 @llvm.ctlz.i64(i64 %a, i1 false)
ret i64 %1
}

```

```

declare i32 @llvm.cttz.i32(i32, i1)

```

```

define signext i32 @cttz_i32(i32 signext %a) nounwind {
; RV64I-LABEL: cttz_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT: beqz a0, .LBB6_2
; RV64I-NEXT: # %bb.1: # %cond.false
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT: negw a1, a0
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: lui a1, 30667
; RV64I-NEXT: addiw a1, a1, 1329

```

```

; RV64I-NEXT:  call __muldi3
; RV64I-NEXT:  srliw a0, a0, 27
;
RV64I-NEXT:  lui a1, %hi(.LCPI6_0)
; RV64I-NEXT:  addi a1, a1, %lo(.LCPI6_0)
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  lbu a0, 0(a0)
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
; RV64I-NEXT:  .LBB6_2:
; RV64I-NEXT:  li a0, 32
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: cttz_i32:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  ctw a0, a0
; RV64ZBB-NEXT:  ret
%1 = call i32 @llvm.cttz.i32(i32 %a, i1 false)
ret i32 %1
}

define signext i32 @cttz_zero_undef_i32(i32 signext %a) nounwind {
; RV64I-LABEL: cttz_zero_undef_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  negw a1, a0
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  lui a1, 30667
; RV64I-NEXT:  addiw a1, a1, 1329
; RV64I-NEXT:  call __muldi3
; RV64I-NEXT:  srliw a0, a0, 27
; RV64I-NEXT:  lui a1, %hi(.LCPI7_0)
; RV64I-NEXT:  addi a1, a1, %lo(.LCPI7_0)
; RV64I-NEXT:
add a0, a1, a0
; RV64I-NEXT:  lbu a0, 0(a0)
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: cttz_zero_undef_i32:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  ctw a0, a0
; RV64ZBB-NEXT:  ret
%1 = call i32 @llvm.cttz.i32(i32 %a, i1 true)
ret i32 %1

```

```
}
```

```
define signext i32 @findFirstSet_i32(i32 signext %a) nounwind {  
; RV64I-LABEL: findFirstSet_i32:  
; RV64I:    # %bb.0:  
; RV64I-NEXT:  addi sp, sp, -16  
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill  
; RV64I-NEXT:  sd s0, 0(sp) # 8-byte Folded Spill  
; RV64I-NEXT:  mv s0, a0  
; RV64I-NEXT:  negw a0, a0  
; RV64I-NEXT:  and a0, s0, a0  
; RV64I-NEXT:  lui a1, 30667  
; RV64I-NEXT:  addiw a1, a1, 1329  
; RV64I-NEXT:  call __muldi3  
; RV64I-NEXT:  srliw a0, a0, 27  
; RV64I-NEXT:  lui a1, %hi(LCPI8_0)  
; RV64I-NEXT:  addi a1, a1, %lo(LCPI8_0)  
; RV64I-NEXT:  add a0, a1, a0  
; RV64I-NEXT:  lbu a0, 0(a0)  
; RV64I-NEXT:  snez a1, s0  
; RV64I-NEXT:  
    addi a1, a1, -1  
; RV64I-NEXT:  or a0, a1, a0  
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload  
; RV64I-NEXT:  ld s0, 0(sp) # 8-byte Folded Reload  
; RV64I-NEXT:  addi sp, sp, 16  
; RV64I-NEXT:  ret  
;  
; RV64ZBB-LABEL: findFirstSet_i32:  
; RV64ZBB:    # %bb.0:  
; RV64ZBB-NEXT:  ctw a1, a0  
; RV64ZBB-NEXT:  snez a0, a0  
; RV64ZBB-NEXT:  addiw a0, a0, -1  
; RV64ZBB-NEXT:  or a0, a0, a1  
; RV64ZBB-NEXT:  ret  
%1 = call i32 @llvm.cttz.i32(i32 %a, i1 true)  
%2 = icmp eq i32 %a, 0  
%3 = select i1 %2, i32 -1, i32 %1  
ret i32 %3  
}
```

```
define signext i32 @ffs_i32(i32 signext %a) nounwind {  
; RV64I-LABEL: ffs_i32:  
; RV64I:    # %bb.0:  
; RV64I-NEXT:  addi sp, sp, -16  
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill  
; RV64I-NEXT:  sd s0, 0(sp) # 8-byte Folded Spill  
; RV64I-NEXT:  mv s0, a0
```

```

; RV64I-NEXT:  negw a0, a0
; RV64I-NEXT:  and a0, s0, a0
; RV64I-NEXT:  lui a1, 30667
; RV64I-NEXT:  addiw a1, a1, 1329
; RV64I-NEXT:  call __muldi3
; RV64I-NEXT:
    srlw a0, a0, 27
; RV64I-NEXT:  lui a1, %hi(.LCPI9_0)
; RV64I-NEXT:  addi a1, a1, %lo(.LCPI9_0)
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  lbu a0, 0(a0)
; RV64I-NEXT:  addi a0, a0, 1
; RV64I-NEXT:  seqz a1, s0
; RV64I-NEXT:  addi a1, a1, -1
; RV64I-NEXT:  and a0, a1, a0
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  ld s0, 0(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: ffs_i32:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  ctzw a1, a0
; RV64ZBB-NEXT:  addi a1, a1, 1
; RV64ZBB-NEXT:  seqz a0, a0
; RV64ZBB-NEXT:  addi a0, a0, -1
; RV64ZBB-NEXT:  and a0, a0, a1
; RV64ZBB-NEXT:  zext.h a0, a0
; RV64ZBB-NEXT:  ret
%1 = call i32 @llvm.cttz.i32(i32 %a, i1 true)
%2 = add i32 %1, 1
%3 = icmp eq i32 %a, 0
%4 = select i1 %3, i32 0, i32 %2
ret i32 %4
}

declare i64 @llvm.cttz.i64(i64, i1)

define i64 @cttz_i64(i64
    %a) nounwind {
; RV64I-LABEL: cttz_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  beqz a0, .LBB10_2
; RV64I-NEXT:  # %bb.1: # %cond.false
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill

```

```

; RV64I-NEXT:  neg a1, a0
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  lui a1, %hi(.LCPI10_0)
; RV64I-NEXT:  ld a1, %lo(.LCPI10_0)(a1)
; RV64I-NEXT:  call __muldi3
; RV64I-NEXT:  srli a0, a0, 58
; RV64I-NEXT:  lui a1, %hi(.LCPI10_1)
; RV64I-NEXT:  addi a1, a1, %lo(.LCPI10_1)
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  lbu a0, 0(a0)
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
; RV64I-NEXT: .LBB10_2:
; RV64I-NEXT:  li a0, 64
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: cttz_i64:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  ctz a0, a0
; RV64ZBB-NEXT:  ret
%1 = call i64 @llvm.cttz.i64(i64 %a, i1 false)
ret i64 %1
}

```

```
declare i32 @llvm.ctpop.i32(i32)
```

```

define signext i32 @ctpop_i32(i32
  signext %a) nounwind {
; RV64I-LABEL: ctpop_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  srliw a1, a0, 1
; RV64I-NEXT:  lui a2, 349525
; RV64I-NEXT:  addi a2, a2, 1365
; RV64I-NEXT:  and a1, a1, a2
; RV64I-NEXT:  subw a0, a0, a1
; RV64I-NEXT:  lui a1, 209715
; RV64I-NEXT:  addi a1, a1, 819
; RV64I-NEXT:  and a2, a0, a1
; RV64I-NEXT:  srliw a0, a0, 2
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  add a0, a2, a0
; RV64I-NEXT:  srliw a1, a0, 4
; RV64I-NEXT:  addw a0, a0, a1
; RV64I-NEXT:  lui a1, 61681
; RV64I-NEXT:  addiw a1, a1, -241

```

```

; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: lui a1, 4112
; RV64I-NEXT: addiw a1, a1, 257
; RV64I-NEXT: call __muldi3
; RV64I-NEXT: srliw a0, a0, 24
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
;
; RV64ZBB-LABEL: ctpop_i32:
; RV64ZBB: # %bb.0:
; RV64ZBB-NEXT: cpopw
a0, a0
; RV64ZBB-NEXT: ret
%1 = call i32 @llvm.ctpop.i32(i32 %a)
ret i32 %1
}

```

```

define signext i32 @ctpop_i32_load(ptr %p) nounwind {

```

```

; RV64I-LABEL: ctpop_i32_load:
; RV64I: # %bb.0:
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT: lw a0, 0(a0)
; RV64I-NEXT: srliw a1, a0, 1
; RV64I-NEXT: lui a2, 349525
; RV64I-NEXT: addi a2, a2, 1365
; RV64I-NEXT: and a1, a1, a2
; RV64I-NEXT: subw a0, a0, a1
; RV64I-NEXT: lui a1, 209715
; RV64I-NEXT: addi a1, a1, 819
; RV64I-NEXT: and a2, a0, a1
; RV64I-NEXT: srliw a0, a0, 2
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: add a0, a2, a0
; RV64I-NEXT: srliw a1, a0, 4
; RV64I-NEXT: addw a0, a0, a1
; RV64I-NEXT: lui a1, 61681
; RV64I-NEXT: addiw a1, a1, -241
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: lui a1, 4112
; RV64I-NEXT: addiw a1, a1, 257
; RV64I-NEXT: call __muldi3
; RV64I-NEXT: srliw a0, a0, 24
; RV64I-NEXT: ld ra, 8(sp)
# 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret

```

```

;
; RV64ZBB-LABEL: ctpop_i32_load:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT: lw a0, 0(a0)
; RV64ZBB-NEXT: cpopw a0, a0
; RV64ZBB-NEXT: ret
%a = load i32, ptr %p
%1 = call i32 @llvm.ctpop.i32(i32 %a)
ret i32 %1
}

declare i64 @llvm.ctpop.i64(i64)

define i64 @ctpop_i64(i64 %a) nounwind {
; RV64I-LABEL: ctpop_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT: srli a1, a0, 1
; RV64I-NEXT: lui a2, 349525
; RV64I-NEXT: addiw a2, a2, 1365
; RV64I-NEXT: slli a3, a2, 32
; RV64I-NEXT: add a2, a2, a3
; RV64I-NEXT: and a1, a1, a2
; RV64I-NEXT: sub a0, a0, a1
; RV64I-NEXT: lui a1, 209715
; RV64I-NEXT: addiw a1, a1, 819
; RV64I-NEXT: slli a2, a1, 32
; RV64I-NEXT: add a1, a1, a2
; RV64I-NEXT: and a2, a0, a1
; RV64I-NEXT: srli a0, a0, 2
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: add a0, a2,
a0
; RV64I-NEXT: srli a1, a0, 4
; RV64I-NEXT: add a0, a0, a1
; RV64I-NEXT: lui a1, 61681
; RV64I-NEXT: addiw a1, a1, -241
; RV64I-NEXT: slli a2, a1, 32
; RV64I-NEXT: add a1, a1, a2
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: lui a1, 4112
; RV64I-NEXT: addiw a1, a1, 257
; RV64I-NEXT: slli a2, a1, 32
; RV64I-NEXT: add a1, a1, a2
; RV64I-NEXT: call __muldi3
; RV64I-NEXT: srli a0, a0, 56
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload

```



```

; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: ctpop_i64:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  cpop a0, a0
; RV64ZBB-NEXT:  ret
%1 = call i64 @llvm.ctpop.i64(i64 %a)
ret i64 %1
}

```

```

define signext i32 @sextb_i32(i32 signext %a) nounwind {
; RV64I-LABEL: sextb_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 56
; RV64I-NEXT:  srai a0, a0, 56
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: sextb_i32:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  sext.b a0, a0
; RV64ZBB-NEXT:
    ret
%shl = shl i32 %a, 24
%shr = ashr exact i32 %shl, 24
ret i32 %shr
}

```

```

define i64 @sextb_i64(i64 %a) nounwind {
; RV64I-LABEL: sextb_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 56
; RV64I-NEXT:  srai a0, a0, 56
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: sextb_i64:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  sext.b a0, a0
; RV64ZBB-NEXT:  ret
%shl = shl i64 %a, 56
%shr = ashr exact i64 %shl, 56
ret i64 %shr
}

```

```

define signext i32 @sextb_i32(i32 signext %a) nounwind {
; RV64I-LABEL: sextb_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 48

```

```

; RV64I-NEXT:  srai a0, a0, 48
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: sixth_i32:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  sext.h a0, a0
; RV64ZBB-NEXT:  ret
%shl = shl i32 %a, 16
%shr = ashr exact i32 %shl, 16
ret i32 %shr
}

define i64 @sixth_i64(i64 %a) nounwind {
; RV64I-LABEL: sixth_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 48
; RV64I-NEXT:  srai a0, a0, 48
; RV64I-NEXT:
    ret
;
; RV64ZBB-LABEL: sixth_i64:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  sext.h a0, a0
; RV64ZBB-NEXT:  ret
%shl = shl i64 %a, 48
%shr = ashr exact i64 %shl, 48
ret i64 %shr
}

define signext i32 @min_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: min_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  blt a0, a1, .LBB18_2
; RV64I-NEXT:  # %bb.1:
; RV64I-NEXT:  mv a0, a1
; RV64I-NEXT:  .LBB18_2:
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: min_i32:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  min a0, a0, a1
; RV64ZBB-NEXT:  ret
%cmp = icmp slt i32 %a, %b
%cond = select i1 %cmp, i32 %a, i32 %b
ret i32 %cond
}

define i64 @min_i64(i64 %a, i64 %b) nounwind {

```

```

; RV64I-LABEL: min_i64:
; RV64I:    # %bb.0:
; RV64I-NEXT:  blt a0, a1, .LBB19_2
; RV64I-NEXT: # %bb.1:
; RV64I-NEXT:  mv a0, a1
; RV64I-NEXT: .LBB19_2:
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: min_i64:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT:  min a0, a0, a1
; RV64ZBB-NEXT:  ret
%cmp = icmp
slt i64 %a, %b
%cond = select i1 %cmp, i64 %a, i64 %b
ret i64 %cond
}

define signext i32 @max_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: max_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT:  blt a1, a0, .LBB20_2
; RV64I-NEXT: # %bb.1:
; RV64I-NEXT:  mv a0, a1
; RV64I-NEXT: .LBB20_2:
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: max_i32:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT:  max a0, a0, a1
; RV64ZBB-NEXT:  ret
%cmp = icmp sgt i32 %a, %b
%cond = select i1 %cmp, i32 %a, i32 %b
ret i32 %cond
}

define i64 @max_i64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: max_i64:
; RV64I:    # %bb.0:
; RV64I-NEXT:  blt a1, a0, .LBB21_2
; RV64I-NEXT: # %bb.1:
; RV64I-NEXT:  mv a0, a1
; RV64I-NEXT: .LBB21_2:
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: max_i64:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT:  max a0, a0, a1

```

```
; RV64ZBB-NEXT:  ret
%cmp = icmp sgt i64 %a, %b
%cond = select i1 %cmp, i64 %a, i64 %b
ret i64 %cond
}
```

```
define signext i32 @minu_i32(i32 signext
%a, i32 signext %b) nounwind {
; RV64I-LABEL: minu_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  bltu a0, a1, .LBB22_2
; RV64I-NEXT: # %bb.1:
; RV64I-NEXT:  mv a0, a1
; RV64I-NEXT: .LBB22_2:
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: minu_i32:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT:  minu a0, a0, a1
; RV64ZBB-NEXT:  ret
%cmp = icmp ult i32 %a, %b
%cond = select i1 %cmp, i32 %a, i32 %b
ret i32 %cond
}
```

```
define i64 @minu_i64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: minu_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  bltu a0, a1, .LBB23_2
; RV64I-NEXT: # %bb.1:
; RV64I-NEXT:  mv a0, a1
; RV64I-NEXT: .LBB23_2:
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: minu_i64:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT:  minu a0, a0, a1
; RV64ZBB-NEXT:  ret
%cmp = icmp ult i64 %a, %b
%cond = select i1 %cmp, i64 %a, i64 %b
ret i64 %cond
}
```

```
define signext i32 @maxu_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: maxu_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  bltu a1,
```

```

a0, .LBB24_2
; RV64I-NEXT: # %bb.1:
; RV64I-NEXT: mv a0, a1
; RV64I-NEXT: .LBB24_2:
; RV64I-NEXT: ret
;
; RV64ZBB-LABEL: maxu_i32:
; RV64ZBB: # %bb.0:
; RV64ZBB-NEXT: maxu a0, a0, a1
; RV64ZBB-NEXT: ret
%cmp = icmp ugt i32 %a, %b
%cond = select i1 %cmp, i32 %a, i32 %b
ret i32 %cond
}

define i64 @maxu_i64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: maxu_i64:
; RV64I: # %bb.0:
; RV64I-NEXT: bltu a1, a0, .LBB25_2
; RV64I-NEXT: # %bb.1:
; RV64I-NEXT: mv a0, a1
; RV64I-NEXT: .LBB25_2:
; RV64I-NEXT: ret
;
; RV64ZBB-LABEL: maxu_i64:
; RV64ZBB: # %bb.0:
; RV64ZBB-NEXT: maxu a0, a0, a1
; RV64ZBB-NEXT: ret
%cmp = icmp ugt i64 %a, %b
%cond = select i1 %cmp, i64 %a, i64 %b
ret i64 %cond
}

declare i32 @llvm.abs.i32(i32, i1 immarg)

define i32 @abs_i32(i32 %x) {
; RV64I-LABEL: abs_i32:
; RV64I: # %bb.0:
; RV64I-NEXT: sraiw a1, a0, 31
; RV64I-NEXT: xor a0, a0, a1
; RV64I-NEXT: subw a0, a0, a1
; RV64I-NEXT: ret
;
; RV64ZBB-LABEL:
abs_i32:
; RV64ZBB: # %bb.0:
; RV64ZBB-NEXT: sraiw a1, a0, 31
; RV64ZBB-NEXT: xor a0, a0, a1

```

```
; RV64ZBB-NEXT:  subw a0, a0, a1
; RV64ZBB-NEXT:  ret
%abs = tail call i32 @llvm.abs.i32(i32 %x, i1 true)
ret i32 %abs
}
```

```
define signext i32 @abs_i32_sext(i32 signext %x) {
; RV64I-LABEL: abs_i32_sext:
; RV64I:      # %bb.0:
; RV64I-NEXT:  sraiw a1, a0, 31
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  subw a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: abs_i32_sext:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT:  sraiw a1, a0, 31
; RV64ZBB-NEXT:  xor a0, a0, a1
; RV64ZBB-NEXT:  subw a0, a0, a1
; RV64ZBB-NEXT:  ret
%abs = tail call i32 @llvm.abs.i32(i32 %x, i1 true)
ret i32 %abs
}
```

```
declare i64 @llvm.abs.i64(i64, i1 immarg)
```

```
define i64 @abs_i64(i64 %x) {
; RV64I-LABEL: abs_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srai a1, a0, 63
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  sub a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: abs_i64:
; RV64ZBB:
;   # %bb.0:
; RV64ZBB-NEXT:  neg a1, a0
; RV64ZBB-NEXT:  max a0, a0, a1
; RV64ZBB-NEXT:  ret
%abs = tail call i64 @llvm.abs.i64(i64 %x, i1 true)
ret i64 %abs
}
```

```
define i32 @zexth_i32(i32 %a) nounwind {
; RV64I-LABEL: zexth_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 48
}
```

```

; RV64I-NEXT: srli a0, a0, 48
; RV64I-NEXT: ret
;
; RV64ZBB-LABEL: zexth_i32:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT: slli a0, a0, 48
; RV64ZBB-NEXT: srli a0, a0, 48
; RV64ZBB-NEXT: ret
%and = and i32 %a, 65535
ret i32 %and
}

define i64 @zexth_i64(i64 %a) nounwind {
; RV64I-LABEL: zexth_i64:
; RV64I:    # %bb.0:
; RV64I-NEXT: slli a0, a0, 48
; RV64I-NEXT: srli a0, a0, 48
; RV64I-NEXT: ret
;
; RV64ZBB-LABEL: zexth_i64:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT: zext.h a0, a0
; RV64ZBB-NEXT: ret
%and = and i64 %a, 65535
ret i64 %and
}

declare i32 @llvm.bswap.i32(i32)

define signext i32 @bswap_i32(i32 signext %a) nounwind {
; RV64I-LABEL: bswap_i32:
;
; RV64I:    # %bb.0:
; RV64I-NEXT: srliw a1, a0, 8
; RV64I-NEXT: lui a2, 16
; RV64I-NEXT: addiw a2, a2, -256
; RV64I-NEXT: and a1, a1, a2
; RV64I-NEXT: srliw a3, a0, 24
; RV64I-NEXT: or a1, a1, a3
; RV64I-NEXT: and a2, a0, a2
; RV64I-NEXT: slliw a2, a2, 8
; RV64I-NEXT: slliw a0, a0, 24
; RV64I-NEXT: or a0, a0, a2
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: ret
;
; RV64ZBB-LABEL: bswap_i32:
; RV64ZBB:    # %bb.0:

```

```

; RV64ZBB-NEXT: rev8 a0, a0
; RV64ZBB-NEXT: srli a0, a0, 32
; RV64ZBB-NEXT: ret
%1 = tail call i32 @llvm.bswap.i32(i32 %a)
ret i32 %1
}

```

; Similar to bswap_i32 but the result is not sign extended.

```

define void @bswap_i32_nosext(i32 signext %a, ptr %x) nounwind {
; RV64I-LABEL: bswap_i32_nosext:
; RV64I:      # %bb.0:
; RV64I-NEXT: srliw a2, a0, 8
; RV64I-NEXT: lui a3, 16
; RV64I-NEXT: addi a3, a3, -256
; RV64I-NEXT: and a2, a2, a3
; RV64I-NEXT: srliw a4, a0, 24
; RV64I-NEXT: or a2, a2, a4
; RV64I-NEXT:
    and a3, a0, a3
; RV64I-NEXT: slli a3, a3, 8
; RV64I-NEXT: slli a0, a0, 24
; RV64I-NEXT: or a0, a0, a3
; RV64I-NEXT: or a0, a0, a2
; RV64I-NEXT: sw a0, 0(a1)
; RV64I-NEXT: ret
;
; RV64ZBB-LABEL: bswap_i32_nosext:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT: rev8 a0, a0
; RV64ZBB-NEXT: srli a0, a0, 32
; RV64ZBB-NEXT: sw a0, 0(a1)
; RV64ZBB-NEXT: ret
%1 = tail call i32 @llvm.bswap.i32(i32 %a)
store i32 %1, ptr %x
ret void
}

```

```

declare i64 @llvm.bswap.i64(i64)

```

```

define i64 @bswap_i64(i64 %a) {
; RV64I-LABEL: bswap_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT: srli a1, a0, 40
; RV64I-NEXT: lui a2, 16
; RV64I-NEXT: addiw a2, a2, -256
; RV64I-NEXT: and a1, a1, a2
; RV64I-NEXT: srli a3, a0, 56
; RV64I-NEXT: or a1, a1, a3

```



```

; RV64I-NEXT: srli a3, a0, 24
; RV64I-NEXT: lui a4, 4080
; RV64I-NEXT: and a3, a3, a4
; RV64I-NEXT: srli a5, a0, 8
; RV64I-NEXT: srliw a5, a5, 24
; RV64I-NEXT: slli a5, a5, 24
; RV64I-NEXT: or a3, a5, a3
; RV64I-NEXT:
    or a1, a3, a1
; RV64I-NEXT: and a4, a0, a4
; RV64I-NEXT: slli a4, a4, 24
; RV64I-NEXT: srliw a3, a0, 24
; RV64I-NEXT: slli a3, a3, 32
; RV64I-NEXT: or a3, a4, a3
; RV64I-NEXT: and a2, a0, a2
; RV64I-NEXT: slli a2, a2, 40
; RV64I-NEXT: slli a0, a0, 56
; RV64I-NEXT: or a0, a0, a2
; RV64I-NEXT: or a0, a0, a3
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: ret
;
; RV64ZBB-LABEL: bswap_i64:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT: rev8 a0, a0
; RV64ZBB-NEXT: ret
%1 = call i64 @llvm.bswap.i64(i64 %a)
ret i64 %1
}
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefix=RV64I
; RUN: llc -mtriple=riscv64 -mattr=+zbbk -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefix=RV64ZBKB

define signext i32 @pack_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: pack_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT: slli a0, a0, 48
; RV64I-NEXT: srli a0, a0, 48
; RV64I-NEXT: slliw a1, a1, 16
; RV64I-NEXT: or a0, a1, a0
; RV64I-NEXT: ret
;
; RV64ZBKB-LABEL: pack_i32:
; RV64ZBKB:    # %bb.0:
; RV64ZBKB-NEXT: packw a0, a0, a1
; RV64ZBKB-NEXT: ret

```

```

%shl = and i32 %a, 65535
%shl1 = shl i32 %b, 16
%or = or i32 %shl1, %shl
ret i32 %or
}

define signext i32 @pack_i32_2(i16 zeroext %a, i16 zeroext %b) nounwind {
; RV64I-LABEL: pack_i32_2:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slliw
a1, a1, 16
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBKB-LABEL: pack_i32_2:
; RV64ZBKB:    # %bb.0:
; RV64ZBKB-NEXT:  packw a0, a0, a1
; RV64ZBKB-NEXT:  ret
%zexta = zext i16 %a to i32
%zextb = zext i16 %b to i32
%shl1 = shl i32 %zextb, 16
%or = or i32 %shl1, %zexta
ret i32 %or
}

; Test case where we don't have a sign_extend_inreg after the or.
define signext i32 @pack_i32_3(i16 zeroext %0, i16 zeroext %1, i32 signext %2) {
; RV64I-LABEL: pack_i32_3:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 16
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  addw a0, a0, a2
; RV64I-NEXT:  ret
;
; RV64ZBKB-LABEL: pack_i32_3:
; RV64ZBKB:    # %bb.0:
; RV64ZBKB-NEXT:  packw a0, a1, a0
; RV64ZBKB-NEXT:  addw a0, a0, a2
; RV64ZBKB-NEXT:  ret
%4 = zext i16 %0 to i32
%5 = shl nuw i32 %4, 16
%6 = zext i16 %1 to i32
%7 = or i32 %5, %6
%8 = add i32 %7, %2
ret i32 %8
}

define i64 @pack_i64(i64 %a, i64 %b) nounwind {

```

```

; RV64I-LABEL: pack_i64:
;
RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBKB-LABEL: pack_i64:
; RV64ZBKB:    # %bb.0:
; RV64ZBKB-NEXT:  pack a0, a0, a1
; RV64ZBKB-NEXT:  ret
%shl = and i64 %a, 4294967295
%shl1 = shl i64 %b, 32
%or = or i64 %shl1, %shl
ret i64 %or
}

define i64 @pack_i64_2(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: pack_i64_2:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBKB-LABEL: pack_i64_2:
; RV64ZBKB:    # %bb.0:
; RV64ZBKB-NEXT:  pack a0, a0, a1
; RV64ZBKB-NEXT:  ret
%zexta = zext i32 %a to i64
%zextb = zext i32 %b to i64
%shl1 = shl i64 %zextb, 32
%or = or i64 %shl1, %zexta
ret i64 %or
}

define i64 @pack_i64_3(ptr %0, ptr %1) {
; RV64I-LABEL: pack_i64_3:
; RV64I:    #
%bb.0:
; RV64I-NEXT:  lw a0, 0(a0)
; RV64I-NEXT:  lwu a1, 0(a1)
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  ret

```

```

;
; RV64ZBKB-LABEL: pack_i64_3:
; RV64ZBKB:    # %bb.0:
; RV64ZBKB-NEXT:  lw a0, 0(a0)
; RV64ZBKB-NEXT:  lwu a1, 0(a1)
; RV64ZBKB-NEXT:  pack a0, a1, a0
; RV64ZBKB-NEXT:  ret
%3 = load i32, ptr %0, align 4
%4 = zext i32 %3 to i64
%5 = shl i64 %4, 32
%6 = load i32, ptr %1, align 4
%7 = zext i32 %6 to i64
%8 = or i64 %5, %7
ret i64 %8
}

define signext i32 @packh_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: packh_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT:  andi a0, a0, 255
; RV64I-NEXT:  slli a1, a1, 56
; RV64I-NEXT:  srli a1, a1, 48
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBKB-LABEL: packh_i32:
; RV64ZBKB:    # %bb.0:
; RV64ZBKB-NEXT:  packh a0, a0, a1
; RV64ZBKB-NEXT:  ret
%and = and i32 %a, 255
%and1 = shl i32 %b, 8
%shl = and i32 %and1, 65280
%or = or
i32 %shl, %and
ret i32 %or
}

define i32 @packh_i32_2(i32 %a, i32 %b) nounwind {
; RV64I-LABEL: packh_i32_2:
; RV64I:    # %bb.0:
; RV64I-NEXT:  andi a0, a0, 255
; RV64I-NEXT:  andi a1, a1, 255
; RV64I-NEXT:  slliw a1, a1, 8
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBKB-LABEL: packh_i32_2:
; RV64ZBKB:    # %bb.0:

```

```
; RV64ZBKB-NEXT: packh a0, a0, a1
; RV64ZBKB-NEXT: ret
%and = and i32 %a, 255
%and1 = and i32 %b, 255
%shl = shl i32 %and1, 8
%or = or i32 %shl, %and
ret i32 %or
}
```

```
define i64 @packh_i64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: packh_i64:
; RV64I:    # %bb.0:
; RV64I-NEXT: andi a0, a0, 255
; RV64I-NEXT: slli a1, a1, 56
; RV64I-NEXT: srli a1, a1, 48
; RV64I-NEXT: or a0, a1, a0
; RV64I-NEXT: ret
;
; RV64ZBKB-LABEL: packh_i64:
; RV64ZBKB:    # %bb.0:
; RV64ZBKB-NEXT: packh a0, a0, a1
; RV64ZBKB-NEXT: ret
%and = and i64 %a, 255
%and1 = shl i64 %b, 8
%shl = and i64 %and1, 65280
%or = or i64 %shl,
%and
ret i64 %or
}
```

```
define i64 @packh_i64_2(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: packh_i64_2:
; RV64I:    # %bb.0:
; RV64I-NEXT: andi a0, a0, 255
; RV64I-NEXT: andi a1, a1, 255
; RV64I-NEXT: slli a1, a1, 8
; RV64I-NEXT: or a0, a1, a0
; RV64I-NEXT: ret
;
; RV64ZBKB-LABEL: packh_i64_2:
; RV64ZBKB:    # %bb.0:
; RV64ZBKB-NEXT: packh a0, a0, a1
; RV64ZBKB-NEXT: ret
%and = and i64 %a, 255
%and1 = and i64 %b, 255
%shl = shl i64 %and1, 8
%or = or i64 %shl, %and
ret i64 %or
}
```

```
}
```

```
define zeroext i16 @packh_i16(i8 zeroext %a, i8 zeroext %b) nounwind {  
; RV64I-LABEL: packh_i16:  
; RV64I:      # %bb.0:  
; RV64I-NEXT: slliw a1, a1, 8  
; RV64I-NEXT: or a0, a1, a0  
; RV64I-NEXT: ret  
;  
; RV64ZBKB-LABEL: packh_i16:  
; RV64ZBKB:   # %bb.0:  
; RV64ZBKB-NEXT: packh a0, a0, a1  
; RV64ZBKB-NEXT: ret  
%zext = zext i8 %a to i16  
%zext1 = zext i8 %b to i16  
%shl = shl i16 %zext1, 8  
%or = or i16 %shl, %zext  
ret i16 %or  
}
```

```
define zeroext i16 @packh_i16_2(i8  
zeroext %0, i8 zeroext %1, i8 zeroext %2) {  
; RV64I-LABEL: packh_i16_2:  
; RV64I:      # %bb.0:  
; RV64I-NEXT: add a0, a1, a0  
; RV64I-NEXT: slli a0, a0, 8  
; RV64I-NEXT: or a0, a0, a2  
; RV64I-NEXT: slli a0, a0, 48  
; RV64I-NEXT: srli a0, a0, 48  
; RV64I-NEXT: ret  
;  
; RV64ZBKB-LABEL: packh_i16_2:  
; RV64ZBKB:   # %bb.0:  
; RV64ZBKB-NEXT: add a0, a1, a0  
; RV64ZBKB-NEXT: packh a0, a2, a0  
; RV64ZBKB-NEXT: ret  
%4 = add i8 %1, %0  
%5 = zext i8 %4 to i16  
%6 = shl i16 %5, 8  
%7 = zext i8 %2 to i16  
%8 = or i16 %6, %7  
ret i16 %8  
}
```

```
define i64 @pack_i64_allWUsers(i32 signext %0, i32 signext %1, i32 signext %2) {  
; RV64I-LABEL: pack_i64_allWUsers:  
; RV64I:      # %bb.0:  
; RV64I-NEXT: add a0, a1, a0
```

```

; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  slli a2, a2, 32
; RV64I-NEXT:  srli a2, a2, 32
; RV64I-NEXT:  or a0, a0, a2
; RV64I-NEXT:  ret
;
; RV64ZBKB-LABEL: pack_i64_allWUsers:
; RV64ZBKB:      # %bb.0:
; RV64ZBKB-NEXT:  add a0, a1, a0
; RV64ZBKB-NEXT:
    pack a0, a2, a0
; RV64ZBKB-NEXT:  ret
%4 = add i32 %1, %0
%5 = zext i32 %4 to i64
%6 = shl i64 %5, 32
%7 = zext i32 %2 to i64
%8 = or i64 %6, %7
ret i64 %8
}

define signext i32 @pack_i32_allWUsers(i16 zeroext %0, i16 zeroext %1, i16 zeroext %2) {
; RV64I-LABEL: pack_i32_allWUsers:
; RV64I:      # %bb.0:
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  slliw a0, a0, 16
; RV64I-NEXT:  or a0, a0, a2
; RV64I-NEXT:  ret
;
; RV64ZBKB-LABEL: pack_i32_allWUsers:
; RV64ZBKB:      # %bb.0:
; RV64ZBKB-NEXT:  add a0, a1, a0
; RV64ZBKB-NEXT:  packw a0, a2, a0
; RV64ZBKB-NEXT:  ret
%4 = add i16 %1, %0
%5 = zext i16 %4 to i32
%6 = shl i32 %5, 16
%7 = zext i16 %2 to i32
%8 = or i32 %6, %7
ret i32 %8
}

define i64 @pack_i64_imm() {
; RV64I-LABEL: pack_i64_imm:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a0, 65793
; RV64I-NEXT:  addiw a0, a0, 16
; RV64I-NEXT:  slli a1, a0, 32
; RV64I-NEXT:  add a0, a0, a1

```

```

; RV64I-NEXT:  ret
;
; RV64ZBKB-LABEL:
pack_i64_imm:
; RV64ZBKB:    # %bb.0:
; RV64ZBKB-NEXT:  lui a0, 65793
; RV64ZBKB-NEXT:  addi a0, a0, 16
; RV64ZBKB-NEXT:  pack a0, a0, a0
; RV64ZBKB-NEXT:  ret
ret i64 1157442765409226768 ; 0x0101010101010101
}

; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -riscv-disable-using-constant-pool-for-large-ints -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefixes=RV64I,RV64I-NOPOOL
; RUN: llc -mtriple=riscv64 -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefixes=RV64I,RV64I-POOL
; RUN: llc -mtriple=riscv64 -riscv-disable-using-constant-pool-for-large-ints -mattr=+zba \
; RUN: -riscv-experimental-rv64-legal-i32 -verify-machineinstrs < %s | FileCheck %s -check-prefix=RV64IZBA
; RUN: llc -mtriple=riscv64 -riscv-disable-using-constant-pool-for-large-ints -mattr=+zbb \
; RUN: -riscv-experimental-rv64-legal-i32 -verify-machineinstrs < %s | FileCheck %s -check-prefix=RV64IZBB
; RUN: llc -mtriple=riscv64 -riscv-disable-using-constant-pool-for-large-ints -mattr=+zbs \
; RUN: -riscv-experimental-rv64-legal-i32 -verify-machineinstrs < %s | FileCheck
% s -check-prefix=RV64IZBS
; RUN: llc -mtriple=riscv64 -riscv-disable-using-constant-pool-for-large-ints -mattr=+xtheadbb \
; RUN: -riscv-experimental-rv64-legal-i32 -verify-machineinstrs < %s | FileCheck %s -check-
prefix=RV64IXTHEADBB

; Materializing constants

; TODO: It would be preferable if anyext constant returns were sign rather
; than zero extended. See PR39092. For now, mark returns as explicitly signext
; (this matches what Clang would generate for equivalent C/C++ anyway).

define signext i32 @zero() nounwind {
; RV64I-LABEL: zero:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a0, 0
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: zero:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  li a0, 0
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: zero:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  li a0, 0
; RV64IZBB-NEXT:  ret

```



```

;
; RV64IZBS-LABEL: zero:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  li a0, 0
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: zero:
; RV64IXTHEADBB:    # %bb.0:
;
; RV64IXTHEADBB-NEXT:  li a0, 0
; RV64IXTHEADBB-NEXT:  ret
ret i32 0
}

```

```

define signext i32 @pos_small() nounwind {
; RV64I-LABEL: pos_small:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a0, 2047
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: pos_small:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  li a0, 2047
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: pos_small:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  li a0, 2047
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: pos_small:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  li a0, 2047
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: pos_small:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  li a0, 2047
; RV64IXTHEADBB-NEXT:  ret
ret i32 2047
}

```

```

define signext i32 @neg_small() nounwind {
; RV64I-LABEL: neg_small:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a0, -2048
; RV64I-NEXT:  ret
;

```

```

; RV64IZBA-LABEL: neg_small:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  li a0, -2048
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL:
neg_small:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  li a0, -2048
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: neg_small:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  li a0, -2048
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: neg_small:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  li a0, -2048
; RV64IXTHEADBB-NEXT:  ret
ret i32 -2048
}

```

```

define signext i32 @pos_i32() nounwind {
; RV64I-LABEL: pos_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 423811
; RV64I-NEXT:  addiw a0, a0, -1297
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: pos_i32:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 423811
; RV64IZBA-NEXT:  addiw a0, a0, -1297
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: pos_i32:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 423811
; RV64IZBB-NEXT:  addiw a0, a0, -1297
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: pos_i32:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 423811
; RV64IZBS-NEXT:  addiw a0, a0, -1297
; RV64IZBS-NEXT:

```

```

    ret
;
; RV64IXTHEADBB-LABEL: pos_i32:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 423811
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -1297
; RV64IXTHEADBB-NEXT:  ret
ret i32 1735928559
}

```

```

define signext i32 @neg_i32() nounwind {
; RV64I-LABEL: neg_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 912092
; RV64I-NEXT:  addiw a0, a0, -273
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: neg_i32:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 912092
; RV64IZBA-NEXT:  addiw a0, a0, -273
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: neg_i32:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 912092
; RV64IZBB-NEXT:  addiw a0, a0, -273
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: neg_i32:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 912092
; RV64IZBS-NEXT:  addiw a0, a0, -273
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: neg_i32:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 912092
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -273
;
RV64IXTHEADBB-NEXT:  ret
ret i32 -559038737
}

```

```

define signext i32 @pos_i32_hi20_only() nounwind {
; RV64I-LABEL: pos_i32_hi20_only:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 16

```

```

; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: pos_i32_hi20_only:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 16
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: pos_i32_hi20_only:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 16
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: pos_i32_hi20_only:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 16
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: pos_i32_hi20_only:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 16
; RV64IXTHEADBB-NEXT:  ret
ret i32 65536 ; 0x10000
}

```

```

define signext i32 @neg_i32_hi20_only() nounwind {
; RV64I-LABEL: neg_i32_hi20_only:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 1048560
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: neg_i32_hi20_only:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0,
1048560
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: neg_i32_hi20_only:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 1048560
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: neg_i32_hi20_only:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 1048560
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: neg_i32_hi20_only:
; RV64IXTHEADBB:  # %bb.0:

```

```
; RV64IXTHEADBB-NEXT: lui a0, 1048560
; RV64IXTHEADBB-NEXT: ret
ret i32 -65536 ; -0x10000
}
```

; This can be materialized with ADDI+SLLI, improving compressibility.

```
define signext i32 @imm_left_shifted_addi() nounwind {
; RV64I-LABEL: imm_left_shifted_addi:
; RV64I:    # %bb.0:
; RV64I-NEXT: lui a0, 32
; RV64I-NEXT: addiw a0, a0, -64
; RV64I-NEXT: ret
;
; RV64IZBA-LABEL: imm_left_shifted_addi:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT: lui a0, 32
; RV64IZBA-NEXT: addiw a0, a0, -64
; RV64IZBA-NEXT: ret
;
; RV64IZBB-LABEL: imm_left_shifted_addi:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT: lui a0, 32
;
; RV64IZBB-NEXT: addiw a0, a0, -64
; RV64IZBB-NEXT: ret
;
; RV64IZBS-LABEL: imm_left_shifted_addi:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT: lui a0, 32
; RV64IZBS-NEXT: addiw a0, a0, -64
; RV64IZBS-NEXT: ret
;
; RV64IXTHEADBB-LABEL: imm_left_shifted_addi:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT: lui a0, 32
; RV64IXTHEADBB-NEXT: addiw a0, a0, -64
; RV64IXTHEADBB-NEXT: ret
ret i32 131008 ; 0x1FFC0
}
```

; This can be materialized with ADDI+SRLI, improving compressibility.

```
define signext i32 @imm_right_shifted_addi() nounwind {
; RV64I-LABEL: imm_right_shifted_addi:
; RV64I:    # %bb.0:
; RV64I-NEXT: lui a0, 524288
; RV64I-NEXT: addiw a0, a0, -1
```

```

; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_right_shifted_addi:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 524288
; RV64IZBA-NEXT:  addiw a0, a0, -1
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_right_shifted_addi:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 524288
; RV64IZBB-NEXT:
;               addiw a0, a0, -1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_right_shifted_addi:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 524288
; RV64IZBS-NEXT:  addiw a0, a0, -1
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_right_shifted_addi:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 524288
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -1
; RV64IXTHEADBB-NEXT:  ret
;               ret i32 2147483647 ; 0x7FFFFFFF
}

```

; This can be materialized with LUI+SRLI, improving compressibility.

```

define signext i32 @imm_right_shifted_lui() nounwind {
; RV64I-LABEL: imm_right_shifted_lui:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 56
; RV64I-NEXT:  addiw a0, a0, 580
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_right_shifted_lui:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 56
; RV64IZBA-NEXT:  addiw a0, a0, 580
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_right_shifted_lui:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 56
; RV64IZBB-NEXT:

```

```

    addiw a0, a0, 580
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_right_shifted_lui:
; RV64IZBS:      # %bb.0:
; RV64IZBS-NEXT:  lui a0, 56
; RV64IZBS-NEXT:  addiw a0, a0, 580
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_right_shifted_lui:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 56
; RV64IXTHEADBB-NEXT:  addiw a0, a0, 580
; RV64IXTHEADBB-NEXT:  ret
ret i32 229956 ; 0x38244
}

```

```

define i64 @imm64_1() nounwind {
; RV64I-LABEL: imm64_1:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a0, 1
; RV64I-NEXT:  slli a0, a0, 31
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm64_1:
; RV64IZBA:      # %bb.0:
; RV64IZBA-NEXT:  li a0, 1
; RV64IZBA-NEXT:  slli a0, a0, 31
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm64_1:
; RV64IZBB:      # %bb.0:
; RV64IZBB-NEXT:  li a0, 1
; RV64IZBB-NEXT:  slli a0, a0, 31
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm64_1:
; RV64IZBS:      # %bb.0:
; RV64IZBS-NEXT:  bseti a0, zero, 31
; RV64IZBS-NEXT:  ret
;
;
; RV64IXTHEADBB-LABEL: imm64_1:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  li a0, 1
; RV64IXTHEADBB-NEXT:  slli a0, a0, 31
; RV64IXTHEADBB-NEXT:  ret
ret i64 2147483648 ; 0x8000_0000
}

```

```
}
```

```
define i64 @imm64_2() nounwind {  
; RV64I-LABEL: imm64_2:  
; RV64I:    # %bb.0:  
; RV64I-NEXT:  li a0, -1  
; RV64I-NEXT:  srli a0, a0, 32  
; RV64I-NEXT:  ret  
;  
; RV64IZBA-LABEL: imm64_2:  
; RV64IZBA:    # %bb.0:  
; RV64IZBA-NEXT:  li a0, -1  
; RV64IZBA-NEXT:  srli a0, a0, 32  
; RV64IZBA-NEXT:  ret  
;  
; RV64IZBB-LABEL: imm64_2:  
; RV64IZBB:    # %bb.0:  
; RV64IZBB-NEXT:  li a0, -1  
; RV64IZBB-NEXT:  srli a0, a0, 32  
; RV64IZBB-NEXT:  ret  
;  
; RV64IZBS-LABEL: imm64_2:  
; RV64IZBS:    # %bb.0:  
; RV64IZBS-NEXT:  li a0, -1  
; RV64IZBS-NEXT:  srli a0, a0, 32  
; RV64IZBS-NEXT:  ret  
;  
; RV64IXTHEADBB-LABEL: imm64_2:  
; RV64IXTHEADBB:    # %bb.0:  
; RV64IXTHEADBB-NEXT:  li a0, -1  
; RV64IXTHEADBB-NEXT:  srli a0, a0, 32  
; RV64IXTHEADBB-NEXT:  ret  
ret i64 4294967295 ;  
0xFFFF_FFFF  
}
```

```
define i64 @imm64_3() nounwind {  
; RV64I-LABEL: imm64_3:  
; RV64I:    # %bb.0:  
; RV64I-NEXT:  li a0, 1  
; RV64I-NEXT:  slli a0, a0, 32  
; RV64I-NEXT:  ret  
;  
; RV64IZBA-LABEL: imm64_3:  
; RV64IZBA:    # %bb.0:  
; RV64IZBA-NEXT:  li a0, 1  
; RV64IZBA-NEXT:  slli a0, a0, 32  
; RV64IZBA-NEXT:  ret
```



```

;
; RV64IZBB-LABEL: imm64_3:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  li a0, 1
; RV64IZBB-NEXT:  slli a0, a0, 32
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm64_3:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  bseti a0, zero, 32
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm64_3:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  li a0, 1
; RV64IXTHEADBB-NEXT:  slli a0, a0, 32
; RV64IXTHEADBB-NEXT:  ret
ret i64 4294967296 ; 0x1_0000_0000
}

```

```

define i64 @imm64_4() nounwind {
; RV64I-LABEL: imm64_4:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a0, -1
; RV64I-NEXT:  slli a0, a0, 63
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm64_4:
; RV64IZBA:
;   # %bb.0:
; RV64IZBA-NEXT:  li a0, -1
; RV64IZBA-NEXT:  slli a0, a0, 63
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm64_4:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  li a0, -1
; RV64IZBB-NEXT:  slli a0, a0, 63
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm64_4:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  bseti a0, zero, 63
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm64_4:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  li a0, -1

```

```
; RV64IXTHEADBB-NEXT:  slli a0, a0, 63
; RV64IXTHEADBB-NEXT:  ret
ret i64 9223372036854775808 ; 0x8000_0000_0000_0000
}
```

```
define i64 @imm64_5() nounwind {
; RV64I-LABEL: imm64_5:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a0, -1
; RV64I-NEXT:  slli a0, a0, 63
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm64_5:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  li a0, -1
; RV64IZBA-NEXT:  slli a0, a0, 63
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm64_5:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  li a0, -1
; RV64IZBB-NEXT:
;               slli a0, a0, 63
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm64_5:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  bseti a0, zero, 63
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm64_5:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  li a0, -1
; RV64IXTHEADBB-NEXT:  slli a0, a0, 63
; RV64IXTHEADBB-NEXT:  ret
ret i64 -9223372036854775808 ; 0x8000_0000_0000_0000
}
```

```
define i64 @imm64_6() nounwind {
; RV64I-LABEL: imm64_6:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a0, 9321
; RV64I-NEXT:  addi a0, a0, -1329
; RV64I-NEXT:  slli a0, a0, 35
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm64_6:
; RV64IZBA:    # %bb.0:
```

```

; RV64IZBA-NEXT: lui a0, 9321
; RV64IZBA-NEXT: addi a0, a0, -1329
; RV64IZBA-NEXT: slli a0, a0, 35
; RV64IZBA-NEXT: ret
;
; RV64IZBB-LABEL: imm64_6:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT: lui a0, 9321
; RV64IZBB-NEXT: addi a0, a0, -1329
; RV64IZBB-NEXT: slli a0, a0, 35
; RV64IZBB-NEXT: ret
;
; RV64IZBS-LABEL: imm64_6:
;
RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT: lui a0, 9321
; RV64IZBS-NEXT: addi a0, a0, -1329
; RV64IZBS-NEXT: slli a0, a0, 35
; RV64IZBS-NEXT: ret
;
; RV64IXTHEADBB-LABEL: imm64_6:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT: lui a0, 9321
; RV64IXTHEADBB-NEXT: addi a0, a0, -1329
; RV64IXTHEADBB-NEXT: slli a0, a0, 35
; RV64IXTHEADBB-NEXT: ret
ret i64 1311768464867721216 ; 0x1234_5678_0000_0000
}

```

```

define i64 @imm64_7() nounwind {
; RV64I-LABEL: imm64_7:
; RV64I:    # %bb.0:
; RV64I-NEXT: li a0, 7
; RV64I-NEXT: slli a0, a0, 36
; RV64I-NEXT: addi a0, a0, 11
; RV64I-NEXT: slli a0, a0, 24
; RV64I-NEXT: addi a0, a0, 15
; RV64I-NEXT: ret
;
; RV64IZBA-LABEL: imm64_7:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT: li a0, 7
; RV64IZBA-NEXT: slli a0, a0, 36
; RV64IZBA-NEXT: addi a0, a0, 11
; RV64IZBA-NEXT: slli a0, a0, 24
; RV64IZBA-NEXT: addi a0, a0, 15
; RV64IZBA-NEXT: ret
;

```

```

; RV64IZBB-LABEL: imm64_7:
; RV64IZBB:    #
%bb.0:
; RV64IZBB-NEXT:  li a0, 7
; RV64IZBB-NEXT:  slli a0, a0, 36
; RV64IZBB-NEXT:  addi a0, a0, 11
; RV64IZBB-NEXT:  slli a0, a0, 24
; RV64IZBB-NEXT:  addi a0, a0, 15
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm64_7:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  li a0, 7
; RV64IZBS-NEXT:  slli a0, a0, 36
; RV64IZBS-NEXT:  addi a0, a0, 11
; RV64IZBS-NEXT:  slli a0, a0, 24
; RV64IZBS-NEXT:  addi a0, a0, 15
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm64_7:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  li a0, 7
; RV64IXTHEADBB-NEXT:  slli a0, a0, 36
; RV64IXTHEADBB-NEXT:  addi a0, a0, 11
; RV64IXTHEADBB-NEXT:  slli a0, a0, 24
; RV64IXTHEADBB-NEXT:  addi a0, a0, 15
; RV64IXTHEADBB-NEXT:  ret
ret i64 8070450532432478223 ; 0x7000_0000_0B00_000F
}

```

; TODO: it can be preferable to put constants that are expensive to materialise
into the constant pool, especially for -Os.

```

define i64 @imm64_8() nounwind {
; RV64-NOPOOL-LABEL: imm64_8:
; RV64-NOPOOL:
    # %bb.0:
; RV64-NOPOOL-NEXT:  lui a0, 583
; RV64-NOPOOL-NEXT:  addiw a0, a0, -1875
; RV64-NOPOOL-NEXT:  slli a0, a0, 14
; RV64-NOPOOL-NEXT:  addi a0, a0, -947
; RV64-NOPOOL-NEXT:  slli a0, a0, 12
; RV64-NOPOOL-NEXT:  addi a0, a0, 1511
; RV64-NOPOOL-NEXT:  slli a0, a0, 13
; RV64-NOPOOL-NEXT:  addi a0, a0, -272
; RV64-NOPOOL-NEXT:  ret
;
; RV64I-POOL-LABEL: imm64_8:
; RV64I-POOL:    # %bb.0:

```

```

; RV64I-POOL-NEXT:  lui a0, %hi(.LCPI17_0)
; RV64I-POOL-NEXT:  ld a0, %lo(.LCPI17_0)(a0)
; RV64I-POOL-NEXT:  ret
;
; RV64IZBA-LABEL: imm64_8:
; RV64IZBA:        # %bb.0:
; RV64IZBA-NEXT:   lui a0, 596523
; RV64IZBA-NEXT:   addi a0, a0, 965
; RV64IZBA-NEXT:   slli.uw a0, a0, 13
; RV64IZBA-NEXT:   addi a0, a0, -1347
; RV64IZBA-NEXT:   slli a0, a0, 12
; RV64IZBA-NEXT:   addi a0, a0, -529
; RV64IZBA-NEXT:   slli a0, a0, 4
; RV64IZBA-NEXT:   ret
;
; RV64IZBB-LABEL: imm64_8:
; RV64IZBB:        # %bb.0:
; RV64IZBB-NEXT:   lui a0, 583
; RV64IZBB-NEXT:   addiw
a0, a0, -1875
; RV64IZBB-NEXT:   slli a0, a0, 14
; RV64IZBB-NEXT:   addi a0, a0, -947
; RV64IZBB-NEXT:   slli a0, a0, 12
; RV64IZBB-NEXT:   addi a0, a0, 1511
; RV64IZBB-NEXT:   slli a0, a0, 13
; RV64IZBB-NEXT:   addi a0, a0, -272
; RV64IZBB-NEXT:   ret
;
; RV64IZBS-LABEL: imm64_8:
; RV64IZBS:        # %bb.0:
; RV64IZBS-NEXT:   lui a0, 583
; RV64IZBS-NEXT:   addiw a0, a0, -1875
; RV64IZBS-NEXT:   slli a0, a0, 14
; RV64IZBS-NEXT:   addi a0, a0, -947
; RV64IZBS-NEXT:   slli a0, a0, 12
; RV64IZBS-NEXT:   addi a0, a0, 1511
; RV64IZBS-NEXT:   slli a0, a0, 13
; RV64IZBS-NEXT:   addi a0, a0, -272
; RV64IZBS-NEXT:   ret
;
; RV64IXTHEADBB-LABEL: imm64_8:
; RV64IXTHEADBB:   # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 583
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -1875
; RV64IXTHEADBB-NEXT:  slli a0, a0, 14
; RV64IXTHEADBB-NEXT:  addi a0, a0, -947
; RV64IXTHEADBB-NEXT:  slli a0, a0, 12
; RV64IXTHEADBB-NEXT:  addi a0, a0, 1511

```

```
; RV64IXTHEADBB-NEXT:  slli a0, a0, 13
; RV64IXTHEADBB-NEXT:
    addi a0, a0, -272
; RV64IXTHEADBB-NEXT:  ret
ret i64 1311768467463790320 ; 0x1234_5678_9ABC_DEF0
}
```

```
define i64 @imm64_9() nounwind {
; RV64I-LABEL: imm64_9:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a0, -1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm64_9:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  li a0, -1
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm64_9:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  li a0, -1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm64_9:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  li a0, -1
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm64_9:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  li a0, -1
; RV64IXTHEADBB-NEXT:  ret
ret i64 -1
}
```

; Various cases where extraneous ADDIs can be inserted where a (left shifted)
; LUI suffices.

```
define i64 @imm_left_shifted_lui_1() nounwind {
; RV64I-LABEL: imm_left_shifted_lui_1:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a0, 262145
; RV64I-NEXT:  slli a0, a0, 1
;
RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_left_shifted_lui_1:
; RV64IZBA:    # %bb.0:
```

```

; RV64IZBA-NEXT: lui a0, 262145
; RV64IZBA-NEXT: slli a0, a0, 1
; RV64IZBA-NEXT: ret
;
; RV64IZBB-LABEL: imm_left_shifted_lui_1:
; RV64IZBB: # %bb.0:
; RV64IZBB-NEXT: lui a0, 262145
; RV64IZBB-NEXT: slli a0, a0, 1
; RV64IZBB-NEXT: ret
;
; RV64IZBS-LABEL: imm_left_shifted_lui_1:
; RV64IZBS: # %bb.0:
; RV64IZBS-NEXT: lui a0, 262145
; RV64IZBS-NEXT: slli a0, a0, 1
; RV64IZBS-NEXT: ret
;
; RV64IXTHEADBB-LABEL: imm_left_shifted_lui_1:
; RV64IXTHEADBB: # %bb.0:
; RV64IXTHEADBB-NEXT: lui a0, 262145
; RV64IXTHEADBB-NEXT: slli a0, a0, 1
; RV64IXTHEADBB-NEXT: ret
ret i64 2147491840 ; 0x8000_2000
}

```

```

define i64 @imm_left_shifted_lui_2() nounwind {
; RV64I-LABEL: imm_left_shifted_lui_2:
; RV64I: # %bb.0:
; RV64I-NEXT: lui a0, 262145
; RV64I-NEXT: slli a0, a0, 2
; RV64I-NEXT: ret
;
; RV64IZBA-LABEL: imm_left_shifted_lui_2:
; RV64IZBA:
; # %bb.0:
; RV64IZBA-NEXT: lui a0, 262145
; RV64IZBA-NEXT: slli a0, a0, 2
; RV64IZBA-NEXT: ret
;
; RV64IZBB-LABEL: imm_left_shifted_lui_2:
; RV64IZBB: # %bb.0:
; RV64IZBB-NEXT: lui a0, 262145
; RV64IZBB-NEXT: slli a0, a0, 2
; RV64IZBB-NEXT: ret
;
; RV64IZBS-LABEL: imm_left_shifted_lui_2:
; RV64IZBS: # %bb.0:
; RV64IZBS-NEXT: lui a0, 262145
; RV64IZBS-NEXT: slli a0, a0, 2

```

```

; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_left_shifted_lui_2:
; RV64IXTHEADBB:   # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 262145
; RV64IXTHEADBB-NEXT:  slli a0, a0, 2
; RV64IXTHEADBB-NEXT:  ret
ret i64 4294983680 ; 0x1_0000_4000
}

```

```

define i64 @imm_left_shifted_lui_3() nounwind {
; RV64I-LABEL: imm_left_shifted_lui_3:
; RV64I:   # %bb.0:
; RV64I-NEXT:  lui a0, 4097
; RV64I-NEXT:  slli a0, a0, 20
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_left_shifted_lui_3:
; RV64IZBA:   # %bb.0:
; RV64IZBA-NEXT:  lui a0, 4097
; RV64IZBA-NEXT:  slli a0, a0, 20
;
RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_left_shifted_lui_3:
; RV64IZBB:   # %bb.0:
; RV64IZBB-NEXT:  lui a0, 4097
; RV64IZBB-NEXT:  slli a0, a0, 20
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_left_shifted_lui_3:
; RV64IZBS:   # %bb.0:
; RV64IZBS-NEXT:  lui a0, 4097
; RV64IZBS-NEXT:  slli a0, a0, 20
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_left_shifted_lui_3:
; RV64IXTHEADBB:   # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 4097
; RV64IXTHEADBB-NEXT:  slli a0, a0, 20
; RV64IXTHEADBB-NEXT:  ret
ret i64 17596481011712 ; 0x1001_0000_0000
}

```

; Various cases where extraneous ADDIs can be inserted where a (right shifted)
; LUI suffices, or where multiple ADDIs can be used instead of a single LUI.

```

define i64 @imm_right_shifted_lui_1() nounwind {

```



```

; RV64I-LABEL: imm_right_shifted_lui_1:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 983056
; RV64I-NEXT:  srli a0, a0, 16
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_right_shifted_lui_1:
; RV64IZBA:
;    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 983056
; RV64IZBA-NEXT:  srli a0, a0, 16
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_right_shifted_lui_1:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 983056
; RV64IZBB-NEXT:  srli a0, a0, 16
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_right_shifted_lui_1:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 983056
; RV64IZBS-NEXT:  srli a0, a0, 16
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_right_shifted_lui_1:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 983056
; RV64IXTHEADBB-NEXT:  srli a0, a0, 16
; RV64IXTHEADBB-NEXT:  ret
ret i64 281474976706561 ; 0xFFFF_FFFF_F001
}

```

```

define i64 @imm_right_shifted_lui_2() nounwind {
; RV64I-LABEL: imm_right_shifted_lui_2:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 1044481
; RV64I-NEXT:  slli a0, a0, 12
; RV64I-NEXT:  srli a0, a0, 24
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_right_shifted_lui_2:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:
;    lui a0, 1044481
; RV64IZBA-NEXT:  slli a0, a0, 12
; RV64IZBA-NEXT:  srli a0, a0, 24
; RV64IZBA-NEXT:  ret
}

```

```

;
; RV64IZBB-LABEL: imm_right_shifted_lui_2:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT: lui a0, 1044481
; RV64IZBB-NEXT: slli a0, a0, 12
; RV64IZBB-NEXT: srli a0, a0, 24
; RV64IZBB-NEXT: ret
;
; RV64IZBS-LABEL: imm_right_shifted_lui_2:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT: lui a0, 1044481
; RV64IZBS-NEXT: slli a0, a0, 12
; RV64IZBS-NEXT: srli a0, a0, 24
; RV64IZBS-NEXT: ret
;
; RV64IXTHEADBB-LABEL: imm_right_shifted_lui_2:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT: lui a0, 1044481
; RV64IXTHEADBB-NEXT: slli a0, a0, 12
; RV64IXTHEADBB-NEXT: srli a0, a0, 24
; RV64IXTHEADBB-NEXT: ret
ret i64 1099511623681 ; 0xFF_FFFF_F001
}

```

; We can materialize the upper bits with a single (shifted) LUI, but that option
; can be missed due to the lower bits, which aren't just 1s or just 0s.

```

define i64 @imm_decoupled_lui_addi() nounwind
{
; RV64I-LABEL: imm_decoupled_lui_addi:
; RV64I:    # %bb.0:
; RV64I-NEXT: lui a0, 4097
; RV64I-NEXT: slli a0, a0, 20
; RV64I-NEXT: addi a0, a0, -3
; RV64I-NEXT: ret
;
; RV64IZBA-LABEL: imm_decoupled_lui_addi:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT: lui a0, 4097
; RV64IZBA-NEXT: slli a0, a0, 20
; RV64IZBA-NEXT: addi a0, a0, -3
; RV64IZBA-NEXT: ret
;
; RV64IZBB-LABEL: imm_decoupled_lui_addi:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT: lui a0, 4097
; RV64IZBB-NEXT: slli a0, a0, 20
; RV64IZBB-NEXT: addi a0, a0, -3

```

```

; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_decoupled_lui_addi:
; RV64IZBS:      # %bb.0:
; RV64IZBS-NEXT:  lui a0, 4097
; RV64IZBS-NEXT:  slli a0, a0, 20
; RV64IZBS-NEXT:  addi a0, a0, -3
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_decoupled_lui_addi:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 4097
; RV64IXTHEADBB-NEXT:  slli a0, a0, 20
; RV64IXTHEADBB-NEXT:  addi a0, a0, -3
; RV64IXTHEADBB-NEXT:
    ret
ret i64 17596481011709 ; 0x1000_FFFF_FFFD
}

```

; This constant can be materialized for RV64 with LUI+SRLI+XORI.

```

define i64 @imm_end_xori_1() nounwind {
; RV64I-LABEL: imm_end_xori_1:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a0, 983040
; RV64I-NEXT:  srli a0, a0, 3
; RV64I-NEXT:  not a0, a0
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_end_xori_1:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 983040
; RV64IZBA-NEXT:  srli a0, a0, 3
; RV64IZBA-NEXT:  not a0, a0
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_end_xori_1:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 983040
; RV64IZBB-NEXT:  srli a0, a0, 3
; RV64IZBB-NEXT:  not a0, a0
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_end_xori_1:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 983040
; RV64IZBS-NEXT:  srli a0, a0, 3
; RV64IZBS-NEXT:  not a0, a0

```

```

; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_end_xori_1:
; RV64IXTHEADBB:   # %bb.0:
; RV64IXTHEADBB-NEXT:
    lui a0, 983040
; RV64IXTHEADBB-NEXT:  srli a0, a0, 3
; RV64IXTHEADBB-NEXT:  not a0, a0
; RV64IXTHEADBB-NEXT:  ret
ret i64 -2305843009180139521 ; 0xE000_0000_01FF_FFFF
}

```

; This constant can be materialized for RV64 with ADDI+SLLI+ADDI+ADDI.

```

define i64 @imm_end_2addi_1() nounwind {
; RV64I-LABEL: imm_end_2addi_1:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a0, -2047
; RV64I-NEXT:  slli a0, a0, 39
; RV64I-NEXT:  addi a0, a0, -2048
; RV64I-NEXT:  addi a0, a0, -1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_end_2addi_1:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  li a0, -2047
; RV64IZBA-NEXT:  slli a0, a0, 39
; RV64IZBA-NEXT:  addi a0, a0, -2048
; RV64IZBA-NEXT:  addi a0, a0, -1
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_end_2addi_1:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  li a0, -2047
; RV64IZBB-NEXT:  slli a0, a0, 39
; RV64IZBB-NEXT:  addi a0, a0, -2048
; RV64IZBB-NEXT:  addi a0, a0, -1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_end_2addi_1:
;
RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  li a0, -2047
; RV64IZBS-NEXT:  slli a0, a0, 39
; RV64IZBS-NEXT:  addi a0, a0, -2048
; RV64IZBS-NEXT:  addi a0, a0, -1
; RV64IZBS-NEXT:  ret
;

```

```

; RV64IXTHEADBB-LABEL: imm_end_2addi_1:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  li a0, -2047
; RV64IXTHEADBB-NEXT:  slli a0, a0, 39
; RV64IXTHEADBB-NEXT:  addi a0, a0, -2048
; RV64IXTHEADBB-NEXT:  addi a0, a0, -1
; RV64IXTHEADBB-NEXT:  ret
ret i64 -1125350151030785 ; 0xFFFC_007F_FFFF_F7FF
}

```

; This constant can be more efficiently materialized for RV64 if we use two
; registers instead of one.

```

define i64 @imm_2reg_1() nounwind {
; RV64I-LABEL: imm_2reg_1:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 74565
; RV64I-NEXT:  addiw a0, a0, 1656
; RV64I-NEXT:  slli a1, a0, 57
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_2reg_1:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 74565
; RV64IZBA-NEXT:  addiw a0, a0, 1656
; RV64IZBA-NEXT:
;   slli a1, a0, 57
; RV64IZBA-NEXT:  add a0, a0, a1
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_2reg_1:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 74565
; RV64IZBB-NEXT:  addiw a0, a0, 1656
; RV64IZBB-NEXT:  slli a1, a0, 57
; RV64IZBB-NEXT:  add a0, a0, a1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_2reg_1:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 74565
; RV64IZBS-NEXT:  addiw a0, a0, 1656
; RV64IZBS-NEXT:  slli a1, a0, 57
; RV64IZBS-NEXT:  add a0, a0, a1
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_2reg_1:

```

```

; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 74565
; RV64IXTHEADBB-NEXT:  addiw a0, a0, 1656
; RV64IXTHEADBB-NEXT:  slli a1, a0, 57
; RV64IXTHEADBB-NEXT:  add a0, a0, a1
; RV64IXTHEADBB-NEXT:  ret
ret i64 -1152921504301427080 ; 0xF000_0000_1234_5678
}

```

; FIXME: This should use a single ADDI for the immediate.

```
define void @imm_store_i16_neg1(ptr %p) nounwind {
```

```
; RV64I-LABEL: imm_store_i16_neg1:
```

```
;
```

```
RV64I:    # %bb.0:
```

```
; RV64I-NEXT:  li a1, -1
```

```
; RV64I-NEXT:  sh a1, 0(a0)
```

```
; RV64I-NEXT:  ret
```

```
;
```

```
; RV64IZBA-LABEL: imm_store_i16_neg1:
```

```
; RV64IZBA:    # %bb.0:
```

```
; RV64IZBA-NEXT:  li a1, -1
```

```
; RV64IZBA-NEXT:  sh a1, 0(a0)
```

```
; RV64IZBA-NEXT:  ret
```

```
;
```

```
; RV64IZBB-LABEL: imm_store_i16_neg1:
```

```
; RV64IZBB:    # %bb.0:
```

```
; RV64IZBB-NEXT:  li a1, -1
```

```
; RV64IZBB-NEXT:  sh a1, 0(a0)
```

```
; RV64IZBB-NEXT:  ret
```

```
;
```

```
; RV64IZBS-LABEL: imm_store_i16_neg1:
```

```
; RV64IZBS:    # %bb.0:
```

```
; RV64IZBS-NEXT:  li a1, -1
```

```
; RV64IZBS-NEXT:  sh a1, 0(a0)
```

```
; RV64IZBS-NEXT:  ret
```

```
;
```

```
; RV64IXTHEADBB-LABEL: imm_store_i16_neg1:
```

```
; RV64IXTHEADBB:    # %bb.0:
```

```
; RV64IXTHEADBB-NEXT:  li a1, -1
```

```
; RV64IXTHEADBB-NEXT:  sh a1, 0(a0)
```

```
; RV64IXTHEADBB-NEXT:  ret
```

```
store i16 -1, ptr %p
```

```
ret void
```

```
}
```

; FIXME: This should use a single ADDI for the immediate.

```
define void @imm_store_i32_neg1(ptr %p) nounwind {
```

```
; RV64I-LABEL: imm_store_i32_neg1:
```

```

; RV64I:    # %bb.0:
; RV64I-NEXT:  li a1, -1
; RV64I-NEXT:
    sw a1, 0(a0)
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_store_i32_neg1:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  li a1, -1
; RV64IZBA-NEXT:  sw a1, 0(a0)
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_store_i32_neg1:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  li a1, -1
; RV64IZBB-NEXT:  sw a1, 0(a0)
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_store_i32_neg1:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  li a1, -1
; RV64IZBS-NEXT:  sw a1, 0(a0)
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_store_i32_neg1:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  li a1, -1
; RV64IXTHEADBB-NEXT:  sw a1, 0(a0)
; RV64IXTHEADBB-NEXT:  ret
    store i32 -1, ptr %p
    ret void
}

```

```

define i64 @imm_5372288229() {
; RV64I-LABEL: imm_5372288229:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 160
; RV64I-NEXT:  addiw a0, a0, 437
; RV64I-NEXT:  slli a0, a0, 13
; RV64I-NEXT:  addi a0, a0, -795
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_5372288229:
; RV64IZBA:
    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 655797
; RV64IZBA-NEXT:  slli.uw a0, a0, 1
; RV64IZBA-NEXT:  addi a0, a0, -795

```

```

; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_5372288229:
; RV64IZBB:      # %bb.0:
; RV64IZBB-NEXT:  lui a0, 160
; RV64IZBB-NEXT:  addiw a0, a0, 437
; RV64IZBB-NEXT:  slli a0, a0, 13
; RV64IZBB-NEXT:  addi a0, a0, -795
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_5372288229:
; RV64IZBS:      # %bb.0:
; RV64IZBS-NEXT:  lui a0, 263018
; RV64IZBS-NEXT:  addiw a0, a0, -795
; RV64IZBS-NEXT:  bseti a0, a0, 32
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_5372288229:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 160
; RV64IXTHEADBB-NEXT:  addiw a0, a0, 437
; RV64IXTHEADBB-NEXT:  slli a0, a0, 13
; RV64IXTHEADBB-NEXT:  addi a0, a0, -795
; RV64IXTHEADBB-NEXT:  ret
ret i64 5372288229
}

```

```

define i64 @imm_neg_5372288229() {
; RV64I-LABEL: imm_neg_5372288229:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a0, 1048416
; RV64I-NEXT:
    addiw a0, a0, -437
; RV64I-NEXT:  slli a0, a0, 13
; RV64I-NEXT:  addi a0, a0, 795
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_neg_5372288229:
; RV64IZBA:      # %bb.0:
; RV64IZBA-NEXT:  lui a0, 611378
; RV64IZBA-NEXT:  addiw a0, a0, 265
; RV64IZBA-NEXT:  sh1add a0, a0, a0
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_neg_5372288229:
; RV64IZBB:      # %bb.0:
; RV64IZBB-NEXT:  lui a0, 1048416
; RV64IZBB-NEXT:  addiw a0, a0, -437

```



```

; RV64IZBB-NEXT:  slli a0, a0, 13
; RV64IZBB-NEXT:  addi a0, a0, 795
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_neg_5372288229:
; RV64IZBS:      # %bb.0:
; RV64IZBS-NEXT:  lui a0, 785558
; RV64IZBS-NEXT:  addiw a0, a0, 795
; RV64IZBS-NEXT:  bclri a0, a0, 32
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_neg_5372288229:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 1048416
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -437
; RV64IXTHEADBB-NEXT:  slli a0, a0, 13
; RV64IXTHEADBB-NEXT:  addi a0, a0,
795
; RV64IXTHEADBB-NEXT:  ret
ret i64 -5372288229
}

```

```

define i64 @imm_8953813715() {
; RV64I-LABEL: imm_8953813715:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a0, 267
; RV64I-NEXT:  addiw a0, a0, -637
; RV64I-NEXT:  slli a0, a0, 13
; RV64I-NEXT:  addi a0, a0, -1325
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_8953813715:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 437198
; RV64IZBA-NEXT:  addiw a0, a0, -265
; RV64IZBA-NEXT:  sh2add a0, a0, a0
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_8953813715:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 267
; RV64IZBB-NEXT:  addiw a0, a0, -637
; RV64IZBB-NEXT:  slli a0, a0, 13
; RV64IZBB-NEXT:  addi a0, a0, -1325
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_8953813715:
; RV64IZBS:    # %bb.0:

```

```

; RV64IZBS-NEXT:  lui a0, 88838
; RV64IZBS-NEXT:  addiw a0, a0, -1325
; RV64IZBS-NEXT:  bseti a0, a0, 33
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_8953813715:
; RV64IXTHEADBB:   # %bb.0:
;
RV64IXTHEADBB-NEXT:  lui a0, 267
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -637
; RV64IXTHEADBB-NEXT:  slli a0, a0, 13
; RV64IXTHEADBB-NEXT:  addi a0, a0, -1325
; RV64IXTHEADBB-NEXT:  ret
ret i64 8953813715
}

```

```

define i64 @imm_neg_8953813715() {
; RV64I-LABEL: imm_neg_8953813715:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a0, 1048309
; RV64I-NEXT:  addiw a0, a0, 637
; RV64I-NEXT:  slli a0, a0, 13
; RV64I-NEXT:  addi a0, a0, 1325
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_neg_8953813715:
; RV64IZBA:   # %bb.0:
; RV64IZBA-NEXT:  lui a0, 611378
; RV64IZBA-NEXT:  addiw a0, a0, 265
; RV64IZBA-NEXT:  sh2add a0, a0, a0
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_neg_8953813715:
; RV64IZBB:   # %bb.0:
; RV64IZBB-NEXT:  lui a0, 1048309
; RV64IZBB-NEXT:  addiw a0, a0, 637
; RV64IZBB-NEXT:  slli a0, a0, 13
; RV64IZBB-NEXT:  addi a0, a0, 1325
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_neg_8953813715:
; RV64IZBS:   # %bb.0:
; RV64IZBS-NEXT:
    lui a0, 959738
; RV64IZBS-NEXT:  addiw a0, a0, 1325
; RV64IZBS-NEXT:  bclri a0, a0, 33
; RV64IZBS-NEXT:  ret
;

```

```
; RV64IXTHEADBB-LABEL: imm_neg_8953813715:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 1048309
; RV64IXTHEADBB-NEXT:  addiw a0, a0, 637
; RV64IXTHEADBB-NEXT:  slli a0, a0, 13
; RV64IXTHEADBB-NEXT:  addi a0, a0, 1325
; RV64IXTHEADBB-NEXT:  ret
ret i64 -8953813715
}
```

```
define i64 @imm_16116864687() {
; RV64I-LABEL: imm_16116864687:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 961
; RV64I-NEXT:  addiw a0, a0, -1475
; RV64I-NEXT:  slli a0, a0, 12
; RV64I-NEXT:  addi a0, a0, 1711
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_16116864687:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 437198
; RV64IZBA-NEXT:  addiw a0, a0, -265
; RV64IZBA-NEXT:  sh3add a0, a0, a0
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_16116864687:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 961
; RV64IZBB-NEXT:  addiw a0, a0, -1475
; RV64IZBB-NEXT:
;   slli a0, a0, 12
; RV64IZBB-NEXT:  addi a0, a0, 1711
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_16116864687:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 961
; RV64IZBS-NEXT:  addiw a0, a0, -1475
; RV64IZBS-NEXT:  slli a0, a0, 12
; RV64IZBS-NEXT:  addi a0, a0, 1711
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_16116864687:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 961
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -1475
; RV64IXTHEADBB-NEXT:  slli a0, a0, 12
```

```

; RV64IXTHEADBB-NEXT:  addi a0, a0, 1711
; RV64IXTHEADBB-NEXT:  ret
ret i64 16116864687
}

define i64 @imm_neg_16116864687() {
; RV64I-LABEL: imm_neg_16116864687:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a0, 1047615
; RV64I-NEXT:  addiw a0, a0, 1475
; RV64I-NEXT:  slli a0, a0, 12
; RV64I-NEXT:  addi a0, a0, -1711
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_neg_16116864687:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 611378
; RV64IZBA-NEXT:
addiw a0, a0, 265
; RV64IZBA-NEXT:  sh3add a0, a0, a0
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_neg_16116864687:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 1047615
; RV64IZBB-NEXT:  addiw a0, a0, 1475
; RV64IZBB-NEXT:  slli a0, a0, 12
; RV64IZBB-NEXT:  addi a0, a0, -1711
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_neg_16116864687:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 1047615
; RV64IZBS-NEXT:  addiw a0, a0, 1475
; RV64IZBS-NEXT:  slli a0, a0, 12
; RV64IZBS-NEXT:  addi a0, a0, -1711
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_neg_16116864687:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 1047615
; RV64IXTHEADBB-NEXT:  addiw a0, a0, 1475
; RV64IXTHEADBB-NEXT:  slli a0, a0, 12
; RV64IXTHEADBB-NEXT:  addi a0, a0, -1711
; RV64IXTHEADBB-NEXT:  ret
ret i64 -16116864687
}

```

```

define i64 @imm_2344336315() {
; RV64I-LABEL: imm_2344336315:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 143087
; RV64I-NEXT:
    slli a0, a0, 2
; RV64I-NEXT:  addi a0, a0, -1093
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_2344336315:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 143087
; RV64IZBA-NEXT:  slli a0, a0, 2
; RV64IZBA-NEXT:  addi a0, a0, -1093
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_2344336315:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 143087
; RV64IZBB-NEXT:  slli a0, a0, 2
; RV64IZBB-NEXT:  addi a0, a0, -1093
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_2344336315:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 143087
; RV64IZBS-NEXT:  slli a0, a0, 2
; RV64IZBS-NEXT:  addi a0, a0, -1093
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_2344336315:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 143087
; RV64IXTHEADBB-NEXT:  slli a0, a0, 2
; RV64IXTHEADBB-NEXT:  addi a0, a0, -1093
; RV64IXTHEADBB-NEXT:  ret
    ret i64 2344336315 ; 0x8bbbbbbb
}

```

```

define i64 @imm_70370820078523() {
; RV64-NOPOOL-LABEL: imm_70370820078523:
;
    RV64-NOPOOL:    # %bb.0:
; RV64-NOPOOL-NEXT:  lui a0, 256
; RV64-NOPOOL-NEXT:  addiw a0, a0, 31
; RV64-NOPOOL-NEXT:  slli a0, a0, 12
; RV64-NOPOOL-NEXT:  addi a0, a0, -273
; RV64-NOPOOL-NEXT:  slli a0, a0, 14

```

```

; RV64-NOPOOL-NEXT:  addi a0, a0, -1093
; RV64-NOPOOL-NEXT:  ret
;
; RV64I-POOL-LABEL: imm_70370820078523:
; RV64I-POOL:        # %bb.0:
; RV64I-POOL-NEXT:   lui a0, %hi(.LCPI37_0)
; RV64I-POOL-NEXT:   ld a0, %lo(.LCPI37_0)(a0)
; RV64I-POOL-NEXT:   ret
;
; RV64IZBA-LABEL: imm_70370820078523:
; RV64IZBA:         # %bb.0:
; RV64IZBA-NEXT:    lui a0, 256
; RV64IZBA-NEXT:    addiw a0, a0, 31
; RV64IZBA-NEXT:    slli a0, a0, 12
; RV64IZBA-NEXT:    addi a0, a0, -273
; RV64IZBA-NEXT:    slli a0, a0, 14
; RV64IZBA-NEXT:    addi a0, a0, -1093
; RV64IZBA-NEXT:    ret
;
; RV64IZBB-LABEL: imm_70370820078523:
; RV64IZBB:         # %bb.0:
; RV64IZBB-NEXT:    lui a0, 256
; RV64IZBB-NEXT:    addiw a0, a0, 31
; RV64IZBB-NEXT:    slli a0, a0, 12
; RV64IZBB-NEXT:    addi a0, a0, -273
;
; RV64IZBB-NEXT:    slli a0, a0, 14
; RV64IZBB-NEXT:    addi a0, a0, -1093
; RV64IZBB-NEXT:    ret
;
; RV64IZBS-LABEL: imm_70370820078523:
; RV64IZBS:         # %bb.0:
; RV64IZBS-NEXT:    lui a0, 506812
; RV64IZBS-NEXT:    addiw a0, a0, -1093
; RV64IZBS-NEXT:    bseti a0, a0, 46
; RV64IZBS-NEXT:    ret
;
; RV64IXTHEADBB-LABEL: imm_70370820078523:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 256
; RV64IXTHEADBB-NEXT:  addiw a0, a0, 31
; RV64IXTHEADBB-NEXT:  slli a0, a0, 12
; RV64IXTHEADBB-NEXT:  addi a0, a0, -273
; RV64IXTHEADBB-NEXT:  slli a0, a0, 14
; RV64IXTHEADBB-NEXT:  addi a0, a0, -1093
; RV64IXTHEADBB-NEXT:  ret
ret i64 70370820078523 ; 0x40007bbbbbbb
}

```

```

define i64 @imm_neg_9223372034778874949() {
; RV64I-LABEL: imm_neg_9223372034778874949:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 506812
; RV64I-NEXT:  addiw a0, a0, -1093
; RV64I-NEXT:  slli a1, a0, 63
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_neg_9223372034778874949:
;
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 506812
; RV64IZBA-NEXT:  addiw a0, a0, -1093
; RV64IZBA-NEXT:  slli a1, a0, 63
; RV64IZBA-NEXT:  add a0, a0, a1
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_neg_9223372034778874949:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 506812
; RV64IZBB-NEXT:  addiw a0, a0, -1093
; RV64IZBB-NEXT:  slli a1, a0, 63
; RV64IZBB-NEXT:  add a0, a0, a1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_neg_9223372034778874949:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 506812
; RV64IZBS-NEXT:  addiw a0, a0, -1093
; RV64IZBS-NEXT:  bseti a0, a0, 63
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_neg_9223372034778874949:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 506812
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -1093
; RV64IXTHEADBB-NEXT:  slli a1, a0, 63
; RV64IXTHEADBB-NEXT:  add a0, a0, a1
; RV64IXTHEADBB-NEXT:  ret
ret i64 -9223372034778874949 ; 0x800000007bbbbbbb
}

define
i64 @imm_neg_9223301666034697285() {
; RV64-NOPOOL-LABEL: imm_neg_9223301666034697285:
; RV64-NOPOOL:    # %bb.0:

```

```

; RV64-NOPOOL-NEXT: lui a0, 917505
; RV64-NOPOOL-NEXT: slli a0, a0, 8
; RV64-NOPOOL-NEXT: addi a0, a0, 31
; RV64-NOPOOL-NEXT: slli a0, a0, 12
; RV64-NOPOOL-NEXT: addi a0, a0, -273
; RV64-NOPOOL-NEXT: slli a0, a0, 14
; RV64-NOPOOL-NEXT: addi a0, a0, -1093
; RV64-NOPOOL-NEXT: ret
;
; RV64I-POOL-LABEL: imm_neg_9223301666034697285:
; RV64I-POOL: # %bb.0:
; RV64I-POOL-NEXT: lui a0, %hi(LCPI39_0)
; RV64I-POOL-NEXT: ld a0, %lo(LCPI39_0)(a0)
; RV64I-POOL-NEXT: ret
;
; RV64IZBA-LABEL: imm_neg_9223301666034697285:
; RV64IZBA: # %bb.0:
; RV64IZBA-NEXT: lui a0, 917505
; RV64IZBA-NEXT: slli a0, a0, 8
; RV64IZBA-NEXT: addi a0, a0, 31
; RV64IZBA-NEXT: slli a0, a0, 12
; RV64IZBA-NEXT: addi a0, a0, -273
; RV64IZBA-NEXT: slli a0, a0, 14
; RV64IZBA-NEXT: addi a0, a0, -1093
; RV64IZBA-NEXT: ret
;
; RV64IZBB-LABEL:
imm_neg_9223301666034697285:
; RV64IZBB: # %bb.0:
; RV64IZBB-NEXT: lui a0, 917505
; RV64IZBB-NEXT: slli a0, a0, 8
; RV64IZBB-NEXT: addi a0, a0, 31
; RV64IZBB-NEXT: slli a0, a0, 12
; RV64IZBB-NEXT: addi a0, a0, -273
; RV64IZBB-NEXT: slli a0, a0, 14
; RV64IZBB-NEXT: addi a0, a0, -1093
; RV64IZBB-NEXT: ret
;
; RV64IZBS-LABEL: imm_neg_9223301666034697285:
; RV64IZBS: # %bb.0:
; RV64IZBS-NEXT: lui a0, 506812
; RV64IZBS-NEXT: addiw a0, a0, -1093
; RV64IZBS-NEXT: bseti a0, a0, 46
; RV64IZBS-NEXT: bseti a0, a0, 63
; RV64IZBS-NEXT: ret
;
; RV64IXTHEADBB-LABEL: imm_neg_9223301666034697285:
; RV64IXTHEADBB: # %bb.0:

```



```

; RV64IXTHEADBB-NEXT: lui a0, 917505
; RV64IXTHEADBB-NEXT: slli a0, a0, 8
; RV64IXTHEADBB-NEXT: addi a0, a0, 31
; RV64IXTHEADBB-NEXT: slli a0, a0, 12
; RV64IXTHEADBB-NEXT: addi a0, a0, -273
; RV64IXTHEADBB-NEXT: slli a0, a0, 14
; RV64IXTHEADBB-NEXT: addi a0, a0, -1093
; RV64IXTHEADBB-NEXT: ret
ret i64 -9223301666034697285 ; 0x800040007bbbbbbb
}

```

```

define i64 @imm_neg_2219066437() {
; RV64I-LABEL: imm_neg_2219066437:
; RV64I:    # %bb.0:
; RV64I-NEXT: lui a0, 913135
; RV64I-NEXT: slli a0, a0, 2
; RV64I-NEXT: addi a0, a0, -1093
; RV64I-NEXT: ret
;
; RV64IZBA-LABEL: imm_neg_2219066437:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT: lui a0, 913135
; RV64IZBA-NEXT: slli a0, a0, 2
; RV64IZBA-NEXT: addi a0, a0, -1093
; RV64IZBA-NEXT: ret
;
; RV64IZBB-LABEL: imm_neg_2219066437:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT: lui a0, 913135
; RV64IZBB-NEXT: slli a0, a0, 2
; RV64IZBB-NEXT: addi a0, a0, -1093
; RV64IZBB-NEXT: ret
;
; RV64IZBS-LABEL: imm_neg_2219066437:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT: lui a0, 913135
; RV64IZBS-NEXT: slli a0, a0, 2
; RV64IZBS-NEXT: addi a0, a0, -1093
; RV64IZBS-NEXT: ret
;
; RV64IXTHEADBB-LABEL: imm_neg_2219066437:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT: lui a0, 913135
; RV64IXTHEADBB-NEXT:
;     slli a0, a0, 2
; RV64IXTHEADBB-NEXT: addi a0, a0, -1093
; RV64IXTHEADBB-NEXT: ret
ret i64 -2219066437 ; 0xffffffff7bbbbbbb
}

```

```

}

define i64 @imm_neg_8798043653189() {
; RV64I-LABEL: imm_neg_8798043653189:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 917475
; RV64I-NEXT:  addiw a0, a0, -273
; RV64I-NEXT:  slli a0, a0, 14
; RV64I-NEXT:  addi a0, a0, -1093
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_neg_8798043653189:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 917475
; RV64IZBA-NEXT:  addiw a0, a0, -273
; RV64IZBA-NEXT:  slli a0, a0, 14
; RV64IZBA-NEXT:  addi a0, a0, -1093
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_neg_8798043653189:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 917475
; RV64IZBB-NEXT:  addiw a0, a0, -273
; RV64IZBB-NEXT:  slli a0, a0, 14
; RV64IZBB-NEXT:  addi a0, a0, -1093
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_neg_8798043653189:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 572348
; RV64IZBS-NEXT:
;   addiw a0, a0, -1093
; RV64IZBS-NEXT:  bclri a0, a0, 43
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_neg_8798043653189:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 917475
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -273
; RV64IXTHEADBB-NEXT:  slli a0, a0, 14
; RV64IXTHEADBB-NEXT:  addi a0, a0, -1093
; RV64IXTHEADBB-NEXT:  ret
;   ret i64 -8798043653189 ; 0xfffff7ff8bbbbbbb
}

```

```

define i64 @imm_9223372034904144827() {
; RV64I-LABEL: imm_9223372034904144827:
; RV64I:    # %bb.0:

```

```

; RV64I-NEXT:  lui a0, 572348
; RV64I-NEXT:  addiw a0, a0, -1093
; RV64I-NEXT:  slli a1, a0, 63
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_9223372034904144827:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 572348
; RV64IZBA-NEXT:  addiw a0, a0, -1093
; RV64IZBA-NEXT:  slli a1, a0, 63
; RV64IZBA-NEXT:  add a0, a0, a1
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_9223372034904144827:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:
    lui a0, 572348
; RV64IZBB-NEXT:  addiw a0, a0, -1093
; RV64IZBB-NEXT:  slli a1, a0, 63
; RV64IZBB-NEXT:  add a0, a0, a1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_9223372034904144827:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 572348
; RV64IZBS-NEXT:  addiw a0, a0, -1093
; RV64IZBS-NEXT:  bclri a0, a0, 63
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_9223372034904144827:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 572348
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -1093
; RV64IXTHEADBB-NEXT:  slli a1, a0, 63
; RV64IXTHEADBB-NEXT:  add a0, a0, a1
; RV64IXTHEADBB-NEXT:  ret
ret i64 9223372034904144827 ; 0x7fffffff8bbbbbbb
}

```

```

define i64 @imm_neg_9223354442718100411() {
; RV64-NOPOOL-LABEL: imm_neg_9223354442718100411:
; RV64-NOPOOL:    # %bb.0:
; RV64-NOPOOL-NEXT:  lui a0, 524287
; RV64-NOPOOL-NEXT:  slli a0, a0, 6
; RV64-NOPOOL-NEXT:  addi a0, a0, -29
; RV64-NOPOOL-NEXT:  slli a0, a0, 12
; RV64-NOPOOL-NEXT:

```

```

    addi a0, a0, -273
; RV64-NOPOOL-NEXT:  slli a0, a0, 14
; RV64-NOPOOL-NEXT:  addi a0, a0, -1093
; RV64-NOPOOL-NEXT:  ret
;
; RV64I-POOL-LABEL: imm_neg_9223354442718100411:
; RV64I-POOL:        # %bb.0:
; RV64I-POOL-NEXT:   lui a0, %hi(.LCPI43_0)
; RV64I-POOL-NEXT:   ld a0, %lo(.LCPI43_0)(a0)
; RV64I-POOL-NEXT:   ret
;
; RV64IZBA-LABEL: imm_neg_9223354442718100411:
; RV64IZBA:          # %bb.0:
; RV64IZBA-NEXT:     lui a0, 524287
; RV64IZBA-NEXT:     slli a0, a0, 6
; RV64IZBA-NEXT:     addi a0, a0, -29
; RV64IZBA-NEXT:     slli a0, a0, 12
; RV64IZBA-NEXT:     addi a0, a0, -273
; RV64IZBA-NEXT:     slli a0, a0, 14
; RV64IZBA-NEXT:     addi a0, a0, -1093
; RV64IZBA-NEXT:     ret
;
; RV64IZBB-LABEL: imm_neg_9223354442718100411:
; RV64IZBB:          # %bb.0:
; RV64IZBB-NEXT:     lui a0, 524287
; RV64IZBB-NEXT:     slli a0, a0, 6
; RV64IZBB-NEXT:     addi a0, a0, -29
; RV64IZBB-NEXT:     slli a0, a0, 12
; RV64IZBB-NEXT:     addi a0, a0, -273
; RV64IZBB-NEXT:     slli a0, a0, 14
; RV64IZBB-NEXT:
    addi a0, a0, -1093
; RV64IZBB-NEXT:     ret
;
; RV64IZBS-LABEL: imm_neg_9223354442718100411:
; RV64IZBS:          # %bb.0:
; RV64IZBS-NEXT:     lui a0, 572348
; RV64IZBS-NEXT:     addiw a0, a0, -1093
; RV64IZBS-NEXT:     bclri a0, a0, 44
; RV64IZBS-NEXT:     bclri a0, a0, 63
; RV64IZBS-NEXT:     ret
;
; RV64IXTHEADBB-LABEL: imm_neg_9223354442718100411:
; RV64IXTHEADBB:     # %bb.0:
; RV64IXTHEADBB-NEXT: lui a0, 524287
; RV64IXTHEADBB-NEXT: slli a0, a0, 6
; RV64IXTHEADBB-NEXT: addi a0, a0, -29
; RV64IXTHEADBB-NEXT: slli a0, a0, 12

```

```

; RV64IXTHEADBB-NEXT:  addi a0, a0, -273
; RV64IXTHEADBB-NEXT:  slli a0, a0, 14
; RV64IXTHEADBB-NEXT:  addi a0, a0, -1093
; RV64IXTHEADBB-NEXT:  ret
ret i64 9223354442718100411 ; 0x7ffeffff8bbbbbbb
}

```

```

define i64 @imm_2863311530() {
; RV64I-LABEL: imm_2863311530:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 349525
; RV64I-NEXT:  addiw a0, a0, 1365
; RV64I-NEXT:  slli a0, a0, 1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_2863311530:
; RV64IZBA:
;   # %bb.0:
; RV64IZBA-NEXT:  lui a0, 349525
; RV64IZBA-NEXT:  addiw a0, a0, 1365
; RV64IZBA-NEXT:  slli a0, a0, 1
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_2863311530:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 349525
; RV64IZBB-NEXT:  addiw a0, a0, 1365
; RV64IZBB-NEXT:  slli a0, a0, 1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_2863311530:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 349525
; RV64IZBS-NEXT:  addiw a0, a0, 1365
; RV64IZBS-NEXT:  slli a0, a0, 1
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_2863311530:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 349525
; RV64IXTHEADBB-NEXT:  addiw a0, a0, 1365
; RV64IXTHEADBB-NEXT:  slli a0, a0, 1
; RV64IXTHEADBB-NEXT:  ret
ret i64 2863311530 ; #0xaaaaaaaa
}

```

```

define i64 @imm_neg_2863311530() {
; RV64I-LABEL: imm_neg_2863311530:

```

```

; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 699051
; RV64I-NEXT:  addiw a0, a0, -1365
; RV64I-NEXT:  slli a0,
a0, 1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_neg_2863311530:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 699051
; RV64IZBA-NEXT:  addiw a0, a0, -1365
; RV64IZBA-NEXT:  slli a0, a0, 1
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_neg_2863311530:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 699051
; RV64IZBB-NEXT:  addiw a0, a0, -1365
; RV64IZBB-NEXT:  slli a0, a0, 1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_neg_2863311530:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 699051
; RV64IZBS-NEXT:  addiw a0, a0, -1365
; RV64IZBS-NEXT:  slli a0, a0, 1
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_neg_2863311530:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 699051
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -1365
; RV64IXTHEADBB-NEXT:  slli a0, a0, 1
; RV64IXTHEADBB-NEXT:  ret
ret i64 -2863311530 ; #0xffffffff55555556
}

```

```

define i64 @imm_2147486378() {
; RV64I-LABEL: imm_2147486378:
; RV64I:    # %bb.0:
; RV64I-NEXT:
li a0, 1
; RV64I-NEXT:  slli a0, a0, 31
; RV64I-NEXT:  addi a0, a0, 1365
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_2147486378:
; RV64IZBA:    # %bb.0:

```

```

; RV64IZBA-NEXT:  li a0, 1
; RV64IZBA-NEXT:  slli a0, a0, 31
; RV64IZBA-NEXT:  addi a0, a0, 1365
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_2147486378:
; RV64IZBB:      # %bb.0:
; RV64IZBB-NEXT:  li a0, 1
; RV64IZBB-NEXT:  slli a0, a0, 31
; RV64IZBB-NEXT:  addi a0, a0, 1365
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_2147486378:
; RV64IZBS:      # %bb.0:
; RV64IZBS-NEXT:  li a0, 1365
; RV64IZBS-NEXT:  bseti a0, a0, 31
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_2147486378:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  li a0, 1
; RV64IXTHEADBB-NEXT:  slli a0, a0, 31
; RV64IXTHEADBB-NEXT:  addi a0, a0, 1365
; RV64IXTHEADBB-NEXT:  ret
ret i64 2147485013
}

```

```

define i64 @imm_neg_2147485013() {
; RV64I-LABEL: imm_neg_2147485013:
; RV64I:      # %bb.0:
; RV64I-NEXT:
lui a0, 524288
; RV64I-NEXT:  addi a0, a0, -1365
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_neg_2147485013:
; RV64IZBA:      # %bb.0:
; RV64IZBA-NEXT:  lui a0, 524288
; RV64IZBA-NEXT:  addi a0, a0, -1365
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_neg_2147485013:
; RV64IZBB:      # %bb.0:
; RV64IZBB-NEXT:  lui a0, 524288
; RV64IZBB-NEXT:  addi a0, a0, -1365
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_neg_2147485013:

```

```

; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 524288
; RV64IZBS-NEXT:  addi a0, a0, -1365
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_neg_2147485013:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 524288
; RV64IXTHEADBB-NEXT:  addi a0, a0, -1365
; RV64IXTHEADBB-NEXT:  ret
ret i64 -2147485013
}

```

```

define i64 @imm_12900924131259() {
; RV64I-LABEL: imm_12900924131259:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 188
; RV64I-NEXT:  addiw a0, a0, -1093
; RV64I-NEXT:  slli a0, a0, 24
; RV64I-NEXT:  addi a0,
a0, 1979
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_12900924131259:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 768955
; RV64IZBA-NEXT:  slli.uw a0, a0, 12
; RV64IZBA-NEXT:  addi a0, a0, 1979
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_12900924131259:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 188
; RV64IZBB-NEXT:  addiw a0, a0, -1093
; RV64IZBB-NEXT:  slli a0, a0, 24
; RV64IZBB-NEXT:  addi a0, a0, 1979
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_12900924131259:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 188
; RV64IZBS-NEXT:  addiw a0, a0, -1093
; RV64IZBS-NEXT:  slli a0, a0, 24
; RV64IZBS-NEXT:  addi a0, a0, 1979
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_12900924131259:
; RV64IXTHEADBB:    # %bb.0:

```



```
; RV64IXTHEADBB-NEXT: lui a0, 188
; RV64IXTHEADBB-NEXT: addiw a0, a0, -1093
; RV64IXTHEADBB-NEXT: slli a0, a0, 24
; RV64IXTHEADBB-NEXT: addi a0, a0, 1979
; RV64IXTHEADBB-NEXT: ret
ret i64 12900924131259
}
```

```
define
i64 @imm_50394234880() {
; RV64I-LABEL: imm_50394234880:
; RV64I:    # %bb.0:
; RV64I-NEXT: lui a0, 188
; RV64I-NEXT: addiw a0, a0, -1093
; RV64I-NEXT: slli a0, a0, 16
; RV64I-NEXT: ret
;
; RV64IZBA-LABEL: imm_50394234880:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT: lui a0, 768955
; RV64IZBA-NEXT: slli.uw a0, a0, 4
; RV64IZBA-NEXT: ret
;
; RV64IZBB-LABEL: imm_50394234880:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT: lui a0, 188
; RV64IZBB-NEXT: addiw a0, a0, -1093
; RV64IZBB-NEXT: slli a0, a0, 16
; RV64IZBB-NEXT: ret
;
; RV64IZBS-LABEL: imm_50394234880:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT: lui a0, 188
; RV64IZBS-NEXT: addiw a0, a0, -1093
; RV64IZBS-NEXT: slli a0, a0, 16
; RV64IZBS-NEXT: ret
;
; RV64IXTHEADBB-LABEL: imm_50394234880:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT: lui a0, 188
; RV64IXTHEADBB-NEXT: addiw a0, a0, -1093
; RV64IXTHEADBB-NEXT: slli a0, a0, 16
; RV64IXTHEADBB-NEXT: ret
ret
i64 50394234880
}
```

```
define i64 @imm_12900936431479() {
```

```

; RV64I-LABEL: imm_12900936431479:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 192239
; RV64I-NEXT:  slli a0, a0, 2
; RV64I-NEXT:  addi a0, a0, -1093
; RV64I-NEXT:  slli a0, a0, 12
; RV64I-NEXT:  addi a0, a0, 1911
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_12900936431479:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 768956
; RV64IZBA-NEXT:  addi a0, a0, -1093
; RV64IZBA-NEXT:  slli.uw a0, a0, 12
; RV64IZBA-NEXT:  addi a0, a0, 1911
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_12900936431479:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 192239
; RV64IZBB-NEXT:  slli a0, a0, 2
; RV64IZBB-NEXT:  addi a0, a0, -1093
; RV64IZBB-NEXT:  slli a0, a0, 12
; RV64IZBB-NEXT:  addi a0, a0, 1911
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_12900936431479:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 192239
; RV64IZBS-NEXT:  slli a0, a0, 2
; RV64IZBS-NEXT:  addi a0, a0, -1093
; RV64IZBS-NEXT:
;     slli a0, a0, 12
; RV64IZBS-NEXT:  addi a0, a0, 1911
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_12900936431479:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 192239
; RV64IXTHEADBB-NEXT:  slli a0, a0, 2
; RV64IXTHEADBB-NEXT:  addi a0, a0, -1093
; RV64IXTHEADBB-NEXT:  slli a0, a0, 12
; RV64IXTHEADBB-NEXT:  addi a0, a0, 1911
; RV64IXTHEADBB-NEXT:  ret
ret i64 12900936431479
}

```

```

define i64 @imm_12900918536874() {

```

```

; RV64I-LABEL: imm_12900918536874:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 384477
; RV64I-NEXT:  addiw a0, a0, 1365
; RV64I-NEXT:  slli a0, a0, 12
; RV64I-NEXT:  addi a0, a0, 1365
; RV64I-NEXT:  slli a0, a0, 1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_12900918536874:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 768955
; RV64IZBA-NEXT:  addi a0, a0, -1365
; RV64IZBA-NEXT:  slli.uw a0, a0, 12
; RV64IZBA-NEXT:  addi a0, a0, -1366
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_12900918536874:
;
RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 384477
; RV64IZBB-NEXT:  addiw a0, a0, 1365
; RV64IZBB-NEXT:  slli a0, a0, 12
; RV64IZBB-NEXT:  addi a0, a0, 1365
; RV64IZBB-NEXT:  slli a0, a0, 1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_12900918536874:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 384477
; RV64IZBS-NEXT:  addiw a0, a0, 1365
; RV64IZBS-NEXT:  slli a0, a0, 12
; RV64IZBS-NEXT:  addi a0, a0, 1365
; RV64IZBS-NEXT:  slli a0, a0, 1
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_12900918536874:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 384477
; RV64IXTHEADBB-NEXT:  addiw a0, a0, 1365
; RV64IXTHEADBB-NEXT:  slli a0, a0, 12
; RV64IXTHEADBB-NEXT:  addi a0, a0, 1365
; RV64IXTHEADBB-NEXT:  slli a0, a0, 1
; RV64IXTHEADBB-NEXT:  ret
ret i64 12900918536874
}

```

```

define i64 @imm_12900925247761() {

```

```

; RV64I-LABEL: imm_12900925247761:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 384478
; RV64I-NEXT:  addiw
a0, a0, -1911
; RV64I-NEXT:  slli a0, a0, 13
; RV64I-NEXT:  addi a0, a0, -2048
; RV64I-NEXT:  addi a0, a0, -1775
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_12900925247761:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 768955
; RV64IZBA-NEXT:  addi a0, a0, 273
; RV64IZBA-NEXT:  slli.uw a0, a0, 12
; RV64IZBA-NEXT:  addi a0, a0, 273
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_12900925247761:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 384478
; RV64IZBB-NEXT:  addiw a0, a0, -1911
; RV64IZBB-NEXT:  slli a0, a0, 13
; RV64IZBB-NEXT:  addi a0, a0, -2048
; RV64IZBB-NEXT:  addi a0, a0, -1775
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_12900925247761:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 384478
; RV64IZBS-NEXT:  addiw a0, a0, -1911
; RV64IZBS-NEXT:  slli a0, a0, 13
; RV64IZBS-NEXT:  addi a0, a0, -2048
; RV64IZBS-NEXT:  addi a0, a0, -1775
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_12900925247761:
; RV64IXTHEADBB:
    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 384478
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -1911
; RV64IXTHEADBB-NEXT:  slli a0, a0, 13
; RV64IXTHEADBB-NEXT:  addi a0, a0, -2048
; RV64IXTHEADBB-NEXT:  addi a0, a0, -1775
; RV64IXTHEADBB-NEXT:  ret
ret i64 12900925247761
}

```

```

define i64 @imm_7158272001() {
; RV64I-LABEL: imm_7158272001:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 427
; RV64I-NEXT:  addiw a0, a0, -1367
; RV64I-NEXT:  slli a0, a0, 12
; RV64I-NEXT:  addi a0, a0, 1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_7158272001:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 349525
; RV64IZBA-NEXT:  sh2add a0, a0, a0
; RV64IZBA-NEXT:  addi a0, a0, 1
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_7158272001:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 427
; RV64IZBB-NEXT:  addiw a0, a0, -1367
; RV64IZBB-NEXT:  slli a0, a0, 12
; RV64IZBB-NEXT:  addi a0, a0, 1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_7158272001:
; RV64IZBS:
;   # %bb.0:
; RV64IZBS-NEXT:  lui a0, 427
; RV64IZBS-NEXT:  addiw a0, a0, -1367
; RV64IZBS-NEXT:  slli a0, a0, 12
; RV64IZBS-NEXT:  addi a0, a0, 1
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_7158272001:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 427
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -1367
; RV64IXTHEADBB-NEXT:  slli a0, a0, 12
; RV64IXTHEADBB-NEXT:  addi a0, a0, 1
; RV64IXTHEADBB-NEXT:  ret
ret i64 7158272001 ; 0x0000_0001_aaaa_9001
}

```

```

define i64 @imm_12884889601() {
; RV64I-LABEL: imm_12884889601:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 768
; RV64I-NEXT:  addiw a0, a0, -3

```

```

; RV64I-NEXT:  slli a0, a0, 12
; RV64I-NEXT:  addi a0, a0, 1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_12884889601:
; RV64IZBA:      # %bb.0:
; RV64IZBA-NEXT:  lui a0, 349525
; RV64IZBA-NEXT:  sh3add a0, a0, a0
; RV64IZBA-NEXT:  addi a0, a0, 1
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_12884889601:
; RV64IZBB:      # %bb.0:
; RV64IZBB-NEXT:
    lui a0, 768
; RV64IZBB-NEXT:  addiw a0, a0, -3
; RV64IZBB-NEXT:  slli a0, a0, 12
; RV64IZBB-NEXT:  addi a0, a0, 1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_12884889601:
; RV64IZBS:      # %bb.0:
; RV64IZBS-NEXT:  lui a0, 768
; RV64IZBS-NEXT:  addiw a0, a0, -3
; RV64IZBS-NEXT:  slli a0, a0, 12
; RV64IZBS-NEXT:  addi a0, a0, 1
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_12884889601:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 768
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -3
; RV64IXTHEADBB-NEXT:  slli a0, a0, 12
; RV64IXTHEADBB-NEXT:  addi a0, a0, 1
; RV64IXTHEADBB-NEXT:  ret
ret i64 12884889601 ; 0x0000_0002_ffff_d001
}

```

```

define i64 @imm_neg_3435982847() {
; RV64I-LABEL: imm_neg_3435982847:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a0, 1048371
; RV64I-NEXT:  addiw a0, a0, 817
; RV64I-NEXT:  slli a0, a0, 12
; RV64I-NEXT:  addi a0, a0, 1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_neg_3435982847:

```

```

; RV64IZBA:
; # %bb.0:
; RV64IZBA-NEXT: lui a0, 768955
; RV64IZBA-NEXT: sh1add a0, a0, a0
; RV64IZBA-NEXT: addi a0, a0, 1
; RV64IZBA-NEXT: ret
;
; RV64IZBB-LABEL: imm_neg_3435982847:
; RV64IZBB: # %bb.0:
; RV64IZBB-NEXT: lui a0, 1048371
; RV64IZBB-NEXT: addiw a0, a0, 817
; RV64IZBB-NEXT: slli a0, a0, 12
; RV64IZBB-NEXT: addi a0, a0, 1
; RV64IZBB-NEXT: ret
;
; RV64IZBS-LABEL: imm_neg_3435982847:
; RV64IZBS: # %bb.0:
; RV64IZBS-NEXT: lui a0, 734001
; RV64IZBS-NEXT: addiw a0, a0, 1
; RV64IZBS-NEXT: bclri a0, a0, 31
; RV64IZBS-NEXT: ret
;
; RV64IXTHEADBB-LABEL: imm_neg_3435982847:
; RV64IXTHEADBB: # %bb.0:
; RV64IXTHEADBB-NEXT: lui a0, 1048371
; RV64IXTHEADBB-NEXT: addiw a0, a0, 817
; RV64IXTHEADBB-NEXT: slli a0, a0, 12
; RV64IXTHEADBB-NEXT: addi a0, a0, 1
; RV64IXTHEADBB-NEXT: ret
ret i64 -3435982847 ; 0xffff_ffff_3333_1001
}

```

```

define i64 @imm_neg_5726842879() {
; RV64I-LABEL: imm_neg_5726842879:
; RV64I: # %bb.0:
; RV64I-NEXT:
    lui a0, 1048235
; RV64I-NEXT: addiw a0, a0, -1419
; RV64I-NEXT: slli a0, a0, 12
; RV64I-NEXT: addi a0, a0, 1
; RV64I-NEXT: ret
;
; RV64IZBA-LABEL: imm_neg_5726842879:
; RV64IZBA: # %bb.0:
; RV64IZBA-NEXT: lui a0, 768945
; RV64IZBA-NEXT: sh2add a0, a0, a0
; RV64IZBA-NEXT: addi a0, a0, 1
; RV64IZBA-NEXT: ret

```

```

;
; RV64IZBB-LABEL: imm_neg_5726842879:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 1048235
; RV64IZBB-NEXT:  addiw a0, a0, -1419
; RV64IZBB-NEXT:  slli a0, a0, 12
; RV64IZBB-NEXT:  addi a0, a0, 1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_neg_5726842879:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  lui a0, 698997
; RV64IZBS-NEXT:  addiw a0, a0, 1
; RV64IZBS-NEXT:  bclri a0, a0, 32
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm_neg_5726842879:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 1048235
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -1419
; RV64IXTHEADBB-NEXT:  slli a0, a0, 12
; RV64IXTHEADBB-NEXT:
;   addi a0, a0, 1
; RV64IXTHEADBB-NEXT:  ret
;   ret i64 -5726842879 ; 0xffff_fffe_aaa7_5001
}

```

```

define i64 @imm_neg_10307948543() {
; RV64I-LABEL: imm_neg_10307948543:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a0, 1047962
; RV64I-NEXT:  addiw a0, a0, -1645
; RV64I-NEXT:  slli a0, a0, 12
; RV64I-NEXT:  addi a0, a0, 1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm_neg_10307948543:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  lui a0, 768955
; RV64IZBA-NEXT:  sh3add a0, a0, a0
; RV64IZBA-NEXT:  addi a0, a0, 1
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm_neg_10307948543:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  lui a0, 1047962
; RV64IZBB-NEXT:  addiw a0, a0, -1645
; RV64IZBB-NEXT:  slli a0, a0, 12

```



```

; RV64IZBB-NEXT:  addi a0, a0, 1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm_neg_10307948543:
; RV64IZBS:      # %bb.0:
; RV64IZBS-NEXT:  lui a0, 629139
; RV64IZBS-NEXT:  addiw a0, a0, 1
; RV64IZBS-NEXT:  bclri a0, a0, 33
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL:
imm_neg_10307948543:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 1047962
; RV64IXTHEADBB-NEXT:  addiw a0, a0, -1645
; RV64IXTHEADBB-NEXT:  slli a0, a0, 12
; RV64IXTHEADBB-NEXT:  addi a0, a0, 1
; RV64IXTHEADBB-NEXT:  ret
ret i64 -10307948543 ; 0xffff_ffff_9999_3001
}

```

```

define i64 @li_ropi_1() {
; RV64I-LABEL: li_ropi_1:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a0, -17
; RV64I-NEXT:  slli a0, a0, 43
; RV64I-NEXT:  addi a0, a0, -1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: li_ropi_1:
; RV64IZBA:   # %bb.0:
; RV64IZBA-NEXT:  li a0, -17
; RV64IZBA-NEXT:  slli a0, a0, 43
; RV64IZBA-NEXT:  addi a0, a0, -1
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: li_ropi_1:
; RV64IZBB:   # %bb.0:
; RV64IZBB-NEXT:  li a0, -18
; RV64IZBB-NEXT:  rori a0, a0, 21
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: li_ropi_1:
; RV64IZBS:   # %bb.0:
; RV64IZBS-NEXT:  li a0, -17
; RV64IZBS-NEXT:  slli a0, a0, 43
; RV64IZBS-NEXT:  addi a0, a0,

```

```

-1
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: li_ropi_1:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  li a0, -18
; RV64IXTHEADBB-NEXT:  th.srri a0, a0, 21
; RV64IXTHEADBB-NEXT:  ret
ret i64 -149533581377537
}

```

```

define i64 @li_ropi_2() {
; RV64I-LABEL: li_ropi_2:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a0, -5
; RV64I-NEXT:  slli a0, a0, 60
; RV64I-NEXT:  addi a0, a0, -6
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: li_ropi_2:
; RV64IZBA:    # %bb.0:
; RV64IZBA-NEXT:  li a0, -5
; RV64IZBA-NEXT:  slli a0, a0, 60
; RV64IZBA-NEXT:  addi a0, a0, -6
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: li_ropi_2:
; RV64IZBB:    # %bb.0:
; RV64IZBB-NEXT:  li a0, -86
; RV64IZBB-NEXT:  rori a0, a0, 4
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: li_ropi_2:
; RV64IZBS:    # %bb.0:
; RV64IZBS-NEXT:  li a0, -5
; RV64IZBS-NEXT:  slli a0, a0, 60
; RV64IZBS-NEXT:  addi a0, a0, -6
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: li_ropi_2:
; RV64IXTHEADBB:
; # %bb.0:
; RV64IXTHEADBB-NEXT:  li a0, -86
; RV64IXTHEADBB-NEXT:  th.srri a0, a0, 4
; RV64IXTHEADBB-NEXT:  ret
ret i64 -5764607523034234886
}

```

```

define i64 @li_ori_3() {
; RV64I-LABEL: li_ori_3:
; RV64I:      # %bb.0:
; RV64I-NEXT: li a0, -17
; RV64I-NEXT: slli a0, a0, 27
; RV64I-NEXT: addi a0, a0, -1
; RV64I-NEXT: ret
;
; RV64IZBA-LABEL: li_ori_3:
; RV64IZBA:   # %bb.0:
; RV64IZBA-NEXT: li a0, -17
; RV64IZBA-NEXT: slli a0, a0, 27
; RV64IZBA-NEXT: addi a0, a0, -1
; RV64IZBA-NEXT: ret
;
; RV64IZBB-LABEL: li_ori_3:
; RV64IZBB:   # %bb.0:
; RV64IZBB-NEXT: li a0, -18
; RV64IZBB-NEXT: rori a0, a0, 37
; RV64IZBB-NEXT: ret
;
; RV64IZBS-LABEL: li_ori_3:
; RV64IZBS:   # %bb.0:
; RV64IZBS-NEXT: li a0, -17
; RV64IZBS-NEXT: slli a0, a0, 27
; RV64IZBS-NEXT: addi a0, a0, -1
; RV64IZBS-NEXT: ret
;
; RV64IXTHEADBB-LABEL: li_ori_3:
; RV64IXTHEADBB:   # %bb.0:
; RV64IXTHEADBB-NEXT: li a0, -18
; RV64IXTHEADBB-NEXT: th.srri a0,
a0, 37
; RV64IXTHEADBB-NEXT: ret
ret i64 -2281701377
}

```

; This used to assert when compiled with Zba.

```

define i64 @PR54812() {
; RV64I-LABEL: PR54812:
; RV64I:      # %bb.0:
; RV64I-NEXT: lui a0, 1048447
; RV64I-NEXT: addiw a0, a0, 1407
; RV64I-NEXT: slli a0, a0, 12
; RV64I-NEXT: ret
;
; RV64IZBA-LABEL: PR54812:
; RV64IZBA:   # %bb.0:

```

```

; RV64IZBA-NEXT:  lui a0, 872917
; RV64IZBA-NEXT:  sh1add a0, a0, a0
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: PR54812:
; RV64IZBB:      # %bb.0:
; RV64IZBB-NEXT:  lui a0, 1048447
; RV64IZBB-NEXT:  addiw a0, a0, 1407
; RV64IZBB-NEXT:  slli a0, a0, 12
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: PR54812:
; RV64IZBS:      # %bb.0:
; RV64IZBS-NEXT:  lui a0, 1045887
; RV64IZBS-NEXT:  bclri a0, a0, 31
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: PR54812:
; RV64IXTHEADBB:  # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 1048447
; RV64IXTHEADBB-NEXT:  addiw a0, a0, 1407
; RV64IXTHEADBB-NEXT:  slli a0, a0, 12
; RV64IXTHEADBB-NEXT:
    ret
ret i64 -2158497792;
}

```

```

define signext i32 @pos_2048() nounwind {

```

```

; RV64I-LABEL: pos_2048:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a0, 1
; RV64I-NEXT:  slli a0, a0, 11
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: pos_2048:
; RV64IZBA:      # %bb.0:
; RV64IZBA-NEXT:  li a0, 1
; RV64IZBA-NEXT:  slli a0, a0, 11
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: pos_2048:
; RV64IZBB:      # %bb.0:
; RV64IZBB-NEXT:  li a0, 1
; RV64IZBB-NEXT:  slli a0, a0, 11
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: pos_2048:
; RV64IZBS:      # %bb.0:

```

```

; RV64IZBS-NEXT:  bseti a0, zero, 11
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: pos_2048:
; RV64IXTHEADBB:   # %bb.0:
; RV64IXTHEADBB-NEXT:  li a0, 1
; RV64IXTHEADBB-NEXT:  slli a0, a0, 11
; RV64IXTHEADBB-NEXT:  ret
ret i32 2048
}

define i64 @imm64_same_lo_hi() nounwind {
; RV64I-LABEL: imm64_same_lo_hi:
; RV64I:   # %bb.0:
; RV64I-NEXT:  lui a0, 65793
; RV64I-NEXT:  addiw a0, a0, 16
; RV64I-NEXT:
slli a1, a0, 32
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64IZBA-LABEL: imm64_same_lo_hi:
; RV64IZBA:   # %bb.0:
; RV64IZBA-NEXT:  lui a0, 65793
; RV64IZBA-NEXT:  addiw a0, a0, 16
; RV64IZBA-NEXT:  slli a1, a0, 32
; RV64IZBA-NEXT:  add a0, a0, a1
; RV64IZBA-NEXT:  ret
;
; RV64IZBB-LABEL: imm64_same_lo_hi:
; RV64IZBB:   # %bb.0:
; RV64IZBB-NEXT:  lui a0, 65793
; RV64IZBB-NEXT:  addiw a0, a0, 16
; RV64IZBB-NEXT:  slli a1, a0, 32
; RV64IZBB-NEXT:  add a0, a0, a1
; RV64IZBB-NEXT:  ret
;
; RV64IZBS-LABEL: imm64_same_lo_hi:
; RV64IZBS:   # %bb.0:
; RV64IZBS-NEXT:  lui a0, 65793
; RV64IZBS-NEXT:  addiw a0, a0, 16
; RV64IZBS-NEXT:  slli a1, a0, 32
; RV64IZBS-NEXT:  add a0, a0, a1
; RV64IZBS-NEXT:  ret
;
; RV64IXTHEADBB-LABEL: imm64_same_lo_hi:
; RV64IXTHEADBB:   # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 65793

```

```

; RV64IXTHEADBB-NEXT: addiw a0, a0, 16
; RV64IXTHEADBB-NEXT: slli a1, a0, 32
; RV64IXTHEADBB-NEXT: add a0, a0, a1
;
RV64IXTHEADBB-NEXT: ret
ret i64 1157442765409226768 ; 0x0101010101010101
}

```

; Same as above with optsize. Make sure we use constant pool on RV64

```
define i64 @imm64_same_lo_hi_optsize() nounwind optsize {
```

```
; RV64-NOPOOL-LABEL: imm64_same_lo_hi_optsize:
```

```
; RV64-NOPOOL:    # %bb.0:
```

```
; RV64-NOPOOL-NEXT: lui a0, 65793
```

```
; RV64-NOPOOL-NEXT: addiw a0, a0, 16
```

```
; RV64-NOPOOL-NEXT: slli a1, a0, 32
```

```
; RV64-NOPOOL-NEXT: add a0, a0, a1
```

```
; RV64-NOPOOL-NEXT: ret
```

```
;
```

```
; RV64I-POOL-LABEL: imm64_same_lo_hi_optsize:
```

```
; RV64I-POOL:    # %bb.0:
```

```
; RV64I-POOL-NEXT: lui a0, %hi(.LCPI64_0)
```

```
; RV64I-POOL-NEXT: ld a0, %lo(.LCPI64_0)(a0)
```

```
; RV64I-POOL-NEXT: ret
```

```
;
```

```
; RV64IZBA-LABEL: imm64_same_lo_hi_optsize:
```

```
; RV64IZBA:    # %bb.0:
```

```
; RV64IZBA-NEXT: lui a0, 65793
```

```
; RV64IZBA-NEXT: addiw a0, a0, 16
```

```
; RV64IZBA-NEXT: slli a1, a0, 32
```

```
; RV64IZBA-NEXT: add a0, a0, a1
```

```
; RV64IZBA-NEXT: ret
```

```
;
```

```
; RV64IZBB-LABEL: imm64_same_lo_hi_optsize:
```

```
; RV64IZBB:    # %bb.0:
```

```
; RV64IZBB-NEXT: lui
```

```
a0, 65793
```

```
; RV64IZBB-NEXT: addiw a0, a0, 16
```

```
; RV64IZBB-NEXT: slli a1, a0, 32
```

```
; RV64IZBB-NEXT: add a0, a0, a1
```

```
; RV64IZBB-NEXT: ret
```

```
;
```

```
; RV64IZBS-LABEL: imm64_same_lo_hi_optsize:
```

```
; RV64IZBS:    # %bb.0:
```

```
; RV64IZBS-NEXT: lui a0, 65793
```

```
; RV64IZBS-NEXT: addiw a0, a0, 16
```

```
; RV64IZBS-NEXT: slli a1, a0, 32
```

```
; RV64IZBS-NEXT: add a0, a0, a1
```

```
; RV64IZBS-NEXT: ret
```

```

;
; RV64IXTHEADBB-LABEL: imm64_same_lo_hi_optsize:
; RV64IXTHEADBB:    # %bb.0:
; RV64IXTHEADBB-NEXT:  lui a0, 65793
; RV64IXTHEADBB-NEXT:  addiw a0, a0, 16
; RV64IXTHEADBB-NEXT:  slli a1, a0, 32
; RV64IXTHEADBB-NEXT:  add a0, a0, a1
; RV64IXTHEADBB-NEXT:  ret
ret i64 1157442765409226768 ; 0x0101010101010101
}
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -verify-machineinstrs < %s \
; RUN:  -riscv-experimental-rv64-legal-i32 | FileCheck -check-prefix=RV64I %s

```

; Check indexed and unindexed, sext, zext and anyext loads

```

define void @lb(ptr %a, ptr %b) nounwind {
; RV64I-LABEL: lb:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lb a2, 1(a0)
; RV64I-NEXT:  lbu zero, 0(a0)
; RV64I-NEXT:  sw a2, 0(a1)
; RV64I-NEXT:  ret
%1 = getelementptr i8, ptr %a, i32 1
%2 = load i8, ptr %1
%3 = sext i8 %2 to i32
; the unused load will produce an anyext for selection
%4 = load volatile i8, ptr %a
store i32 %3, ptr %b
ret void
}

```

```

define void @lbu(ptr %a, ptr %b) nounwind {
; RV64I-LABEL: lbu:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lbu a0, 1(a0)
; RV64I-NEXT:  sw a0, 0(a1)
; RV64I-NEXT:  ret
%1 = getelementptr i8, ptr %a, i32 1
%2 = load i8, ptr %1
%3 = zext i8 %2 to i32
store i32 %3, ptr %b
ret void
}

```

```

define void @lh(ptr
%a, ptr %b) nounwind {
; RV64I-LABEL: lh:

```

```

; RV64I:    # %bb.0:
; RV64I-NEXT:  lh a2, 2(a0)
; RV64I-NEXT:  lh zero, 0(a0)
; RV64I-NEXT:  sw a2, 0(a1)
; RV64I-NEXT:  ret
%1 = getelementptr i16, ptr %a, i32 1
%2 = load i16, ptr %1
%3 = sext i16 %2 to i32
; the unused load will produce an anyext for selection
%4 = load volatile i16, ptr %a
store i32 %3, ptr %b
ret void
}

```

```

define void @lhu(ptr %a, ptr %b) nounwind {
; RV64I-LABEL: lhu:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lhu a0, 2(a0)
; RV64I-NEXT:  sw a0, 0(a1)
; RV64I-NEXT:  ret
%1 = getelementptr i16, ptr %a, i32 1
%2 = load i16, ptr %1
%3 = zext i16 %2 to i32
store i32 %3, ptr %b
ret void
}

```

```

define void @lw(ptr %a, ptr %b) nounwind {
; RV64I-LABEL: lw:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lw a2, 4(a0)
; RV64I-NEXT:  lw zero, 0(a0)
; RV64I-NEXT:  sd a2, 0(a1)
; RV64I-NEXT:  ret
%1 = getelementptr i32, ptr %a, i64 1
%2 = load i32, ptr %1
%3 = sext i32 %2 to i64
; the unused load
will produce an anyext for selection
%4 = load volatile i32, ptr %a
store i64 %3, ptr %b
ret void
}

```

```

define void @lwu(ptr %a, ptr %b) nounwind {
; RV64I-LABEL: lwu:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lwu a0, 4(a0)

```



```

; RV64I-NEXT:  sd a0, 0(a1)
; RV64I-NEXT:  ret
%1 = getelementptr i32, ptr %a, i64 1
%2 = load i32, ptr %1
%3 = zext i32 %2 to i64
store i64 %3, ptr %b
ret void
}

```

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=====

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*/

; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit | FileCheck %s

--check-prefixes=CHECK,CHECK-SKX

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit,avx512vbmi |

FileCheck %s --check-prefixes=CHECK,CHECK-SKX,CHECK-SKX-VBMI

; Make sure CPUs default to prefer-256-bit. avx512vnni isn't interesting as it just adds an isel peephole for
vpmaddwd+vpadd

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 | FileCheck %s --check-
prefixes=CHECK,CHECK-AVX512

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cascadelake | FileCheck %s --
check-prefixes=CHECK,CHECK-AVX512

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cooperlake | FileCheck %s --

```

check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=cannonlake | FileCheck %s --check-
prefixes=CHECK,CHECK-VBMMI
;
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=icelake-client | FileCheck %s --
check-prefixes=CHECK,CHECK-VBMMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=icelake-server | FileCheck %s --
check-prefixes=CHECK,CHECK-VBMMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=tigerlake | FileCheck %s --check-
prefixes=CHECK,CHECK-VBMMI

```

; This file primarily contains tests for specific places in X86ISelLowering.cpp that needed be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

```

define dso_local void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-
width"="256" {
; CHECK-LABEL: add256:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpaddd 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:  vpaddd (%rsi), %ymm0, %ymm0
; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:
;               vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
; %d = load <16 x i32>, <16 x i32>* %a
; %e = load <16 x i32>, <16 x i32>* %b
; %f = add <16 x i32> %d, %e
; store <16 x i32> %f, <16 x i32>* %c
; ret void
}

```

```

define dso_local void @add512(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-
width"="512" {
; CHECK-LABEL: add512:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:  vpaddd (%rsi), %zmm0, %zmm0
; CHECK-NEXT:  vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
; %d = load <16 x i32>, <16 x i32>* %a
; %e = load <16 x i32>, <16 x i32>* %b
; %f = add <16 x i32> %d, %e
; store <16 x i32> %f, <16 x i32>* %c
; ret void

```


[illegible]

```
define dso_local void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="512" {
; CHECK-LABEL: pmaddwd_32_512:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:  vpmaddwd (%rsi), %zmm0, %zmm0
; CHECK-NEXT:  vmovdqa64 %zmm0, (%rdx)
```

```

; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%A = load <32 x i16>, <32 x i16>* %APtr
%B = load <32 x i16>, <32 x i16>* %BPtr
%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

```

```

define dso_local void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="256" {
; CHECK-LABEL: psubus_64i8_max_256:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpsubusb 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:  vpsubusb (%rsi), %ymm0, %ymm0
; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %yptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

```

```

define
dso_local void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="512" {
; CHECK-LABEL: psubus_64i8_max_512:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:  vpsubusb (%rsi), %zmm0, %zmm0
; CHECK-NEXT:  vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq

```

```

%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %yptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

```

```

define dso_local i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-
vector-width"="256" {

```

```

; CHECK-SKX-LABEL: _Z9test_charPcS_i_256:
; CHECK-SKX:      # %bb.0: # %entry
; CHECK-SKX-NEXT:  movl %edx, %eax
; CHECK-SKX-NEXT:  vpxor %xmm0, %xmm0, %xmm0
; CHECK-SKX-NEXT:  xorl %ecx, %ecx
; CHECK-SKX-NEXT:  vpxor %xmm1, %xmm1, %xmm1
;
; CHECK-SKX-NEXT:  vpxor %xmm2, %xmm2, %xmm2
; CHECK-SKX-NEXT:  .p2align 4, 0x90
; CHECK-SKX-NEXT:  .LBB8_1: # %vector.body
; CHECK-SKX-NEXT:  # =>This Inner Loop Header: Depth=1
; CHECK-SKX-NEXT:  vpmovsxbw 16(%rdi,%rcx), %ymm3
; CHECK-SKX-NEXT:  vpmovsxbw (%rdi,%rcx), %ymm4
; CHECK-SKX-NEXT:  vpmovsxbw 16(%rsi,%rcx), %ymm5
; CHECK-SKX-NEXT:  vpmaddwd %ymm3, %ymm5, %ymm3
; CHECK-SKX-NEXT:  vpadd %ymm2, %ymm3, %ymm2
; CHECK-SKX-NEXT:  vpmovsxbw (%rsi,%rcx), %ymm3
; CHECK-SKX-NEXT:  vpmaddwd %ymm4, %ymm3, %ymm3
; CHECK-SKX-NEXT:  vpadd %ymm1, %ymm3, %ymm1
; CHECK-SKX-NEXT:  addq $32, %rcx
; CHECK-SKX-NEXT:  cmpq %rcx, %rax
; CHECK-SKX-NEXT:  jne .LBB8_1
; CHECK-SKX-NEXT:  # %bb.2: # %middle.block
; CHECK-SKX-NEXT:  vpadd %ymm0, %ymm1, %ymm1
; CHECK-SKX-NEXT:  vpadd %ymm0, %ymm2, %ymm0
; CHECK-SKX-NEXT:  vpadd %ymm0, %ymm1, %ymm0
; CHECK-SKX-NEXT:  vextracti128 $1, %ymm0, %xmm1
; CHECK-SKX-NEXT:  vpadd %xmm1, %xmm0, %xmm0
; CHECK-SKX-NEXT:
;     vpslq $32, %xmm0, %xmm1
; CHECK-SKX-NEXT:  vpadd %xmm1, %xmm0, %xmm0
; CHECK-SKX-NEXT:  vpsrlq $32, %xmm0, %xmm1
; CHECK-SKX-NEXT:  vpadd %xmm1, %xmm0, %xmm0
; CHECK-SKX-NEXT:  vmovd %xmm0, %eax
; CHECK-SKX-NEXT:  vzeroupper
; CHECK-SKX-NEXT:  retq
;

```

```

; CHECK-AVX512-LABEL: _Z9test_charPcS_i_256:
; CHECK-AVX512:    # %bb.0: # %entry
; CHECK-AVX512-NEXT:    movl %edx, %eax
; CHECK-AVX512-NEXT:    vpxor %xmm0, %xmm0, %xmm0
; CHECK-AVX512-NEXT:    xorl %ecx, %ecx
; CHECK-AVX512-NEXT:    vpxor %xmm1, %xmm1, %xmm1
; CHECK-AVX512-NEXT:    vpxor %xmm2, %xmm2, %xmm2
; CHECK-AVX512-NEXT:    .p2align 4, 0x90
; CHECK-AVX512-NEXT:    .LBB8_1: # %vector.body
; CHECK-AVX512-NEXT:    # =>This Inner Loop Header: Depth=1
; CHECK-AVX512-NEXT:    vpmovsxbw 16(%rdi,%rcx), %ymm3
; CHECK-AVX512-NEXT:    vpmovsxbw (%rdi,%rcx), %ymm4
; CHECK-AVX512-NEXT:    vpmovsxbw 16(%rsi,%rcx), %ymm5
; CHECK-AVX512-NEXT:    vpmaddwd %ymm3, %ymm5, %ymm3
; CHECK-AVX512-NEXT:    vpaddd %ymm2, %ymm3,
%ymm2
; CHECK-AVX512-NEXT:    vpmovsxbw (%rsi,%rcx), %ymm3
; CHECK-AVX512-NEXT:    vpmaddwd %ymm4, %ymm3, %ymm3
; CHECK-AVX512-NEXT:    vpaddd %ymm1, %ymm3, %ymm1
; CHECK-AVX512-NEXT:    addq $32, %rcx
; CHECK-AVX512-NEXT:    cmpq %rcx, %rax
; CHECK-AVX512-NEXT:    jne .LBB8_1
; CHECK-AVX512-NEXT:    # %bb.2: # %middle.block
; CHECK-AVX512-NEXT:    vpaddd %ymm0, %ymm1, %ymm1
; CHECK-AVX512-NEXT:    vpaddd %ymm0, %ymm2, %ymm0
; CHECK-AVX512-NEXT:    vpaddd %ymm0, %ymm1, %ymm0
; CHECK-AVX512-NEXT:    vextracti128 $1, %ymm0, %xmm1
; CHECK-AVX512-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-AVX512-NEXT:    vpslq $32, %xmm0, %xmm1
; CHECK-AVX512-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-AVX512-NEXT:    vpsrlq $32, %xmm0, %xmm1
; CHECK-AVX512-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-AVX512-NEXT:    vmovd %xmm0, %eax
; CHECK-AVX512-NEXT:    vzeroupper
; CHECK-AVX512-NEXT:    retq
;
; CHECK-VBMI-LABEL: _Z9test_charPcS_i_256:
; CHECK-VBMI:    # %bb.0: # %entry
; CHECK-VBMI-NEXT:
    movl %edx, %eax
; CHECK-VBMI-NEXT:    vpxor %xmm0, %xmm0, %xmm0
; CHECK-VBMI-NEXT:    xorl %ecx, %ecx
; CHECK-VBMI-NEXT:    vpxor %xmm1, %xmm1, %xmm1
; CHECK-VBMI-NEXT:    vpxor %xmm2, %xmm2, %xmm2
; CHECK-VBMI-NEXT:    .p2align 4, 0x90
; CHECK-VBMI-NEXT:    .LBB8_1: # %vector.body
; CHECK-VBMI-NEXT:    # =>This Inner Loop Header: Depth=1
; CHECK-VBMI-NEXT:    vpmovsxbw 16(%rdi,%rcx), %ymm3

```



```

; CHECK-VBMI-NEXT: vpmovsxbw (%rdi,%rcx), %ymm4
; CHECK-VBMI-NEXT: vpmovsxbw 16(%rsi,%rcx), %ymm5
; CHECK-VBMI-NEXT: vpmaddwd %ymm3, %ymm5, %ymm3
; CHECK-VBMI-NEXT: vpadd %ymm2, %ymm3, %ymm2
; CHECK-VBMI-NEXT: vpmovsxbw (%rsi,%rcx), %ymm3
; CHECK-VBMI-NEXT: vpmaddwd %ymm4, %ymm3, %ymm3
; CHECK-VBMI-NEXT: vpadd %ymm1, %ymm3, %ymm1
; CHECK-VBMI-NEXT: addq $32, %rcx
; CHECK-VBMI-NEXT: cmpq %rcx, %rax
; CHECK-VBMI-NEXT: jne .LBB8_1
; CHECK-VBMI-NEXT: # %bb.2: # %middle.block
; CHECK-VBMI-NEXT: vpadd %ymm0, %ymm1, %ymm1
; CHECK-VBMI-NEXT: vpadd %ymm0, %ymm2,
%ymm0
; CHECK-VBMI-NEXT: vpadd %ymm0, %ymm1, %ymm0
; CHECK-VBMI-NEXT: vextracti128 $1, %ymm0, %xmm1
; CHECK-VBMI-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-VBMI-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[2,3,2,3]
; CHECK-VBMI-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-VBMI-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[1,1,1,1]
; CHECK-VBMI-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-VBMI-NEXT: vmovd %xmm0, %eax
; CHECK-VBMI-NEXT: vzeroupper
; CHECK-VBMI-NEXT: retq

```

entry:

%3 = zext i32 %2 to i64

br label %vector.body

vector.body:

```

%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x
i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body

```

middle.block:

%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,

```

i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef>
%bin.rdx1 = add <32 x i32> %i11, %rdx.shuf1
%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32
12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef>
%bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef>
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13
}

```

```

define dso_local i32 @_Z9test_charPcS_i_512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-
vector-width"="512" {
; CHECK-SKX-LABEL: _Z9test_charPcS_i_512:
; CHECK-SKX:      # %bb.0: # %entry
; CHECK-SKX-NEXT:  movl %edx, %eax
; CHECK-SKX-NEXT:  vpxor %xmm0, %xmm0, %xmm0
; CHECK-SKX-NEXT:  xorl %ecx,
%ecx
; CHECK-SKX-NEXT:  vpxor %xmm1, %xmm1, %xmm1
; CHECK-SKX-NEXT:  .p2align 4, 0x90
; CHECK-SKX-NEXT:  .LBB9_1: # %vector.body
; CHECK-SKX-NEXT:  # =>This Inner Loop Header: Depth=1
; CHECK-SKX-NEXT:  vpmovsxbw (%rdi,%rcx), %zmm2
; CHECK-SKX-NEXT:  vpmovsxbw (%rsi,%rcx), %zmm3
; CHECK-SKX-NEXT:  vpmaddwd %zmm2, %zmm3, %zmm2
; CHECK-SKX-NEXT:  vpaddq %zmm1, %zmm2, %zmm1
; CHECK-SKX-NEXT:  addq $32, %rcx
; CHECK-SKX-NEXT:  cmpq %rcx, %rax

```

```

; CHECK-SKX-NEXT:   jne .LBB9_1
; CHECK-SKX-NEXT:   # %bb.2: # %middle.block
; CHECK-SKX-NEXT:   vpaddd %zmm0, %zmm1, %zmm0
; CHECK-SKX-NEXT:   vextracti64x4 $1, %zmm0, %ymm1
; CHECK-SKX-NEXT:   vpaddd %zmm1, %zmm0, %zmm0
; CHECK-SKX-NEXT:   vextracti128 $1, %ymm0, %xmm1
; CHECK-SKX-NEXT:   vpaddd %xmm1, %xmm0, %xmm0
; CHECK-SKX-NEXT:   vpslufd {{.*#+}} xmm1 = xmm0[2,3,2,3]
; CHECK-SKX-NEXT:   vpaddd %xmm1, %xmm0, %xmm0
; CHECK-SKX-NEXT:   vpsrlq $32, %xmm0, %xmm1
; CHECK-SKX-NEXT:   vpaddd %xmm1, %xmm0, %xmm0
; CHECK-SKX-NEXT:
    vmovd %xmm0, %eax
; CHECK-SKX-NEXT:   vzeroupper
; CHECK-SKX-NEXT:   retq
;
; CHECK-AVX512-LABEL: _Z9test_charPcS_i_512:
; CHECK-AVX512:     # %bb.0: # %entry
; CHECK-AVX512-NEXT:   movl %edx, %eax
; CHECK-AVX512-NEXT:   vpxor %xmm0, %xmm0, %xmm0
; CHECK-AVX512-NEXT:   xorl %ecx, %ecx
; CHECK-AVX512-NEXT:   vpxor %xmm1, %xmm1, %xmm1
; CHECK-AVX512-NEXT:   .p2align 4, 0x90
; CHECK-AVX512-NEXT:   .LBB9_1: # %vector.body
; CHECK-AVX512-NEXT:   # =>This Inner Loop Header: Depth=1
; CHECK-AVX512-NEXT:   vpmovsxbw (%rdi,%rcx), %zmm2
; CHECK-AVX512-NEXT:   vpmovsxbw (%rsi,%rcx), %zmm3
; CHECK-AVX512-NEXT:   vpmaddwd %zmm2, %zmm3, %zmm2
; CHECK-AVX512-NEXT:   vpaddd %zmm1, %zmm2, %zmm1
; CHECK-AVX512-NEXT:   addq $32, %rcx
; CHECK-AVX512-NEXT:   cmpq %rcx, %rax
; CHECK-AVX512-NEXT:   jne .LBB9_1
; CHECK-AVX512-NEXT:   # %bb.2: # %middle.block
; CHECK-AVX512-NEXT:   vpaddd %zmm0, %zmm1, %zmm0
; CHECK-AVX512-NEXT:   vextracti64x4 $1, %zmm0, %ymm1
; CHECK-AVX512-NEXT:   vpaddd
    %zmm1, %zmm0, %zmm0
; CHECK-AVX512-NEXT:   vextracti128 $1, %ymm0, %xmm1
; CHECK-AVX512-NEXT:   vpaddd %xmm1, %xmm0, %xmm0
; CHECK-AVX512-NEXT:   vpslufd {{.*#+}} xmm1 = xmm0[2,3,2,3]
; CHECK-AVX512-NEXT:   vpaddd %xmm1, %xmm0, %xmm0
; CHECK-AVX512-NEXT:   vpsrlq $32, %xmm0, %xmm1
; CHECK-AVX512-NEXT:   vpaddd %xmm1, %xmm0, %xmm0
; CHECK-AVX512-NEXT:   vmovd %xmm0, %eax
; CHECK-AVX512-NEXT:   vzeroupper
; CHECK-AVX512-NEXT:   retq
;
; CHECK-VBMI-LABEL: _Z9test_charPcS_i_512:

```

```

; CHECK-VBMI:      # %bb.0: # %entry
; CHECK-VBMI-NEXT:  movl %edx, %eax
; CHECK-VBMI-NEXT:  vpxor %xmm0, %xmm0, %xmm0
; CHECK-VBMI-NEXT:  xorl %ecx, %ecx
; CHECK-VBMI-NEXT:  vpxor %xmm1, %xmm1, %xmm1
; CHECK-VBMI-NEXT:  .p2align 4, 0x90
; CHECK-VBMI-NEXT:  .LBB9_1: # %vector.body
; CHECK-VBMI-NEXT:  # =>This Inner Loop Header: Depth=1
; CHECK-VBMI-NEXT:  vpmovsxbw (%rdi,%rcx), %zmm2
; CHECK-VBMI-NEXT:  vpmovsxbw (%rsi,%rcx), %zmm3
; CHECK-VBMI-NEXT:  vpmaddwd %zmm2, %zmm3, %zmm2
;
; CHECK-VBMI-NEXT:  vpaddd %zmm1, %zmm2, %zmm1
; CHECK-VBMI-NEXT:  addq $32, %rcx
; CHECK-VBMI-NEXT:  cmpq %rcx, %rax
; CHECK-VBMI-NEXT:  jne .LBB9_1
; CHECK-VBMI-NEXT:  # %bb.2: # %middle.block
; CHECK-VBMI-NEXT:  vpaddd %zmm0, %zmm1, %zmm0
; CHECK-VBMI-NEXT:  vextracti64x4 $1, %zmm0, %ymm1
; CHECK-VBMI-NEXT:  vpaddd %zmm1, %zmm0, %zmm0
; CHECK-VBMI-NEXT:  vextracti128 $1, %ymm0, %xmm1
; CHECK-VBMI-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-VBMI-NEXT:  vpslufd {{.*#+}} xmm1 = xmm0[2,3,2,3]
; CHECK-VBMI-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-VBMI-NEXT:  vpslufd {{.*#+}} xmm1 = xmm0[1,1,1,1]
; CHECK-VBMI-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-VBMI-NEXT:  vmovd %xmm0, %eax
; CHECK-VBMI-NEXT:  vzeroupper
; CHECK-VBMI-NEXT:  retq
entry:
%3 = zext i32 %2 to i64
br label %vector.body

vector.body:
%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr
inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32

```

```
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body
```

middle.block:

```
%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,
i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef>
%bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32
12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef,
<32 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef>
%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13
}
```

```
@a = dso_local global [1024 x i8]
zeroinitializer, align 16
@b = dso_local global [1024 x i8] zeroinitializer, align 16
```

```
define dso_local i32 @sad_16i8_256() "min-legal-vector-width"="256" {
; CHECK-SKX-LABEL: sad_16i8_256:
; CHECK-SKX:      # %bb.0: # %entry
; CHECK-SKX-NEXT:  vpxor %xmm0, %xmm0, %xmm0
; CHECK-SKX-NEXT:  movq $-1024, %rax # imm = 0xFC00
; CHECK-SKX-NEXT:  vpxor %xmm1, %xmm1, %xmm1
; CHECK-SKX-NEXT:  .p2align 4, 0x90
; CHECK-SKX-NEXT:  .LBB10_1: # %vector.body
; CHECK-SKX-NEXT:  # =>This Inner Loop Header: Depth=1
; CHECK-SKX-NEXT:  vmovdqu a+1024(%rax), %xmm2
```

```

; CHECK-SKX-NEXT: vpsadbw b+1024(%rax), %xmm2, %xmm2
; CHECK-SKX-NEXT: vpadd %ymm1, %ymm2, %ymm1
; CHECK-SKX-NEXT: addq $4, %rax
; CHECK-SKX-NEXT: jne .LBB10_1
; CHECK-SKX-NEXT: # %bb.2: # %middle.block
; CHECK-SKX-NEXT: vpadd %ymm0, %ymm1, %ymm0
; CHECK-SKX-NEXT: vextracti128 $1, %ymm0, %xmm1
; CHECK-SKX-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-SKX-NEXT: vpslhd {{.*#+}} xmm1 = xmm0[2,3,2,3]
; CHECK-SKX-NEXT:
    vpadd %xmm1, %xmm0, %xmm0
; CHECK-SKX-NEXT: vpsrlq $32, %xmm0, %xmm1
; CHECK-SKX-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-SKX-NEXT: vmovd %xmm0, %eax
; CHECK-SKX-NEXT: vzeroupper
; CHECK-SKX-NEXT: retq
;
; CHECK-AVX512-LABEL: sad_16i8_256:
; CHECK-AVX512:    # %bb.0: # %entry
; CHECK-AVX512-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-AVX512-NEXT: movq $-1024, %rax # imm = 0xFC00
; CHECK-AVX512-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-AVX512-NEXT: .p2align 4, 0x90
; CHECK-AVX512-NEXT: .LBB10_1: # %vector.body
; CHECK-AVX512-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-AVX512-NEXT: vmovdqu a+1024(%rax), %xmm2
; CHECK-AVX512-NEXT: vpsadbw b+1024(%rax), %xmm2, %xmm2
; CHECK-AVX512-NEXT: vpadd %ymm1, %ymm2, %ymm1
; CHECK-AVX512-NEXT: addq $4, %rax
; CHECK-AVX512-NEXT: jne .LBB10_1
; CHECK-AVX512-NEXT: # %bb.2: # %middle.block
; CHECK-AVX512-NEXT: vpadd %ymm0, %ymm1, %ymm0
; CHECK-AVX512-NEXT: vextracti128 $1, %ymm0, %xmm1
;
    CHECK-AVX512-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-AVX512-NEXT: vpslhd {{.*#+}} xmm1 = xmm0[2,3,2,3]
; CHECK-AVX512-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-AVX512-NEXT: vpsrlq $32, %xmm0, %xmm1
; CHECK-AVX512-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-AVX512-NEXT: vmovd %xmm0, %eax
; CHECK-AVX512-NEXT: vzeroupper
; CHECK-AVX512-NEXT: retq
;
; CHECK-VBMI-LABEL: sad_16i8_256:
; CHECK-VBMI:    # %bb.0: # %entry
; CHECK-VBMI-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-VBMI-NEXT: movq $-1024, %rax # imm = 0xFC00
; CHECK-VBMI-NEXT: vpxor %xmm1, %xmm1, %xmm1

```

```

; CHECK-VBMI-NEXT: .p2align 4, 0x90
; CHECK-VBMI-NEXT: .LBB10_1: # %vector.body
; CHECK-VBMI-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-VBMI-NEXT: vmovdqu a+1024(%rax), %xmm2
; CHECK-VBMI-NEXT: vpsadbw b+1024(%rax), %xmm2, %xmm2
; CHECK-VBMI-NEXT: vpadd %ymm1, %ymm2, %ymm1
; CHECK-VBMI-NEXT: addq $4, %rax
; CHECK-VBMI-NEXT: jne .LBB10_1
; CHECK-VBMI-NEXT: # %bb.2: # %middle.block
;
CHECK-VBMI-NEXT: vpadd %ymm0, %ymm1, %ymm0
; CHECK-VBMI-NEXT: vextracti128 $1, %ymm0, %xmm1
; CHECK-VBMI-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-VBMI-NEXT: vpsltd {{.*#+}} xmm1 = xmm0[2,3,2,3]
; CHECK-VBMI-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-VBMI-NEXT: vpsltd {{.*#+}} xmm1 = xmm0[1,1,1,1]
; CHECK-VBMI-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-VBMI-NEXT: vmovd %xmm0, %eax
; CHECK-VBMI-NEXT: vzeroupper
; CHECK-VBMI-NEXT: retq
entry:
br label %vector.body

```

vector.body:

```

%index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
%vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
%0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
%1 = bitcast i8* %0 to <16 x i8>*
%wide.load = load <16 x i8>, <16 x i8>* %1, align 4
%2 = zext <16 x i8> %wide.load to <16 x i32>
%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
%4 = bitcast i8* %3 to <16 x i8>*
%wide.load1
= load <16 x i8>, <16 x i8>* %4, align 4
%5 = zext <16 x i8> %wide.load1 to <16 x i32>
%6 = sub nsw <16 x i32> %2, %5
%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
%8 = sub nsw <16 x i32> zeroinitializer, %6
%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

```

middle.block:

```

%rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>

```

```

%bin.rdx = add <16 x i32> %10, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

```

```

define dso_local i32 @sad_16i8_512() "min-legal-vector-width"="512" {
; CHECK-SKX-LABEL: sad_16i8_512:
; CHECK-SKX:      # %bb.0: # %entry
; CHECK-SKX-NEXT:  vpxor %xmm0, %xmm0, %xmm0
; CHECK-SKX-NEXT:
    movq $-1024, %rax # imm = 0xFC00
; CHECK-SKX-NEXT:  .p2align 4, 0x90
; CHECK-SKX-NEXT:  .LBB11_1: # %vector.body
; CHECK-SKX-NEXT:  # =>This Inner Loop Header: Depth=1
; CHECK-SKX-NEXT:  vmovdqu a+1024(%rax), %xmm1
; CHECK-SKX-NEXT:  vpsadbw b+1024(%rax), %xmm1, %xmm1
; CHECK-SKX-NEXT:  vpaddq %zmm0, %zmm1, %zmm0
; CHECK-SKX-NEXT:  addq $4, %rax
; CHECK-SKX-NEXT:  jne .LBB11_1
; CHECK-SKX-NEXT:  # %bb.2: # %middle.block
; CHECK-SKX-NEXT:  vextracti64x4 $1, %zmm0, %ymm1
; CHECK-SKX-NEXT:  vpaddq %zmm1, %zmm0, %zmm0
; CHECK-SKX-NEXT:  vextracti128 $1, %ymm0, %xmm1
; CHECK-SKX-NEXT:  vpaddq %xmm1, %xmm0, %xmm0
; CHECK-SKX-NEXT:  vpshufd {{.*#+}} xmm1 = xmm0[2,3,2,3]
; CHECK-SKX-NEXT:  vpaddq %xmm1, %xmm0, %xmm0
; CHECK-SKX-NEXT:  vpsrlq $32, %xmm0, %xmm1
; CHECK-SKX-NEXT:  vpaddq %xmm1, %xmm0, %xmm0
; CHECK-SKX-NEXT:  vmovd %xmm0, %eax
; CHECK-SKX-NEXT:  vzeroupper
; CHECK-SKX-NEXT:  retq
;
; CHECK-AVX512-LABEL: sad_16i8_512:
; CHECK-AVX512:
    # %bb.0: # %entry
; CHECK-AVX512-NEXT:  vpxor %xmm0, %xmm0, %xmm0

```



```

; CHECK-AVX512-NEXT:  movq $-1024, %rax # imm = 0xFC00
; CHECK-AVX512-NEXT:  .p2align 4, 0x90
; CHECK-AVX512-NEXT:  .LBB11_1: # %vector.body
; CHECK-AVX512-NEXT:  # =>This Inner Loop Header: Depth=1
; CHECK-AVX512-NEXT:  vmovdqu a+1024(%rax), %xmm1
; CHECK-AVX512-NEXT:  vpsadbw b+1024(%rax), %xmm1, %xmm1
; CHECK-AVX512-NEXT:  vpaddd %zmm0, %zmm1, %zmm0
; CHECK-AVX512-NEXT:  addq $4, %rax
; CHECK-AVX512-NEXT:  jne .LBB11_1
; CHECK-AVX512-NEXT:  # %bb.2: # %middle.block
; CHECK-AVX512-NEXT:  vextracti64x4 $1, %zmm0, %ymm1
; CHECK-AVX512-NEXT:  vpaddd %zmm1, %zmm0, %zmm0
; CHECK-AVX512-NEXT:  vextracti128 $1, %ymm0, %xmm1
; CHECK-AVX512-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-AVX512-NEXT:  vpslq $32, %xmm0, %xmm1
; CHECK-AVX512-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-AVX512-NEXT:
    vmovd %xmm0, %eax
; CHECK-AVX512-NEXT:  vzeroupper
; CHECK-AVX512-NEXT:  retq
;
; CHECK-VBMI-LABEL: sad_16i8_512:
; CHECK-VBMI:      # %bb.0: # %entry
; CHECK-VBMI-NEXT:  vpxor %xmm0, %xmm0, %xmm0
; CHECK-VBMI-NEXT:  movq $-1024, %rax # imm = 0xFC00
; CHECK-VBMI-NEXT:  .p2align 4, 0x90
; CHECK-VBMI-NEXT:  .LBB11_1: # %vector.body
; CHECK-VBMI-NEXT:  # =>This Inner Loop Header: Depth=1
; CHECK-VBMI-NEXT:  vmovdqu a+1024(%rax), %xmm1
; CHECK-VBMI-NEXT:  vpsadbw b+1024(%rax), %xmm1, %xmm1
; CHECK-VBMI-NEXT:  vpaddd %zmm0, %zmm1, %zmm0
; CHECK-VBMI-NEXT:  addq $4, %rax
; CHECK-VBMI-NEXT:  jne .LBB11_1
; CHECK-VBMI-NEXT:  # %bb.2: # %middle.block
; CHECK-VBMI-NEXT:  vextracti64x4 $1, %zmm0, %ymm1
; CHECK-VBMI-NEXT:  vpaddd %zmm1, %zmm0, %zmm0
; CHECK-VBMI-NEXT:  vextracti128 $1, %ymm0, %xmm1
; CHECK-VBMI-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-VBMI-NEXT:  vpslq $32, %xmm0, %xmm1
; CHECK-VBMI-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-VBMI-NEXT:
    vpslq $32, %xmm0, %xmm1
; CHECK-VBMI-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-VBMI-NEXT:  vmovd %xmm0, %eax
; CHECK-VBMI-NEXT:  vzeroupper
; CHECK-VBMI-NEXT:  retq

```

entry:

br label %vector.body

vector.body:

%index = phi i64 [0, %entry], [%index.next, %vector.body]

%vec.phi = phi <16 x i32> [zeroinitializer, %entry], [%10, %vector.body]

%0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index

%1 = bitcast i8* %0 to <16 x i8>*

%wide.load = load <16 x i8>, <16 x i8>* %1, align 4

%2 = zext <16 x i8> %wide.load to <16 x i32>

%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index

%4 = bitcast i8* %3 to <16 x i8>*

%wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4

%5 = zext <16 x i8> %wide.load1 to <16 x i32>

%6 = sub nsw <16 x i32> %2, %5

%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
-1, i32 -1>

%8 = sub nsw <16 x i32> zeroinitializer, %6

%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8

%10 = add nsw <16 x i32> %9, %vec.phi

%index.next = add i64 %index, 4

%11 = icmp eq i64 %index.next, 1024

br i1 %11, label %middle.block, label %vector.body

middle.block:

%rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>

%bin.rdx = add <16 x i32> %10, %rdx.shuf

%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>

%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2

%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>

%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3

%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>

%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4

%12 = extractelement <16 x i32> %bin.rdx4, i32 0

ret i32 %12

}

define dso_local void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {

; CHECK-LABEL: sbto16f32_256:

; CHECK: # %bb.0:

```

; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm1
; CHECK-NEXT: vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT: vmovaps %ymm1, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT:
    vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

```

```

define dso_local void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

```

```

define dso_local void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f64_256:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT:
    vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT: vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT: vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT: vmovaps %ymm3, (%rdi)

```

```

; CHECK-NEXT: vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT: vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

```

```

define dso_local void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f64_512:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm1
; CHECK-NEXT: vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT: vcvtdq2pd
               %ymm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT: vmovaps %zmm1, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

```

```

define dso_local void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f32_256:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT: vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm1
; CHECK-NEXT: vpsrld $31, %ymm1, %ymm1
; CHECK-NEXT: vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT: vmovaps %ymm1, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

```

```
}
```

```
define dso_local void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {  
; CHECK-LABEL: ubto16f32_512:  
; CHECK:      # %bb.0:  
; CHECK-NEXT: vpmovw2m %ymm0, %k0  
; CHECK-NEXT: vpmovm2d %k0, %zmm0  
; CHECK-NEXT: vpsrld $31, %zmm0, %zmm0  
; CHECK-NEXT: vcvtdq2ps %zmm0, %zmm0  
; CHECK-NEXT: vmovaps %zmm0, (%rdi)  
; CHECK-NEXT: vzeroupper  
; CHECK-NEXT: retq  
%mask = icmp slt <16 x i16> %a, zeroinitializer  
%1 = uitofp <16 x i1> %mask to <16 x float>  
store <16 x float> %1, <16 x float>* %res  
ret void  
}
```

```
define dso_local void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {  
; CHECK-LABEL: ubto16f64_256:  
; CHECK:      # %bb.0:  
; CHECK-NEXT: vpmovw2m %ymm0, %k0  
; CHECK-NEXT: kshiftrw $8, %k0, %k1  
; CHECK-NEXT: vpmovm2d %k1, %ymm0  
; CHECK-NEXT: vpsrld $31, %ymm0, %ymm0  
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm1  
; CHECK-NEXT: vextracti128  
$1, %ymm0, %xmm0  
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm0  
; CHECK-NEXT: vpmovm2d %k0, %ymm2  
; CHECK-NEXT: vpsrld $31, %ymm2, %ymm2  
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm3  
; CHECK-NEXT: vextracti128 $1, %ymm2, %xmm2  
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm2  
; CHECK-NEXT: vmovaps %ymm2, 32(%rdi)  
; CHECK-NEXT: vmovaps %ymm3, (%rdi)  
; CHECK-NEXT: vmovaps %ymm0, 96(%rdi)  
; CHECK-NEXT: vmovaps %ymm1, 64(%rdi)  
; CHECK-NEXT: vzeroupper  
; CHECK-NEXT: retq  
%mask = icmp slt <16 x i16> %a, zeroinitializer  
%1 = uitofp <16 x i1> %mask to <16 x double>  
store <16 x double> %1, <16 x double>* %res  
ret void  
}
```

```
define dso_local void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {  
; CHECK-LABEL: ubto16f64_512:
```

```

; CHECK:    # %bb.0:
; CHECK-NEXT:  vpmovw2m %ymm0, %k0
; CHECK-NEXT:  vpmovm2d %k0, %zmm0
; CHECK-NEXT:  vpsrld $31, %zmm0, %zmm0
; CHECK-NEXT:  vcvtdq2pd %ymm0, %zmm1
; CHECK-NEXT:  vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT:
    vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT:  vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:  vmovaps %zmm1, (%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

```

```

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="256" {

```

```

; CHECK-LABEL: test_16f32toub_256:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:  vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k0
; CHECK-NEXT:  vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT:  vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k1
; CHECK-NEXT:  kunpckbw %k0, %k1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru,
<16 x i16> zeroinitializer
ret <16 x i16> %select
}

```

```

define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="512" {

```

```

; CHECK-LABEL: test_16f32toub_512:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT:  vpslld $31, %zmm1, %zmm1
; CHECK-NEXT:  vpmovd2m %zmm1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr

```

```

%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

```

```

define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="256" {
; CHECK-LABEL: test_16f32tosb_256:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k0
; CHECK-NEXT:  vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k1
; CHECK-NEXT:  kunpckbw %k0, %k1, %k1
; CHECK-NEXT:
    vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

```

```

define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="512" {
; CHECK-LABEL: test_16f32tosb_512:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT:  vpmovd2m %zmm1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

```

```

define dso_local void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {
; CHECK-SKX-VBMI-LABEL: mul256:
; CHECK-SKX-VBMI:      # %bb.0:
; CHECK-SKX-VBMI-NEXT:  vmovdqa
    (%rdi), %ymm0
; CHECK-SKX-VBMI-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-SKX-VBMI-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-SKX-VBMI-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-SKX-VBMI-NEXT:  vpunpckhbw {{.*#+}} %ymm4 =
    ymm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-SKX-VBMI-NEXT:  vpunpckhbw {{.*#+}} %ymm5 =

```

```

ymm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-SKX-VBMI-NEXT:  vmullw %ymm4, %ymm5, %ymm4
; CHECK-SKX-VBMI-NEXT:  vpunpcklbw {{.*#+}} ymm3 =
ymm3[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-SKX-VBMI-NEXT:  vpunpcklbw {{.*#+}} ymm1 =
ymm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-SKX-VBMI-NEXT:  vmullw %ymm3, %ymm1, %ymm1
; CHECK-SKX-VBMI-NEXT:  vmovdqa {{.*#+}} ymm3 =
[0,2,4,6,8,10,12,14,32,34,36,38,40,42,44,46,16,18,20,22,24,26,28,30,48,50,52,54,56,58,60,62]
;
CHECK-SKX-VBMI-NEXT:  vpermt2b %ymm4, %ymm3, %ymm1
; CHECK-SKX-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm4 =
ymm2[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-SKX-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm5 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-SKX-VBMI-NEXT:  vmullw %ymm4, %ymm5, %ymm4
; CHECK-SKX-VBMI-NEXT:  vpunpcklbw {{.*#+}} ymm2 =
ymm2[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-SKX-VBMI-NEXT:  vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-SKX-VBMI-NEXT:  vmullw %ymm2, %ymm0, %ymm0
; CHECK-SKX-VBMI-NEXT:  vpermt2b %ymm4, %ymm3, %ymm0
; CHECK-SKX-VBMI-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-SKX-VBMI-NEXT:  vmovdqa %ymm1, 32(%rdx)
; CHECK-SKX-VBMI-NEXT:  vzeroupper
; CHECK-SKX-VBMI-NEXT:  retq
;
; CHECK-AVX512-LABEL: mul256:
; CHECK-AVX512:
    # %bb.0:
; CHECK-AVX512-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-AVX512-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-AVX512-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-AVX512-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} ymm4 =
ymm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} ymm5 =
ymm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT:  vmullw %ymm4, %ymm5, %ymm4
; CHECK-AVX512-NEXT:  vpbroadcastw {{.*#+}} ymm5 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255]
; CHECK-AVX512-NEXT:  vpand %ymm5, %ymm4, %ymm4
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} ymm3 =
ymm3[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} ymm1 =
ymm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
;

```



```

CHECK-AVX512-NEXT: vpmullw %ymm3, %ymm1, %ymm1
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm1, %ymm1
; CHECK-AVX512-NEXT: vpackuswb %ymm4, %ymm1, %ymm1
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm3 =
ymm2[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT: vpmullw %ymm3, %ymm4, %ymm3
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm3, %ymm3
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm2 =
ymm2[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT: vpmullw %ymm2, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vpackuswb %ymm3, %ymm0, %ymm0
; CHECK-AVX512-NEXT:
    vmovdqa %ymm0, (%rdx)
; CHECK-AVX512-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-AVX512-NEXT: vzeroupper
; CHECK-AVX512-NEXT: retq
;
; CHECK-VBMI-LABEL: mul256:
; CHECK-VBMI:    # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-VBMI-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-VBMI-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-VBMI-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm5 =
ymm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT: vpmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm3 =
ymm3[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm1 =
ymm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
;
CHECK-VBMI-NEXT: vpmullw %ymm3, %ymm1, %ymm1
; CHECK-VBMI-NEXT: vmovdqa {{.*#+}} ymm3 =
[0,2,4,6,8,10,12,14,32,34,36,38,40,42,44,46,16,18,20,22,24,26,28,30,48,50,52,54,56,58,60,62]
; CHECK-VBMI-NEXT: vpermt2b %ymm4, %ymm3, %ymm1
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm2[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm5 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT: vpmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm2 =

```

```

ymm2[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT:  vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT:  vpmullw %ymm2, %ymm0, %ymm0
; CHECK-VBMI-NEXT:  vpermt2b %ymm4, %ymm3, %ymm0
; CHECK-VBMI-NEXT:  vmovdqa %ymm0, (%rdx)
;
CHECK-VBMI-NEXT:  vmovdqa %ymm1, 32(%rdx)
; CHECK-VBMI-NEXT:  vzeroupper
; CHECK-VBMI-NEXT:  retq
%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void
}

define dso_local void @mul512(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="512" {
; CHECK-SKX-VBMI-LABEL: mul512:
; CHECK-SKX-VBMI:      # %bb.0:
; CHECK-SKX-VBMI-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-SKX-VBMI-NEXT:  vmovdqa64 (%rsi), %zmm1
; CHECK-SKX-VBMI-NEXT:  vpunpckhbw {{.*#+}} zmm2 =
zmm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-SKX-VBMI-NEXT:  vpunpckhbw {{.*#+}} zmm3 =
zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
;
CHECK-SKX-VBMI-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-SKX-VBMI-NEXT:  vpunpcklbw {{.*#+}} zmm1 =
zmm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-SKX-VBMI-NEXT:  vpunpcklbw {{.*#+}} zmm0 =
zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-SKX-VBMI-NEXT:  vpmullw %zmm1, %zmm0, %zmm0
; CHECK-SKX-VBMI-NEXT:  vmovdqa64 {{.*#+}} zmm1 =
[0,2,4,6,8,10,12,14,64,66,68,70,72,74,76,78,16,18,20,22,24,26,28,30,80,82,84,86,88,90,92,94,32,34,36,38,40,42,44,
46,96,98,100,102,104,106,108,110,48,50,52,54,56,58,60,62,112,114,116,118,120,122,124,126]
; CHECK-SKX-VBMI-NEXT:  vpermi2b %zmm2, %zmm0, %zmm1
; CHECK-SKX-VBMI-NEXT:  vmovdqa64 %zmm1, (%rdx)
; CHECK-SKX-VBMI-NEXT:  vzeroupper
;
CHECK-SKX-VBMI-NEXT:  retq
;
; CHECK-AVX512-LABEL: mul512:
; CHECK-AVX512:      # %bb.0:

```

```

; CHECK-AVX512-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-AVX512-NEXT: vmovdqa64 (%rsi), %zmm1
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} zmm2 =
zmm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} zmm3 =
zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT: vpmullw %zmm2, %zmm3, %zmm2
; CHECK-AVX512-NEXT: vpbroadcastw {{.*#+}} zmm3 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,2
55,255,255,255,255]
; CHECK-AVX512-NEXT: vpandq %zmm3, %zmm2, %zmm2
; CHECK-AVX512-NEXT: vpunpcklbw
{{.*#+}} zmm1 =
zmm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} zmm0 =
zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-AVX512-NEXT: vpmullw %zmm1, %zmm0, %zmm0
; CHECK-AVX512-NEXT: vpandq %zmm3, %zmm0, %zmm0
; CHECK-AVX512-NEXT: vpackuswb %zmm2, %zmm0, %zmm0
; CHECK-AVX512-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-AVX512-NEXT: vzeroupper
; CHECK-AVX512-NEXT: retq
;
; CHECK-VBMI-LABEL: mul512:
; CHECK-VBMI:    # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-VBMI-NEXT: vmovdqa64 (%rsi), %zmm1
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} zmm2 =
zmm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
;
CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} zmm3 =
zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT: vpmullw %zmm2, %zmm3, %zmm2
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} zmm1 =
zmm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} zmm0 =
zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-VBMI-NEXT: vpmullw %zmm1, %zmm0, %zmm0
; CHECK-VBMI-NEXT: vmovdqa64 {{.*#+}} zmm1 =
[0,2,4,6,8,10,12,14,64,66,68,70,72,74,76,78,16,18,20,22,24,26,28,30,80,82,84,86,88,90,92,94,32,34,36,38,40,42,44,

```

46,96,98,100,102,104,106,108,110,48,50,52,54,56,58,60,62,112,114,116,118,120,122,124,126]

```
;
CHECK-VBMI-NEXT:  vpermi2b %zmm2, %zmm0, %zmm1
; CHECK-VBMI-NEXT:  vmovdqa64 %zmm1, (%rdx)
; CHECK-VBMI-NEXT:  vzeroupper
; CHECK-VBMI-NEXT:  retq
%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void
}
```

; This threw an assertion at one point.

```
define <4 x i32> @mload_v4i32(<4 x i32> %trigger, <4 x i32>* %addr, <4 x i32> %dst) "min-legal-vector-
width"="256" {
; CHECK-LABEL: mload_v4i32:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vptestnmd %xmm0, %xmm0, %k1
; CHECK-NEXT:  vpblendmd (%rdi), %xmm1, %xmm0 {%k1}
; CHECK-NEXT:  retq
%mask = icmp eq <4 x i32> %trigger, zeroinitializer
%res = call <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* %addr, i32 4, <4 x i1> %mask, <4 x i32>
%dst)
ret <4 x i32> %res
}
declare <4 x i32>
@llvm.masked.load.v4i32.p0v4i32(<4 x i32>*, i32, <4 x i1>, <4 x i32>)
```

```
define <16 x i32> @trunc_v16i64_v16i32(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i64_v16i32:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vmovdqa 64(%rdi), %ymm2
; CHECK-NEXT:  vmovdqa 96(%rdi), %ymm3
; CHECK-NEXT:  vpmovqd %ymm0, %xmm0
; CHECK-NEXT:  vpmovqd %ymm1, %xmm1
; CHECK-NEXT:  vinserti128 $1, %xmm1, %ymm0, %ymm0
; CHECK-NEXT:  vpmovqd %ymm2, %xmm1
; CHECK-NEXT:  vpmovqd %ymm3, %xmm2
; CHECK-NEXT:  vinserti128 $1, %xmm2, %ymm1, %ymm1
; CHECK-NEXT:  retq
%a = load <16 x i64>, <16 x i64>* %x
%b = trunc <16 x i64> %a to <16 x i32>
ret <16 x i32> %b
}
```

```

define <16 x i8> @trunc_v16i64_v16i8(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i64_v16i8:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi),
;               %ymm1
; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
; CHECK-NEXT: vmovdqa 96(%rdi), %ymm3
; CHECK-NEXT: vpmovqb %ymm3, %xmm3
; CHECK-NEXT: vpmovqb %ymm2, %xmm2
; CHECK-NEXT: vpunpckldq { {. *#+} } xmm2 = xmm2[0],xmm3[0],xmm2[1],xmm3[1]
; CHECK-NEXT: vpmovqb %ymm1, %xmm1
; CHECK-NEXT: vpmovqb %ymm0, %xmm0
; CHECK-NEXT: vpunpckldq { {. *#+} } xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT: vpunpckldq { {. *#+} } xmm0 = xmm0[0],xmm2[0]
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
; %a = load <16 x i64>, <16 x i64>* %x
; %b = trunc <16 x i64> %a to <16 x i8>
ret <16 x i8> %b
}

```

```

define <16 x i8> @trunc_v16i32_v16i8(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i8:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmovdb %ymm1, %xmm1
; CHECK-NEXT: vpmovdb %ymm0, %xmm0
; CHECK-NEXT: vpunpckldq { {. *#+} } xmm0 = xmm0[0],xmm1[0]
; CHECK-NEXT: vzeroupper
;
; CHECK-NEXT: retq
; %a = load <16 x i32>, <16 x i32>* %x
; %b = trunc <16 x i32> %a to <16 x i8>
ret <16 x i8> %b
}

```

```

define <8 x i8> @trunc_v8i64_v8i8(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i8:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmovqb %ymm1, %xmm1
; CHECK-NEXT: vpmovqb %ymm0, %xmm0
; CHECK-NEXT: vpunpckldq { {. *#+} } xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq

```

```

%a = load <8 x i64>, <8 x i64>* %x
%b = trunc <8 x i64> %a to <8 x i8>
ret <8 x i8> %b
}

```

```

define <8 x i16> @trunc_v8i64_v8i16(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i16:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmovqw %ymm1, %xmm1
; CHECK-NEXT: vpmovqw %ymm0, %xmm0
; CHECK-NEXT: vpunpcklqdq {{.*#+}} xmm0
               = xmm0[0],xmm1[0]
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <8 x i64>, <8 x i64>* %x
%b = trunc <8 x i64> %a to <8 x i16>
ret <8 x i16> %b
}

```

```

define <8 x i32> @trunc_v8i64_v8i32_zeroes(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i32_zeroes:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpsrlq $48, 32(%rdi), %ymm0
; CHECK-NEXT: vpsrlq $48, (%rdi), %ymm1
; CHECK-NEXT: vpackusdw %ymm0, %ymm1, %ymm0
; CHECK-NEXT: vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT: retq
%a = load <8 x i64>, <8 x i64>* %x
%b = lshr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>
%c = trunc <8 x i64> %b to <8 x i32>
ret <8 x i32> %c
}

```

```

define <16 x i16> @trunc_v16i32_v16i16_zeroes(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i16_zeroes:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-NEXT: vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]
;
; CHECK-NEXT: vperm2w 32(%rdi), %ymm1, %ymm0
; CHECK-NEXT: retq
%a = load <16 x i32>, <16 x i32>* %x
%b = lshr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16>
%c = trunc <16 x i32> %b to <16 x i16>
ret <16 x i16> %c
}

```

```

}

define <32 x i8> @trunc_v32i16_v32i8_zeroes(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-SKX-VBMI-LABEL: trunc_v32i16_v32i8_zeroes:
; CHECK-SKX-VBMI:      # %bb.0:
; CHECK-SKX-VBMI-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-SKX-VBMI-NEXT: vmovdqa {{.*#+}} ymm0 =
[1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63]
; CHECK-SKX-VBMI-NEXT: vperm2b 32(%rdi), %ymm1, %ymm0
; CHECK-SKX-VBMI-NEXT: retq
;
; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_zeroes:
; CHECK-AVX512:      # %bb.0:
; CHECK-AVX512-NEXT: vpsrlw $8, 32(%rdi), %ymm0
; CHECK-AVX512-NEXT: vpsrlw $8, (%rdi),
%ymm1
; CHECK-AVX512-NEXT: vpackuswb %ymm0, %ymm1, %ymm0
; CHECK-AVX512-NEXT: vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-AVX512-NEXT: retq
;
; CHECK-VBMI-LABEL: trunc_v32i16_v32i8_zeroes:
; CHECK-VBMI:      # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-VBMI-NEXT: vmovdqa {{.*#+}} ymm0 =
[1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63]
; CHECK-VBMI-NEXT: vperm2b 32(%rdi), %ymm1, %ymm0
; CHECK-VBMI-NEXT: retq
%a = load <32 x i16>, <32 x i16>* %x
%b = lshr <32 x i16> %a, <i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8>
%c = trunc <32 x i16> %b to <32 x i8>
ret <32 x i8> %c
}

```

```

define <8 x i32> @trunc_v8i64_v8i32_sign(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i32_sign:
; CHECK:
# %bb.0:
; CHECK-NEXT: vpsraq $48, 32(%rdi), %ymm0
; CHECK-NEXT: vpsraq $48, (%rdi), %ymm1
; CHECK-NEXT: vpackssdw %ymm0, %ymm1, %ymm0
; CHECK-NEXT: vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT: retq
%a = load <8 x i64>, <8 x i64>* %x
%b = ashr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>
%c = trunc <8 x i64> %b to <8 x i32>
ret <8 x i32> %c
}

```

```

define <16 x i16> @trunc_v16i32_v16i16_sign(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i16_sign:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm1
; CHECK-NEXT:  vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]
; CHECK-NEXT:  vperm2w 32(%rdi), %ymm1, %ymm0
; CHECK-NEXT:  retq

%a = load <16 x i32>, <16 x i32>* %x
%b = ashr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16>
%c = trunc <16 x i32> %b to <16
x i16>
ret <16 x i16> %c
}

define <32 x i8> @trunc_v32i16_v32i8_sign(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-SKX-VBMI-LABEL: trunc_v32i16_v32i8_sign:
; CHECK-SKX-VBMI:      # %bb.0:
; CHECK-SKX-VBMI-NEXT:  vmovdqa (%rdi), %ymm1
; CHECK-SKX-VBMI-NEXT:  vmovdqa {{.*#+}} ymm0 =
[1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63]
; CHECK-SKX-VBMI-NEXT:  vperm2b 32(%rdi), %ymm1, %ymm0
; CHECK-SKX-VBMI-NEXT:  retq
;
; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_sign:
; CHECK-AVX512:      # %bb.0:
; CHECK-AVX512-NEXT:  vpsrlw $8, 32(%rdi), %ymm0
; CHECK-AVX512-NEXT:  vpsrlw $8, (%rdi), %ymm1
; CHECK-AVX512-NEXT:  vpackuswb %ymm0, %ymm1, %ymm0
; CHECK-AVX512-NEXT:  vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-AVX512-NEXT:  retq
;
; CHECK-VBMI-LABEL: trunc_v32i16_v32i8_sign:
; CHECK-VBMI:      # %bb.0:
; CHECK-VBMI-NEXT:  vmovdqa (%rdi), %ymm1
; CHECK-VBMI-NEXT:  vmovdqa {{.*#+}} ymm0 =
[1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63]
;
CHECK-VBMI-NEXT:  vperm2b 32(%rdi), %ymm1, %ymm0
; CHECK-VBMI-NEXT:  retq

%a = load <32 x i16>, <32 x i16>* %x
%b = ashr <32 x i16> %a, <i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8>
%c = trunc <32 x i16> %b to <32 x i8>
ret <32 x i8> %c
}

```



```

define dso_local void @zext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-
width"="256" {
; CHECK-LABEL: zext_v16i8_v16i64:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vpmovzxbw {{.*#+}} ymm1 =
xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zer
o,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xm
m0[15],zero
; CHECK-NEXT:  vpshufd {{.*#+}} xmm2 = xmm1[2,3,2,3]
; CHECK-NEXT:
    vpmovzxwq {{.*#+}} ymm2 =
xmm2[0],zero,zero,zero,xmm2[1],zero,zero,zero,xmm2[2],zero,zero,zero,xmm2[3],zero,zero,zero
; CHECK-NEXT:  vextracti128 $1, %ymm1, %xmm1
; CHECK-NEXT:  vpshufd {{.*#+}} xmm3 = xmm1[2,3,2,3]
; CHECK-NEXT:  vpmovzxwq {{.*#+}} ymm3 =
xmm3[0],zero,zero,zero,xmm3[1],zero,zero,zero,xmm3[2],zero,zero,zero,xmm3[3],zero,zero,zero
; CHECK-NEXT:  vpmovzxwq {{.*#+}} ymm1 =
xmm1[0],zero,zero,zero,xmm1[1],zero,zero,zero,xmm1[2],zero,zero,zero,xmm1[3],zero,zero,zero
; CHECK-NEXT:  vpmovzxbq {{.*#+}} ymm0 =
xmm0[0],zero,zero,zero,zero,zero,zero,zero,xmm0[1],zero,zero,zero,zero,zero,zero,zero,xmm0[2],zero,zero,zero,zer
o,zero,zero,zero,xmm0[3],zero,zero,zero,zero,zero,zero,zero,zero,zero,zero
; CHECK-NEXT:  vmovdqa %ymm0, (%rdi)
; CHECK-NEXT:  vmovdqa %ymm1, 64(%rdi)
; CHECK-NEXT:  vmovdqa %ymm3, 96(%rdi)
; CHECK-NEXT:  vmovdqa %ymm2, 32(%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
    %a = zext <16 x i8> %x to <16 x i64>
    store <16 x i64> %a, <16 x i64>*
    %y
    ret void
}

```

```

define dso_local void @sext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-
width"="256" {
; CHECK-LABEL: sext_v16i8_v16i64:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vpmovsxbw %xmm0, %ymm1
; CHECK-NEXT:  vpshufd {{.*#+}} xmm2 = xmm1[2,3,2,3]
; CHECK-NEXT:  vpmovswwq %xmm2, %ymm2
; CHECK-NEXT:  vextracti128 $1, %ymm1, %xmm1
; CHECK-NEXT:  vpshufd {{.*#+}} xmm3 = xmm1[2,3,2,3]
; CHECK-NEXT:  vpmovswwq %xmm3, %ymm3
; CHECK-NEXT:  vpmovswwq %xmm1, %ymm1
; CHECK-NEXT:  vpmovsxbq %xmm0, %ymm0
; CHECK-NEXT:  vmovdqa %ymm0, (%rdi)
; CHECK-NEXT:  vmovdqa %ymm1, 64(%rdi)
; CHECK-NEXT:  vmovdqa %ymm3, 96(%rdi)

```

```
; CHECK-NEXT: vmovdqa %ymm2, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = sext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}
```

```
define dso_local void @vselect_split_v8i16_setcc(<8 x i16> %s, <8 x i16> %t, <8 x i64>* %p, <8 x i64>* %q, <8
x i64>* %r) "min-legal-vector-width"="256"
{
; CHECK-LABEL: vselect_split_v8i16_setcc:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqw %xmm1, %xmm0, %k1
; CHECK-NEXT: kshiftrb $4, %k1, %k2
; CHECK-NEXT: vmovdqa64 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
%a = icmp eq <8 x i16> %s, %t
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}
```

```
define dso_local void @vselect_split_v8i32_setcc(<8 x i32> %s, <8 x i32> %t, <8 x i64>* %p, <8 x i64>* %q, <8
x i64>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v8i32_setcc:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqd %ymm1,
%ymm0, %k1
; CHECK-NEXT: kshiftrb $4, %k1, %k2
; CHECK-NEXT: vmovdqa64 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
```

```

%a = icmp eq <8 x i32> %s, %t
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}

```

```

define dso_local void @vselect_split_v16i8_setcc(<16 x i8> %s, <16 x i8> %t, <16 x i32>* %p, <16 x i32>* %q,
<16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i8_setcc:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqb %xmm1, %xmm0, %k1
; CHECK-NEXT: kshiftrw $8, %k1, %k2
; CHECK-NEXT: vmovdqa32 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa32 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2,
(%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <16 x i32>, <16 x i32>* %p
%y = load <16 x i32>, <16 x i32>* %q
%a = icmp eq <16 x i8> %s, %t
%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
store <16 x i32> %b, <16 x i32>* %r
ret void
}

```

```

define dso_local void @vselect_split_v16i16_setcc(<16 x i16> %s, <16 x i16> %t, <16 x i32>* %p, <16 x i32>*
%q, <16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i16_setcc:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqw %ymm1, %ymm0, %k1
; CHECK-NEXT: kshiftrw $8, %k1, %k2
; CHECK-NEXT: vmovdqa32 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa32 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <16 x i32>, <16 x i32>* %p
%y = load <16 x i32>,
<16 x i32>* %q
%a = icmp eq <16 x i16> %s, %t
%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y

```

```

store <16 x i32> %b, <16 x i32>* %r
ret void
}

define <16 x i8> @trunc_packus_v16i32_v16i8(<16 x i32>* %p) "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_packus_v16i32_v16i8:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vpackusdw 32(%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT: vpmovuswb %ymm0, %xmm0
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <16 x i32>, <16 x i32>* %p
%b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%d = icmp sgt <16 x i32> %c, zeroinitializer
%e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zeroinitializer
%f = trunc <16 x i32> %e to <16 x i8>
ret <16 x i8> %f
}

define dso_local void @trunc_packus_v16i32_v16i8_store(<16 x i32>* %p, <16 x i8>* %q) "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_packus_v16i32_v16i8_store:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vpackusdw 32(%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT: vpmovuswb %ymm0, (%rsi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <16 x i32>, <16 x i32>* %p
%b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%d = icmp sgt <16 x i32> %c, zeroinitializer
%e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zeroinitializer
%f = trunc <16 x i32> %e to <16 x i8>
store <16 x i8> %f, <16 x i8>* %q
ret void
}

define <64 x i1> @v64i1_argument_return(<64 x i1> %x) "min-legal-vector-width"="256" {

```

```

; CHECK-LABEL: v64i1_argument_return:
; CHECK:      # %bb.0:
; CHECK-NEXT:  retq
ret <64 x i1> %x
}

```

```

define dso_local void @v64i1_shuffle(<64 x i8>* %x, <64 x i8>* %y) "min-legal-vector-width"="256" {

```

```

; CHECK-LABEL: v64i1_shuffle:
; CHECK:      # %bb.0: # %entry
; CHECK-NEXT:  vmovdqa (%rdi), %ymm1
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm0
; CHECK-NEXT:  vptestnmb %ymm1, %ymm1, %k0
; CHECK-NEXT:  kshiftrd $1, %k0, %k1
; CHECK-NEXT:  kshiftrlq $63, %k0, %k2
; CHECK-NEXT:  kshiftrq $62, %k2, %k2
; CHECK-NEXT:  kshiftrlq $63, %k1, %k1
; CHECK-NEXT:  kshiftrq $63, %k1, %k1
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-5, %rax
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1,
%k1
; CHECK-NEXT:  kshiftrd $3, %k0, %k2
; CHECK-NEXT:  kshiftrlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $61, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-9, %rax
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $2, %k0, %k2
; CHECK-NEXT:  kshiftrlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $60, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-17, %rax
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $5, %k0, %k2
; CHECK-NEXT:  kshiftrlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $59, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-33, %rax
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1
; CHECK-NEXT:  kshiftrd $4, %k0, %k2
; CHECK-NEXT:  kshiftrlq $63, %k2, %k2
; CHECK-NEXT:  kshiftrq $58, %k2, %k2
; CHECK-NEXT:  korq %k2, %k1, %k1
; CHECK-NEXT:  movq $-65, %rax

```

```

; CHECK-NEXT:    kmovq %rax, %k2
;
CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $7, %k0, %k2
; CHECK-NEXT:    kshiftrlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $57, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-129, %rax
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $6, %k0, %k2
; CHECK-NEXT:    kshiftrlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $56, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-257, %rax # imm = 0xFEFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $9, %k0, %k2
; CHECK-NEXT:    kshiftrlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $55, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-513, %rax # imm = 0xFDFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $8, %k0, %k2
; CHECK-NEXT:    kshiftrlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $54, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
;
CHECK-NEXT:    movq $-1025, %rax # imm = 0xFBFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $11, %k0, %k2
; CHECK-NEXT:    kshiftrlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $53, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-2049, %rax # imm = 0xF7FF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $10, %k0, %k2
; CHECK-NEXT:    kshiftrlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $52, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-4097, %rax # imm = 0xEFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $13, %k0, %k2
; CHECK-NEXT:    kshiftrlq $63, %k2, %k2

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```

; CHECK-NEXT: kshiftrq $51, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-8193, %rax # imm = 0xDFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $12, %k0, %k2
; CHECK-NEXT:
    kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $50, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-16385, %rax # imm = 0xBFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $15, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $49, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-32769, %rax # imm = 0xFFFF7FFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $14, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $48, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-65537, %rax # imm = 0xFFFFEFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $17, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $47, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-131073, %rax # imm = 0xFFFFDFFFF
;
CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $16, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $46, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-262145, %rax # imm = 0xFFFFBFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $19, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $45, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-524289, %rax # imm = 0xFFFF7FFFF
; CHECK-NEXT: kmovq %rax, %k2

```

```

; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $18, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $44, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-1048577, %rax # imm = 0xFFEFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $21, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT:
    kshiftrq $43, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-2097153, %rax # imm = 0xFFDFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $20, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $42, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-4194305, %rax # imm = 0xFFBFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $23, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $41, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-8388609, %rax # imm = 0xFF7FFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $22, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $40, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-16777217, %rax # imm = 0xFEFFFFFFF
; CHECK-NEXT: kmovq
    %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $25, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $39, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-33554433, %rax # imm = 0xFDFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $24, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $38, %k2, %k2

```



```

; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-67108865, %rax # imm = 0xFBFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $27, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $37, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-134217729, %rax # imm = 0xF7FFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $26, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq
$36, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-268435457, %rax # imm = 0xEFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $29, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $35, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-536870913, %rax # imm = 0xDFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $28, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $34, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-1073741825, %rax # imm = 0xBFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $31, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $33, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movabsq $-2147483649, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT:
kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k2
; CHECK-NEXT: vptestnmb %ymm0, %ymm0, %k1
; CHECK-NEXT: kshiftrd $30, %k0, %k0
; CHECK-NEXT: kshiftrlq $63, %k0, %k0
; CHECK-NEXT: kshiftrq $32, %k0, %k0
; CHECK-NEXT: korq %k0, %k2, %k0
; CHECK-NEXT: movabsq $-4294967297, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2

```

```

; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $1, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $31, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-8589934593, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrlq $63, %k1, %k2
; CHECK-NEXT: kshiftrq $30, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-17179869185, %rax # imm = 0xFFFFFFFFBFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $3, %k1, %k2
; CHECK-NEXT:
    kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $29, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-34359738369, %rax # imm = 0xFFFFFFFF7FFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $2, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $28, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-68719476737, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $5, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $27, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-137438953473, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $4, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $26, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
;
CHECK-NEXT: movabsq $-274877906945, %rax # imm = 0xFFFFFFFFBFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $7, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $25, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0

```

```

; CHECK-NEXT: movabsq $-549755813889, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $6, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $24, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-1099511627777, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $9, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $23, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-2199023255553, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
;
CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $8, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $22, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-4398046511105, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $11, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $21, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-8796093022209, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $10, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $20, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-17592186044417, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $13, %k1, %k2
; CHECK-NEXT: kshiftrlq
$63, %k2, %k2
; CHECK-NEXT: kshiftrq $19, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-35184372088833, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $12, %k1, %k2

```

```

; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $18, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-70368744177665, %rax # imm = 0xFFFFBFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $15, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $17, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-140737488355329, %rax # imm = 0xFFFF7FFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $14, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $16, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT:
    movabsq $-281474976710657, %rax # imm = 0xFFFEFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $17, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $15, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-562949953421313, %rax # imm = 0xFFFDFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $16, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $14, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-1125899906842625, %rax # imm = 0xFFFBFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $19, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $13, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-2251799813685249, %rax # imm = 0xFFF7FFFFFFFFFFFFF
; CHECK-NEXT: kmovq
    %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $18, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $12, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-4503599627370497, %rax # imm = 0xFFEFFFFFFFFFFFFF

```

```

; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $21, %k1, %k2
; CHECK-NEXT:    kshiftrlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $11, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-9007199254740993, %rax # imm = 0xFFDFFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $20, %k1, %k2
; CHECK-NEXT:    kshiftrlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $10, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-18014398509481985, %rax # imm = 0xFFBFFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $23, %k1, %k2
;
CHECK-NEXT:    kshiftrlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $9, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-36028797018963969, %rax # imm = 0xFF7FFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $22, %k1, %k2
; CHECK-NEXT:    kshiftrlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $8, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-72057594037927937, %rax # imm = 0xFEFFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $25, %k1, %k2
; CHECK-NEXT:    kshiftrlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $7, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-144115188075855873, %rax # imm = 0xFDFFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $24, %k1, %k2
; CHECK-NEXT:    kshiftrlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $6, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-288230376151711745, %rax # imm = 0xFBFFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $27, %k1, %k2
; CHECK-NEXT:    kshiftrlq $63, %k2, %k2

```

```

; CHECK-NEXT: kshiftrq $5, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-576460752303423489, %rax # imm = 0xF7FFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $26, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $4, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-1152921504606846977, %rax # imm = 0xEFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $29, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $3, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-2305843009213693953, %rax # imm =
0xDFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $28, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $2, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-4611686018427387905, %rax # imm = 0xBFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $31, %k1, %k2
; CHECK-NEXT: kshiftrlq $62, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $30, %k1, %k1
; CHECK-NEXT: kshiftrlq $1, %k0, %k0
; CHECK-NEXT: kshiftrq $1, %k0, %k0
; CHECK-NEXT: kshiftrlq $63, %k1, %k1
; CHECK-NEXT: korq %k1, %k0, %k1
; CHECK-NEXT: vmovdqu8 %ymm1, (%rsi) {%k1}
; CHECK-NEXT: kshiftrq $32, %k1, %k1
; CHECK-NEXT: vmovdqu8 %ymm0, 32(%rsi) {%k1}
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
entry:
%a = load <64 x i8>, <64 x i8>* %x
%b = icmp eq <64 x i8> %a, zeroinitializer
%shuf = shufflevector
<64 x i1> %b, <64 x i1> undef, <64 x i32> <i32 1, i32 0, i32 3, i32 2, i32 5, i32 4, i32 7, i32 6, i32 9, i32 8, i32 11,
i32 10, i32 13, i32 12, i32 15, i32 14, i32 17, i32 16, i32 19, i32 18, i32 21, i32 20, i32 23, i32 22, i32 25, i32 24, i32
27, i32 26, i32 29, i32 28, i32 31, i32 30, i32 33, i32 32, i32 35, i32 34, i32 37, i32 36, i32 39, i32 38, i32 41, i32 40,
i32 43, i32 42, i32 45, i32 44, i32 47, i32 46, i32 49, i32 48, i32 51, i32 50, i32 53, i32 52, i32 55, i32 54, i32 57, i32

```

```

56, i32 59, i32 58, i32 61, i32 60, i32 63, i32 62>
call void @llvm.masked.store.v64i8.p0v64i8(<64 x i8> %a, <64 x i8>* %y, i32 1, <64 x i1> %shuf)
ret void
}
declare void @llvm.masked.store.v64i8.p0v64i8(<64 x i8>, <64 x i8>*, i32, <64 x i1>)

@mem64_dst = dso_local global i64 0, align 8
@mem64_src = dso_local global i64 0, align 8
define dso_local i32 @v64i1_inline_asm() "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_inline_asm:
; CHECK:      # %bb.0:
; CHECK-NEXT:  kmovq mem64_src(%rip),
%k0
; CHECK-NEXT:  #APP
; CHECK-NEXT:  #NO_APP
; CHECK-NEXT:  kmovq %k0, mem64_dst(%rip)
; CHECK-NEXT:  movl -{[0-9]+}}(%rsp), %eax
; CHECK-NEXT:  retq
%1 = alloca i32, align 4
%2 = load i64, i64* @mem64_src, align 8
%3 = call i64 @asm "", "=k,k,~{dirflag},~{fpsr},~{flags}"(i64 %2)
store i64 %3, i64* @mem64_dst, align 8
%4 = load i32, i32* %1, align 4
ret i32 %4
}

define dso_local void @cmp_v8i64_sext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-
vector-width"="256" {
; CHECK-LABEL: cmp_v8i64_sext:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa (%rsi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT:  vpcmpgtq 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT:  vpcmpgtq (%rdi), %ymm0, %ymm0
; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%x = load <8 x i64>, <8 x i64>* %xptr
%y = load <8 x i64>, <8 x i64>* %yptr
%cmp = icmp slt <8 x i64> %x, %y
%ext
= sext <8 x i1> %cmp to <8 x i64>
store <8 x i64> %ext, <8 x i64>* %zptr
ret void
}

define dso_local void @cmp_v8i64_zext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-

```

```

vector-width"="256" {
; CHECK-LABEL: cmp_v8i64_zext:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT: vpcmpgtq 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT: vpcmpgtq (%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpsrlq $63, %ymm1, %ymm1
; CHECK-NEXT: vpsrlq $63, %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %xptr
%y = load <8 x i64>, <8 x i64>* %yptr
%cmp = icmp slt <8 x i64> %x, %y
%ext = zext <8 x i1> %cmp to <8 x i64>
store <8 x i64> %ext, <8 x i64>* %zptr
ret void
}

define <16 x i8> @var_rotate_v16i8(<16 x i8> %a, <16 x i8> %b) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: var_rotate_v16i8:
;
; CHECK:      # %bb.0:
; CHECK-NEXT: vpandd {{\.?LCPI[0-9]+_[0-9]+}}(%rip){1to4}, %xmm1, %xmm1
; CHECK-NEXT: vpxor %xmm2, %xmm2, %xmm2
; CHECK-NEXT: vpunpckhbw {{\.*#+}} %xmm2 =
xmm1[8],xmm2[8],xmm1[9],xmm2[9],xmm1[10],xmm2[10],xmm1[11],xmm2[11],xmm1[12],xmm2[12],xmm1[13],
xmm2[13],xmm1[14],xmm2[14],xmm1[15],xmm2[15]
; CHECK-NEXT: vpunpckhbw {{\.*#+}} %xmm3 = xmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15]
; CHECK-NEXT: vpsllvw %xmm2, %xmm3, %xmm2
; CHECK-NEXT: vpsrlw $8, %xmm2, %xmm2
; CHECK-NEXT: vpunpcklbw {{\.*#+}} %xmm0 = xmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7]
; CHECK-NEXT: vpmovzxbw {{\.*#+}} %xmm1 =
xmm1[0],zero,xmm1[1],zero,xmm1[2],zero,xmm1[3],zero,xmm1[4],zero,xmm1[5],zero,xmm1[6],zero,xmm1[7],zer
o
; CHECK-NEXT: vpsllvw %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpsrlw $8, %xmm0, %xmm0
; CHECK-NEXT: vpackuswb %xmm2, %xmm0, %xmm0
; CHECK-NEXT: retq
%bb8 = sub <16 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %b
%shl = shl <16 x i8> %a, %b
%lshr = lshr <16 x i8> %a, %bb8
%or = or <16 x i8> %shl, %lshr
ret <16 x i8> %or
}

```



```

define <32 x i8> @var_rotate_v32i8(<32 x i8> %a, <32 x i8> %b) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: var_rotate_v32i8:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vpadd {{\.?LCPI[0-9]+_[0-9]+}}(%rip){1to8}, %ymm1, %ymm1
; CHECK-NEXT:  vpxor %xmm2, %xmm2, %xmm2
; CHECK-NEXT:  vpunpckhbw {{\.*#+}} ymm3 =
ymm1[8],ymm2[8],ymm1[9],ymm2[9],ymm1[10],ymm2[10],ymm1[11],ymm2[11],ymm1[12],ymm2[12],ymm1[13],
ymm2[13],ymm1[14],ymm2[14],ymm1[15],ymm2[15],ymm1[24],ymm2[24],ymm1[25],ymm2[25],ymm1[26],ymm2[26],ymm1[27],ymm2[27],ymm1[28],ymm2[28],ymm1[29],ymm2[29],ymm1[30],ymm2[30],ymm1[31],ymm2[31]
; CHECK-NEXT:  vpunpckhbw {{\.*#+}} ymm4 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-NEXT:  vpsllvw %ymm3, %ymm4, %ymm3
; CHECK-NEXT:  vpsrlw $8, %ymm3, %ymm3
; CHECK-NEXT:  vpunpcklbw
{{\.*#+}} ymm1 =
ymm1[0],ymm2[0],ymm1[1],ymm2[1],ymm1[2],ymm2[2],ymm1[3],ymm2[3],ymm1[4],ymm2[4],ymm1[5],ymm2[5],ymm1[6],ymm2[6],ymm1[7],ymm2[7],ymm1[16],ymm2[16],ymm1[17],ymm2[17],ymm1[18],ymm2[18],ymm1[19],ymm2[19],ymm1[20],ymm2[20],ymm1[21],ymm2[21],ymm1[22],ymm2[22],ymm1[23],ymm2[23]
; CHECK-NEXT:  vpunpcklbw {{\.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-NEXT:  vpsllvw %ymm1, %ymm0, %ymm0
; CHECK-NEXT:  vpsrlw $8, %ymm0, %ymm0
; CHECK-NEXT:  vpackuswb %ymm3, %ymm0, %ymm0
; CHECK-NEXT:  retq
%b8 = sub <32 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %b
%shl = shl <32 x i8> %a, %b
%lshr = lshr <32 x i8> %a, %b8
%or = or <32 x i8> %shl, %lshr
ret <32 x i8> %or
}

```

```

define <32 x i8> @splatvar_rotate_v32i8(<32 x i8> %a, <32 x i8> %b) nounwind "min-legal-vector-width"="256"
{
; CHECK-LABEL: splatvar_rotate_v32i8:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vpunpckhbw {{\.*#+}} ymm2 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-NEXT:  vpand {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm1, %xmm1
; CHECK-NEXT:  vpsllw %xmm1, %ymm2, %ymm2
; CHECK-NEXT:  vpsrlw $8, %ymm2, %ymm2
; CHECK-NEXT:  vpunpcklbw {{\.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-NEXT:  vpsllw %xmm1, %ymm0, %ymm0
; CHECK-NEXT:  vpsrlw $8, %ymm0, %ymm0
; CHECK-NEXT:  vpackuswb %ymm2, %ymm0, %ymm0

```

```
; CHECK-NEXT:    retq
%$splat = shufflevector <32 x i8> %b, <32 x i8> undef, <32 x i32> zeroinitializer
%$splat8 = sub <32 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %$splat
%$shl = shl <32 x i8>
%a, %$splat
%$lshr = lshr <32 x i8> %a, %$splat8
%or = or <32 x i8> %$shl, %$lshr
ret <32 x i8> %or
}
```

```
define <32 x i8> @constant_rotate_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: constant_rotate_v32i8:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vpunpckhbw {{.*#+}} ymm1 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-NEXT:  vpsllvw {{\.?LCPI[0-9]+\_[0-9]+\}}(%rip), %ymm1, %ymm1
; CHECK-NEXT:  vpsrlw $8, %ymm1, %ymm1
; CHECK-NEXT:  vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-NEXT:  vpsllvw {{\.?LCPI[0-9]+\_[0-9]+\}}(%rip), %ymm0, %ymm0
; CHECK-NEXT:  vpsrlw $8, %ymm0, %ymm0
; CHECK-NEXT:  vpackuswb %ymm1, %ymm0, %ymm0
; CHECK-NEXT:  retq
%$shl = shl <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 7, i8 6, i8 5, i8 4, i8 3, i8 2, i8 1, i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 7, i8 6, i8 5, i8 4, i8 3, i8 2, i8 1>
%$lshr = lshr <32 x i8> %a, <i8 8, i8 7, i8 6, i8 5, i8 4, i8 3, i8 2, i8 1, i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 7, i8 6, i8 5, i8 4, i8 3, i8 2, i8 1, i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7>
%or = or <32 x i8> %$shl, %$lshr
ret <32 x i8> %or
}
```

```
define <32 x i8> @splatconstant_rotate_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: splatconstant_rotate_v32i8:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vpsllw $4, %ymm0, %ymm1
; CHECK-NEXT:  vpsrlw $4, %ymm0, %ymm0
; CHECK-NEXT:  vpternlogd $216, {{\.?LCPI[0-9]+\_[0-9]+\}}(%rip){1to8}, %ymm1, %ymm0
; CHECK-NEXT:  retq
%$shl = shl <32 x i8> %a, <i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4>
%$lshr = lshr <32 x i8> %a, <i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4>
%or = or <32 x i8> %$shl, %$lshr
ret <32 x i8> %or
}
```

```

define <32 x i8> @splatconstant_rotate_mask_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: splatconstant_rotate_mask_v32i8:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vpsllw $4, %ymm0, %ymm1
; CHECK-NEXT:  vpsrlw $4, %ymm0, %ymm0
; CHECK-NEXT:  vpternlogd $216, {{\?.LCPI[0-9]+\_[0-9]+}}(%rip){1to8}, %ymm1, %ymm0
; CHECK-NEXT:  vpandd {{\?.LCPI[0-9]+\_[0-9]+}}(%rip){1to8}, %ymm0, %ymm0
; CHECK-NEXT:  retq

%shl = shl <32 x i8> %a, <i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4>
%lshr = lshr <32 x i8> %a, <i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4>
%rmask = and <32 x i8> %lshr, <i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55>
%lmask = and <32 x i8> %shl, <i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33>
%or = or <32 x i8> %lmask, %rmask
ret <32 x i8> %or
}

```

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py

; RUN: llc -mtriple=riscv64 -verify-machineinstrs < %s \

; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefixes=CHECK,RV64I

; RUN: llc -mtriple=riscv64 -mattr=+zbs -verify-machineinstrs < %s \

; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefixes=CHECK,RV64ZBS

```
define signext i32 @bclr_i32(i32 signext %a, i32 signext %b) nounwind {
```

```
; RV64I-LABEL: bclr_i32:
```

```
; RV64I:      # %bb.0:
```

```
; RV64I-NEXT: li a2, 1
```

```
; RV64I-NEXT: sllw a1, a2, a1
```

```
; RV64I-NEXT: not a1, a1
```

```
; RV64I-NEXT: and a0, a1, a0
```

```
; RV64I-NEXT: ret
```

```
;
```

```
; RV64ZBS-LABEL: bclr_i32:
```

```
; RV64ZBS:    # %bb.0:
```

```
; RV64ZBS-NEXT: andi a1, a1, 31
```

```
; RV64ZBS-NEXT: bclr a0, a0, a1
```

```
; RV64ZBS-NEXT: sext.w a0, a0
```

```
; RV64ZBS-NEXT: ret
```

```
%and = and i32 %b, 31
```

```
%shl = shl nuw i32 1, %and
```

```
%neg = xor i32 %shl, -1
```

```
%and1 = and i32 %neg, %a
```

```
ret i32 %and1
```

```
}
```

```
define signext i32 @bclr_i32_no_mask(i32 signext %a,
```

```
i32 signext %b) nounwind {
```

```
; RV64I-LABEL: bclr_i32_no_mask:
```

```
; RV64I:      # %bb.0:
```

```
; RV64I-NEXT: li a2, 1
```

```
; RV64I-NEXT: sllw a1, a2, a1
```

```
; RV64I-NEXT: not a1, a1
```

```
; RV64I-NEXT: and a0, a1, a0
```

```
; RV64I-NEXT: ret
```

```
;
```

```
; RV64ZBS-LABEL: bclr_i32_no_mask:
```

```
; RV64ZBS:    # %bb.0:
```

```
; RV64ZBS-NEXT: bclr a0, a0, a1
```

```
; RV64ZBS-NEXT: sext.w a0, a0
```

```
; RV64ZBS-NEXT: ret
```

```
%shl = shl i32 1, %b
```

```
%neg = xor i32 %shl, -1
```

```

%and1 = and i32 %neg, %a
ret i32 %and1
}

define signext i32 @bclr_i32_load(ptr %p, i32 signext %b) nounwind {
; RV64I-LABEL: bclr_i32_load:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lw a0, 0(a0)
; RV64I-NEXT:  li a2, 1
; RV64I-NEXT:  sllw a1, a2, a1
; RV64I-NEXT:  not a1, a1
; RV64I-NEXT:  and a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bclr_i32_load:
; RV64ZBS:      # %bb.0:
; RV64ZBS-NEXT:  lw a0, 0(a0)
; RV64ZBS-NEXT:  bclr a0, a0, a1
; RV64ZBS-NEXT:  sext.w a0, a0
; RV64ZBS-NEXT:  ret
%a = load i32, ptr %p
%shl = shl i32 1, %b
%neg
= xor i32 %shl, -1
%and1 = and i32 %neg, %a
ret i32 %and1
}

define i64 @bclr_i64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: bclr_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 1
; RV64I-NEXT:  sll a1, a2, a1
; RV64I-NEXT:  not a1, a1
; RV64I-NEXT:  and a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bclr_i64:
; RV64ZBS:      # %bb.0:
; RV64ZBS-NEXT:  bclr a0, a0, a1
; RV64ZBS-NEXT:  ret
%and = and i64 %b, 63
%shl = shl nuw i64 1, %and
%neg = xor i64 %shl, -1
%and1 = and i64 %neg, %a
ret i64 %and1
}

```

```

define i64 @bclr_i64_no_mask(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: bclr_i64_no_mask:
; RV64I:      # %bb.0:
; RV64I-NEXT: li a2, 1
; RV64I-NEXT: sll a1, a2, a1
; RV64I-NEXT: not a1, a1
; RV64I-NEXT: and a0, a1, a0
; RV64I-NEXT: ret
;
; RV64ZBS-LABEL: bclr_i64_no_mask:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT: bclr a0, a0, a1
; RV64ZBS-NEXT: ret
%shl = shl i64 1, %b
%neg = xor i64 %shl, -1
%and1 = and i64 %neg, %a
ret i64
%and1
}

define signext i32 @bset_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: bset_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT: li a2, 1
; RV64I-NEXT: sllw a1, a2, a1
; RV64I-NEXT: or a0, a1, a0
; RV64I-NEXT: ret
;
; RV64ZBS-LABEL: bset_i32:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT: andi a1, a1, 31
; RV64ZBS-NEXT: bset a0, a0, a1
; RV64ZBS-NEXT: sext.w a0, a0
; RV64ZBS-NEXT: ret
%and = and i32 %b, 31
%shl = shl nuw i32 1, %and
%or = or i32 %shl, %a
ret i32 %or
}

define signext i32 @bset_i32_no_mask(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: bset_i32_no_mask:
; RV64I:      # %bb.0:
; RV64I-NEXT: li a2, 1
; RV64I-NEXT: sllw a1, a2, a1
; RV64I-NEXT: or a0, a1, a0
; RV64I-NEXT: ret
;

```

```

; RV64ZBS-LABEL: bset_i32_no_mask:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bset a0, a0, a1
; RV64ZBS-NEXT:  sext.w a0, a0
; RV64ZBS-NEXT:  ret
%shl = shl i32 1, %b
%or = or i32 %shl, %a
ret i32 %or
}

```

```

define signext i32
@bset_i32_load(ptr %p, i32 signext %b) nounwind {
; RV64I-LABEL: bset_i32_load:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lw a0, 0(a0)
; RV64I-NEXT:  li a2, 1
; RV64I-NEXT:  sllw a1, a2, a1
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bset_i32_load:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  lw a0, 0(a0)
; RV64ZBS-NEXT:  bset a0, a0, a1
; RV64ZBS-NEXT:  sext.w a0, a0
; RV64ZBS-NEXT:  ret
%a = load i32, ptr %p
%shl = shl i32 1, %b
%or = or i32 %shl, %a
ret i32 %or
}

```

; We can use bsetw for $1 \ll x$ by setting the first source to zero.

```

define signext i32 @bset_i32_zero(i32 signext %a) nounwind {
; RV64I-LABEL: bset_i32_zero:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a1, 1
; RV64I-NEXT:  sllw a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bset_i32_zero:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bset a0, zero, a0
; RV64ZBS-NEXT:  sext.w a0, a0
; RV64ZBS-NEXT:  ret
%shl = shl i32 1, %a
ret i32 %shl
}

```

```

define i64 @bset_i64(i64 %a,
i64 %b) nounwind {
; RV64I-LABEL: bset_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 1
; RV64I-NEXT:  sll a1, a2, a1
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bset_i64:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bset a0, a0, a1
; RV64ZBS-NEXT:  ret
%conv = and i64 %b, 63
%shl = shl nuw i64 1, %conv
%or = or i64 %shl, %a
ret i64 %or
}

```

```

define i64 @bset_i64_no_mask(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: bset_i64_no_mask:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 1
; RV64I-NEXT:  sll a1, a2, a1
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bset_i64_no_mask:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bset a0, a0, a1
; RV64ZBS-NEXT:  ret
%shl = shl i64 1, %b
%or = or i64 %shl, %a
ret i64 %or
}

```

; We can use bsetw for $1 \ll x$ by setting the first source to zero.

```

define signext i64 @bset_i64_zero(i64 signext %a) nounwind {
; RV64I-LABEL: bset_i64_zero:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li
a1, 1
; RV64I-NEXT:  sll a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bset_i64_zero:
; RV64ZBS:    # %bb.0:

```



```

; RV64ZBS-NEXT:  bset a0, zero, a0
; RV64ZBS-NEXT:  ret
%shl = shl i64 1, %a
ret i64 %shl
}

define signext i32 @binv_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: binv_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 1
; RV64I-NEXT:  sllw a1, a2, a1
; RV64I-NEXT:  xor a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: binv_i32:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  andi a1, a1, 31
; RV64ZBS-NEXT:  binv a0, a0, a1
; RV64ZBS-NEXT:  sext.w a0, a0
; RV64ZBS-NEXT:  ret
%and = and i32 %b, 31
%shl = shl nuw i32 1, %and
%xor = xor i32 %shl, %a
ret i32 %xor
}

define signext i32 @binv_i32_no_mask(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: binv_i32_no_mask:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 1
; RV64I-NEXT:  sllw a1, a2, a1
; RV64I-NEXT:  xor a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: binv_i32_no_mask:
;
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  binv a0, a0, a1
; RV64ZBS-NEXT:  sext.w a0, a0
; RV64ZBS-NEXT:  ret
%shl = shl i32 1, %b
%xor = xor i32 %shl, %a
ret i32 %xor
}

define signext i32 @binv_i32_load(ptr %p, i32 signext %b) nounwind {
; RV64I-LABEL: binv_i32_load:
; RV64I:      # %bb.0:

```

```

; RV64I-NEXT:  lw a0, 0(a0)
; RV64I-NEXT:  li a2, 1
; RV64I-NEXT:  sllw a1, a2, a1
; RV64I-NEXT:  xor a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: binv_i32_load:
; RV64ZBS:      # %bb.0:
; RV64ZBS-NEXT:  lw a0, 0(a0)
; RV64ZBS-NEXT:  binv a0, a0, a1
; RV64ZBS-NEXT:  sext.w a0, a0
; RV64ZBS-NEXT:  ret
%a = load i32, ptr %p
%shl = shl i32 1, %b
%xor = xor i32 %shl, %a
ret i32 %xor
}

```

```

define i64 @binv_i64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: binv_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 1
; RV64I-NEXT:  sll a1, a2, a1
; RV64I-NEXT:  xor a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: binv_i64:
; RV64ZBS:      # %bb.0:
;
RV64ZBS-NEXT:  binv a0, a0, a1
; RV64ZBS-NEXT:  ret
%conv = and i64 %b, 63
%shl = shl nuw i64 1, %conv
%xor = xor i64 %shl, %a
ret i64 %xor
}

```

```

define i64 @binv_i64_no_mask(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: binv_i64_no_mask:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 1
; RV64I-NEXT:  sll a1, a2, a1
; RV64I-NEXT:  xor a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: binv_i64_no_mask:
; RV64ZBS:      # %bb.0:
; RV64ZBS-NEXT:  binv a0, a0, a1

```

```
; RV64ZBS-NEXT:  ret
%shl = shl nuw i64 1, %b
%xor = xor i64 %shl, %a
ret i64 %xor
}
```

```
define signext i32 @bext_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: bext_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srlw a0, a0, a1
; RV64I-NEXT:  andi a0, a0, 1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bext_i32:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  andi a1, a1, 31
; RV64ZBS-NEXT:  bext a0, a0, a1
; RV64ZBS-NEXT:  ret
%and = and i32 %b, 31
%shr = lshr i32 %a, %and
%and1 = and i32
%shr, 1
ret i32 %and1
}
```

```
define signext i32 @bext_i32_no_mask(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: bext_i32_no_mask:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srlw a0, a0, a1
; RV64I-NEXT:  andi a0, a0, 1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bext_i32_no_mask:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bext a0, a0, a1
; RV64ZBS-NEXT:  ret
%shr = lshr i32 %a, %b
%and1 = and i32 %shr, 1
ret i32 %and1
}
```

; This gets previous converted to (i1 (truncate (srl X, Y))). Make sure we are
; able to use bext.

```
define void @bext_i32_trunc(i32 signext %0, i32 signext %1) {
; RV64I-LABEL: bext_i32_trunc:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srlw a0, a0, a1
; RV64I-NEXT:  andi a0, a0, 1
```

```

; RV64I-NEXT: beqz a0, .LBB19_2
; RV64I-NEXT: # %bb.1:
; RV64I-NEXT: ret
; RV64I-NEXT: .LBB19_2:
; RV64I-NEXT: tail bar
;
; RV64ZBS-LABEL: bext_i32_trunc:
; RV64ZBS: # %bb.0:
; RV64ZBS-NEXT: bext a0, a0, a1
; RV64ZBS-NEXT: beqz a0, .LBB19_2
; RV64ZBS-NEXT:
# %bb.1:
; RV64ZBS-NEXT: ret
; RV64ZBS-NEXT: .LBB19_2:
; RV64ZBS-NEXT: tail bar
%3 = shl i32 1, %1
%4 = and i32 %3, %0
%5 = icmp eq i32 %4, 0
br i1 %5, label %6, label %7

6:                                ; preds = %2
tail call void @bar()
br label %7

7:                                ; preds = %6, %2
ret void
}

declare void @bar()

define i64 @bext_i64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: bext_i64:
; RV64I: # %bb.0:
; RV64I-NEXT: srl a0, a0, a1
; RV64I-NEXT: andi a0, a0, 1
; RV64I-NEXT: ret
;
; RV64ZBS-LABEL: bext_i64:
; RV64ZBS: # %bb.0:
; RV64ZBS-NEXT: bext a0, a0, a1
; RV64ZBS-NEXT: ret
%conv = and i64 %b, 63
%shr = lshr i64 %a, %conv
%and1 = and i64 %shr, 1
ret i64 %and1
}

define i64 @bext_i64_no_mask(i64 %a, i64 %b) nounwind {

```

```

; RV64I-LABEL: bext_i64_no_mask:
; RV64I:    # %bb.0:
; RV64I-NEXT:  srl a0, a0, a1
; RV64I-NEXT:  andi a0, a0, 1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL:
bext_i64_no_mask:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bext a0, a0, a1
; RV64ZBS-NEXT:  ret
%shr = lshr i64 %a, %b
%and1 = and i64 %shr, 1
ret i64 %and1
}

define signext i32 @bexti_i32(i32 signext %a) nounwind {
; RV64I-LABEL: bexti_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 58
; RV64I-NEXT:  srli a0, a0, 63
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bexti_i32:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bexti a0, a0, 5
; RV64ZBS-NEXT:  ret
%shr = lshr i32 %a, 5
%and = and i32 %shr, 1
ret i32 %and
}

define i64 @bexti_i64(i64 %a) nounwind {
; RV64I-LABEL: bexti_i64:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 58
; RV64I-NEXT:  srli a0, a0, 63
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bexti_i64:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bexti a0, a0, 5
; RV64ZBS-NEXT:  ret
%shr = lshr i64 %a, 5
%and = and i64 %shr, 1
ret i64 %and
}

```

```

define signext i32 @bexti_i32_cmp(i32 signext %a) nounwind {
; CHECK-LABEL: bexti_i32_cmp:
;
CHECK:    # %bb.0:
; CHECK-NEXT:  andi a0, a0, 32
; CHECK-NEXT:  snez a0, a0
; CHECK-NEXT:  ret
%and = and i32 %a, 32
%cmp = icmp ne i32 %and, 0
%zext = zext i1 %cmp to i32
ret i32 %zext
}

```

```

define i64 @bexti_i64_cmp(i64 %a) nounwind {
; RV64I-LABEL: bexti_i64_cmp:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 58
; RV64I-NEXT:  srli a0, a0, 63
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bexti_i64_cmp:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bexti a0, a0, 5
; RV64ZBS-NEXT:  ret
%and = and i64 %a, 32
%cmp = icmp ne i64 %and, 0
%zext = zext i1 %cmp to i64
ret i64 %zext
}

```

```

define signext i32 @bclri_i32_10(i32 signext %a) nounwind {
; CHECK-LABEL: bclri_i32_10:
; CHECK:    # %bb.0:
; CHECK-NEXT:  andi a0, a0, -1025
; CHECK-NEXT:  ret
%and = and i32 %a, -1025
ret i32 %and
}

```

```

define signext i32 @bclri_i32_11(i32 signext %a) nounwind {
; RV64I-LABEL: bclri_i32_11:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a1, 1048575
; RV64I-NEXT:  addiw a1,
a1, 2047
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  ret
;

```

```

; RV64ZBS-LABEL: bclri_i32_11:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bclri a0, a0, 11
; RV64ZBS-NEXT:  ret
%and = and i32 %a, -2049
ret i32 %and
}

```

```

define signext i32 @bclri_i32_30(i32 signext %a) nounwind {
; RV64I-LABEL: bclri_i32_30:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a1, 786432
; RV64I-NEXT:  addiw a1, a1, -1
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bclri_i32_30:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bclri a0, a0, 30
; RV64ZBS-NEXT:  ret
%and = and i32 %a, -1073741825
ret i32 %and
}

```

```

define signext i32 @bclri_i32_31(i32 signext %a) nounwind {
; RV64I-LABEL: bclri_i32_31:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 33
; RV64I-NEXT:  srli a0, a0, 33
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bclri_i32_31:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bclri a0, a0, 31
; RV64ZBS-NEXT:  sext.w a0, a0
; RV64ZBS-NEXT:  ret
%and = and i32 %a,
-2147483649
ret i32 %and
}

```

```

define i64 @bclri_i64_10(i64 %a) nounwind {
; CHECK-LABEL: bclri_i64_10:
; CHECK:    # %bb.0:
; CHECK-NEXT:  andi a0, a0, -1025
; CHECK-NEXT:  ret
%and = and i64 %a, -1025
ret i64 %and
}

```

```
}
```

```
define i64 @bclri_i64_11(i64 %a) nounwind {  
; RV64I-LABEL: bclri_i64_11:  
; RV64I:    # %bb.0:  
; RV64I-NEXT:  lui a1, 1048575  
; RV64I-NEXT:  addiw a1, a1, 2047  
; RV64I-NEXT:  and a0, a0, a1  
; RV64I-NEXT:  ret  
;  
; RV64ZBS-LABEL: bclri_i64_11:  
; RV64ZBS:    # %bb.0:  
; RV64ZBS-NEXT:  bclri a0, a0, 11  
; RV64ZBS-NEXT:  ret  
%and = and i64 %a, -2049  
ret i64 %and  
}
```

```
define i64 @bclri_i64_30(i64 %a) nounwind {  
; RV64I-LABEL: bclri_i64_30:  
; RV64I:    # %bb.0:  
; RV64I-NEXT:  lui a1, 786432  
; RV64I-NEXT:  addiw a1, a1, -1  
; RV64I-NEXT:  and a0, a0, a1  
; RV64I-NEXT:  ret  
;  
; RV64ZBS-LABEL: bclri_i64_30:  
; RV64ZBS:    # %bb.0:  
; RV64ZBS-NEXT:  bclri a0, a0, 30  
; RV64ZBS-NEXT:  ret  
%and = and i64 %a, -1073741825  
ret i64 %and  
}
```

```
define  
i64 @bclri_i64_31(i64 %a) nounwind {  
; RV64I-LABEL: bclri_i64_31:  
; RV64I:    # %bb.0:  
; RV64I-NEXT:  lui a1, 524288  
; RV64I-NEXT:  addi a1, a1, -1  
; RV64I-NEXT:  and a0, a0, a1  
; RV64I-NEXT:  ret  
;  
; RV64ZBS-LABEL: bclri_i64_31:  
; RV64ZBS:    # %bb.0:  
; RV64ZBS-NEXT:  bclri a0, a0, 31  
; RV64ZBS-NEXT:  ret  
%and = and i64 %a, -2147483649
```



```

ret i64 %and
}

define i64 @bclri_i64_62(i64 %a) nounwind {
; RV64I-LABEL: bclri_i64_62:
; RV64I:      # %bb.0:
; RV64I-NEXT: li a1, -1
; RV64I-NEXT: slli a1, a1, 62
; RV64I-NEXT: addi a1, a1, -1
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: ret
;
; RV64ZBS-LABEL: bclri_i64_62:
; RV64ZBS:      # %bb.0:
; RV64ZBS-NEXT: bclri a0, a0, 62
; RV64ZBS-NEXT: ret
%and = and i64 %a, -4611686018427387905
ret i64 %and
}

define i64 @bclri_i64_63(i64 %a) nounwind {
; RV64I-LABEL: bclri_i64_63:
; RV64I:      # %bb.0:
; RV64I-NEXT: slli a0, a0, 1
; RV64I-NEXT: srli a0, a0, 1
; RV64I-NEXT: ret
;
; RV64ZBS-LABEL:
bclri_i64_63:
; RV64ZBS:      # %bb.0:
; RV64ZBS-NEXT: bclri a0, a0, 63
; RV64ZBS-NEXT: ret
%and = and i64 %a, -9223372036854775809
ret i64 %and
}

define i64 @bclri_i64_large0(i64 %a) nounwind {
; RV64I-LABEL: bclri_i64_large0:
; RV64I:      # %bb.0:
; RV64I-NEXT: lui a1, 1044480
; RV64I-NEXT: addiw a1, a1, -256
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: ret
;
; RV64ZBS-LABEL: bclri_i64_large0:
; RV64ZBS:      # %bb.0:
; RV64ZBS-NEXT: andi a0, a0, -256
; RV64ZBS-NEXT: bclri a0, a0, 24

```

```

; RV64ZBS-NEXT:  ret
%and = and i64 %a, -16777472
ret i64 %and
}

define i64 @bclri_i64_large1(i64 %a) nounwind {
; RV64I-LABEL: bclri_i64_large1:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a1, 1044464
; RV64I-NEXT:  addiw a1, a1, -1
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bclri_i64_large1:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bclri a0, a0, 16
; RV64ZBS-NEXT:  bclri a0, a0, 24
; RV64ZBS-NEXT:  ret
%and = and i64 %a,
-16842753
ret i64 %and
}

define signext i32 @bseti_i32_10(i32 signext %a) nounwind {
; CHECK-LABEL: bseti_i32_10:
; CHECK:      # %bb.0:
; CHECK-NEXT:  ori a0, a0, 1024
; CHECK-NEXT:  ret
%or = or i32 %a, 1024
ret i32 %or
}

define signext i32 @bseti_i32_11(i32 signext %a) nounwind {
; RV64I-LABEL: bseti_i32_11:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 1
; RV64I-NEXT:  slliw a1, a1, 11
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bseti_i32_11:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bseti a0, a0, 11
; RV64ZBS-NEXT:  ret
%or = or i32 %a, 2048
ret i32 %or
}

```

```

define signext i32 @bseti_i32_30(i32 signext %a) nounwind {
; RV64I-LABEL: bseti_i32_30:
; RV64I:      # %bb.0:
; RV64I-NEXT: lui a1, 262144
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: ret
;
; RV64ZBS-LABEL: bseti_i32_30:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT: bseti a0, a0, 30
; RV64ZBS-NEXT: ret
%or = or i32 %a, 1073741824
ret i32 %or
}

```

```

define signext i32
@bseti_i32_31(i32 signext %a) nounwind {
; RV64I-LABEL: bseti_i32_31:
; RV64I:      # %bb.0:
; RV64I-NEXT: lui a1, 524288
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: ret
;
; RV64ZBS-LABEL: bseti_i32_31:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT: bseti a0, a0, 31
; RV64ZBS-NEXT: sext.w a0, a0
; RV64ZBS-NEXT: ret
%or = or i32 %a, 2147483648
ret i32 %or
}

```

```

define i64 @bseti_i64_10(i64 %a) nounwind {
; CHECK-LABEL: bseti_i64_10:
; CHECK:      # %bb.0:
; CHECK-NEXT: ori a0, a0, 1024
; CHECK-NEXT: ret
%or = or i64 %a, 1024
ret i64 %or
}

```

```

define i64 @bseti_i64_11(i64 %a) nounwind {
; RV64I-LABEL: bseti_i64_11:
; RV64I:      # %bb.0:
; RV64I-NEXT: li a1, 1
; RV64I-NEXT: slli a1, a1, 11
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: ret

```

```

;
; RV64ZBS-LABEL: bseti_i64_11:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bseti a0, a0, 11
; RV64ZBS-NEXT:  ret
%or = or i64 %a, 2048
ret i64 %or
}

define i64 @bseti_i64_30(i64 %a) nounwind {
; RV64I-LABEL: bseti_i64_30:
;
RV64I:    # %bb.0:
; RV64I-NEXT:  lui a1, 262144
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bseti_i64_30:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bseti a0, a0, 30
; RV64ZBS-NEXT:  ret
%or = or i64 %a, 1073741824
ret i64 %or
}

define i64 @bseti_i64_31(i64 %a) nounwind {
; RV64I-LABEL: bseti_i64_31:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a1, 1
; RV64I-NEXT:  slli a1, a1, 31
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bseti_i64_31:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bseti a0, a0, 31
; RV64ZBS-NEXT:  ret
%or = or i64 %a, 2147483648
ret i64 %or
}

define i64 @bseti_i64_62(i64 %a) nounwind {
; RV64I-LABEL: bseti_i64_62:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a1, 1
; RV64I-NEXT:  slli a1, a1, 62
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  ret

```

```

;
; RV64ZBS-LABEL: bseti_i64_62:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bseti a0, a0, 62
; RV64ZBS-NEXT:  ret
%or = or i64 %a,
4611686018427387904
ret i64 %or
}

define i64 @bseti_i64_63(i64 %a) nounwind {
; RV64I-LABEL: bseti_i64_63:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a1, -1
; RV64I-NEXT:  slli a1, a1, 63
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bseti_i64_63:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bseti a0, a0, 63
; RV64ZBS-NEXT:  ret
%or = or i64 %a, 9223372036854775808
ret i64 %or
}

define signext i32 @binvi_i32_10(i32 signext %a) nounwind {
; CHECK-LABEL: binvi_i32_10:
; CHECK:    # %bb.0:
; CHECK-NEXT:  xori a0, a0, 1024
; CHECK-NEXT:  ret
%xor = xor i32 %a, 1024
ret i32 %xor
}

define signext i32 @binvi_i32_11(i32 signext %a) nounwind {
; RV64I-LABEL: binvi_i32_11:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a1, 1
; RV64I-NEXT:  slliw a1, a1, 11
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: binvi_i32_11:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  binvi a0, a0, 11
; RV64ZBS-NEXT:  ret
%xor = xor i32 %a,

```

```

2048
ret i32 %xor
}

define signext i32 @binvi_i32_30(i32 signext %a) nounwind {
; RV64I-LABEL: binvi_i32_30:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a1, 262144
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: binvi_i32_30:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  binvi a0, a0, 30
; RV64ZBS-NEXT:  ret
%xor = xor i32 %a, 1073741824
ret i32 %xor
}

```

```

define signext i32 @binvi_i32_31(i32 signext %a) nounwind {
; RV64I-LABEL: binvi_i32_31:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lui a1, 524288
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: binvi_i32_31:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  binvi a0, a0, 31
; RV64ZBS-NEXT:  sext.w a0, a0
; RV64ZBS-NEXT:  ret
%xor = xor i32 %a, 2147483648
ret i32 %xor
}

```

```

define i64 @binvi_i64_10(i64 %a) nounwind {
; CHECK-LABEL: binvi_i64_10:
; CHECK:    # %bb.0:
; CHECK-NEXT:  xori a0, a0, 1024
; CHECK-NEXT:  ret
%xor = xor i64 %a, 1024
ret i64 %xor
}

```

```

define i64 @binvi_i64_11(i64
%a) nounwind {
; RV64I-LABEL: binvi_i64_11:
; RV64I:    # %bb.0:

```

```

; RV64I-NEXT:  li a1, 1
; RV64I-NEXT:  slli a1, a1, 11
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: binvi_i64_11:
; RV64ZBS:      # %bb.0:
; RV64ZBS-NEXT:  binvi a0, a0, 11
; RV64ZBS-NEXT:  ret
%xor = xor i64 %a, 2048
ret i64 %xor
}

define i64 @binvi_i64_30(i64 %a) nounwind {
; RV64I-LABEL: binvi_i64_30:
; RV64I:        # %bb.0:
; RV64I-NEXT:   lui a1, 262144
; RV64I-NEXT:   xor a0, a0, a1
; RV64I-NEXT:   ret
;
; RV64ZBS-LABEL: binvi_i64_30:
; RV64ZBS:      # %bb.0:
; RV64ZBS-NEXT:  binvi a0, a0, 30
; RV64ZBS-NEXT:  ret
%xor = xor i64 %a, 1073741824
ret i64 %xor
}

define i64 @binvi_i64_31(i64 %a) nounwind {
; RV64I-LABEL: binvi_i64_31:
; RV64I:        # %bb.0:
; RV64I-NEXT:   li a1, 1
; RV64I-NEXT:   slli a1, a1, 31
; RV64I-NEXT:   xor a0, a0, a1
; RV64I-NEXT:   ret
;
; RV64ZBS-LABEL: binvi_i64_31:
; RV64ZBS:      # %bb.0:
; RV64ZBS-NEXT:  binvi
a0, a0, 31
; RV64ZBS-NEXT:  ret
%xor = xor i64 %a, 2147483648
ret i64 %xor
}

define i64 @binvi_i64_62(i64 %a) nounwind {
; RV64I-LABEL: binvi_i64_62:
; RV64I:        # %bb.0:

```

```

; RV64I-NEXT:  li a1, 1
; RV64I-NEXT:  slli a1, a1, 62
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: binvi_i64_62:
; RV64ZBS:     # %bb.0:
; RV64ZBS-NEXT:  binvi a0, a0, 62
; RV64ZBS-NEXT:  ret
%xor = xor i64 %a, 4611686018427387904
ret i64 %xor
}

define i64 @binvi_i64_63(i64 %a) nounwind {
; RV64I-LABEL: binvi_i64_63:
; RV64I:       # %bb.0:
; RV64I-NEXT:  li a1, -1
; RV64I-NEXT:  slli a1, a1, 63
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: binvi_i64_63:
; RV64ZBS:     # %bb.0:
; RV64ZBS-NEXT:  binvi a0, a0, 63
; RV64ZBS-NEXT:  ret
%xor = xor i64 %a, 9223372036854775808
ret i64 %xor
}

define i64 @xor_i64_large(i64 %a) nounwind {
; RV64I-LABEL: xor_i64_large:
; RV64I:       # %bb.0:
; RV64I-NEXT:  li a1, 1
; RV64I-NEXT:  slli
a1, a1, 32
; RV64I-NEXT:  addi a1, a1, 1
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: xor_i64_large:
; RV64ZBS:     # %bb.0:
; RV64ZBS-NEXT:  binvi a0, a0, 0
; RV64ZBS-NEXT:  binvi a0, a0, 32
; RV64ZBS-NEXT:  ret
%xor = xor i64 %a, 4294967297
ret i64 %xor
}

```



```

define i64 @xor_i64_4099(i64 %a) nounwind {
; RV64I-LABEL: xor_i64_4099:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a1, 1
; RV64I-NEXT:  addiw a1, a1, 3
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: xor_i64_4099:
; RV64ZBS:      # %bb.0:
; RV64ZBS-NEXT:  xori a0, a0, 3
; RV64ZBS-NEXT:  binvi a0, a0, 12
; RV64ZBS-NEXT:  ret
%xor = xor i64 %a, 4099
ret i64 %xor
}

```

```

define i64 @xor_i64_96(i64 %a) nounwind {
; CHECK-LABEL: xor_i64_96:
; CHECK:      # %bb.0:
; CHECK-NEXT:  xori a0, a0, 96
; CHECK-NEXT:  ret
%xor = xor i64 %a, 96
ret i64 %xor
}

```

```

define i64 @or_i64_large(i64 %a) nounwind {
; RV64I-LABEL: or_i64_large:
; RV64I:      # %bb.0:
; RV64I-NEXT:
    li a1, 1
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  addi a1, a1, 1
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: or_i64_large:
; RV64ZBS:      # %bb.0:
; RV64ZBS-NEXT:  bseti a0, a0, 0
; RV64ZBS-NEXT:  bseti a0, a0, 32
; RV64ZBS-NEXT:  ret
%or = or i64 %a, 4294967297
ret i64 %or
}

```

```

define i64 @xor_i64_66901(i64 %a) nounwind {
; RV64I-LABEL: xor_i64_66901:
; RV64I:      # %bb.0:

```

```

; RV64I-NEXT:  lui a1, 16
; RV64I-NEXT:  addiw a1, a1, 1365
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: xor_i64_66901:
; RV64ZBS:     # %bb.0:
; RV64ZBS-NEXT: xori a0, a0, 1365
; RV64ZBS-NEXT: binvi a0, a0, 16
; RV64ZBS-NEXT: ret
%xor = xor i64 %a, 66901
ret i64 %xor
}

define i64 @or_i64_4099(i64 %a) nounwind {
; RV64I-LABEL: or_i64_4099:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a1, 1
; RV64I-NEXT:  addiw a1, a1, 3
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: or_i64_4099:
; RV64ZBS:
; RV64ZBS:     # %bb.0:
; RV64ZBS-NEXT: ori a0, a0, 3
; RV64ZBS-NEXT: bseti a0, a0, 12
; RV64ZBS-NEXT: ret
%or = or i64 %a, 4099
ret i64 %or
}

define i64 @or_i64_96(i64 %a) nounwind {
; CHECK-LABEL: or_i64_96:
; CHECK:      # %bb.0:
; CHECK-NEXT:  ori a0, a0, 96
; CHECK-NEXT:  ret
%or = or i64 %a, 96
ret i64 %or
}

define i64 @or_i64_66901(i64 %a) nounwind {
; RV64I-LABEL: or_i64_66901:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a1, 16
; RV64I-NEXT:  addiw a1, a1, 1365
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  ret

```

```

;
; RV64ZBS-LABEL: or_i64_66901:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  ori a0, a0, 1365
; RV64ZBS-NEXT:  bseti a0, a0, 16
; RV64ZBS-NEXT:  ret
%or = or i64 %a, 66901
ret i64 %or
}

define signext i32 @bset_trailing_ones_i32_mask(i32 signext %a) nounwind {
; RV64I-LABEL: bset_trailing_ones_i32_mask:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a1, -1
; RV64I-NEXT:  sllw a0, a1, a0
; RV64I-NEXT:  not a0, a0
; RV64I-NEXT:  ret
;
;
RV64ZBS-LABEL: bset_trailing_ones_i32_mask:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  andi a0, a0, 31
; RV64ZBS-NEXT:  bset a0, zero, a0
; RV64ZBS-NEXT:  addiw a0, a0, -1
; RV64ZBS-NEXT:  ret
%and = and i32 %a, 31
%shift = shl nsw i32 -1, %and
%not = xor i32 %shift, -1
ret i32 %not
}

define signext i32 @bset_trailing_ones_i32_no_mask(i32 signext %a) nounwind {
; RV64I-LABEL: bset_trailing_ones_i32_no_mask:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a1, -1
; RV64I-NEXT:  sllw a0, a1, a0
; RV64I-NEXT:  not a0, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bset_trailing_ones_i32_no_mask:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bset a0, zero, a0
; RV64ZBS-NEXT:  addiw a0, a0, -1
; RV64ZBS-NEXT:  ret
%shift = shl nsw i32 -1, %a
%not = xor i32 %shift, -1
ret i32 %not
}

```

```

define signext i64 @bset_trailing_ones_i64_mask(i64 signext %a) nounwind {
; RV64I-LABEL: bset_trailing_ones_i64_mask:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, -1
; RV64I-NEXT:  sll
a0, a1, a0
; RV64I-NEXT:  not a0, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bset_trailing_ones_i64_mask:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bset a0, zero, a0
; RV64ZBS-NEXT:  addi a0, a0, -1
; RV64ZBS-NEXT:  ret
%and = and i64 %a, 63
%shift = shl nsw i64 -1, %and
%not = xor i64 %shift, -1
ret i64 %not
}

```

```

define signext i64 @bset_trailing_ones_i64_no_mask(i64 signext %a) nounwind {
; RV64I-LABEL: bset_trailing_ones_i64_no_mask:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, -1
; RV64I-NEXT:  sll a0, a1, a0
; RV64I-NEXT:  not a0, a0
; RV64I-NEXT:  ret
;
; RV64ZBS-LABEL: bset_trailing_ones_i64_no_mask:
; RV64ZBS:    # %bb.0:
; RV64ZBS-NEXT:  bset a0, zero, a0
; RV64ZBS-NEXT:  addi a0, a0, -1
; RV64ZBS-NEXT:  ret
%shift = shl nsw i64 -1, %a
%not = xor i64 %shift, -1
ret i64 %not
}

```

=====

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```
; RUN: opt -passes=consttoist -S -o - %s | FileCheck %s
target datalayout = "e-m:e-p:32:32-i64:64-v128:64:128-a:0:32-n32-S64"
target triple = "thumbv6m-none--musleabi"
```

```
; Check that for i8 type, the maximum legal offset is 31.
; Also check that an constant used as value to be stored rather than
; pointer in a store instruction is hoisted.
; CHECK: foo_i8
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874720 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK-DAG: %[[C3:const[0-9]?]] = bitcast i32 805873720 to i32
; CHECK-DAG: %[[C4:const[0-9]?]] = bitcast i32 805873688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to ptr
; CHECK-NEXT: %1 = load volatile i8, ptr %0
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to ptr
; CHECK-NEXT: %3 = load volatile i8, ptr %2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 31
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to ptr
; CHECK-NEXT: %5 = load volatile
i8, ptr %4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to ptr
```

```

; CHECK-NEXT: %7 = load volatile i8, ptr %6
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 7
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to ptr
; CHECK-NEXT: %9 = load volatile i8, ptr %8
; CHECK-NEXT: %10 = inttoptr i32 %[[C4]] to ptr
; CHECK-NEXT: store i8 %9, ptr %10
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C4]], 31
; CHECK-NEXT: %11 = inttoptr i32 %[[M4]] to ptr
; CHECK-NEXT: store i8 %7, ptr %11
; CHECK-NEXT: %12 = inttoptr i32 %[[C3]] to ptr
; CHECK-NEXT: store i8 %5, ptr %12
; CHECK-NEXT: %[[M5:const_mat[0-9]?]] = add i32 %[[C3]], 7
; CHECK-NEXT: %13 = inttoptr i32 %[[M5]] to ptr
; CHECK-NEXT: store i8 %3, ptr %13
; CHECK-NEXT: %[[M6:const_mat[0-9]?]] = add i32 %[[C1]], 80
; CHECK-NEXT: %14 = inttoptr i32 %[[M6]] to ptr
; CHECK-NEXT: store ptr %14, ptr @goo

```

@goo = global ptr undef

```

define void @foo_i8() {
entry:
  %0 = load volatile i8, ptr inttoptr (i32 805874688 to ptr)
  %1 = load volatile
i8, ptr inttoptr (i32 805874692 to ptr)
  %2 = load volatile i8, ptr inttoptr (i32 805874719 to ptr)
  %3 = load volatile i8, ptr inttoptr (i32 805874720 to ptr)
  %4 = load volatile i8, ptr inttoptr (i32 805874727 to ptr)
  store i8 %4, ptr inttoptr(i32 805873688 to ptr)
  store i8 %3, ptr inttoptr(i32 805873719 to ptr)
  store i8 %2, ptr inttoptr(i32 805873720 to ptr)
  store i8 %1, ptr inttoptr(i32 805873727 to ptr)
  store ptr inttoptr(i32 805874800 to ptr), ptr @goo
  ret void
}

```

```

; Check that for i16 type, the maximum legal offset is 62.
; CHECK: foo_i16
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874752 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to ptr
; CHECK-NEXT: %1 = load volatile i16, ptr %0, align 2
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to ptr
; CHECK-NEXT: %3 = load volatile i16, ptr %2, align 2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add
i32 %[[C2]], 32
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to ptr

```

```
; CHECK-NEXT: %5 = load volatile i16, ptr %4, align 2
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C2]], 62
; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to ptr
; CHECK-NEXT: %7 = load volatile i16, ptr %6, align 2
; CHECK-NEXT: %8 = inttoptr i32 %[[C1]] to ptr
; CHECK-NEXT: %9 = load volatile i16, ptr %8, align 2
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 22
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to ptr
; CHECK-NEXT: %11 = load volatile i16, ptr %10, align 2
```

```
define void @foo_i16() {
entry:
%0 = load volatile i16, ptr inttoptr (i32 805874688 to ptr), align 2
%1 = load volatile i16, ptr inttoptr (i32 805874692 to ptr), align 2
%2 = load volatile i16, ptr inttoptr (i32 805874720 to ptr), align 2
%3 = load volatile i16, ptr inttoptr (i32 805874750 to ptr), align 2
%4 = load volatile i16, ptr inttoptr (i32 805874752 to ptr), align 2
%5 = load volatile i16, ptr inttoptr (i32 805874774 to ptr), align
2
ret void
}
```

```
; Check that for i32 type, the maximum legal offset is 124.
; CHECK: foo_i32
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to ptr
; CHECK-NEXT: %1 = load volatile i32, ptr %0, align 4
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to ptr
; CHECK-NEXT: %3 = load volatile i32, ptr %2, align 4
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 124
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to ptr
; CHECK-NEXT: %5 = load volatile i32, ptr %4, align 4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to ptr
; CHECK-NEXT: %7 = load volatile i32, ptr %6, align 4
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 8
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to ptr
; CHECK-NEXT: %9 = load volatile i32, ptr %8, align 4
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 12
; CHECK-NEXT: %10 = inttoptr
i32 %[[M4]] to ptr
; CHECK-NEXT: %11 = load volatile i32, ptr %10, align 4
```

```
define void @foo_i32() {
entry:
%0 = load volatile i32, ptr inttoptr (i32 805874688 to ptr), align 4
%1 = load volatile i32, ptr inttoptr (i32 805874692 to ptr), align 4
```

```

%2 = load volatile i32, ptr inttoptr (i32 805874812 to ptr), align 4
%3 = load volatile i32, ptr inttoptr (i32 805874816 to ptr), align 4
%4 = load volatile i32, ptr inttoptr (i32 805874824 to ptr), align 4
%5 = load volatile i32, ptr inttoptr (i32 805874828 to ptr), align 4
ret void
}
; RUN: llc -march=hexagon < %s
; REQUIRES: asserts

; The two loads based on %struct.0, loading two different data types
; cause LSR to assume type "void" for the memory type. This would then
; cause an assert in isLegalAddressingMode. Make sure we no longer crash.

target triple = "hexagon"

%struct.0 = type { ptr, i8, %union.anon.0 }
%union.anon.0 = type { ptr }

define hidden fastcc void @fred() unnamed_addr #0 {
entry:
br i1 undef, label %while.end, label %while.body.lr.ph

while.body.lr.ph:                                ; preds = %entry
br label %while.body

while.body:                                       ; preds = %exit.2, %while.body.lr.ph
%lsr.iv = phi ptr [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
switch i32 undef, label %exit [
  i32 1, label %sw.bb.i
  i32 2, label %sw.bb3.i
]

sw.bb.i:                                         ; preds = %while.body
unreachable

sw.bb3.i:                                       ; preds = %while.body
unreachable

exit:
                                           ; preds = %while.body
switch i32 undef, label %exit.2 [
  i32 1, label %sw.bb.i17
  i32 2, label %sw.bb3.i20
]

sw.bb.i17:                                       ; preds = %exit
%0 = load i32, ptr %lsr.iv, align 4
unreachable

```

```
sw.bb3.i20:                                ; preds = %exit
%1 = load ptr, ptr %lsr.iv, align 4
unreachable
```

```
exit.2:                                    ; preds = %exit
%cgep22 = getelementptr %struct.0, ptr %lsr.iv, i32 1
br label %while.body
```

```
while.end:                                ; preds = %entry
ret void
}
```

```
attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }
; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --include-generated-funcs
; RUN: opt -S -passes=verify,iroutliner -ir-outlining-no-cost < %s | FileCheck %s
; FIXME: Disabled run-line after running into some turbulence with debuginfo-iterators
; run: opt -S -passes=verify,iroutliner -ir-outlining-no-cost < %s --try-experimental-debuginfo-iterators | FileCheck %s
```

```
; This test checks that debug info is recognized as able to be extracted along
; with the other instructions, but is not included in the consolidated function.
```

```
define void @function1() !dbg !6 {
entry:
%a = alloca i32, align 4, !dbg !17
call void @llvm.dbg.value(metadata ptr %a, metadata !9, metadata !DIExpression()), !dbg !17
%b = alloca i32, align 4, !dbg !18
call void @llvm.dbg.value(metadata ptr %b, metadata !11, metadata !DIExpression()), !dbg !18
%c = alloca i32, align 4, !dbg !19
call void @llvm.dbg.value(metadata ptr %c, metadata !12, metadata !DIExpression()), !dbg !19
```

```
store i32 2, ptr %a, align 4, !dbg !20
store i32 3, ptr %b, align 4, !dbg !21
store i32 4, ptr %c, align 4, !dbg !22
%al = load i32, ptr %a, align 4, !dbg !23
call void @llvm.dbg.value(metadata i32 %al, metadata !13, metadata !DIExpression()), !dbg !23
%bl = load i32, ptr %b, align 4, !dbg !24
call void @llvm.dbg.value(metadata i32 %bl, metadata !15, metadata !DIExpression()), !dbg !24
%cl = load i32, ptr %c, align 4, !dbg !25
call void @llvm.dbg.value(metadata i32 %cl, metadata !16, metadata !DIExpression()), !dbg !25
ret void, !dbg !26
}
```

```
define void @function2() !dbg !27 {
entry:
%a = alloca i32, align 4, !dbg !35
```

```

call void @llvm.dbg.value(metadata ptr %a, metadata !29, metadata !DIExpression()), !dbg !35
%b = alloca i32, align 4, !dbg !36
call void @llvm.dbg.value(metadata ptr %b, metadata !30, metadata !DIExpression()), !dbg !36
%c = alloca i32, align 4, !dbg !37
call void @llvm.dbg.value(metadata ptr %c, metadata !31, metadata !DIExpression()), !dbg
!37
store i32 2, ptr %a, align 4, !dbg !38
store i32 3, ptr %b, align 4, !dbg !39
store i32 4, ptr %c, align 4, !dbg !40
%a1 = load i32, ptr %a, align 4, !dbg !41
call void @llvm.dbg.value(metadata i32 %a1, metadata !32, metadata !DIExpression()), !dbg !41
%b1 = load i32, ptr %b, align 4, !dbg !42
call void @llvm.dbg.value(metadata i32 %b1, metadata !33, metadata !DIExpression()), !dbg !42
%c1 = load i32, ptr %c, align 4, !dbg !43
call void @llvm.dbg.value(metadata i32 %c1, metadata !34, metadata !DIExpression()), !dbg !43
ret void, !dbg !44
}

```

```

; Function Attrs: nounwind readnone speculatable willreturn
declare void @llvm.dbg.value(metadata, metadata, metadata) #0

```

```

attributes #0 = { nounwind readnone speculatable willreturn }

```

```

!llvm.dbg.cu = !{!0}
!llvm.debugify = !{!3, !4}
!llvm.module.flags = !{!5}

```

```

!0 = distinct !DICompileUnit(language: DW_LANG_C, file: !1, producer: "debugify", isOptimized: true,
runtimeVersion: 0, emissionKind: FullDebug, enums: !2)
!1 = !DIFile(filename:
"legal-debug.ll", directory: "/")
!2 = !{}
!3 = !{i32 20}
!4 = !{i32 12}
!5 = !{i32 2, !"Debug Info Version", i32 3}
!6 = distinct !DISubprogram(name: "function1", linkageName: "function1", scope: null, file: !1, line: 1, type: !7,
scopeLine: 1, spFlags: DISPFlagDefinition | DISPFlagOptimized, unit: !0, retainedNodes: !8)
!7 = !DISubroutineType(types: !2)
!8 = !{!9, !11, !12, !13, !15, !16}
!9 = !DILocalVariable(name: "1", scope: !6, file: !1, line: 1, type: !10)
!10 = !DIBasicType(name: "ty64", size: 64, encoding: DW_ATE_unsigned)
!11 = !DILocalVariable(name: "2", scope: !6, file: !1, line: 2, type: !10)
!12 = !DILocalVariable(name: "3", scope: !6, file: !1, line: 3, type: !10)
!13 = !DILocalVariable(name: "4", scope: !6, file: !1, line: 7, type: !14)
!14 = !DIBasicType(name: "ty32", size: 32, encoding: DW_ATE_unsigned)
!15 = !DILocalVariable(name: "5", scope: !6, file: !1, line: 8, type: !14)
!16 = !DILocalVariable(name: "6", scope: !6, file: !1, line: 9, type: !14)

```

```

!17
= !DILocation(line: 1, column: 1, scope: !6)
!18 = !DILocation(line: 2, column: 1, scope: !6)
!19 = !DILocation(line: 3, column: 1, scope: !6)
!20 = !DILocation(line: 4, column: 1, scope: !6)
!21 = !DILocation(line: 5, column: 1, scope: !6)
!22 = !DILocation(line: 6, column: 1, scope: !6)
!23 = !DILocation(line: 7, column: 1, scope: !6)
!24 = !DILocation(line: 8, column: 1, scope: !6)
!25 = !DILocation(line: 9, column: 1, scope: !6)
!26 = !DILocation(line: 10, column: 1, scope: !6)
!27 = distinct !DISubprogram(name: "function2", linkageName: "function2", scope: null, file: !1, line: 11, type: !7,
scopeLine: 11, spFlags: DISPFlagDefinition | DISPFlagOptimized, unit: !0, retainedNodes: !28)
!28 = !{!29, !30, !31, !32, !33, !34}
!29 = !DILocalVariable(name: "7", scope: !27, file: !1, line: 11, type: !10)
!30 = !DILocalVariable(name: "8", scope: !27, file: !1, line: 12, type: !10)
!31 = !DILocalVariable(name: "9", scope: !27, file: !1, line: 13, type: !10)
!32 = !DILocalVariable(name: "10",
scope: !27, file: !1, line: 17, type: !14)
!33 = !DILocalVariable(name: "11", scope: !27, file: !1, line: 18, type: !14)
!34 = !DILocalVariable(name: "12", scope: !27, file: !1, line: 19, type: !14)
!35 = !DILocation(line: 11, column: 1, scope: !27)
!36 = !DILocation(line: 12, column: 1, scope: !27)
!37 = !DILocation(line: 13, column: 1, scope: !27)
!38 = !DILocation(line: 14, column: 1, scope: !27)
!39 = !DILocation(line: 15, column: 1, scope: !27)
!40 = !DILocation(line: 16, column: 1, scope: !27)
!41 = !DILocation(line: 17, column: 1, scope: !27)
!42 = !DILocation(line: 18, column: 1, scope: !27)
!43 = !DILocation(line: 19, column: 1, scope: !27)
!44 = !DILocation(line: 20, column: 1, scope: !27)
; CHECK-LABEL: @function1(
; CHECK-NEXT: entry:
; CHECK-NEXT:  [[A:%.*]] = alloca i32, align 4, !dbg [[DBG17:![0-9]+]]
; CHECK-NEXT:  call void @llvm.dbg.value(metadata ptr [[A]], metadata [[META9:![0-9]+]], metadata
!DIExpression()), !dbg [[DBG17]]
; CHECK-NEXT:  [[B:%.*]] = alloca
i32, align 4, !dbg [[DBG18:![0-9]+]]
; CHECK-NEXT:  call void @llvm.dbg.value(metadata ptr [[B]], metadata [[META11:![0-9]+]], metadata
!DIExpression()), !dbg [[DBG18]]
; CHECK-NEXT:  [[C:%.*]] = alloca i32, align 4, !dbg [[DBG19:![0-9]+]]
; CHECK-NEXT:  call void @llvm.dbg.value(metadata ptr [[C]], metadata [[META12:![0-9]+]], metadata
!DIExpression()), !dbg [[DBG19]]
; CHECK-NEXT:  call void @outlined_ir_func_0(ptr [[A]], ptr [[B]], ptr [[C]]), !dbg [[DBG20:![0-9]+]]
; CHECK-NEXT:  ret void, !dbg [[DBG21:![0-9]+]]
;
;
; CHECK-LABEL: @function2(

```

```

; CHECK-NEXT: entry:
; CHECK-NEXT: [[A:%.*]] = alloca i32, align 4, !dbg [[DBG30:![0-9]+]]
; CHECK-NEXT: call void @llvm.dbg.value(metadata ptr [[A]], metadata [[META24:![0-9]+]], metadata
!DIExpression()), !dbg [[DBG30]]
; CHECK-NEXT: [[B:%.*]] = alloca i32, align 4, !dbg [[DBG31:![0-9]+]]
; CHECK-NEXT: call void @llvm.dbg.value(metadata ptr [[B]], metadata [[META25:![0-9]+]], metadata
!DIExpression()), !dbg [[DBG31]]
;
CHECK-NEXT: [[C:%.*]] = alloca i32, align 4, !dbg [[DBG32:![0-9]+]]
; CHECK-NEXT: call void @llvm.dbg.value(metadata ptr [[C]], metadata [[META26:![0-9]+]], metadata
!DIExpression()), !dbg [[DBG32]]
; CHECK-NEXT: call void @outlined_ir_func_0(ptr [[A]], ptr [[B]], ptr [[C]]), !dbg [[DBG33:![0-9]+]]
; CHECK-NEXT: ret void, !dbg [[DBG34:![0-9]+]]
;
;
; CHECK: @outlined_ir_func_0(ptr [[TMP0:%.*]], ptr [[TMP1:%.*]], ptr [[TMP2:%.*]])
; CHECK: entry_to_outline:
; CHECK-NEXT: store i32 2, ptr [[TMP0]], align 4
; CHECK-NEXT: store i32 3, ptr [[TMP1]], align 4
; CHECK-NEXT: store i32 4, ptr [[TMP2]], align 4
; CHECK-NEXT: [[AL:%.*]] = load i32, ptr [[TMP0]], align 4
; CHECK-NEXT: [[BL:%.*]] = load i32, ptr [[TMP1]], align 4
; CHECK-NEXT: [[CL:%.*]] = load i32, ptr [[TMP2]], align 4
; CHECK-NEXT: br label [[ENTRY_AFTER_OUTLINE_EXITSTUB:%.*]]
;
; RUN: opt < %s -passes=argpromotion -S | FileCheck %s

; CHECK-LABEL: define i32 @foo() #0 {
; CHECK-NEXT:    %.val = load <32 x half>, ptr undef, align 4
; CHECK-NEXT:    call void @bar(<32 x half> %.val)
; CHECK-NEXT:    ret i32 0
; CHECK-NEXT: }

; CHECK-LABEL: define internal void @bar(<32 x half> %.0.val) #0 {
; CHECK-NEXT:    ret void
; CHECK-NEXT: }

; CHECK: attributes #0 = { uwtable "min-legal-vector-width"="512" }

define i32 @foo() #0 {
call void @bar(ptr undef)
ret i32 0
}

define internal void @bar(ptr) #0 {
%2 = load <32 x half>, ptr %0, align 4
ret void
}

```


attributes #0 = { uwtable "min-legal-vector-width"="0" }

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```
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -mattr=+m -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefixes=CHECK,RV64I
; RUN: llc -mtriple=riscv64 -mattr=+m,+zba -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-
prefixes=CHECK,RV64ZBA,RV64ZBANOZBB
; RUN: llc -mtriple=riscv64 -mattr=+m,+zba,+zbb -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefixes=CHECK,RV64ZBA,RV64ZBAZBB
```

```
define i64 @slliuv(i64 %a) nounwind {
; RV64I-LABEL: slliuv:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 31
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: slliuv:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  slli.uw a0, a0, 1
; RV64ZBA-NEXT:  ret
%conv1 = shl i64 %a, 1
%shl = and i64 %conv1, 8589934590
ret i64 %shl
}
```

```
define i128 @slliuv_2(i32 signext %0, ptr %1) {
```

```

; RV64I-LABEL:
slliuw_2:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 28
; RV64I-NEXT:  add a1, a1, a0
; RV64I-NEXT:  ld a0, 0(a1)
; RV64I-NEXT:  ld a1, 8(a1)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: slliuw_2:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  slli.uw a0, a0, 4
; RV64ZBA-NEXT:  add a1, a1, a0
; RV64ZBA-NEXT:  ld a0, 0(a1)
; RV64ZBA-NEXT:  ld a1, 8(a1)
; RV64ZBA-NEXT:  ret
%3 = zext i32 %0 to i64
%4 = getelementptr inbounds i128, ptr %1, i64 %3
%5 = load i128, ptr %4
ret i128 %5
}

```

```

define i128 @slliuw_3(i32 signext %0, ptr %1) {
; RV64I-LABEL: slliuw_3:
; RV64I:    # %bb.0:
; RV64I-NEXT:  addi a0, a0, 1
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 28
; RV64I-NEXT:  add a1, a1, a0
; RV64I-NEXT:  ld a0, 0(a1)
; RV64I-NEXT:  ld a1, 8(a1)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: slliuw_3:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  addi a0, a0, 1
; RV64ZBA-NEXT:  slli.uw a0, a0, 4
; RV64ZBA-NEXT:
    add a1, a1, a0
; RV64ZBA-NEXT:  ld a0, 0(a1)
; RV64ZBA-NEXT:  ld a1, 8(a1)
; RV64ZBA-NEXT:  ret
%add = add i32 %0, 1
%3 = zext i32 %add to i64
%4 = getelementptr inbounds i128, ptr %1, i64 %3
%5 = load i128, ptr %4
ret i128 %5
}

```



```
}
```

```
define i64 @adduw(i64 %a, i64 %b) nounwind {  
; RV64I-LABEL: adduw:  
; RV64I:      # %bb.0:  
; RV64I-NEXT: slli a1, a1, 32  
; RV64I-NEXT: srli a1, a1, 32  
; RV64I-NEXT: add a0, a1, a0  
; RV64I-NEXT: ret  
;  
; RV64ZBA-LABEL: adduw:  
; RV64ZBA:    # %bb.0:  
; RV64ZBA-NEXT: add.uw a0, a1, a0  
; RV64ZBA-NEXT: ret  
%and = and i64 %b, 4294967295  
%add = add i64 %and, %a  
ret i64 %add  
}
```

```
define signext i8 @adduw_2(i32 signext %0, ptr %1) {  
; RV64I-LABEL: adduw_2:  
; RV64I:      # %bb.0:  
; RV64I-NEXT: slli a0, a0, 32  
; RV64I-NEXT: srli a0, a0, 32  
; RV64I-NEXT: add a0, a1, a0  
; RV64I-NEXT: lb a0, 0(a0)  
; RV64I-NEXT: ret  
;  
; RV64ZBA-LABEL: adduw_2:  
; RV64ZBA:    # %bb.0:  
; RV64ZBA-NEXT: add.uw a0, a0, a1  
; RV64ZBA-NEXT:  
    lb a0, 0(a0)  
; RV64ZBA-NEXT: ret  
%3 = zext i32 %0 to i64  
%4 = getelementptr inbounds i8, ptr %1, i64 %3  
%5 = load i8, ptr %4  
ret i8 %5  
}
```

```
define signext i8 @adduw_3(i32 signext %0, ptr %1) {  
; RV64I-LABEL: adduw_3:  
; RV64I:      # %bb.0:  
; RV64I-NEXT: addi a0, a0, 1  
; RV64I-NEXT: slli a0, a0, 32  
; RV64I-NEXT: srli a0, a0, 32  
; RV64I-NEXT: add a0, a1, a0  
; RV64I-NEXT: lb a0, 0(a0)
```

```

; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: adduw_3:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  addi a0, a0, 1
; RV64ZBA-NEXT:  add.uw a0, a0, a1
; RV64ZBA-NEXT:  lb a0, 0(a0)
; RV64ZBA-NEXT:  ret
%add = add i32 %0, 1
%3 = zext i32 %add to i64
%4 = getelementptr inbounds i8, ptr %1, i64 %3
%5 = load i8, ptr %4
ret i8 %5
}

```

```

define i64 @zextw_i64(i64 %a) nounwind {
; RV64I-LABEL: zextw_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: zextw_i64:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:
    zext.w a0, a0
; RV64ZBA-NEXT:  ret
%and = and i64 %a, 4294967295
ret i64 %and
}

```

; This makes sure targetShrinkDemandedConstant changes the and immediate to
; allow zext.w or slli+srli.

```

define i64 @zextw_demandedbits_i64(i64 %0) {
; RV64I-LABEL: zextw_demandedbits_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  ori a0, a0, 1
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: zextw_demandedbits_i64:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  ori a0, a0, 1
; RV64ZBA-NEXT:  zext.w a0, a0
; RV64ZBA-NEXT:  ret
%2 = and i64 %0, 4294967294
%3 = or i64 %2, 1

```

```

ret i64 %3
}

define signext i16 @sh1add(i64 %0, ptr %1) {
; RV64I-LABEL: sh1add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 1
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  lh a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sh1add:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh1add a0, a0, a1
; RV64ZBA-NEXT:  lh a0, 0(a0)
; RV64ZBA-NEXT:
    ret
%3 = getelementptr inbounds i16, ptr %1, i64 %0
%4 = load i16, ptr %3
ret i16 %4
}

```

```

define signext i32 @sh2add(i64 %0, ptr %1) {
; RV64I-LABEL: sh2add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 2
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  lw a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sh2add:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh2add a0, a0, a1
; RV64ZBA-NEXT:  lw a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = getelementptr inbounds i32, ptr %1, i64 %0
%4 = load i32, ptr %3
ret i32 %4
}

```

```

define i64 @sh3add(i64 %0, ptr %1) {
; RV64I-LABEL: sh3add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 3
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  ld a0, 0(a0)
; RV64I-NEXT:  ret
;

```

```

; RV64ZBA-LABEL: sh3add:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh3add a0, a0, a1
; RV64ZBA-NEXT:  ld a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = getelementptr inbounds i64, ptr %1, i64 %0
%4 = load i64, ptr %3
ret i64 %4
}

```

```

define signext i16 @sh1adduw(i32
signext %0, ptr %1) {
; RV64I-LABEL: sh1adduw:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 31
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  lh a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sh1adduw:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh1add.uw a0, a0, a1
; RV64ZBA-NEXT:  lh a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = zext i32 %0 to i64
%4 = getelementptr inbounds i16, ptr %1, i64 %3
%5 = load i16, ptr %4
ret i16 %5
}

```

```

define i64 @sh1adduw_2(i64 %0, i64 %1) {
; RV64I-LABEL: sh1adduw_2:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 31
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sh1adduw_2:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh1add.uw a0, a0, a1
; RV64ZBA-NEXT:  ret
%3 = shl i64 %0, 1
%4 = and i64 %3, 8589934590
%5 = add i64 %4, %1
ret i64 %5
}

```

```

define signext i32 @sh2adduw(i32 signext %0, ptr %1) {
; RV64I-LABEL: sh2adduw:
; RV64I:
    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 30
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  lw a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sh2adduw:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh2add.uw a0, a0, a1
; RV64ZBA-NEXT:  lw a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = zext i32 %0 to i64
%4 = getelementptr inbounds i32, ptr %1, i64 %3
%5 = load i32, ptr %4
ret i32 %5
}

```

```

define i64 @sh2adduw_2(i64 %0, i64 %1) {
; RV64I-LABEL: sh2adduw_2:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 30
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sh2adduw_2:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh2add.uw a0, a0, a1
; RV64ZBA-NEXT:  ret
%3 = shl i64 %0, 2
%4 = and i64 %3, 17179869180
%5 = add i64 %4, %1
ret i64 %5
}

```

```

define i64 @sh3adduw(i32 signext %0, ptr %1) {
; RV64I-LABEL: sh3adduw:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:
    srli a0, a0, 29
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  ld a0, 0(a0)

```

```

; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sh3adduw:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh3add.uw a0, a0, a1
; RV64ZBA-NEXT:  ld a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = zext i32 %0 to i64
%4 = getelementptr inbounds i64, ptr %1, i64 %3
%5 = load i64, ptr %4
ret i64 %5
}

```

```

define i64 @sh3adduw_2(i64 %0, i64 %1) {
; RV64I-LABEL: sh3adduw_2:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 29
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sh3adduw_2:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh3add.uw a0, a0, a1
; RV64ZBA-NEXT:  ret
%3 = shl i64 %0, 3
%4 = and i64 %3, 34359738360
%5 = add i64 %4, %1
ret i64 %5
}

```

; Type legalization inserts a sext_inreg after the first add. That add will be
; selected as sh2add which does not sign extend. SimplifyDemandedBits is unable
; to remove the sext_inreg because it has multiple uses.

The ashr will use the

; sext_inreg to become srai. This leaves the sext_inreg only used by the shl.

; If the shl is selected as sllw, we don't need the sext_inreg.

```
define i64 @sh2add_extra_sext(i32 %x, i32 %y, i32 %z) {
```

```

; RV64I-LABEL: sh2add_extra_sext:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 2
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  sllw a1, a2, a0
; RV64I-NEXT:  srai a0, a0, 2
; RV64I-NEXT:  mul a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sh2add_extra_sext:

```

```

; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh2add a0, a0, a1
; RV64ZBA-NEXT:  sllw a1, a2, a0
; RV64ZBA-NEXT:  sraiw a0, a0, 2
; RV64ZBA-NEXT:  mul a0, a1, a0
; RV64ZBA-NEXT:  ret
%a = shl i32 %x, 2
%b = add i32 %a, %y
%c = shl i32 %z, %b
%d = ashr i32 %b, 2
%e = sext i32 %c to i64
%f = sext i32 %d to i64
%g = mul i64 %e, %f
ret i64 %g
}

```

```

define i64 @addmul6(i64 %a, i64 %b) {
; RV64I-LABEL: addmul6:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a2, 6
; RV64I-NEXT:  mul
a0, a0, a2
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addmul6:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh1add a0, a0, a0
; RV64ZBA-NEXT:  sh1add a0, a0, a1
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 6
%d = add i64 %c, %b
ret i64 %d
}

```

```

define i64 @addmul10(i64 %a, i64 %b) {
; RV64I-LABEL: addmul10:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a2, 10
; RV64I-NEXT:  mul a0, a0, a2
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addmul10:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh2add a0, a0, a0
; RV64ZBA-NEXT:  sh1add a0, a0, a1
; RV64ZBA-NEXT:  ret

```

```

%c = mul i64 %a, 10
%d = add i64 %c, %b
ret i64 %d
}

```

```

define i64 @addmul12(i64 %a, i64 %b) {
; RV64I-LABEL: addmul12:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 12
; RV64I-NEXT:  mul a0, a0, a2
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addmul12:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh1add a0, a0, a0
; RV64ZBA-NEXT:  sh2add
a0, a0, a1
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 12
%d = add i64 %c, %b
ret i64 %d
}

```

```

define i64 @addmul18(i64 %a, i64 %b) {
; RV64I-LABEL: addmul18:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 18
; RV64I-NEXT:  mul a0, a0, a2
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addmul18:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh3add a0, a0, a0
; RV64ZBA-NEXT:  sh1add a0, a0, a1
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 18
%d = add i64 %c, %b
ret i64 %d
}

```

```

define i64 @addmul20(i64 %a, i64 %b) {
; RV64I-LABEL: addmul20:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 20
; RV64I-NEXT:  mul a0, a0, a2
; RV64I-NEXT:  add a0, a0, a1

```



```

; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addmul20:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh2add a0, a0, a0
; RV64ZBA-NEXT:  sh2add a0, a0, a1
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 20
%d = add i64 %c, %b
ret i64 %d
}

```

```

define i64 @addmul24(i64 %a, i64 %b) {
; RV64I-LABEL: addmul24:
; RV64I:
    # %bb.0:
; RV64I-NEXT:  li a2, 24
; RV64I-NEXT:  mul a0, a0, a2
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addmul24:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh1add a0, a0, a0
; RV64ZBA-NEXT:  sh3add a0, a0, a1
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 24
%d = add i64 %c, %b
ret i64 %d
}

```

```

define i64 @addmul36(i64 %a, i64 %b) {
; RV64I-LABEL: addmul36:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 36
; RV64I-NEXT:  mul a0, a0, a2
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addmul36:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh3add a0, a0, a0
; RV64ZBA-NEXT:  sh2add a0, a0, a1
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 36
%d = add i64 %c, %b
ret i64 %d
}

```

```

define i64 @addmul40(i64 %a, i64 %b) {
; RV64I-LABEL: addmul40:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 40
; RV64I-NEXT:  mul a0, a0, a2
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addmul40:
; RV64ZBA:    # %bb.0:
;
; RV64ZBA-NEXT: sh2add a0, a0, a0
; RV64ZBA-NEXT: sh3add a0, a0, a1
; RV64ZBA-NEXT: ret
%c = mul i64 %a, 40
%d = add i64 %c, %b
ret i64 %d
}

```

```

define i64 @addmul72(i64 %a, i64 %b) {
; RV64I-LABEL: addmul72:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 72
; RV64I-NEXT:  mul a0, a0, a2
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addmul72:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT: sh3add a0, a0, a0
; RV64ZBA-NEXT: sh3add a0, a0, a1
; RV64ZBA-NEXT: ret
%c = mul i64 %a, 72
%d = add i64 %c, %b
ret i64 %d
}

```

```

define i64 @mul96(i64 %a) {
; RV64I-LABEL: mul96:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 96
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul96:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT: sh1add a0, a0, a0

```

```

; RV64ZBA-NEXT:  slli a0, a0, 5
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 96
ret i64 %c
}

define i64 @mul160(i64 %a) {
; RV64I-LABEL: mul160:
; RV64I:      # %bb.0:
; RV64I-NEXT:
    li a1, 160
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul160:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh2add a0, a0, a0
; RV64ZBA-NEXT:  slli a0, a0, 5
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 160
ret i64 %c
}

```

```

define i64 @mul288(i64 %a) {
; RV64I-LABEL: mul288:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 288
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul288:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh3add a0, a0, a0
; RV64ZBA-NEXT:  slli a0, a0, 5
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 288
ret i64 %c
}

```

```

define i64 @zext_mul96(i32 signext %a) {
; RV64I-LABEL: zext_mul96:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 3
; RV64I-NEXT:  slli a1, a1, 37
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  mulhu a0, a0, a1
; RV64I-NEXT:  ret
;

```

```

; RV64ZBA-LABEL: zext_mul96:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  slli.uw a0, a0, 5
; RV64ZBA-NEXT:  sh1add a0, a0, a0
; RV64ZBA-NEXT:  ret
%b = zext
i32 %a to i64
%c = mul i64 %b, 96
ret i64 %c
}

```

```

define i64 @zext_mul160(i32 signext %a) {
; RV64I-LABEL: zext_mul160:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 5
; RV64I-NEXT:  slli a1, a1, 37
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  mulhu a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: zext_mul160:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  slli.uw a0, a0, 5
; RV64ZBA-NEXT:  sh2add a0, a0, a0
; RV64ZBA-NEXT:  ret
%b = zext i32 %a to i64
%c = mul i64 %b, 160
ret i64 %c
}

```

```

define i64 @zext_mul288(i32 signext %a) {
; RV64I-LABEL: zext_mul288:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 9
; RV64I-NEXT:  slli a1, a1, 37
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  mulhu a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: zext_mul288:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  slli.uw a0, a0, 5
; RV64ZBA-NEXT:  sh3add a0, a0, a0
; RV64ZBA-NEXT:  ret
%b = zext i32 %a to i64
%c = mul i64 %b, 288
ret i64 %c
}

```

```

; We can't use slli.uw becaues
the shift amount is more than 31.
; FIXME: The zext.w is unneeded.
define i64 @zext_mul12884901888(i32 signext %a) {
; RV64I-LABEL: zext_mul12884901888:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  li a1, 3
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: zext_mul12884901888:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  andi a0, a0, -1
; RV64ZBA-NEXT:  sh1add a0, a0, a0
; RV64ZBA-NEXT:  slli a0, a0, 32
; RV64ZBA-NEXT:  ret
%b = zext i32 %a to i64
%c = mul i64 %b, 12884901888
ret i64 %c
}

```

```

; We can't use slli.uw becaues the shift amount is more than 31.
; FIXME: The zext.w is unneeded.
define i64 @zext_mul21474836480(i32 signext %a) {
; RV64I-LABEL: zext_mul21474836480:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  li a1, 5
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:
ret
;
; RV64ZBA-LABEL: zext_mul21474836480:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  andi a0, a0, -1
; RV64ZBA-NEXT:  sh2add a0, a0, a0
; RV64ZBA-NEXT:  slli a0, a0, 32
; RV64ZBA-NEXT:  ret
%b = zext i32 %a to i64
%c = mul i64 %b, 21474836480
ret i64 %c
}

```

; We can't use slli.uw because the shift amount is more than 31.

; FIXME: The zext.w is unneeded.

define i64 @zext_mul38654705664(i32 signext %a) {

; RV64I-LABEL: zext_mul38654705664:

; RV64I: # %bb.0:

; RV64I-NEXT: slli a0, a0, 32

; RV64I-NEXT: srli a0, a0, 32

; RV64I-NEXT: li a1, 9

; RV64I-NEXT: slli a1, a1, 32

; RV64I-NEXT: mul a0, a0, a1

; RV64I-NEXT: ret

;

; RV64ZBA-LABEL: zext_mul38654705664:

; RV64ZBA: # %bb.0:

; RV64ZBA-NEXT: andi a0, a0, -1

; RV64ZBA-NEXT: sh3add a0, a0, a0

; RV64ZBA-NEXT: slli a0, a0, 32

; RV64ZBA-NEXT: ret

%b = zext i32 %a to i64

%c = mul i64 %b, 38654705664

ret i64 %c

}

define i64 @sh1add_imm(i64 %0) {

; CHECK-LABEL: sh1add_imm:

;

CHECK: # %bb.0:

; CHECK-NEXT: slli a0, a0, 1

; CHECK-NEXT: addi a0, a0, 5

; CHECK-NEXT: ret

%a = shl i64 %0, 1

%b = add i64 %a, 5

ret i64 %b

}

define i64 @sh2add_imm(i64 %0) {

; CHECK-LABEL: sh2add_imm:

; CHECK: # %bb.0:

; CHECK-NEXT: slli a0, a0, 2

; CHECK-NEXT: addi a0, a0, -6

; CHECK-NEXT: ret

%a = shl i64 %0, 2

%b = add i64 %a, -6

ret i64 %b

}

define i64 @sh3add_imm(i64 %0) {

```

; CHECK-LABEL: sh3add_imm:
; CHECK:      # %bb.0:
; CHECK-NEXT:  slli a0, a0, 3
; CHECK-NEXT:  addi a0, a0, 7
; CHECK-NEXT:  ret
%a = shl i64 %0, 3
%b = add i64 %a, 7
ret i64 %b
}

define i64 @sh1adduw_imm(i32 signext %0) {
; RV64I-LABEL: sh1adduw_imm:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 31
; RV64I-NEXT:  addi a0, a0, 11
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sh1adduw_imm:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  slli.uw a0, a0, 1
; RV64ZBA-NEXT:  addi a0, a0, 11
; RV64ZBA-NEXT:  ret
%a =
zext i32 %0 to i64
%b = shl i64 %a, 1
%c = add i64 %b, 11
ret i64 %c
}

define i64 @sh2adduw_imm(i32 signext %0) {
; RV64I-LABEL: sh2adduw_imm:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 30
; RV64I-NEXT:  addi a0, a0, -12
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sh2adduw_imm:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  slli.uw a0, a0, 2
; RV64ZBA-NEXT:  addi a0, a0, -12
; RV64ZBA-NEXT:  ret
%a = zext i32 %0 to i64
%b = shl i64 %a, 2
%c = add i64 %b, -12
ret i64 %c
}

```

```

define i64 @sh3adduw_imm(i32 signext %0) {
; RV64I-LABEL: sh3adduw_imm:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 29
; RV64I-NEXT:  addi a0, a0, 13
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sh3adduw_imm:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  slli.uw a0, a0, 3
; RV64ZBA-NEXT:  addi a0, a0, 13
; RV64ZBA-NEXT:  ret
%a = zext i32 %0 to i64
%b = shl i64 %a, 3
%c = add i64 %b, 13
ret i64 %c
}

```

```

define i64
@adduw_imm(i32 signext %0) nounwind {
; RV64I-LABEL: adduw_imm:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  addi a0, a0, 5
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: adduw_imm:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  zext.w a0, a0
; RV64ZBA-NEXT:  addi a0, a0, 5
; RV64ZBA-NEXT:  ret
%a = zext i32 %0 to i64
%b = add i64 %a, 5
ret i64 %b
}

```

```

define i64 @mul258(i64 %a) {
; CHECK-LABEL: mul258:
; CHECK:      # %bb.0:
; CHECK-NEXT:  li a1, 258
; CHECK-NEXT:  mul a0, a0, a1
; CHECK-NEXT:  ret
%c = mul i64 %a, 258
ret i64 %c
}

```



```

define i64 @mul260(i64 %a) {
; CHECK-LABEL: mul260:
; CHECK:      # %bb.0:
; CHECK-NEXT:  li a1, 260
; CHECK-NEXT:  mul a0, a0, a1
; CHECK-NEXT:  ret
    %c = mul i64 %a, 260
    ret i64 %c
}

```

```

define i64 @mul264(i64 %a) {
; CHECK-LABEL: mul264:
; CHECK:      # %bb.0:
; CHECK-NEXT:  li a1, 264
; CHECK-NEXT:  mul a0, a0, a1
; CHECK-NEXT:  ret
    %c = mul i64 %a, 264
    ret i64
    %c
}

```

```

define i64 @imm_zextw() nounwind {
; RV64I-LABEL: imm_zextw:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a0, 1
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  addi a0, a0, -2
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: imm_zextw:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  li a0, -2
; RV64ZBA-NEXT:  zext.w a0, a0
; RV64ZBA-NEXT:  ret
    ret i64 4294967294 ; -2 in 32 bits.
}

```

```

define i64 @mul11(i64 %a) {
; RV64I-LABEL: mul11:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 11
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul11:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh2add a1, a0, a0

```

```
; RV64ZBA-NEXT:  sh1add a0, a1, a0
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 11
ret i64 %c
}
```

```
define i64 @mul19(i64 %a) {
; RV64I-LABEL: mul19:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 19
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul19:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh3add a1, a0, a0
; RV64ZBA-NEXT:  sh1add a0,
a1, a0
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 19
ret i64 %c
}
```

```
define i64 @mul13(i64 %a) {
; RV64I-LABEL: mul13:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 13
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul13:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh1add a1, a0, a0
; RV64ZBA-NEXT:  sh2add a0, a1, a0
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 13
ret i64 %c
}
```

```
define i64 @mul21(i64 %a) {
; RV64I-LABEL: mul21:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 21
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul21:
; RV64ZBA:    # %bb.0:
```

```

; RV64ZBA-NEXT:  sh2add a1, a0, a0
; RV64ZBA-NEXT:  sh2add a0, a1, a0
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 21
ret i64 %c
}

```

```

define i64 @mul37(i64 %a) {
; RV64I-LABEL: mul37:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 37
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul37:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh3add a1, a0, a0
; RV64ZBA-NEXT:
    sh2add a0, a1, a0
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 37
ret i64 %c
}

```

```

define i64 @mul25(i64 %a) {
; RV64I-LABEL: mul25:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 25
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul25:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh1add a1, a0, a0
; RV64ZBA-NEXT:  sh3add a0, a1, a0
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 25
ret i64 %c
}

```

```

define i64 @mul41(i64 %a) {
; RV64I-LABEL: mul41:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 41
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul41:

```

```

; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh2add a1, a0, a0
; RV64ZBA-NEXT:  sh3add a0, a1, a0
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 41
ret i64 %c
}

```

```

define i64 @mul73(i64 %a) {
; RV64I-LABEL: mul73:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a1, 73
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul73:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh3add
a1, a0, a0
; RV64ZBA-NEXT:  sh3add a0, a1, a0
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 73
ret i64 %c
}

```

```

define i64 @mul27(i64 %a) {
; RV64I-LABEL: mul27:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a1, 27
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul27:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh3add a0, a0, a0
; RV64ZBA-NEXT:  sh1add a0, a0, a0
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 27
ret i64 %c
}

```

```

define i64 @mul45(i64 %a) {
; RV64I-LABEL: mul45:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a1, 45
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;

```

```

; RV64ZBA-LABEL: mul45:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh3add a0, a0, a0
; RV64ZBA-NEXT:  sh2add a0, a0, a0
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 45
ret i64 %c
}

```

```

define i64 @mul81(i64 %a) {
; RV64I-LABEL: mul81:
; RV64I:    # %bb.0:
; RV64I-NEXT:  li a1, 81
; RV64I-NEXT:  mul a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul81:
; RV64ZBA:    # %bb.0:
;
; RV64ZBA-NEXT:  sh3add a0, a0, a0
; RV64ZBA-NEXT:  sh3add a0, a0, a0
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 81
ret i64 %c
}

```

```

define i64 @mul4098(i64 %a) {
; RV64I-LABEL: mul4098:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a1, a0, 1
; RV64I-NEXT:  slli a0, a0, 12
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul4098:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  slli a1, a0, 12
; RV64ZBA-NEXT:  sh1add a0, a0, a1
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 4098
ret i64 %c
}

```

```

define i64 @mul4100(i64 %a) {
; RV64I-LABEL: mul4100:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a1, a0, 2
; RV64I-NEXT:  slli a0, a0, 12

```

```

; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul4100:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  slli a1, a0, 12
; RV64ZBA-NEXT:  sh2add a0, a0, a1
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 4100
ret i64 %c
}

```

```

define i64 @mul4104(i64 %a) {
; RV64I-LABEL: mul4104:
; RV64I:        # %bb.0:
; RV64I-NEXT:
    slli a1, a0, 3
; RV64I-NEXT:  slli a0, a0, 12
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: mul4104:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  slli a1, a0, 12
; RV64ZBA-NEXT:  sh3add a0, a0, a1
; RV64ZBA-NEXT:  ret
%c = mul i64 %a, 4104
ret i64 %c
}

```

```

define signext i32 @mulw192(i32 signext %a) {
; CHECK-LABEL: mulw192:
; CHECK:        # %bb.0:
; CHECK-NEXT:   li a1, 192
; CHECK-NEXT:   mulw a0, a0, a1
; CHECK-NEXT:   ret
%c = mul i32 %a, 192
ret i32 %c
}

```

```

define signext i32 @mulw320(i32 signext %a) {
; CHECK-LABEL: mulw320:
; CHECK:        # %bb.0:
; CHECK-NEXT:   li a1, 320
; CHECK-NEXT:   mulw a0, a0, a1
; CHECK-NEXT:   ret
%c = mul i32 %a, 320
ret i32 %c
}

```

```
}
```

```
define signext i32 @mulw576(i32 signext %a) {  
; CHECK-LABEL: mulw576:  
; CHECK:      # %bb.0:  
; CHECK-NEXT:  li a1, 576  
; CHECK-NEXT:  mulw a0, a0, a1  
; CHECK-NEXT:  ret  
%c = mul i32 %a, 576  
ret i32 %c  
}
```

```
define i64 @add4104(i64 %a) {  
; RV64I-LABEL: add4104:  
; RV64I:  
    # %bb.0:  
; RV64I-NEXT:  lui a1, 1  
; RV64I-NEXT:  addiw a1, a1, 8  
; RV64I-NEXT:  add a0, a0, a1  
; RV64I-NEXT:  ret  
;  
; RV64ZBA-LABEL: add4104:  
; RV64ZBA:      # %bb.0:  
; RV64ZBA-NEXT:  li a1, 1026  
; RV64ZBA-NEXT:  sh2add a0, a1, a0  
; RV64ZBA-NEXT:  ret  
%c = add i64 %a, 4104  
ret i64 %c  
}
```

```
define i64 @add8208(i64 %a) {  
; RV64I-LABEL: add8208:  
; RV64I:      # %bb.0:  
; RV64I-NEXT:  lui a1, 2  
; RV64I-NEXT:  addiw a1, a1, 16  
; RV64I-NEXT:  add a0, a0, a1  
; RV64I-NEXT:  ret  
;  
; RV64ZBA-LABEL: add8208:  
; RV64ZBA:      # %bb.0:  
; RV64ZBA-NEXT:  li a1, 1026  
; RV64ZBA-NEXT:  sh3add a0, a1, a0  
; RV64ZBA-NEXT:  ret  
%c = add i64 %a, 8208  
ret i64 %c  
}
```

; Make sure we prefer LUI for the 8192 instead of using sh3add.

```

define signext i32 @add8192_i32(i32 signext %a) {
; CHECK-LABEL: add8192_i32:
; CHECK:      # %bb.0:
; CHECK-NEXT:  lui a1, 2
; CHECK-NEXT:  addw a0, a0, a1
; CHECK-NEXT:  ret
%c = add i32 %a, 8192
ret i32 %c
}

; Make sure we prefer LUI
for the 8192 instead of using sh3add.
define i64 @add8192(i64 %a) {
; CHECK-LABEL: add8192:
; CHECK:      # %bb.0:
; CHECK-NEXT:  lui a1, 2
; CHECK-NEXT:  add a0, a0, a1
; CHECK-NEXT:  ret
%c = add i64 %a, 8192
ret i64 %c
}

define signext i32 @addshl32_5_6(i32 signext %a, i32 signext %b) {
; RV64I-LABEL: addshl32_5_6:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 5
; RV64I-NEXT:  slli a1, a1, 6
; RV64I-NEXT:  addw a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addshl32_5_6:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  sh1add a0, a1, a0
; RV64ZBA-NEXT:  slliw a0, a0, 5
; RV64ZBA-NEXT:  ret
%c = shl i32 %a, 5
%d = shl i32 %b, 6
%e = add i32 %c, %d
ret i32 %e
}

define i64 @addshl64_5_6(i64 %a, i64 %b) {
; RV64I-LABEL: addshl64_5_6:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 5
; RV64I-NEXT:  slli a1, a1, 6
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret

```



```

;
; RV64ZBA-LABEL: addshl64_5_6:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:
    sh1add a0, a1, a0
; RV64ZBA-NEXT:  slli a0, a0, 5
; RV64ZBA-NEXT:  ret
%c = shl i64 %a, 5
%d = shl i64 %b, 6
%e = add i64 %c, %d
ret i64 %e
}

```

```

define signext i32 @addshl32_5_7(i32 signext %a, i32 signext %b) {
; RV64I-LABEL: addshl32_5_7:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 5
; RV64I-NEXT:  slli a1, a1, 7
; RV64I-NEXT:  addw a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addshl32_5_7:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh2add a0, a1, a0
; RV64ZBA-NEXT:  slliw a0, a0, 5
; RV64ZBA-NEXT:  ret
%c = shl i32 %a, 5
%d = shl i32 %b, 7
%e = add i32 %c, %d
ret i32 %e
}

```

```

define i64 @addshl64_5_7(i64 %a, i64 %b) {
; RV64I-LABEL: addshl64_5_7:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 5
; RV64I-NEXT:  slli a1, a1, 7
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addshl64_5_7:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh2add a0, a1, a0
; RV64ZBA-NEXT:  slli a0, a0, 5
; RV64ZBA-NEXT:  ret
%c
= shl i64 %a, 5
%d = shl i64 %b, 7

```

```

    %e = add i64 %c, %d
    ret i64 %e
}

define signext i32 @addshl32_5_8(i32 signext %a, i32 signext %b) {
; RV64I-LABEL: addshl32_5_8:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 5
; RV64I-NEXT:  slli a1, a1, 8
; RV64I-NEXT:  addw a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addshl32_5_8:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh3add a0, a1, a0
; RV64ZBA-NEXT:  slliw a0, a0, 5
; RV64ZBA-NEXT:  ret
    %c = shl i32 %a, 5
    %d = shl i32 %b, 8
    %e = add i32 %c, %d
    ret i32 %e
}

define i64 @addshl64_5_8(i64 %a, i64 %b) {
; RV64I-LABEL: addshl64_5_8:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 5
; RV64I-NEXT:  slli a1, a1, 8
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: addshl64_5_8:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  sh3add a0, a1, a0
; RV64ZBA-NEXT:  slli a0, a0, 5
; RV64ZBA-NEXT:  ret
    %c = shl i64 %a, 5
    %d = shl i64 %b, 8
    %e = add i64 %c, %d
    ret i64 %e
}

; Make
; sure we use sext.h+slli+srli for Zba+Zbb.
; FIXME: The RV64I and Zba only cases can be done with only 3 shifts.
define zeroext i32 @sext_ashr_zext_i8(i8 %a) nounwind {
; RV64I-LABEL: sext_ashr_zext_i8:
; RV64I:      # %bb.0:

```

```

; RV64I-NEXT:  slli a0, a0, 24
; RV64I-NEXT:  sraiw a0, a0, 31
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  ret
;
; RV64ZBANOBZBB-LABEL: sext_ashr_zext_i8:
; RV64ZBANOBZBB:    # %bb.0:
; RV64ZBANOBZBB-NEXT:  slli a0, a0, 24
; RV64ZBANOBZBB-NEXT:  sraiw a0, a0, 31
; RV64ZBANOBZBB-NEXT:  zext.w a0, a0
; RV64ZBANOBZBB-NEXT:  ret
;
; RV64ZBAZBB-LABEL: sext_ashr_zext_i8:
; RV64ZBAZBB:    # %bb.0:
; RV64ZBAZBB-NEXT:  sext.b a0, a0
; RV64ZBAZBB-NEXT:  sraiw a0, a0, 9
; RV64ZBAZBB-NEXT:  zext.w a0, a0
; RV64ZBAZBB-NEXT:  ret
%ext = sext i8 %a to i32
%1 = ashr i32 %ext, 9
ret i32 %1
}

; Make sure we use sext.h+slli+srli for Zba+Zbb.
; FIXME: The RV64I and Zba only cases can be done with only 3 shifts.
define
  zeroext i32 @sext_ashr_zext_i16(i16 %a) nounwind {
; RV64I-LABEL: sext_ashr_zext_i16:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 16
; RV64I-NEXT:  sraiw a0, a0, 25
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  ret
;
; RV64ZBANOBZBB-LABEL: sext_ashr_zext_i16:
; RV64ZBANOBZBB:    # %bb.0:
; RV64ZBANOBZBB-NEXT:  slli a0, a0, 16
; RV64ZBANOBZBB-NEXT:  sraiw a0, a0, 25
; RV64ZBANOBZBB-NEXT:  zext.w a0, a0
; RV64ZBANOBZBB-NEXT:  ret
;
; RV64ZBAZBB-LABEL: sext_ashr_zext_i16:
; RV64ZBAZBB:    # %bb.0:
; RV64ZBAZBB-NEXT:  slli a0, a0, 48
; RV64ZBAZBB-NEXT:  srai a0, a0, 57
; RV64ZBAZBB-NEXT:  zext.w a0, a0

```

```
; RV64ZBAZBB-NEXT:  ret
%ext = sext i16 %a to i32
%1 = ashr i32 %ext, 9
ret i32 %1
}
```

; This the IR you get from InstCombine if take the difference of 2 pointers and
; cast is to unsigned before using as an index.

```
define signext i16 @sh1adduw_ptrdiff(i64 %diff, ptr %baseptr) {
```

```
; RV64I-LABEL: sh1adduw_ptrdiff:
```

```
; RV64I:
```

```
    # %bb.0:
```

```
; RV64I-NEXT:  li a2, 1
```

```
; RV64I-NEXT:  slli a2, a2, 33
```

```
; RV64I-NEXT:  addi a2, a2, -2
```

```
; RV64I-NEXT:  and a0, a0, a2
```

```
; RV64I-NEXT:  add a0, a1, a0
```

```
; RV64I-NEXT:  lh a0, 0(a0)
```

```
; RV64I-NEXT:  ret
```

```
;
```

```
; RV64ZBA-LABEL: sh1adduw_ptrdiff:
```

```
; RV64ZBA:    # %bb.0:
```

```
; RV64ZBA-NEXT: srli a0, a0, 1
```

```
; RV64ZBA-NEXT: sh1add.uw a0, a0, a1
```

```
; RV64ZBA-NEXT: lh a0, 0(a0)
```

```
; RV64ZBA-NEXT: ret
```

```
%ptrdiff = lshr exact i64 %diff, 1
```

```
%cast = and i64 %ptrdiff, 4294967295
```

```
%ptr = getelementptr inbounds i16, ptr %baseptr, i64 %cast
```

```
%res = load i16, ptr %ptr
```

```
ret i16 %res
```

```
}
```

```
define signext i32 @sh2adduw_ptrdiff(i64 %diff, ptr %baseptr) {
```

```
; RV64I-LABEL: sh2adduw_ptrdiff:
```

```
; RV64I:    # %bb.0:
```

```
; RV64I-NEXT:  li a2, 1
```

```
; RV64I-NEXT:  slli a2, a2, 34
```

```
; RV64I-NEXT:  addi a2, a2, -4
```

```
; RV64I-NEXT:  and a0, a0, a2
```

```
; RV64I-NEXT:  add a0, a1, a0
```

```
; RV64I-NEXT:  lw a0, 0(a0)
```

```
; RV64I-NEXT:  ret
```

```
;
```

```
; RV64ZBA-LABEL: sh2adduw_ptrdiff:
```

```
; RV64ZBA:    # %bb.0:
```

```
; RV64ZBA-NEXT:
```

```

    srli a0, a0, 2
; RV64ZBA-NEXT:  sh2add.uw a0, a0, a1
; RV64ZBA-NEXT:  lw a0, 0(a0)
; RV64ZBA-NEXT:  ret
%ptrdiff = lshr exact i64 %diff, 2
%cast = and i64 %ptrdiff, 4294967295
%ptr = getelementptr inbounds i32, ptr %baseptr, i64 %cast
%res = load i32, ptr %ptr
ret i32 %res
}

```

```

define i64 @sh3adduw_ptrdiff(i64 %diff, ptr %baseptr) {
; RV64I-LABEL: sh3adduw_ptrdiff:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 1
; RV64I-NEXT:  slli a2, a2, 35
; RV64I-NEXT:  addi a2, a2, -8
; RV64I-NEXT:  and a0, a0, a2
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  ld a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sh3adduw_ptrdiff:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  srli a0, a0, 3
; RV64ZBA-NEXT:  sh3add.uw a0, a0, a1
; RV64ZBA-NEXT:  ld a0, 0(a0)
; RV64ZBA-NEXT:  ret
%ptrdiff = lshr exact i64 %diff, 3
%cast = and i64 %ptrdiff, 4294967295
%ptr = getelementptr inbounds i64, ptr %baseptr, i64 %cast
%res = load i64, ptr %ptr
ret i64 %res
}

```

```

define signext
i16 @srliw_1_sh1add(ptr %0, i32 signext %1) {
; RV64I-LABEL: srliw_1_sh1add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srliw a1, a1, 1
; RV64I-NEXT:  slli a1, a1, 1
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  lh a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: srliw_1_sh1add:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  srliw a1, a1, 1

```

```

; RV64ZBA-NEXT:  sh1add a0, a1, a0
; RV64ZBA-NEXT:  lh a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = lshr i32 %1, 1
%4 = zext i32 %3 to i64
%5 = getelementptr inbounds i16, ptr %0, i64 %4
%6 = load i16, ptr %5, align 2
ret i16 %6
}

define i128 @sliuw_ptrdiff(i64 %diff, ptr %baseptr) {
; RV64I-LABEL: sliuw_ptrdiff:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a2, 1
; RV64I-NEXT:  slli a2, a2, 36
; RV64I-NEXT:  addi a2, a2, -16
; RV64I-NEXT:  and a0, a0, a2
; RV64I-NEXT:  add a1, a1, a0
; RV64I-NEXT:  ld a0, 0(a1)
; RV64I-NEXT:  ld a1, 8(a1)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: sliuw_ptrdiff:
; RV64ZBA:    # %bb.0:
;
RV64ZBA-NEXT:  srli a0, a0, 4
; RV64ZBA-NEXT:  slli.uw a0, a0, 4
; RV64ZBA-NEXT:  add a1, a1, a0
; RV64ZBA-NEXT:  ld a0, 0(a1)
; RV64ZBA-NEXT:  ld a1, 8(a1)
; RV64ZBA-NEXT:  ret
%ptrdiff = lshr exact i64 %diff, 4
%cast = and i64 %ptrdiff, 4294967295
%ptr = getelementptr inbounds i128, ptr %baseptr, i64 %cast
%res = load i128, ptr %ptr
ret i128 %res
}

define signext i32 @srliw_2_sh2add(ptr %0, i32 signext %1) {
; RV64I-LABEL: srliw_2_sh2add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srliw a1, a1, 2
; RV64I-NEXT:  slli a1, a1, 2
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  lw a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: srliw_2_sh2add:

```

```

; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  srlw a1, a1, 2
; RV64ZBA-NEXT:  sh2add a0, a1, a0
; RV64ZBA-NEXT:  lw a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = lshr i32 %1, 2
%4 = zext i32 %3 to i64
%5 = getelementptr inbounds i32, ptr %0, i64 %4
%6 = load i32, ptr %5, align 4
ret i32 %6
}

```

```

define i64 @srlw_3_sh3add(ptr
%0, i32 signext %1) {
; RV64I-LABEL: srlw_3_sh3add:
; RV64I:    # %bb.0:
; RV64I-NEXT:  srlw a1, a1, 3
; RV64I-NEXT:  slli a1, a1, 3
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ld a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: srlw_3_sh3add:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  srlw a1, a1, 3
; RV64ZBA-NEXT:  sh3add a0, a1, a0
; RV64ZBA-NEXT:  ld a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = lshr i32 %1, 3
%4 = zext i32 %3 to i64
%5 = getelementptr inbounds i64, ptr %0, i64 %4
%6 = load i64, ptr %5, align 8
ret i64 %6
}

```

```

define signext i32 @srlw_1_sh2add(ptr %0, i32 signext %1) {
; RV64I-LABEL: srlw_1_sh2add:
; RV64I:    # %bb.0:
; RV64I-NEXT:  srlw a1, a1, 1
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  srli a1, a1, 30
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  lw a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: srlw_1_sh2add:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  srlw a1, a1, 1

```

```

; RV64ZBA-NEXT:  sh2add a0, a1, a0
;
RV64ZBA-NEXT:  lw a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = lshr i32 %1, 1
%4 = zext i32 %3 to i64
%5 = getelementptr inbounds i32, ptr %0, i64 %4
%6 = load i32, ptr %5, align 4
ret i32 %6
}

define i64 @srliw_1_sh3add(ptr %0, i32 signext %1) {
; RV64I-LABEL: srliw_1_sh3add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srliw a1, a1, 1
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  srli a1, a1, 29
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ld a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: srliw_1_sh3add:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  srliw a1, a1, 1
; RV64ZBA-NEXT:  sh3add a0, a1, a0
; RV64ZBA-NEXT:  ld a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = lshr i32 %1, 1
%4 = zext i32 %3 to i64
%5 = getelementptr inbounds i64, ptr %0, i64 %4
%6 = load i64, ptr %5, align 8
ret i64 %6
}

define i64 @srliw_2_sh3add(ptr %0, i32 signext %1) {
; RV64I-LABEL: srliw_2_sh3add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srliw a1, a1, 2
; RV64I-NEXT:  slli a1, a1, 32
;
RV64I-NEXT:  srli a1, a1, 29
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ld a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: srliw_2_sh3add:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  srliw a1, a1, 2

```



```

; RV64ZBA-NEXT:  sh3add a0, a1, a0
; RV64ZBA-NEXT:  ld a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = lshr i32 %1, 2
%4 = zext i32 %3 to i64
%5 = getelementptr inbounds i64, ptr %0, i64 %4
%6 = load i64, ptr %5, align 8
ret i64 %6
}

```

```

define signext i16 @srliw_2_sh1add(ptr %0, i32 signext %1) {
; RV64I-LABEL: srliw_2_sh1add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srliw a1, a1, 2
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  srli a1, a1, 31
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  lh a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: srliw_2_sh1add:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  srliw a1, a1, 2
; RV64ZBA-NEXT:  sh1add a0, a1, a0
; RV64ZBA-NEXT:  lh a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = lshr i32 %1, 2
%4 = zext i32 %3 to i64
%5 = getelementptr
inbounds i16, ptr %0, i64 %4
%6 = load i16, ptr %5, align 2
ret i16 %6
}

```

```

define signext i32 @srliw_3_sh2add(ptr %0, i32 signext %1) {
; RV64I-LABEL: srliw_3_sh2add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srliw a1, a1, 3
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  srli a1, a1, 30
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  lw a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: srliw_3_sh2add:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  srliw a1, a1, 3

```

```

; RV64ZBA-NEXT:  sh2add a0, a1, a0
; RV64ZBA-NEXT:  lw a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = lshr i32 %1, 3
%4 = zext i32 %3 to i64
%5 = getelementptr inbounds i32, ptr %0, i64 %4
%6 = load i32, ptr %5, align 4
ret i32 %6
}

define i64 @srliw_4_sh3add(ptr %0, i32 signext %1) {
; RV64I-LABEL: srliw_4_sh3add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srliw a1, a1, 4
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  srli a1, a1, 29
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ld a0, 0(a0)
; RV64I-NEXT:
    ret
;
; RV64ZBA-LABEL: srliw_4_sh3add:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  srliw a1, a1, 4
; RV64ZBA-NEXT:  sh3add a0, a1, a0
; RV64ZBA-NEXT:  ld a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = lshr i32 %1, 4
%4 = zext i32 %3 to i64
%5 = getelementptr inbounds i64, ptr %0, i64 %4
%6 = load i64, ptr %5, align 8
ret i64 %6
}

define signext i32 @srli_1_sh2add(ptr %0, i64 %1) {
; RV64I-LABEL: srli_1_sh2add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a1, a1, 1
; RV64I-NEXT:  andi a1, a1, -4
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  lw a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: srli_1_sh2add:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  srli a1, a1, 1
; RV64ZBA-NEXT:  sh2add a0, a1, a0
; RV64ZBA-NEXT:  lw a0, 0(a0)

```

```
; RV64ZBA-NEXT:  ret
%3 = lshr i64 %1, 1
%4 = getelementptr inbounds i32, ptr %0, i64 %3
%5 = load i32, ptr %4, align 4
ret i32 %5
}
```

```
define i64 @srli_2_sh3add(ptr %0, i64 %1) {
; RV64I-LABEL: srli_2_sh3add:
; RV64I:      # %bb.0:
;
RV64I-NEXT:  slli a1, a1, 1
; RV64I-NEXT:  andi a1, a1, -8
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ld a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: srli_2_sh3add:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  srli a1, a1, 2
; RV64ZBA-NEXT:  sh3add a0, a1, a0
; RV64ZBA-NEXT:  ld a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = lshr i64 %1, 2
%4 = getelementptr inbounds i64, ptr %0, i64 %3
%5 = load i64, ptr %4, align 8
ret i64 %5
}
```

```
define signext i16 @srli_2_sh1add(ptr %0, i64 %1) {
; RV64I-LABEL: srli_2_sh1add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srli a1, a1, 1
; RV64I-NEXT:  andi a1, a1, -2
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  lh a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: srli_2_sh1add:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  srli a1, a1, 2
; RV64ZBA-NEXT:  sh1add a0, a1, a0
; RV64ZBA-NEXT:  lh a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = lshr i64 %1, 2
%4 = getelementptr inbounds i16, ptr %0, i64 %3
%5 = load i16, ptr %4, align
```

```

2
ret i16 %5
}

define signext i32 @srli_3_sh2add(ptr %0, i64 %1) {
; RV64I-LABEL: srli_3_sh2add:
; RV64I:      # %bb.0:
; RV64I-NEXT: srli a1, a1, 1
; RV64I-NEXT: andi a1, a1, -4
; RV64I-NEXT: add a0, a0, a1
; RV64I-NEXT: lw a0, 0(a0)
; RV64I-NEXT: ret
;
; RV64ZBA-LABEL: srli_3_sh2add:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT: srli a1, a1, 3
; RV64ZBA-NEXT: sh2add a0, a1, a0
; RV64ZBA-NEXT: lw a0, 0(a0)
; RV64ZBA-NEXT: ret
%3 = lshr i64 %1, 3
%4 = getelementptr inbounds i32, ptr %0, i64 %3
%5 = load i32, ptr %4, align 4
ret i32 %5
}

define i64 @srli_4_sh3add(ptr %0, i64 %1) {
; RV64I-LABEL: srli_4_sh3add:
; RV64I:      # %bb.0:
; RV64I-NEXT: srli a1, a1, 1
; RV64I-NEXT: andi a1, a1, -8
; RV64I-NEXT: add a0, a0, a1
; RV64I-NEXT: ld a0, 0(a0)
; RV64I-NEXT: ret
;
; RV64ZBA-LABEL: srli_4_sh3add:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT: srli a1, a1, 4
; RV64ZBA-NEXT: sh3add a0, a1, a0
; RV64ZBA-NEXT: ld a0, 0(a0)
; RV64ZBA-NEXT:
ret
%3 = lshr i64 %1, 4
%4 = getelementptr inbounds i64, ptr %0, i64 %3
%5 = load i64, ptr %4, align 8
ret i64 %5
}

define signext i16 @shl_2_sh1add(ptr %0, i32 signext %1) {

```

```

; RV64I-LABEL: shl_2_sh1add:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a1, a1, 2
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  srli a1, a1, 31
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  lh a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: shl_2_sh1add:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  slli a1, a1, 2
; RV64ZBA-NEXT:  zext.w a1, a1
; RV64ZBA-NEXT:  sh1add a0, a1, a0
; RV64ZBA-NEXT:  lh a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = shl i32 %1, 2
%4 = zext i32 %3 to i64
%5 = getelementptr inbounds i16, ptr %0, i64 %4
%6 = load i16, ptr %5, align 2
ret i16 %6
}

define signext i32 @shl_16_sh2add(ptr %0, i32 signext %1) {
; RV64I-LABEL: shl_16_sh2add:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a1, a1, 16
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  srli a1, a1, 30
;
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  lw a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: shl_16_sh2add:
; RV64ZBA:    # %bb.0:
; RV64ZBA-NEXT:  slli a1, a1, 16
; RV64ZBA-NEXT:  zext.w a1, a1
; RV64ZBA-NEXT:  sh2add a0, a1, a0
; RV64ZBA-NEXT:  lw a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = shl i32 %1, 16
%4 = zext i32 %3 to i64
%5 = getelementptr inbounds i32, ptr %0, i64 %4
%6 = load i32, ptr %5, align 4
ret i32 %6
}

```

```

define i64 @shl_31_sh3add(ptr %0, i32 signext %1) {
; RV64I-LABEL: shl_31_sh3add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a1, a1, 31
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  srli a1, a1, 29
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ld a0, 0(a0)
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: shl_31_sh3add:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  slli a1, a1, 31
; RV64ZBA-NEXT:  zext.w a1, a1
; RV64ZBA-NEXT:  sh3add a0, a1, a0
; RV64ZBA-NEXT:  ld a0, 0(a0)
; RV64ZBA-NEXT:  ret
%3 = shl i32 %1, 31
%4 = zext i32 %3
to i64
%5 = getelementptr inbounds i64, ptr %0, i64 %4
%6 = load i64, ptr %5, align 8
ret i64 %6
}

define i64 @pack_i64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: pack_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: pack_i64:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  slli a1, a1, 32
; RV64ZBA-NEXT:  add.uw a0, a0, a1
; RV64ZBA-NEXT:  ret
%shl = and i64 %a, 4294967295
%shl1 = shl i64 %b, 32
%or = or i64 %shl1, %shl
ret i64 %or
}

define i64 @pack_i64_2(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: pack_i64_2:
; RV64I:      # %bb.0:

```

```

; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: pack_i64_2:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  slli a1, a1, 32
; RV64ZBA-NEXT:  add.uw a0, a0,
a1
; RV64ZBA-NEXT:  ret
%zexta = zext i32 %a to i64
%zextb = zext i32 %b to i64
%shl1 = shl i64 %zextb, 32
%or = or i64 %shl1, %zexta
ret i64 %or
}

```

```

define i64 @pack_i64_3(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: pack_i64_3:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi a0, a0, 1
; RV64I-NEXT:  addi a1, a1, 1
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBA-LABEL: pack_i64_3:
; RV64ZBA:      # %bb.0:
; RV64ZBA-NEXT:  addi a0, a0, 1
; RV64ZBA-NEXT:  addi a1, a1, 1
; RV64ZBA-NEXT:  slli a1, a1, 32
; RV64ZBA-NEXT:  add.uw a0, a0, a1
; RV64ZBA-NEXT:  ret
%adda = add i32 %a, 1
%addb = add i32 %b, 1
%zexta = zext i32 %adda to i64
%zextb = zext i32 %addb to i64
%shl1 = shl i64 %zextb, 32
%or = or i64 %shl1, %zexta
ret i64 %or
}

```

```

=====
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```
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -mattr=+zbb -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefix=RV64ZBB
```

```
declare i32 @llvm.riscv.orc.b.i32(i32)
```

```
define signext i32 @orc32(i32 signext %a) nounwind {
; RV64ZBB-LABEL: orc32:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  orc.b a0, a0
; RV64ZBB-NEXT:  sext.w a0, a0
; RV64ZBB-NEXT:  ret
  %tmp = call i32 @llvm.riscv.orc.b.i32(i32 %a)
  ret i32 %tmp
}
```

```
define zeroext i32 @orc32_zext(i32 zeroext %a) nounwind {
; RV64ZBB-LABEL: orc32_zext:
; RV64ZBB:      # %bb.0:
```

```
; RV64ZBB-NEXT:   orc.b a0, a0
; RV64ZBB-NEXT:   ret
    %tmp = call i32 @llvm.riscv.orc.b.i32(i32 %a)
    ret i32 %tmp
}
```

; Second and+or is redundant with the first, make sure we remove them.

```
define signext i32 @orc32_knownbits(i32 signext %a) nounwind {
; RV64ZBB-LABEL: orc32_knownbits:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT: lui a1, 1044480
; RV64ZBB-NEXT:
    and a0, a0, a1
; RV64ZBB-NEXT: lui a1, 2048
; RV64ZBB-NEXT: addi a1, a1, 1
; RV64ZBB-NEXT: or a0, a0, a1
; RV64ZBB-NEXT: orc.b a0, a0
; RV64ZBB-NEXT: sext.w a0, a0
; RV64ZBB-NEXT: ret
    %tmp = and i32 %a, 4278190080 ; 0xFF000000
    %tmp2 = or i32 %tmp, 8388609 ; 0x800001
    %tmp3 = call i32 @llvm.riscv.orc.b.i32(i32 %tmp2)
    %tmp4 = and i32 %tmp3, 4278190080 ; 0xFF000000
    %tmp5 = or i32 %tmp4, 16711935 ; 0xFF00FF
    ret i32 %tmp5
}
```

```
declare i64 @llvm.riscv.orc.b.i64(i64)
```

```
define i64 @orc64(i64 %a) nounwind {
; RV64ZBB-LABEL: orc64:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT: orc.b a0, a0
; RV64ZBB-NEXT: ret
    %tmp = call i64 @llvm.riscv.orc.b.i64(i64 %a)
    ret i64 %tmp
}
```

; Second and+or is redundant with the first, make sure we remove them.

```
define i64 @orc64_knownbits(i64 %a) nounwind {
; RV64ZBB-LABEL: orc64_knownbits:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT: lui a1, 65535
; RV64ZBB-NEXT: slli a1, a1, 12
; RV64ZBB-NEXT: and a0, a0, a1
;
    RV64ZBB-NEXT: lui a1, 256
; RV64ZBB-NEXT: addiw a1, a1, 8
```

```

; RV64ZBB-NEXT:  slli a2, a1, 42
; RV64ZBB-NEXT:  add a1, a1, a2
; RV64ZBB-NEXT:  or a0, a0, a1
; RV64ZBB-NEXT:  orc.b a0, a0
; RV64ZBB-NEXT:  ret
%tmp = and i64 %a, 1099494850560 ; 0x000000ffff000000
%tmp2 = or i64 %tmp, 4611721202800525320 ; 0x4000200000100008
%tmp3 = call i64 @llvm.riscv.orc.b.i64(i64 %tmp2)
%tmp4 = and i64 %tmp3, 1099494850560 ; 0x000000ffff000000
%tmp5 = or i64 %tmp4, 18374966855153418495 ; 0xff00ff0000ff00ff
ret i64 %tmp5
}

```

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```

; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -mattr=+zbc -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefix=RV64ZBC

```

```

declare i64 @llvm.riscv.clmulr.i64(i64 %a, i64 %b)

```

```

define i64 @clmul64r(i64 %a, i64 %b) nounwind {
; RV64ZBC-LABEL: clmul64r:
; RV64ZBC:      # %bb.0:
; RV64ZBC-NEXT:  clmulr a0, a0, a1
; RV64ZBC-NEXT:  ret
%tmp = call i64 @llvm.riscv.clmulr.i64(i64 %a, i64 %b)
ret i64 %tmp
}

```



```
declare i32 @llvm.riscv.clmulr.i32(i32 %a, i32 %b)
```

```
define signext i32 @clmul32r(i32 signext %a, i32 signext %b) nounwind {  
; RV64ZBC-LABEL: clmul32r:  
; RV64ZBC:      # %bb.0:  
; RV64ZBC-NEXT: slli a1, a1, 32  
; RV64ZBC-NEXT: slli a0, a0, 32  
; RV64ZBC-NEXT: clmulr a0, a0, a1  
; RV64ZBC-NEXT: srai a0, a0, 32  
; RV64ZBC-NEXT: ret  
%tmp = call i32 @llvm.riscv.clmulr.i32(i32 %a, i32 %b)  
ret i32 %tmp  
}
```

; FIXME: We could avoid the slli instructions by using clmul+srli+sext.w
since

; the inputs are zero extended.

```
define signext i32 @clmul32r_zext(i32 zeroext %a, i32 zeroext %b) nounwind {  
; RV64ZBC-LABEL: clmul32r_zext:  
; RV64ZBC:      # %bb.0:  
; RV64ZBC-NEXT: slli a1, a1, 32  
; RV64ZBC-NEXT: slli a0, a0, 32  
; RV64ZBC-NEXT: clmulr a0, a0, a1  
; RV64ZBC-NEXT: srai a0, a0, 32  
; RV64ZBC-NEXT: ret  
%tmp = call i32 @llvm.riscv.clmulr.i32(i32 %a, i32 %b)  
ret i32 %tmp  
}  
; RUN: opt %s -passes=inline -S | FileCheck %s
```

```
define internal void @innerSmall() "min-legal-vector-width"="128" {  
ret void  
}
```

```
define internal void @innerLarge() "min-legal-vector-width"="512" {  
ret void  
}
```

```
define internal void @innerNoAttribute() {  
ret void  
}
```

; We should not add an attribute during inlining. No attribute means unknown.
; Inlining doesn't change the fact that we don't know anything about this
; function.

```
define void @outerNoAttribute() {  
call void @innerLarge()  
ret void  
}
```

```

}

define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
  call void @innerLarge()
  ret void
}

define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
  call void @innerSmall()
  ret void
}

; We should remove the attribute after inlining since the callee's
; vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
  call void @innerNoAttribute()
  ret void
}

; CHECK: define void @outerNoAttribute()
; {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }
; RUN: opt -mtriple=aarch64-linux-gnu -mattr=+sve -passes=sanitize-masked-mem-intrin -S < %s | FileCheck %s

; Testing that masked scatters operating on scalable vectors that are
; packed in SVE registers are not scalarized.

; CHECK-LABEL: @masked_scatter_nxv4i32(
; CHECK: call void @llvm.masked.scatter.nxv4i32
define void @masked_scatter_nxv4i32(<vscale x 4 x i32> %data, <vscale x 4 x ptr> %ptrs, <vscale x 4 x i1>
%mask) {
  call void @llvm.masked.scatter.nxv4i32(<vscale x 4 x i32> %data, <vscale x 4 x ptr> %ptrs, i32 0, <vscale x 4 x
i1> %mask)
  ret void
}

; Testing that masked scatters operating on scalable vectors of FP
; data that is packed in SVE registers are not scalarized.

; CHECK-LABEL: @masked_scatter_nxv2f64(
; CHECK: call void @llvm.masked.scatter.nxv2f64
define void @masked_scatter_nxv2f64(<vscale x 2 x double> %data, <vscale x 2 x ptr> %ptrs, <vscale x 2 x i1>
%mask) {
  call void @llvm.masked.scatter.nxv2f64(<vscale x 2 x double> %data, <vscale x 2 x ptr> %ptrs,

```

```

i32 0, <vscale x 2 x i1> %masks)
ret void
}

; Testing that masked scatters operating on scalable vectors of FP
; data that is unpacked in SVE registers are not scalarized.

; CHECK-LABEL: @masked_scatter_nxv2f16(
; CHECK: call void @llvm.masked.scatter.nxv2f16
define void @masked_scatter_nxv2f16(<vscale x 2 x half> %data, <vscale x 2 x ptr> %ptrs, <vscale x 2 x i1>
%.masks) {
    call void @llvm.masked.scatter.nxv2f16(<vscale x 2 x half> %data, <vscale x 2 x ptr> %ptrs, i32 0, <vscale x 2 x
i1> %masks)
    ret void
}

; Testing that masked scatters operating on 64-bit fixed vectors are
; scalarized because NEON doesn't have support for masked scatter
; instructions.

; CHECK-LABEL: @masked_scatter_v2f32(
; CHECK-NOT: @llvm.masked.scatter.v2f32(
define void @masked_scatter_v2f32(<2 x float> %data, <2 x ptr> %ptrs, <2 x i1> %masks) {
    call void @llvm.masked.scatter.v2f32(<2 x float> %data, <2 x ptr> %ptrs, i32 0, <2 x i1> %masks)
    ret void
}

; Testing that masked scatters operating on 128-bit
fixed vectors are
; scalarized because NEON doesn't have support for masked scatter
; instructions and because we are not targeting fixed width SVE.

; CHECK-LABEL: @masked_scatter_v4i32(
; CHECK-NOT: @llvm.masked.scatter.v4i32(
define void @masked_scatter_v4i32(<4 x i32> %data, <4 x ptr> %ptrs, <4 x i1> %masks) {
    call void @llvm.masked.scatter.v4i32(<4 x i32> %data, <4 x ptr> %ptrs, i32 0, <4 x i1> %masks)
    ret void
}

declare void @llvm.masked.scatter.nxv4i32(<vscale x 4 x i32> %data, <vscale x 4 x ptr> %ptrs, i32 %align,
<vscale x 4 x i1> %masks)
declare void @llvm.masked.scatter.nxv2f64(<vscale x 2 x double> %data, <vscale x 2 x ptr> %ptrs, i32 %align,
<vscale x 2 x i1> %masks)
declare void @llvm.masked.scatter.nxv2f16(<vscale x 2 x half> %data, <vscale x 2 x ptr> %ptrs, i32 %align,
<vscale x 2 x i1> %masks)
declare void @llvm.masked.scatter.v2f32(<2 x float> %data, <2 x ptr> %ptrs, i32 %align, <2 x i1> %masks)
declare void @llvm.masked.scatter.v4i32(<4 x i32> %data, <4 x

```

```
ptr> %ptrs, i32 %align, <4 x i1> %masks)
! RUN: %python %S/../test_errors.py %s %flang -fopenmp -Werror -pedantic
! OpenMP Version 5.0
! 2.19.4.4 firstprivate Clause
! 2.19.4.5 lastprivate Clause
! 2.19.6.1 copyin Clause
! 2.19.6.2 copyprivate Clause
! If the list item is a polymorphic variable with the allocatable attribute,
! the behavior is unspecified.
```

```
subroutine firstprivate()
  class(*), allocatable, save :: x
```

!PORTABILITY: If a polymorphic variable with allocatable attribute 'x' is in FIRSTPRIVATE clause, the behavior is unspecified

```
!$omp parallel firstprivate(x)
  call sub()
!$omp end parallel
```

```
end
```

```
subroutine lastprivate()
  class(*), allocatable, save :: x
```

!PORTABILITY: If a polymorphic variable with allocatable attribute 'x' is in LASTPRIVATE clause, the behavior is unspecified

```
!$omp do lastprivate(x)
do i = 1, 10
  call sub()
enddo
!$omp end do
```

```
end
```

```
subroutine copyin()
  class(*), allocatable, save :: x
!$omp threadprivate(x)
```

!PORTABILITY: If a polymorphic variable with allocatable attribute 'x' is in COPYIN clause, the behavior is unspecified

```
!$omp parallel copyin(x)
  call sub()
!$omp end parallel
```

```
end
```

```
subroutine copyprivate()
  class(*), allocatable, save :: x
```

!\$omp threadprivate(x)

!\$omp single

call sub()

!PORTABILITY: If a polymorphic variable with allocatable attribute 'x' is in COPYPRIVATE clause, the behavior is unspecified

!\$omp end single copyprivate(x)

end

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```
static_library("BSD-Archive") {  
    output_name = "lldbPluginObjectContainerBSDArchive"
```

```

configs += [ "//llvm/utils/gn/build:lldb_code" ]
deps = [
    "//lldb/source/Core",
    "//lldb/source/Host",
    "//lldb/source/Symbol",
    "//llvm/lib/Support",
]
sources = [ "ObjectContainerBSDArchive.cpp" ]
}
; RUN: opt -mtriple=aarch64-linux-gnu -mattr=+sve -passes=sccp,scalarize-masked-mem-intrin -S <%s | FileCheck %s

; Testing that masked gathers operating on scalable vectors that are
; packed in SVE registers are not scalarized.

; CHECK-LABEL: @masked_gather_nxv4i32(
; CHECK: call <vscale x 4 x i32> @llvm.masked.gather.nxv4i32
define <vscale x 4 x i32> @masked_gather_nxv4i32(<vscale x 4 x ptr> %ld, <vscale x 4 x i1> %masks, <vscale x 4
x i32> %passthru) {
    %res = call <vscale x 4 x i32> @llvm.masked.gather.nxv4i32(<vscale x 4 x ptr> %ld, i32 0, <vscale x 4 x i1>
%masks, <vscale x 4 x i32> %passthru)
    ret <vscale x 4 x i32> %res
}

; Testing that masked gathers operating on scalable vectors of FP data
; that is packed in SVE registers are not scalarized.

; CHECK-LABEL: @masked_gather_nxv2f64(
; CHECK: call <vscale x 2 x double> @llvm.masked.gather.nxv2f64
define <vscale x 2 x double> @masked_gather_nxv2f64(<vscale x 2 x ptr> %ld, <vscale x 2 x i1> %masks, <vscale
x 2 x double> %passthru)
{
    %res = call <vscale x 2 x double> @llvm.masked.gather.nxv2f64(<vscale x 2 x ptr> %ld, i32 0, <vscale x 2 x i1>
%masks, <vscale x 2 x double> %passthru)
    ret <vscale x 2 x double> %res
}

; Testing that masked gathers operating on scalable vectors of FP data
; that is unpacked in SVE registers are not scalarized.

; CHECK-LABEL: @masked_gather_nxv2f16(
; CHECK: call <vscale x 2 x half> @llvm.masked.gather.nxv2f16
define <vscale x 2 x half> @masked_gather_nxv2f16(<vscale x 2 x ptr> %ld, <vscale x 2 x i1> %masks, <vscale x
2 x half> %passthru) {
    %res = call <vscale x 2 x half> @llvm.masked.gather.nxv2f16(<vscale x 2 x ptr> %ld, i32 0, <vscale x 2 x i1>
%masks, <vscale x 2 x half> %passthru)
    ret <vscale x 2 x half> %res
}

```

; Testing that masked gathers operating on 64-bit fixed vectors are
; scalarized because NEON doesn't have support for masked gather
; instructions.

```
; CHECK-LABEL: @masked_gather_v2f32(  
; CHECK-NOT: @llvm.masked.gather.v2f32(  
define <2 x float> @masked_gather_v2f32(<2  
  x ptr> %ld, <2 x i1> %masks, <2 x float> %passthru) {  
  %res = call <2 x float> @llvm.masked.gather.v2f32(<2 x ptr> %ld, i32 0, <2 x i1> %masks, <2 x float> %passthru)  
  ret <2 x float> %res  
}
```

; Testing that masked gathers operating on 128-bit fixed vectors are
; scalarized because NEON doesn't have support for masked gather
; instructions and because we are not targeting fixed width SVE.

```
; CHECK-LABEL: @masked_gather_v4i32(  
; CHECK-NOT: @llvm.masked.gather.v4i32(  
define <4 x i32> @masked_gather_v4i32(<4 x ptr> %ld, <4 x i1> %masks, <4 x i32> %passthru) {  
  %res = call <4 x i32> @llvm.masked.gather.v4i32(<4 x ptr> %ld, i32 0, <4 x i1> %masks, <4 x i32> %passthru)  
  ret <4 x i32> %res  
}
```

```
declare <vscale x 4 x i32> @llvm.masked.gather.nxv4i32(<vscale x 4 x ptr> %ptrs, i32 %align, <vscale x 4 x i1>  
  %masks, <vscale x 4 x i32> %passthru)  
declare <vscale x 2 x double> @llvm.masked.gather.nxv2f64(<vscale x 2 x ptr> %ptrs, i32 %align, <vscale x 2 x  
  i1> %masks, <vscale x 2 x double>  
  %passthru)  
declare <vscale x 2 x half> @llvm.masked.gather.nxv2f16(<vscale x 2 x ptr> %ptrs, i32 %align, <vscale x 2 x i1>  
  %masks, <vscale x 2 x half> %passthru)  
declare <2 x float> @llvm.masked.gather.v2f32(<2 x ptr> %ptrs, i32 %align, <2 x i1> %masks, <2 x float>  
  %passthru)  
declare <4 x i32> @llvm.masked.gather.v4i32(<4 x ptr> %ptrs, i32 %align, <4 x i1> %masks, <4 x i32> %passthru)  
# RUN: llc -O0 -mtriple=m68k -start-after=prologuepilog -verify-machineinstrs %s -o - | FileCheck %s
```

name: is-pcrel-register-operand-legal

body: |

bb.0.entry:

```
; CHECK: move.l (0,%pc,%a0), (%a1)  
; CHECK: move.l (%a0), (0,%pc,%a1)
```

MOV32jk \$a1, 0, \$a0, implicit-def \$ccr

MOV32kj 0, \$a1, \$a0, implicit-def \$ccr

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py

; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s

;

; D31946

; Check that we dont end up with the ""LLVM ERROR: Cannot select" error.

; Additionally ensure that the output code actually put fp128 values in SSE registers.

declare fp128 @llvm.fabs.f128(fp128)

declare fp128 @llvm.copysign.f128(fp128, fp128)

define fp128 @TestSelect(fp128 %a, fp128 %b) {

; CHECK-LABEL: TestSelect:

; CHECK: # %bb.0:

; CHECK-NEXT: pushq %rbx

; CHECK-NEXT: .cfi_def_cfa_offset 16

; CHECK-NEXT: subq \$32, %rsp

; CHECK-NEXT: .cfi_def_cfa_offset 48

; CHECK-NEXT: .cfi_offset %rbx, -16

; CHECK-NEXT: movaps %xmm1, {[[-0-9]+]}(%r{[sb]})p) # 16-byte Spill

; CHECK-NEXT: movaps %xmm0, (%rsp) # 16-byte Spill

; CHECK-NEXT: callq __gttf2@PLT

; CHECK-NEXT: movl %eax, %ebx

; CHECK-NEXT: movaps (%rsp), %xmm0 # 16-byte Reload

; CHECK-NEXT: movaps {[[-0-9]+]}(%r{[sb]})p),

%xmm1 # 16-byte Reload

; CHECK-NEXT: callq __subtf3@PLT

; CHECK-NEXT: testl %ebx, %ebx

; CHECK-NEXT: jg .LBB0_2

; CHECK-NEXT: # %bb.1:

; CHECK-NEXT: xorps %xmm0, %xmm0

; CHECK-NEXT: .LBB0_2:

; CHECK-NEXT: addq \$32, %rsp

; CHECK-NEXT: .cfi_def_cfa_offset 16

; CHECK-NEXT: popq %rbx

; CHECK-NEXT: .cfi_def_cfa_offset 8

; CHECK-NEXT: retq

%cmp = fcmp ogt fp128 %a, %b

%sub = fsub fp128 %a, %b

%res = select i1 %cmp, fp128 %sub, fp128 0xL00000000000000000000000000000000

```

ret fp128 %res
}

define fp128 @TestFabs(fp128 %a) {
; CHECK-LABEL: TestFabs:
; CHECK:      # %bb.0:
; CHECK-NEXT: andps {{\.?LCPI[0-9]+\_[0-9]+\}}(%rip), %xmm0
; CHECK-NEXT: retq
%res = call fp128 @llvm.fabs.f128(fp128 %a)
ret fp128 %res
}

define fp128 @TestCopysign(fp128 %a, fp128 %b) {
; CHECK-LABEL: TestCopysign:
; CHECK:      # %bb.0:
; CHECK-NEXT: andps {{\.?LCPI[0-9]+\_[0-9]+\}}(%rip), %xmm1
; CHECK-NEXT: andps {{\.?LCPI[0-9]+\_[0-9]+\}}(%rip), %xmm0
; CHECK-NEXT:
    orps %xmm1, %xmm0
; CHECK-NEXT: retq
%res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
ret fp128 %res
}

define fp128 @TestFneg(fp128 %a) {
; CHECK-LABEL: TestFneg:
; CHECK:      # %bb.0:
; CHECK-NEXT: pushq %rax
; CHECK-NEXT: .cfi_def_cfa_offset 16
; CHECK-NEXT: movaps %xmm0, %xmm1
; CHECK-NEXT: callq __multf3@PLT
; CHECK-NEXT: xorps {{\.?LCPI[0-9]+\_[0-9]+\}}(%rip), %xmm0
; CHECK-NEXT: popq %rax
; CHECK-NEXT: .cfi_def_cfa_offset 8
; CHECK-NEXT: retq
%mul = fmul fp128 %a, %a
%res = fsub fp128 0xL00000000000000008000000000000000, %mul
ret fp128 %res
}

```

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -mattr=+zbkb -verify-machineinstrs < %s \
; RUN: | FileCheck %s -check-prefix=RV64ZBKB

declare i64 @llvm.riscv.brev8.i64(i64)

define i64 @brev8(i64 %a) nounwind {

```

; RV64ZBKB-LABEL: brev8:
; RV64ZBKB:      # %bb.0:
; RV64ZBKB-NEXT:  brev8 a0, a0
; RV64ZBKB-NEXT:  ret
%val = call i64 @llvm.riscv.brev8.i64(i64 %a)
ret i64 %val
}

; Test that rev8 is recognized as preserving zero extension.
define zeroext i16 @brev8_knownbits(i16 zeroext %a) nounwind {
; RV64ZBKB-LABEL: brev8_knownbits:
; RV64ZBKB:      # %bb.0:
; RV64ZBKB-NEXT:  brev8 a0, a0
; RV64ZBKB-NEXT:  ret
%zext = zext i16 %a to i64
%val = call i64 @llvm.riscv.brev8.i64(i64 %zext)
%trunc = trunc i64 %val to i16
ret i16 %trunc
}

declare i64 @llvm.bswap.i64(i64)

define i64 @rev8_i64(i64 %a) {
; RV64ZBKB-LABEL: rev8_i64:
; RV64ZBKB:      # %bb.0:
; RV64ZBKB-NEXT:  rev8 a0, a0
; RV64ZBKB-NEXT:  ret
%1 = call i64 @llvm.bswap.i64(i64 %a)
ret i64 %1
}

declare i32 @llvm.riscv.brev8.i32(i32)

define signext i32 @brev8_i32(i32 signext %a) nounwind {
; RV64ZBKB-LABEL: brev8_i32:
; RV64ZBKB:      # %bb.0:
; RV64ZBKB-NEXT:  brev8 a0, a0
; RV64ZBKB-NEXT:  sext.w a0, a0
; RV64ZBKB-NEXT:  ret
%val = call i32 @llvm.riscv.brev8.i32(i32 %a)
ret i32 %val
}

; Test that rev8 is recognized as preserving zero extension.
define zeroext i16 @brev8_i32_knownbits(i16 zeroext %a) nounwind {
; RV64ZBKB-LABEL: brev8_i32_knownbits:
; RV64ZBKB:      # %bb.0:
; RV64ZBKB-NEXT:  brev8 a0, a0

```

```

; RV64ZBKB-NEXT:  ret
%zext = zext i16 %a to i32
%val = call i32 @llvm.riscv.brev8.i32(i32 %zext)
%trunc = trunc i32 %val to i16
ret i16 %trunc
}

declare i32 @llvm.bswap.i32(i32)

define signext i32 @rev8_i32(i32 signext %a) {
; RV64ZBKB-LABEL: rev8_i32:
; RV64ZBKB:      # %bb.0:
; RV64ZBKB-NEXT:  rev8 a0, a0
; RV64ZBKB-NEXT:  srai a0, a0, 32
; RV64ZBKB-NEXT:  ret
%1 = call i32 @llvm.bswap.i32(i32
%a)
ret i32 %1
}

; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=amdgc -mcpu=fiji < %s | FileCheck -check-prefixes=VI %s

; FIXME: This one should fold to rcp
define half @select_fneg_posk_src_rcp_f16(i32 %c, half %x, half %y) {
; VI-LABEL: select_fneg_posk_src_rcp_f16:
; VI:      ; %bb.0:
; VI-NEXT:  s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; VI-NEXT:  v_rcp_f16_e64 v1, -v1
; VI-NEXT:  v_mov_b32_e32 v2, 0x4000
; VI-NEXT:  v_cmp_eq_u32_e32 vcc, 0, v0
; VI-NEXT:  v_cndmask_b32_e32 v0, v2, v1, vcc
; VI-NEXT:  s_setpc_b64 s[30:31]
%cmp = icmp eq i32 %c, 0
%rcp = call half @llvm.amdgcn.rcp.f16(half %x)
%fneg = fneg half %rcp
%select = select i1 %cmp, half %fneg, half 2.0
ret half %select
}

declare half @llvm.amdgcn.rcp.f16(half) #0

attributes #0 = { nocallback noreturn nosync nounwind speculatable willreturn memory(none) }
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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -verify-machineinstrs < %s \
; RUN:  -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefixes=CHECK,RV64I
; RUN: llc -mtriple=riscv64 -mattr=+zbb -verify-machineinstrs < %s \
; RUN:  -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefixes=CHECK,RV64ZBB-ZBKB,RV64ZBB

```

```
; RUN: llc -mtriple=riscv64 -mattr=+zbbk -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefixes=CHECK,RV64ZBB-
ZBKB,RV64ZBKB
```

```
define signext i32 @andn_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: andn_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  not a1, a1
; RV64I-NEXT:  and a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBB-ZBKB-LABEL: andn_i32:
; RV64ZBB-ZBKB:  # %bb.0:
; RV64ZBB-ZBKB-NEXT:  andn a0, a0, a1
; RV64ZBB-ZBKB-NEXT:  ret
%neg = xor i32 %b, -1
%and = and i32 %neg, %a
ret i32 %and
}
```

```
define i64 @andn_i64(i64 %a, i64
%b) nounwind {
; RV64I-LABEL: andn_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  not a1, a1
; RV64I-NEXT:  and a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBB-ZBKB-LABEL: andn_i64:
; RV64ZBB-ZBKB:  # %bb.0:
; RV64ZBB-ZBKB-NEXT:  andn a0, a0, a1
; RV64ZBB-ZBKB-NEXT:  ret
%neg = xor i64 %b, -1
%and = and i64 %neg, %a
ret i64 %and
}
```

```
define signext i32 @orn_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: orn_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  not a1, a1
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64ZBB-ZBKB-LABEL: orn_i32:
; RV64ZBB-ZBKB:  # %bb.0:
; RV64ZBB-ZBKB-NEXT:  orn a0, a0, a1
; RV64ZBB-ZBKB-NEXT:  ret
```

```

%neg = xor i32 %b, -1
%or = or i32 %neg, %a
ret i32 %or
}

```

```

define i64 @orn_i64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: orn_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT: not a1, a1
; RV64I-NEXT: or a0, a1, a0
; RV64I-NEXT: ret
;
; RV64ZBB-ZBKB-LABEL: orn_i64:
; RV64ZBB-ZBKB:  # %bb.0:
; RV64ZBB-ZBKB-NEXT:
    orn a0, a0, a1
; RV64ZBB-ZBKB-NEXT: ret
%neg = xor i64 %b, -1
%or = or i64 %neg, %a
ret i64 %or
}

```

```

define signext i32 @xnor_i32(i32 signext %a, i32 signext %b) nounwind {
; CHECK-LABEL: xnor_i32:
; CHECK:      # %bb.0:
; CHECK-NEXT: xor a0, a0, a1
; CHECK-NEXT: not a0, a0
; CHECK-NEXT: ret
%neg = xor i32 %a, -1
%xor = xor i32 %neg, %b
ret i32 %xor
}

```

```

define i64 @xnor_i64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: xnor_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT: xor a0, a0, a1
; RV64I-NEXT: not a0, a0
; RV64I-NEXT: ret
;
; RV64ZBB-ZBKB-LABEL: xnor_i64:
; RV64ZBB-ZBKB:  # %bb.0:
; RV64ZBB-ZBKB-NEXT: xnor a0, a0, a1
; RV64ZBB-ZBKB-NEXT: ret
%neg = xor i64 %a, -1
%xor = xor i64 %neg, %b
ret i64 %xor
}

```

```

declare i32 @llvm.fshl.i32(i32, i32, i32)

define signext i32 @rol_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: rol_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT: andi a2, a1, -1
; RV64I-NEXT: sllw a1, a0, a1
; RV64I-NEXT:
    negw a2, a2
; RV64I-NEXT: srlw a0, a0, a2
; RV64I-NEXT: or a0, a1, a0
; RV64I-NEXT: ret
;
; RV64ZBB-ZBKB-LABEL: rol_i32:
; RV64ZBB-ZBKB:      # %bb.0:
; RV64ZBB-ZBKB-NEXT: rolw a0, a0, a1
; RV64ZBB-ZBKB-NEXT: ret
    %1 = tail call i32 @llvm.fshl.i32(i32 %a, i32 %a, i32 %b)
    ret i32 %1
}

; Similar to rol_i32, but doesn't sign extend the result.
define void @rol_i32_nosext(i32 signext %a, i32 signext %b, ptr %x) nounwind {
; RV64I-LABEL: rol_i32_nosext:
; RV64I:      # %bb.0:
; RV64I-NEXT: andi a3, a1, -1
; RV64I-NEXT: sllw a1, a0, a1
; RV64I-NEXT: negw a3, a3
; RV64I-NEXT: srlw a0, a0, a3
; RV64I-NEXT: or a0, a1, a0
; RV64I-NEXT: sw a0, 0(a2)
; RV64I-NEXT: ret
;
; RV64ZBB-ZBKB-LABEL: rol_i32_nosext:
; RV64ZBB-ZBKB:      # %bb.0:
; RV64ZBB-ZBKB-NEXT: rolw a0, a0, a1
; RV64ZBB-ZBKB-NEXT: sw a0, 0(a2)
; RV64ZBB-ZBKB-NEXT: ret
    %1 = tail call i32 @llvm.fshl.i32(i32 %a, i32 %a, i32 %b)
    store i32 %1, ptr %x
    ret void
}

define signext
i32 @rol_i32_neg_constant_rhs(i32 signext %a) nounwind {
; RV64I-LABEL: rol_i32_neg_constant_rhs:
; RV64I:      # %bb.0:

```



```

; RV64I-NEXT: andi a1, a0, -1
; RV64I-NEXT: li a2, -2
; RV64I-NEXT: sllw a0, a2, a0
; RV64I-NEXT: negw a1, a1
; RV64I-NEXT: srlw a1, a2, a1
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: ret
;
; RV64ZBB-ZBKB-LABEL: rol_i32_neg_constant_rhs:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT: li a1, -2
; RV64ZBB-ZBKB-NEXT: rolw a0, a1, a0
; RV64ZBB-ZBKB-NEXT: ret
%1 = tail call i32 @llvm.fshl.i32(i32 -2, i32 -2, i32 %a)
ret i32 %1
}

```

```
declare i64 @llvm.fshl.i64(i64, i64, i64)
```

```

define i64 @rol_i64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: rol_i64:
; RV64I:    # %bb.0:
; RV64I-NEXT: sll a2, a0, a1
; RV64I-NEXT: negw a1, a1
; RV64I-NEXT: srl a0, a0, a1
; RV64I-NEXT: or a0, a2, a0
; RV64I-NEXT: ret
;
; RV64ZBB-ZBKB-LABEL: rol_i64:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT: rol a0, a0, a1
; RV64ZBB-ZBKB-NEXT:
ret
%or = tail call i64 @llvm.fshl.i64(i64 %a, i64 %a, i64 %b)
ret i64 %or
}

```

```
declare i32 @llvm.fshr.i32(i32, i32, i32)
```

```

define signext i32 @ror_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: ror_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT: andi a2, a1, -1
; RV64I-NEXT: srlw a1, a0, a1
; RV64I-NEXT: negw a2, a2
; RV64I-NEXT: sllw a0, a0, a2
; RV64I-NEXT: or a0, a1, a0
; RV64I-NEXT: ret

```

```

;
; RV64ZBB-ZBKB-LABEL: ror_i32:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT:  rorw a0, a0, a1
; RV64ZBB-ZBKB-NEXT:  ret
%1 = tail call i32 @llvm.fshr.i32(i32 %a, i32 %a, i32 %b)
ret i32 %1
}

; Similar to ror_i32, but doesn't sign extend the result.
define void @ror_i32_nosext(i32 signext %a, i32 signext %b, ptr %x) nounwind {
; RV64I-LABEL: ror_i32_nosext:
; RV64I:    # %bb.0:
; RV64I-NEXT:  andi a3, a1, -1
; RV64I-NEXT:  srlw a1, a0, a1
; RV64I-NEXT:  negw a3, a3
; RV64I-NEXT:  sllw a0, a0, a3
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:
    sw a0, 0(a2)
; RV64I-NEXT:  ret
;
; RV64ZBB-ZBKB-LABEL: ror_i32_nosext:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT:  rorw a0, a0, a1
; RV64ZBB-ZBKB-NEXT:  sw a0, 0(a2)
; RV64ZBB-ZBKB-NEXT:  ret
%1 = tail call i32 @llvm.fshr.i32(i32 %a, i32 %a, i32 %b)
store i32 %1, ptr %x
ret void
}

define signext i32 @ror_i32_neg_constant_rhs(i32 signext %a) nounwind {
; RV64I-LABEL: ror_i32_neg_constant_rhs:
; RV64I:    # %bb.0:
; RV64I-NEXT:  andi a1, a0, -1
; RV64I-NEXT:  li a2, -2
; RV64I-NEXT:  srlw a0, a2, a0
; RV64I-NEXT:  negw a1, a1
; RV64I-NEXT:  sllw a1, a2, a1
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBB-ZBKB-LABEL: ror_i32_neg_constant_rhs:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT:  li a1, -2
; RV64ZBB-ZBKB-NEXT:  rorw a0, a1, a0
; RV64ZBB-ZBKB-NEXT:  ret

```

```

%1 = tail call i32 @llvm.fshr.i32(i32 -2, i32 -2, i32 %a)
ret i32 %1
}

```

```

declare i64 @llvm.fshr.i64(i64, i64, i64)

```

```

define i64 @ror_i64(i64 %a, i64 %b) nounwind {
;
RV64I-LABEL: ror_i64:
; RV64I:    # %bb.0:
; RV64I-NEXT:  srl a2, a0, a1
; RV64I-NEXT:  negw a1, a1
; RV64I-NEXT:  sll a0, a0, a1
; RV64I-NEXT:  or a0, a2, a0
; RV64I-NEXT:  ret
;
; RV64ZBB-ZBKB-LABEL: ror_i64:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT:  ror a0, a0, a1
; RV64ZBB-ZBKB-NEXT:  ret
%or = tail call i64 @llvm.fshr.i64(i64 %a, i64 %a, i64 %b)
ret i64 %or
}

```

```

define signext i32 @rori_i32_fshl(i32 signext %a) nounwind {
; RV64I-LABEL: rori_i32_fshl:
; RV64I:    # %bb.0:
; RV64I-NEXT:  srliw a1, a0, 1
; RV64I-NEXT:  slliw a0, a0, 31
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64ZBB-ZBKB-LABEL: rori_i32_fshl:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT:  roriw a0, a0, 1
; RV64ZBB-ZBKB-NEXT:  ret
%1 = tail call i32 @llvm.fshl.i32(i32 %a, i32 %a, i32 31)
ret i32 %1
}

```

; Similar to rori_i32_fshl, but doesn't sign extend the result.

```

define void @rori_i32_fshl_nosext(i32 signext %a, ptr %x) nounwind {
; RV64I-LABEL: rori_i32_fshl_nosext:
;
RV64I:    # %bb.0:
; RV64I-NEXT:  srliw a2, a0, 1
; RV64I-NEXT:  slli a0, a0, 31
; RV64I-NEXT:  or a0, a0, a2

```

```

; RV64I-NEXT: sw a0, 0(a1)
; RV64I-NEXT: ret
;
; RV64ZBB-ZBKB-LABEL: rori_i32_fshl_nosext:
; RV64ZBB-ZBKB: # %bb.0:
; RV64ZBB-ZBKB-NEXT: roriw a0, a0, 1
; RV64ZBB-ZBKB-NEXT: sw a0, 0(a1)
; RV64ZBB-ZBKB-NEXT: ret
%1 = tail call i32 @llvm.fshl.i32(i32 %a, i32 %a, i32 31)
store i32 %1, ptr %x
ret void
}

```

```

define signext i32 @rori_i32_fshr(i32 signext %a) nounwind {
; RV64I-LABEL: rori_i32_fshr:
; RV64I: # %bb.0:
; RV64I-NEXT: slliw a1, a0, 1
; RV64I-NEXT: srliw a0, a0, 31
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: ret
;
; RV64ZBB-ZBKB-LABEL: rori_i32_fshr:
; RV64ZBB-ZBKB: # %bb.0:
; RV64ZBB-ZBKB-NEXT: roriw a0, a0, 31
; RV64ZBB-ZBKB-NEXT: ret
%1 = tail call i32 @llvm.fshr.i32(i32 %a, i32 %a, i32 31)
ret i32 %1
}

```

; Similar to rori_i32_fshr, but doesn't sign extend the result.

```

define void @rori_i32_fshr_nosext(i32
signext %a, ptr %x) nounwind {
; RV64I-LABEL: rori_i32_fshr_nosext:
; RV64I: # %bb.0:
; RV64I-NEXT: slli a2, a0, 1
; RV64I-NEXT: srliw a0, a0, 31
; RV64I-NEXT: or a0, a0, a2
; RV64I-NEXT: sw a0, 0(a1)
; RV64I-NEXT: ret
;
; RV64ZBB-ZBKB-LABEL: rori_i32_fshr_nosext:
; RV64ZBB-ZBKB: # %bb.0:
; RV64ZBB-ZBKB-NEXT: roriw a0, a0, 31
; RV64ZBB-ZBKB-NEXT: sw a0, 0(a1)
; RV64ZBB-ZBKB-NEXT: ret
%1 = tail call i32 @llvm.fshr.i32(i32 %a, i32 %a, i32 31)
store i32 %1, ptr %x
ret void

```

```
}
```

```
; This test is similar to the type legalized version of the fshl/fshr tests, but
; instead of having the same input to both shifts it has different inputs. Make
; sure we don't match it as a roriw.
define signext i32 @not_rori_i32(i32 signext %x, i32 signext %y) nounwind {
; CHECK-LABEL: not_rori_i32:
; CHECK:      # %bb.0:
; CHECK-NEXT:  slliw a0, a0, 31
; CHECK-NEXT:  srliw a1, a1, 1
; CHECK-NEXT:  or a0, a0, a1
; CHECK-NEXT:  ret
    %a = shl
    i32 %x, 31
    %b = lshr i32 %y, 1
    %c = or i32 %a, %b
    ret i32 %c
}
```

```
; This is similar to the type legalized roriw pattern, but the and mask is more
; than 32 bits so the lshr doesn't shift zeroes into the lower 32 bits. Make
; sure we don't match it to roriw.
define i64 @roriw_bug(i64 %x) nounwind {
; CHECK-LABEL: roriw_bug:
; CHECK:      # %bb.0:
; CHECK-NEXT:  slli a1, a0, 31
; CHECK-NEXT:  andi a2, a0, -2
; CHECK-NEXT:  srli a0, a0, 1
; CHECK-NEXT:  or a0, a1, a0
; CHECK-NEXT:  sext.w a0, a0
; CHECK-NEXT:  xor a0, a2, a0
; CHECK-NEXT:  ret
    %a = shl i64 %x, 31
    %b = and i64 %x, 18446744073709551614
    %c = lshr i64 %b, 1
    %d = or i64 %a, %c
    %e = shl i64 %d, 32
    %f = ashr i64 %e, 32
    %g = xor i64 %b, %f ; to increase the use count on %b to disable SimplifyDemandedBits.
    ret i64 %g
}
```

```
define i64 @rori_i64_fshl(i64 %a) nounwind {
; RV64I-LABEL: rori_i64_fshl:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srli a1, a0, 1
; RV64I-NEXT:  slli a0, a0, 63
; RV64I-NEXT:
```

```

    or a0, a0, a1
; RV64I-NEXT:    ret
;
; RV64ZBB-ZBKB-LABEL: rori_i64_fshl:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT:    rori a0, a0, 1
; RV64ZBB-ZBKB-NEXT:    ret
%1 = tail call i64 @llvm.fshl.i64(i64 %a, i64 %a, i64 63)
ret i64 %1
}

```

```

define i64 @rori_i64_fshr(i64 %a) nounwind {
; RV64I-LABEL: rori_i64_fshr:
; RV64I:    # %bb.0:
; RV64I-NEXT:    slli a1, a0, 1
; RV64I-NEXT:    srli a0, a0, 63
; RV64I-NEXT:    or a0, a0, a1
; RV64I-NEXT:    ret
;
; RV64ZBB-ZBKB-LABEL: rori_i64_fshr:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT:    rori a0, a0, 63
; RV64ZBB-ZBKB-NEXT:    ret
%1 = tail call i64 @llvm.fshr.i64(i64 %a, i64 %a, i64 63)
ret i64 %1
}

```

```

define signext i32 @not_shl_one_i32(i32 signext %x) {
; RV64I-LABEL: not_shl_one_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT:    li a1, 1
; RV64I-NEXT:    sllw a0, a1, a0
; RV64I-NEXT:    not a0, a0
; RV64I-NEXT:    ret
;
; RV64ZBB-ZBKB-LABEL: not_shl_one_i32:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT:    li a1,
-2
; RV64ZBB-ZBKB-NEXT:    rolw a0, a1, a0
; RV64ZBB-ZBKB-NEXT:    ret
%1 = shl i32 1, %x
%2 = xor i32 %1, -1
ret i32 %2
}

```

```

define i64 @not_shl_one_i64(i64 %x) {
; RV64I-LABEL: not_shl_one_i64:

```

```

; RV64I:    # %bb.0:
; RV64I-NEXT:  li a1, 1
; RV64I-NEXT:  sll a0, a1, a0
; RV64I-NEXT:  not a0, a0
; RV64I-NEXT:  ret
;
; RV64ZBB-ZBKB-LABEL: not_shl_one_i64:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT:  li a1, -2
; RV64ZBB-ZBKB-NEXT:  rol a0, a1, a0
; RV64ZBB-ZBKB-NEXT:  ret
%1 = shl i64 1, %x
%2 = xor i64 %1, -1
ret i64 %2
}

```

```

define i8 @srli_i8(i8 %a) nounwind {
; CHECK-LABEL: srli_i8:
; CHECK:    # %bb.0:
; CHECK-NEXT:  slli a0, a0, 56
; CHECK-NEXT:  srli a0, a0, 62
; CHECK-NEXT:  ret
%1 = lshr i8 %a, 6
ret i8 %1
}

```

; We could use sext.b+srai, but slli+srai offers more opportunities for
; compressed instructions.

```

define i8 @srai_i8(i8 %a) nounwind {
; RV64I-LABEL: srai_i8:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 24
; RV64I-NEXT:
    sraiw a0, a0, 29
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: srai_i8:
; RV64ZBB:    # %bb.0:
; RV64ZBB-NEXT:  slli a0, a0, 56
; RV64ZBB-NEXT:  srai a0, a0, 61
; RV64ZBB-NEXT:  ret
;
; RV64ZBKB-LABEL: srai_i8:
; RV64ZBKB:    # %bb.0:
; RV64ZBKB-NEXT:  slli a0, a0, 24
; RV64ZBKB-NEXT:  sraiw a0, a0, 29
; RV64ZBKB-NEXT:  ret
%1 = ashr i8 %a, 5

```

```
ret i8 %1
}
```

; We could use zext.h+srli, but slli+srli offers more opportunities for
; compressed instructions.

```
define i16 @srli_i16(i16 %a) nounwind {
; CHECK-LABEL: srli_i16:
; CHECK:      # %bb.0:
; CHECK-NEXT:  slli a0, a0, 48
; CHECK-NEXT:  srli a0, a0, 54
; CHECK-NEXT:  ret
%1 = lshr i16 %a, 6
ret i16 %1
}
```

; We could use sext.h+srai, but slli+srai offers more opportunities for
; compressed instructions.

```
define i16 @srai_i16(i16 %a) nounwind {
; RV64I-LABEL: srai_i16:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 16
; RV64I-NEXT:  sraiw a0, a0, 25
; RV64I-NEXT:  ret
;
; RV64ZBB-LABEL: srai_i16:
;
; RV64ZBB:     # %bb.0:
; RV64ZBB-NEXT: slli a0, a0, 48
; RV64ZBB-NEXT: srai a0, a0, 57
; RV64ZBB-NEXT: ret
;
; RV64ZBKB-LABEL: srai_i16:
; RV64ZBKB:    # %bb.0:
; RV64ZBKB-NEXT: slli a0, a0, 16
; RV64ZBKB-NEXT: sraiw a0, a0, 25
; RV64ZBKB-NEXT: ret
%1 = ashr i16 %a, 9
ret i16 %1
}
```

```
define i1 @andn_seqz_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: andn_seqz_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  seqz a0, a0
; RV64I-NEXT:  ret
;
;
```



```

; RV64ZBB-ZBKB-LABEL: andn_seqz_i32:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT:  andn a0, a1, a0
; RV64ZBB-ZBKB-NEXT:  seqz a0, a0
; RV64ZBB-ZBKB-NEXT:  ret
%and = and i32 %a, %b
%cmpeq = icmp eq i32 %and, %b
ret i1 %cmpeq
}

define i1 @andn_seqz_i64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: andn_seqz_i64:
; RV64I:    # %bb.0:
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  seqz a0, a0
; RV64I-NEXT:
    ret
;
; RV64ZBB-ZBKB-LABEL: andn_seqz_i64:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT:  andn a0, a1, a0
; RV64ZBB-ZBKB-NEXT:  seqz a0, a0
; RV64ZBB-ZBKB-NEXT:  ret
%and = and i64 %a, %b
%cmpeq = icmp eq i64 %and, %b
ret i1 %cmpeq
}

define i1 @andn_snez_i32(i32 signext %a, i32 signext %b) nounwind {
; RV64I-LABEL: andn_snez_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  snez a0, a0
; RV64I-NEXT:  ret
;
; RV64ZBB-ZBKB-LABEL: andn_snez_i32:
; RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT:  andn a0, a1, a0
; RV64ZBB-ZBKB-NEXT:  snez a0, a0
; RV64ZBB-ZBKB-NEXT:  ret
%and = and i32 %a, %b
%cmpeq = icmp ne i32 %and, %b
ret i1 %cmpeq
}

define i1 @andn_snez_i64(i64 %a, i64 %b) nounwind {

```

```

; RV64I-LABEL: andn_snez_i64:
; RV64I:    # %bb.0:
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  snez a0, a0
; RV64I-NEXT:  ret
;
; RV64ZBB-ZBKB-LABEL: andn_snez_i64:
;
RV64ZBB-ZBKB:    # %bb.0:
; RV64ZBB-ZBKB-NEXT:  andn a0, a1, a0
; RV64ZBB-ZBKB-NEXT:  snez a0, a0
; RV64ZBB-ZBKB-NEXT:  ret
%and = and i64 %a, %b
%cmpeq = icmp ne i64 %and, %b
ret i1 %cmpeq
}
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck -check-prefix=RV64I %s
; RUN: llc -mtriple=riscv64 -mattr=+m -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck -check-prefix=RV64IM %s

```

```

define i32 @urem(i32 %a, i32 %b) nounwind {
; RV64I-LABEL: urem:
; RV64I:    # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  srli a1, a1, 32
; RV64I-NEXT:  call __umoddi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: urem:
; RV64IM:    # %bb.0:
; RV64IM-NEXT:  remuw a0, a0, a1
; RV64IM-NEXT:  ret
%1 = urem i32 %a, %b
ret i32 %1
}

```

```

define i32 @urem_constant_lhs(i32 %a) nounwind {
;

```

```

RV64I-LABEL: urem_constant_lhs:
; RV64I:    # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a1, a0, 32
; RV64I-NEXT:  li a0, 10
; RV64I-NEXT:  call __umoddi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: urem_constant_lhs:
; RV64IM:    # %bb.0:
; RV64IM-NEXT:  li a1, 10
; RV64IM-NEXT:  remuw a0, a1, a0
; RV64IM-NEXT:  ret
%1 = urem i32 10, %a
ret i32 %1
}

```

```

define i32 @srem(i32 %a, i32 %b) nounwind {
; RV64I-LABEL: srem:
; RV64I:    # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  sext.w a0, a0
; RV64I-NEXT:  sext.w a1, a1
; RV64I-NEXT:  call __moddi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: srem:
; RV64IM:    # %bb.0:
; RV64IM-NEXT:
    remw a0, a0, a1
; RV64IM-NEXT:  ret
%1 = srem i32 %a, %b
ret i32 %1
}

```

```

define i32 @srem_pow2(i32 %a) nounwind {
; RV64I-LABEL: srem_pow2:
; RV64I:    # %bb.0:
; RV64I-NEXT:  sraiw a1, a0, 31
; RV64I-NEXT:  srliw a1, a1, 29
; RV64I-NEXT:  add a1, a0, a1

```

```

; RV64I-NEXT: andi a1, a1, -8
; RV64I-NEXT: subw a0, a0, a1
; RV64I-NEXT: ret
;
; RV64IM-LABEL: srem_pow2:
; RV64IM:    # %bb.0:
; RV64IM-NEXT: sraiw a1, a0, 31
; RV64IM-NEXT: srlw a1, a1, 29
; RV64IM-NEXT: add a1, a0, a1
; RV64IM-NEXT: andi a1, a1, -8
; RV64IM-NEXT: subw a0, a0, a1
; RV64IM-NEXT: ret
%1 = srem i32 %a, 8
ret i32 %1
}

```

```

define i32 @srem_pow2_2(i32 %a) nounwind {
; RV64I-LABEL: srem_pow2_2:
; RV64I:    # %bb.0:
; RV64I-NEXT: sraiw a1, a0, 31
; RV64I-NEXT: srlw a1, a1, 16
; RV64I-NEXT: add a1, a0, a1
; RV64I-NEXT: lui a2, 1048560
; RV64I-NEXT: and a1, a1, a2
; RV64I-NEXT: subw a0, a0, a1
; RV64I-NEXT: ret
;
; RV64IM-LABEL: srem_pow2_2:
; RV64IM:
; RV64IM:    # %bb.0:
; RV64IM-NEXT: sraiw a1, a0, 31
; RV64IM-NEXT: srlw a1, a1, 16
; RV64IM-NEXT: add a1, a0, a1
; RV64IM-NEXT: lui a2, 1048560
; RV64IM-NEXT: and a1, a1, a2
; RV64IM-NEXT: subw a0, a0, a1
; RV64IM-NEXT: ret
%1 = srem i32 %a, 65536
ret i32 %1
}

```

```

define i32 @srem_constant_lhs(i32 %a) nounwind {
; RV64I-LABEL: srem_constant_lhs:
; RV64I:    # %bb.0:
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT: sext.w a1, a0
; RV64I-NEXT: li a0, -10

```

```

; RV64I-NEXT:  call __moddi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: srem_constant_lhs:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  li a1, -10
; RV64IM-NEXT:  remw a0, a1, a0
; RV64IM-NEXT:  ret
%1 = srem i32 -10, %a
ret i32 %1
}

```

```

define i64 @urem64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: urem64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  tail __umoddi3
;
; RV64IM-LABEL:
urem64:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  remu a0, a0, a1
; RV64IM-NEXT:  ret
%1 = urem i64 %a, %b
ret i64 %1
}

```

```

define i64 @urem64_constant_lhs(i64 %a) nounwind {
; RV64I-LABEL: urem64_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT:  mv a1, a0
; RV64I-NEXT:  li a0, 10
; RV64I-NEXT:  tail __umoddi3
;
; RV64IM-LABEL: urem64_constant_lhs:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  li a1, 10
; RV64IM-NEXT:  remu a0, a1, a0
; RV64IM-NEXT:  ret
%1 = urem i64 10, %a
ret i64 %1
}

```

```

define i64 @srem64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: srem64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  tail __moddi3

```

```

;
; RV64IM-LABEL: srem64:
; RV64IM:    # %bb.0:
; RV64IM-NEXT:  rem a0, a0, a1
; RV64IM-NEXT:  ret
%1 = srem i64 %a, %b
ret i64 %1
}

define i64 @srem64_constant_lhs(i64 %a) nounwind {
; RV64I-LABEL: srem64_constant_lhs:
; RV64I:    # %bb.0:
; RV64I-NEXT:  mv a1, a0
; RV64I-NEXT:  li a0, -10
; RV64I-NEXT:  tail __moddi3
;
; RV64IM-LABEL: srem64_constant_lhs:
;
; RV64IM:    # %bb.0:
; RV64IM-NEXT:  li a1, -10
; RV64IM-NEXT:  rem a0, a1, a0
; RV64IM-NEXT:  ret
%1 = srem i64 -10, %a
ret i64 %1
}

define i8 @urem8(i8 %a, i8 %b) nounwind {
; RV64I-LABEL: urem8:
; RV64I:    # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  andi a0, a0, 255
; RV64I-NEXT:  andi a1, a1, 255
; RV64I-NEXT:  call __umoddi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: urem8:
; RV64IM:    # %bb.0:
; RV64IM-NEXT:  andi a1, a1, 255
; RV64IM-NEXT:  andi a0, a0, 255
; RV64IM-NEXT:  remuw a0, a0, a1
; RV64IM-NEXT:  ret
%1 = urem i8 %a, %b
ret i8 %1
}

```

```

define i8 @urem8_constant_lhs(i8 %a) nounwind {
; RV64I-LABEL: urem8_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  andi a1, a0, 255
; RV64I-NEXT:
    li a0, 10
; RV64I-NEXT:  call __umoddi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: urem8_constant_lhs:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  andi a0, a0, 255
; RV64IM-NEXT:  li a1, 10
; RV64IM-NEXT:  remuw a0, a1, a0
; RV64IM-NEXT:  ret
    %1 = urem i8 10, %a
    ret i8 %1
}

```

```

define i8 @srem8(i8 %a, i8 %b) nounwind {
; RV64I-LABEL: srem8:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a1, a1, 24
; RV64I-NEXT:  sraiw a1, a1, 24
; RV64I-NEXT:  slli a0, a0, 24
; RV64I-NEXT:  sraiw a0, a0, 24
; RV64I-NEXT:  call __moddi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: srem8:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  slli a1, a1, 24
; RV64IM-NEXT:  sraiw a1, a1, 24
; RV64IM-NEXT:  slli a0, a0, 24
; RV64IM-NEXT:  sraiw
a0, a0, 24
; RV64IM-NEXT:  remw a0, a0, a1
; RV64IM-NEXT:  ret
    %1 = srem i8 %a, %b
}

```

```

ret i8 %1
}

define i8 @srem8_constant_lhs(i8 %a) nounwind {
; RV64I-LABEL: srem8_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a0, a0, 24
; RV64I-NEXT:  sraiw a1, a0, 24
; RV64I-NEXT:  li a0, -10
; RV64I-NEXT:  call __moddi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: srem8_constant_lhs:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  slli a0, a0, 24
; RV64IM-NEXT:  sraiw a0, a0, 24
; RV64IM-NEXT:  li a1, -10
; RV64IM-NEXT:  remw a0, a1, a0
; RV64IM-NEXT:  ret
    %1 = srem i8 -10, %a
ret i8 %1
}

```

```

define i16 @urem16(i16 %a, i16 %b) nounwind {
; RV64I-LABEL: urem16:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  lui a2, 16
; RV64I-NEXT:
    addiw a2, a2, -1
; RV64I-NEXT:  and a0, a0, a2
; RV64I-NEXT:  and a1, a1, a2
; RV64I-NEXT:  call __umoddi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: urem16:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  lui a2, 16
; RV64IM-NEXT:  addi a2, a2, -1
; RV64IM-NEXT:  and a1, a1, a2

```



```

; RV64IM-NEXT:  and a0, a0, a2
; RV64IM-NEXT:  remuw a0, a0, a1
; RV64IM-NEXT:  ret
%1 = urem i16 %a, %b
ret i16 %1
}

define i16 @urem16_constant_lhs(i16 %a) nounwind {
; RV64I-LABEL: urem16_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a0, a0, 48
; RV64I-NEXT:  srli a1, a0, 48
; RV64I-NEXT:  li a0, 10
; RV64I-NEXT:  call __umoddi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: urem16_constant_lhs:
; RV64IM:      # %bb.0:
;
RV64IM-NEXT:  slli a0, a0, 48
; RV64IM-NEXT:  srli a0, a0, 48
; RV64IM-NEXT:  li a1, 10
; RV64IM-NEXT:  remuw a0, a1, a0
; RV64IM-NEXT:  ret
%1 = urem i16 10, %a
ret i16 %1
}

define i16 @srem16(i16 %a, i16 %b) nounwind {
; RV64I-LABEL: srem16:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a1, a1, 16
; RV64I-NEXT:  sraiw a1, a1, 16
; RV64I-NEXT:  slli a0, a0, 16
; RV64I-NEXT:  sraiw a0, a0, 16
; RV64I-NEXT:  call __moddi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: srem16:
; RV64IM:      # %bb.0:

```

```

; RV64IM-NEXT:  slli a1, a1, 16
; RV64IM-NEXT:  sraiw a1, a1, 16
; RV64IM-NEXT:  slli a0, a0, 16
; RV64IM-NEXT:  sraiw a0, a0, 16
; RV64IM-NEXT:  remw a0, a0, a1
; RV64IM-NEXT:  ret
%1 = srem i16 %a, %b
ret i16 %1
}

define i16 @srem16_constant_lhs(i16 %a) nounwind {
; RV64I-LABEL: srem16_constant_lhs:
;
RV64I:    # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a0, a0, 16
; RV64I-NEXT:  sraiw a1, a0, 16
; RV64I-NEXT:  li a0, -10
; RV64I-NEXT:  call __moddi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: srem16_constant_lhs:
; RV64IM:    # %bb.0:
; RV64IM-NEXT:  slli a0, a0, 16
; RV64IM-NEXT:  sraiw a0, a0, 16
; RV64IM-NEXT:  li a1, -10
; RV64IM-NEXT:  remw a0, a1, a0
; RV64IM-NEXT:  ret
%1 = srem i16 -10, %a
ret i16 %1
}

; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s

```

```

define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
; CHECK-LABEL: test_sitofp_fixed:
; CHECK:      ; %bb.0:
; CHECK-NEXT:  sshll2.2d v4, v0, #0
; CHECK-NEXT:  sshll.2d v0, v0, #0
; CHECK-NEXT:  sshll2.2d v5, v1, #0
; CHECK-NEXT:  sshll.2d v6, v1, #0
; CHECK-NEXT:  sshll.2d v7, v2, #0
; CHECK-NEXT:  sshll2.2d v16, v2, #0
; CHECK-NEXT:  sshll2.2d v17, v3, #0
; CHECK-NEXT:  sshll.2d v18, v3, #0

```

```
; CHECK-NEXT:   scvtf.2d v1, v4, #6
; CHECK-NEXT:   scvtf.2d v0, v0, #6
; CHECK-NEXT:   scvtf.2d v3, v5, #6
; CHECK-NEXT:   scvtf.2d v2, v6, #6
; CHECK-NEXT:   scvtf.2d v4, v7, #6
; CHECK-NEXT:   scvtf.2d v5, v16, #6
; CHECK-NEXT:   scvtf.2d v7, v17, #6
; CHECK-NEXT:   scvtf.2d v6, v18, #6
; CHECK-NEXT:   ret
```

```
%flt = sitofp <16 x i32> %in to <16 x double>
%res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0,
double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0>
ret <16 x double> %res
}
```

```
; This one is small enough to satisfy isSimple, but still illegally large.
define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
; CHECK-LABEL: test_sitofp_fixed_shortish:
; CHECK:      ; %bb.0:
; CHECK-NEXT:   scvtf.2d v0, v0, #6
; CHECK-NEXT:   scvtf.2d v1, v1, #6
; CHECK-NEXT:   ret
```

```
%flt = sitofp <4 x i64> %in to <4 x double>
%res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
ret <4 x double> %res
}
```

```
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefix=RV64I
```

```
; These tests are each targeted at a particular RISC-V ALU instruction. Most
; other files in this folder exercise LLVM IR instructions that don't directly
; match a RISC-V instruction.
```

```
; Register-immediate instructions.
```

```
define i32 @addi(i32 %a) nounwind {
; RV64I-LABEL: addi:
; RV64I:      # %bb.0:
; RV64I-NEXT:   addiw a0, a0, 1
; RV64I-NEXT:   ret
%1 = add i32 %a, 1
ret i32 %1
}
```

```

define i32 @slti(i32 %a) nounwind {
; RV64I-LABEL: slti:
; RV64I:      # %bb.0:
; RV64I-NEXT: sext.w a0, a0
; RV64I-NEXT: slti a0, a0, 2
; RV64I-NEXT: ret
%1 = icmp slt i32 %a, 2
%2 = zext i1 %1 to i32
ret i32 %2
}

```

```

define i32 @sltiu(i32 %a) nounwind {
; RV64I-LABEL: sltiu:
; RV64I:      # %bb.0:
; RV64I-NEXT: sext.w a0, a0
; RV64I-NEXT: sltiu a0, a0, 3
; RV64I-NEXT:
ret
%1 = icmp ult i32 %a, 3
%2 = zext i1 %1 to i32
ret i32 %2
}

```

```

define i32 @xori(i32 %a) nounwind {
; RV64I-LABEL: xori:
; RV64I:      # %bb.0:
; RV64I-NEXT: xori a0, a0, 4
; RV64I-NEXT: ret
%1 = xor i32 %a, 4
ret i32 %1
}

```

```

define i32 @ori(i32 %a) nounwind {
; RV64I-LABEL: ori:
; RV64I:      # %bb.0:
; RV64I-NEXT: ori a0, a0, 5
; RV64I-NEXT: ret
%1 = or i32 %a, 5
ret i32 %1
}

```

```

define i32 @andi(i32 %a) nounwind {
; RV64I-LABEL: andi:
; RV64I:      # %bb.0:
; RV64I-NEXT: andi a0, a0, 6
; RV64I-NEXT: ret
%1 = and i32 %a, 6

```

```

ret i32 %1
}

define i32 @slli(i32 %a) nounwind {
; RV64I-LABEL: slli:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slliw a0, a0, 7
; RV64I-NEXT:  ret
%1 = shl i32 %a, 7
ret i32 %1
}

define i32 @srli(i32 %a) nounwind {
; RV64I-LABEL: srli:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srliw a0, a0, 8
; RV64I-NEXT:  ret
%1 = lshr i32 %a, 8
ret i32 %1
}

define i32 @srai(i32 %a) nounwind {
; RV64I-LABEL: srai:
; RV64I:
; RV64I:      # %bb.0:
; RV64I-NEXT:  sraiw a0, a0, 9
; RV64I-NEXT:  ret
%1 = ashr i32 %a, 9
ret i32 %1
}

; Register-register instructions

define i32 @add(i32 %a, i32 %b) nounwind {
; RV64I-LABEL: add:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addw a0, a0, a1
; RV64I-NEXT:  ret
%1 = add i32 %a, %b
ret i32 %1
}

define i32 @sub(i32 %a, i32 %b) nounwind {
; RV64I-LABEL: sub:
; RV64I:      # %bb.0:
; RV64I-NEXT:  subw a0, a0, a1
; RV64I-NEXT:  ret
%1 = sub i32 %a, %b

```

```

ret i32 %1
}

define i32 @sub_negative_constant_lhs(i32 %a) nounwind {
; RV64I-LABEL: sub_negative_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, -2
; RV64I-NEXT:  subw a0, a1, a0
; RV64I-NEXT:  ret
%1 = sub i32 -2, %a
ret i32 %1
}

define i32 @sll(i32 %a, i32 %b) nounwind {
; RV64I-LABEL: sll:
; RV64I:      # %bb.0:
; RV64I-NEXT:  sllw a0, a0, a1
; RV64I-NEXT:  ret
%1 = shl i32 %a, %b
ret i32 %1
}

; Make sure we don't emit instructions to zero extend the shift amount to i64.
define
i32 @sll_shamt_zext(i32 %a, i32 %b) nounwind {
; RV64I-LABEL: sll_shamt_zext:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi a1, a1, 1
; RV64I-NEXT:  sllw a0, a0, a1
; RV64I-NEXT:  ret
%shamt = add i32 %b, 1
%1 = shl i32 %a, %shamt
ret i32 %1
}

define i32 @sll_negative_constant_lhs(i32 %a) nounwind {
; RV64I-LABEL: sll_negative_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, -1
; RV64I-NEXT:  sllw a0, a1, a0
; RV64I-NEXT:  ret
%1 = shl i32 -1, %a
ret i32 %1
}

define i32 @slt(i32 %a, i32 %b) nounwind {
; RV64I-LABEL: slt:
; RV64I:      # %bb.0:

```

```

; RV64I-NEXT:  sext.w a1, a1
; RV64I-NEXT:  sext.w a0, a0
; RV64I-NEXT:  slt a0, a0, a1
; RV64I-NEXT:  ret
%1 = icmp slt i32 %a, %b
%2 = zext i1 %1 to i32
ret i32 %2
}

define i32 @sltu(i32 %a, i32 %b) nounwind {
;
; RV64I-LABEL: sltu:
; RV64I:      # %bb.0:
; RV64I-NEXT:  sext.w a1, a1
; RV64I-NEXT:  sext.w a0, a0
; RV64I-NEXT:  sltu a0, a0, a1
; RV64I-NEXT:  ret
%1 = icmp ult i32 %a,
%b
%2 = zext i1 %1 to i32
ret i32 %2
}

define i32 @xor(i32 %a, i32 %b) nounwind {
;
; RV64I-LABEL: xor:
; RV64I:      # %bb.0:
; RV64I-NEXT:  xor a0, a0, a1
; RV64I-NEXT:  ret
%1 = xor i32 %a, %b
ret i32 %1
}

define i32 @srl(i32 %a, i32 %b) nounwind {
;
; RV64I-LABEL: srl:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srlw a0, a0, a1
; RV64I-NEXT:  ret
%1 = lshr i32 %a, %b
ret i32 %1
}

; Make sure we don't emit instructions to zero extend the shift amount to i64.
define i32 @srl_shamt_zext(i32 %a, i32 %b) nounwind {
; RV64I-LABEL: srl_shamt_zext:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi a1, a1, 1

```

```

; RV64I-NEXT:  srlw a0, a0, a1
; RV64I-NEXT:  ret
%shamt = add i32 %b, 1
%1 = lshr i32 %a, %shamt
ret i32 %1
}

define i32 @srl_negative_constant_lhs(i32 %a) nounwind {
;
; RV64I-LABEL: srl_negative_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, -1
; RV64I-NEXT:  srlw a0, a1, a0
; RV64I-NEXT:  ret
%1 = lshr i32 -1, %a
ret i32 %1
}

define
i32 @sra(i32 %a, i32 %b) nounwind {
;
; RV64I-LABEL: sra:
; RV64I:      # %bb.0:
; RV64I-NEXT:  saw a0, a0, a1
; RV64I-NEXT:  ret
%1 = ashr i32 %a, %b
ret i32 %1
}

; Make sure we don't emit instructions to zero extend the shift amount to i64.
define i32 @sra_shamt_zext(i32 %a, i32 %b) nounwind {
; RV64I-LABEL: sra_shamt_zext:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi a1, a1, 1
; RV64I-NEXT:  saw a0, a0, a1
; RV64I-NEXT:  ret
%shamt = add i32 %b, 1
%1 = ashr i32 %a, %shamt
ret i32 %1
}

define i32 @sra_negative_constant_lhs(i32 %a) nounwind {
;
; RV64I-LABEL: sra_negative_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a1, 524288
; RV64I-NEXT:  saw a0, a1, a0
; RV64I-NEXT:  ret

```



```

%1 = ashr i32 2147483648, %a
ret i32 %1
}

```

```

define i32 @or(i32 %a, i32 %b) nounwind {
;
; RV64I-LABEL: or:
; RV64I:      # %bb.0:
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: ret
%1 = or i32 %a, %b
ret i32 %1
}

```

```

define i32 @and(i32 %a, i32 %b) nounwind {
;
; RV64I-LABEL:
and:
; RV64I:      # %bb.0:
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: ret
%1 = and i32 %a, %b
ret i32 %1
}

```

; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --include-generated-funcs

; RUN: opt -S -passes=verify,iroutliner -ir-outlining-no-cost < %s | FileCheck %s

; This test checks that we do outline indirect calls when it is not specified
; that we should not.

```

declare void @f1(ptr, ptr);
declare void @f2(ptr, ptr);

```

```

define void @function1(ptr %func) {
entry:
%a = alloca i32, align 4
%b = alloca i32, align 4
%c = alloca i32, align 4
store i32 2, ptr %a, align 4
store i32 3, ptr %b, align 4
store i32 4, ptr %c, align 4
call void %func()
%al = load i32, ptr %a
%bl = load i32, ptr %b
%cl = load i32, ptr %c
ret void
}

```

```

define void @function2(ptr %func) {
entry:
    %a = alloca i32, align 4
    %b = alloca i32, align 4
    %c = alloca i32, align 4
    store i32 2, ptr %a, align 4
    store i32 3, ptr %b, align 4
    store i32 4, ptr %c, align 4
    call void %func()
    %al = load i32, ptr %a
    %bl = load i32, ptr %b
    %cl = load i32, ptr %c
    ret void
}
;
CHECK-LABEL: @function1(
; CHECK-NEXT: entry:
; CHECK-NEXT: [[A:%.*]] = alloca i32, align 4
; CHECK-NEXT: [[B:%.*]] = alloca i32, align 4
; CHECK-NEXT: [[C:%.*]] = alloca i32, align 4
; CHECK-NEXT: call void @outlined_ir_func_0(ptr [[A]], ptr [[B]], ptr [[C]], ptr [[FUNC:%.*]])
; CHECK-NEXT: ret void
;
;
; CHECK-LABEL: @function2(
; CHECK-NEXT: entry:
; CHECK-NEXT: [[A:%.*]] = alloca i32, align 4
; CHECK-NEXT: [[B:%.*]] = alloca i32, align 4
; CHECK-NEXT: [[C:%.*]] = alloca i32, align 4
; CHECK-NEXT: call void @outlined_ir_func_0(ptr [[A]], ptr [[B]], ptr [[C]], ptr [[FUNC:%.*]])
; CHECK-NEXT: ret void
;
;
; CHECK-LABEL: define internal void @outlined_ir_func_0(
; CHECK-NEXT: newFuncRoot:
; CHECK-NEXT: br label [[ENTRY_TO_OUTLINE:%.*]]
; CHECK: entry_to_outline:
; CHECK-NEXT: store i32 2, ptr [[TMP0:%.*]], align 4
; CHECK-NEXT: store i32 3, ptr [[TMP1:%.*]], align 4
; CHECK-NEXT: store i32 4, ptr [[TMP2:%.*]], align 4
; CHECK-NEXT:
; CHECK-NEXT: call void [[TMP3:%.*]]()
; CHECK-NEXT: [[AL:%.*]] = load i32, ptr [[TMP0]], align 4
; CHECK-NEXT: [[BL:%.*]] = load i32, ptr [[TMP1]], align 4
; CHECK-NEXT: [[CL:%.*]] = load i32, ptr [[TMP2]], align 4
; CHECK-NEXT: br label [[ENTRY_AFTER_OUTLINE_EXITSTUB:%.*]]
; CHECK: entry_after_outline.exitStub:

```

```
; CHECK-NEXT:  ret void
;
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -verify-machineinstrs < %s \
; RUN:  -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefix=RV64I
; RUN: llc -mtriple=riscv64 -mattr=+xtheadbb -verify-machineinstrs < %s \
; RUN:  -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefix=RV64XTHEADBB
```

```
declare i32 @llvmctlz.i32(i32, i1)
```

```
define signext i32 @ctlz_i32(i32 signext %a) nounwind {
```

```
; RV64I-LABEL: ctlz_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  beqz a0, .LBB0_2
; RV64I-NEXT: # %bb.1: # %cond.false
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  srliw a1, a0, 1
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 2
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 4
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 8
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 16
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:
    not a0, a0
; RV64I-NEXT:  srliw a1, a0, 1
; RV64I-NEXT:  lui a2, 349525
; RV64I-NEXT:  addi a2, a2, 1365
; RV64I-NEXT:  and a1, a1, a2
; RV64I-NEXT:  subw a0, a0, a1
; RV64I-NEXT:  lui a1, 209715
; RV64I-NEXT:  addi a1, a1, 819
; RV64I-NEXT:  and a2, a0, a1
; RV64I-NEXT:  srliw a0, a0, 2
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  add a0, a2, a0
; RV64I-NEXT:  srliw a1, a0, 4
; RV64I-NEXT:  addw a0, a0, a1
; RV64I-NEXT:  lui a1, 61681
; RV64I-NEXT:  addiw a1, a1, -241
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  lui a1, 4112
; RV64I-NEXT:  addiw a1, a1, 257
; RV64I-NEXT:  call __muldi3
```

```

; RV64I-NEXT:  srlw a0, a0, 24
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
; RV64I-NEXT: .LBB0_2:
; RV64I-NEXT:  li a0, 32
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: ctlz_i32:
; RV64XTHEADBB:    # %bb.0:
; RV64XTHEADBB-NEXT:  th.extu a0, a0, 31, 0
; RV64XTHEADBB-NEXT:  th.ff1 a0,
a0
; RV64XTHEADBB-NEXT:  addi a0, a0, -32
; RV64XTHEADBB-NEXT:  ret
%1 = call i32 @llvm.ctlz.i32(i32 %a, i1 false)
ret i32 %1
}

```

```

define signext i32 @log2_i32(i32 signext %a) nounwind {

```

```

; RV64I-LABEL: log2_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT:  beqz a0, .LBB1_2
; RV64I-NEXT: # %bb.1: # %cond.false
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  srlw a1, a0, 1
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srlw a1, a0, 2
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srlw a1, a0, 4
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srlw a1, a0, 8
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srlw a1, a0, 16
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  not a0, a0
; RV64I-NEXT:  srlw a1, a0, 1
; RV64I-NEXT:  lui a2, 349525
; RV64I-NEXT:  addi a2, a2, 1365
; RV64I-NEXT:  and a1, a1, a2
; RV64I-NEXT:  subw a0, a0, a1
; RV64I-NEXT:  lui a1, 209715
; RV64I-NEXT:  addi a1, a1, 819
; RV64I-NEXT:
and a2, a0, a1
; RV64I-NEXT:  srlw a0, a0, 2
; RV64I-NEXT:  and a0, a0, a1

```

```

; RV64I-NEXT:  add a0, a2, a0
; RV64I-NEXT:  srliw a1, a0, 4
; RV64I-NEXT:  addw a0, a0, a1
; RV64I-NEXT:  lui a1, 61681
; RV64I-NEXT:  addiw a1, a1, -241
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  lui a1, 4112
; RV64I-NEXT:  addiw a1, a1, 257
; RV64I-NEXT:  call __muldi3
; RV64I-NEXT:  srliw a0, a0, 24
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  j .LBB1_3
; RV64I-NEXT:  .LBB1_2:
; RV64I-NEXT:  li a0, 32
; RV64I-NEXT:  .LBB1_3: # %cond.end
; RV64I-NEXT:  li a1, 31
; RV64I-NEXT:  subw a0, a1, a0
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: log2_i32:
; RV64XTHEADBB:      # %bb.0:
; RV64XTHEADBB-NEXT:  th.extu a0, a0, 31, 0
; RV64XTHEADBB-NEXT:  th.ff1 a0, a0
; RV64XTHEADBB-NEXT:  addi a0, a0, -32
; RV64XTHEADBB-NEXT:  li a1, 31
; RV64XTHEADBB-NEXT:  subw a0, a1, a0
; RV64XTHEADBB-NEXT:  ret
%1 = call i32 @llvmctlz.i32(i32
%a, i1 false)
%2 = sub i32 31, %1
ret i32 %2
}

```

```

define signext i32 @log2_ceil_i32(i32 signext %a) nounwind {

```

```

; RV64I-LABEL: log2_ceil_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  sd s0, 0(sp) # 8-byte Folded Spill
; RV64I-NEXT:  addiw a0, a0, -1
; RV64I-NEXT:  li s0, 32
; RV64I-NEXT:  li a1, 32
; RV64I-NEXT:  beqz a0, .LBB2_2
; RV64I-NEXT:  # %bb.1: # %cond.false
; RV64I-NEXT:  srliw a1, a0, 1
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 2

```

```

; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srliw a1, a0, 4
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srliw a1, a0, 8
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srliw a1, a0, 16
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: not a0, a0
; RV64I-NEXT: srliw a1, a0, 1
; RV64I-NEXT: lui a2, 349525
; RV64I-NEXT: addi a2, a2, 1365
; RV64I-NEXT: and a1, a1, a2
; RV64I-NEXT: subw a0, a0, a1
; RV64I-NEXT:
    lui a1, 209715
; RV64I-NEXT: addi a1, a1, 819
; RV64I-NEXT: and a2, a0, a1
; RV64I-NEXT: srliw a0, a0, 2
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: add a0, a2, a0
; RV64I-NEXT: srliw a1, a0, 4
; RV64I-NEXT: addw a0, a0, a1
; RV64I-NEXT: lui a1, 61681
; RV64I-NEXT: addiw a1, a1, -241
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: lui a1, 4112
; RV64I-NEXT: addiw a1, a1, 257
; RV64I-NEXT: call __muldi3
; RV64I-NEXT: srliw a1, a0, 24
; RV64I-NEXT: .LBB2_2: # %cond.end
; RV64I-NEXT: subw a0, s0, a1
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: ld s0, 0(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
;
; RV64XTHEADBB-LABEL: log2_ceil_i32:
; RV64XTHEADBB:    # %bb.0:
; RV64XTHEADBB-NEXT: addi a0, a0, -1
; RV64XTHEADBB-NEXT: slli a0, a0, 32
; RV64XTHEADBB-NEXT: srli a0, a0, 32
; RV64XTHEADBB-NEXT: th.ff1 a0, a0
; RV64XTHEADBB-NEXT: addi a0, a0, -32
; RV64XTHEADBB-NEXT:
    li a1, 32
; RV64XTHEADBB-NEXT: subw a0, a1, a0
; RV64XTHEADBB-NEXT: ret
%1 = sub i32 %a, 1

```

```

%2 = call i32 @llvm.ctlz.i32(i32 %1, i1 false)
%3 = sub i32 32, %2
ret i32 %3
}

```

```

define signext i32 @findLastSet_i32(i32 signext %a) nounwind {
; RV64I-LABEL: findLastSet_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  sd s0, 0(sp) # 8-byte Folded Spill
; RV64I-NEXT:  mv s0, a0
; RV64I-NEXT:  srliw a0, a0, 1
; RV64I-NEXT:  or a0, s0, a0
; RV64I-NEXT:  srliw a1, a0, 2
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 4
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 8
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  srliw a1, a0, 16
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  not a0, a0
; RV64I-NEXT:  srliw a1, a0, 1
; RV64I-NEXT:  lui a2, 349525
; RV64I-NEXT:  addi a2, a2, 1365
; RV64I-NEXT:  and a1, a1, a2
; RV64I-NEXT:  subw a0, a0, a1
; RV64I-NEXT:
    lui a1, 209715
; RV64I-NEXT:  addi a1, a1, 819
; RV64I-NEXT:  and a2, a0, a1
; RV64I-NEXT:  srliw a0, a0, 2
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  add a0, a2, a0
; RV64I-NEXT:  srliw a1, a0, 4
; RV64I-NEXT:  addw a0, a0, a1
; RV64I-NEXT:  lui a1, 61681
; RV64I-NEXT:  addiw a1, a1, -241
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  lui a1, 4112
; RV64I-NEXT:  addiw a1, a1, 257
; RV64I-NEXT:  call __muldi3
; RV64I-NEXT:  srliw a0, a0, 24
; RV64I-NEXT:  xori a0, a0, 31
; RV64I-NEXT:  snez a1, s0
; RV64I-NEXT:  addiw a1, a1, -1
; RV64I-NEXT:  or a0, a1, a0

```

```

; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: ld s0, 0(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
;
; RV64XTHEADBB-LABEL: findLastSet_i32:
; RV64XTHEADBB:    # %bb.0:
; RV64XTHEADBB-NEXT: th.extu a1, a0, 31, 0
; RV64XTHEADBB-NEXT: th.ff1 a1, a1
; RV64XTHEADBB-NEXT: addiw a1, a1, -32
; RV64XTHEADBB-NEXT: xori a1, a1,
31
; RV64XTHEADBB-NEXT: snez a0, a0
; RV64XTHEADBB-NEXT: addiw a0, a0, -1
; RV64XTHEADBB-NEXT: or a0, a0, a1
; RV64XTHEADBB-NEXT: ret
%1 = call i32 @llvm.ctlz.i32(i32 %a, i1 true)
%2 = xor i32 31, %1
%3 = icmp eq i32 %a, 0
%4 = select i1 %3, i32 -1, i32 %2
ret i32 %4
}

```

```

define i32 @ctlz_lshr_i32(i32 signext %a) {
; RV64I-LABEL: ctlz_lshr_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT: srlw a0, a0, 1
; RV64I-NEXT: beqz a0, .LBB4_2
; RV64I-NEXT: # %bb.1: # %cond.false
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: .cfi_def_cfa_offset 16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT: .cfi_offset ra, -8
; RV64I-NEXT: srlw a1, a0, 1
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srlw a1, a0, 2
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srlw a1, a0, 4
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srlw a1, a0, 8
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srlw a1, a0, 16
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: not
a0, a0
; RV64I-NEXT: srlw a1, a0, 1
; RV64I-NEXT: lui a2, 349525
; RV64I-NEXT: addi a2, a2, 1365

```



```

; RV64I-NEXT: and a1, a1, a2
; RV64I-NEXT: subw a0, a0, a1
; RV64I-NEXT: lui a1, 209715
; RV64I-NEXT: addi a1, a1, 819
; RV64I-NEXT: and a2, a0, a1
; RV64I-NEXT: srliw a0, a0, 2
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: add a0, a2, a0
; RV64I-NEXT: srliw a1, a0, 4
; RV64I-NEXT: addw a0, a0, a1
; RV64I-NEXT: lui a1, 61681
; RV64I-NEXT: addiw a1, a1, -241
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: lui a1, 4112
; RV64I-NEXT: addiw a1, a1, 257
; RV64I-NEXT: call __muldi3
; RV64I-NEXT: srliw a0, a0, 24
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
; RV64I-NEXT: .LBB4_2:
; RV64I-NEXT: li a0, 32
; RV64I-NEXT: ret
;
; RV64XTHEADBB-LABEL: ctlz_lshr_i32:
; RV64XTHEADBB: # %bb.0:
; RV64XTHEADBB-NEXT: srliw a0, a0, 1
; RV64XTHEADBB-NEXT: th.ff1 a0, a0
; RV64XTHEADBB-NEXT:
    addi a0, a0, -32
; RV64XTHEADBB-NEXT: ret
%1 = lshr i32 %a, 1
%2 = call i32 @llvm.ctlz.i32(i32 %1, i1 false)
ret i32 %2
}

```

```
declare i64 @llvm.ctlz.i64(i64, i1)
```

```

define i64 @ctlz_i64(i64 %a) nounwind {
; RV64I-LABEL: ctlz_i64:
; RV64I: # %bb.0:
; RV64I-NEXT: beqz a0, .LBB5_2
; RV64I-NEXT: # %bb.1: # %cond.false
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT: srli a1, a0, 1
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srli a1, a0, 2

```

```

; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srli a1, a0, 4
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srli a1, a0, 8
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srli a1, a0, 16
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: srli a1, a0, 32
; RV64I-NEXT: or a0, a0, a1
; RV64I-NEXT: not a0, a0
; RV64I-NEXT: srli a1, a0, 1
; RV64I-NEXT: lui a2, 349525
; RV64I-NEXT: addiw a2, a2, 1365
; RV64I-NEXT: slli a3, a2, 32
; RV64I-NEXT: add a2, a2,
a3
; RV64I-NEXT: and a1, a1, a2
; RV64I-NEXT: sub a0, a0, a1
; RV64I-NEXT: lui a1, 209715
; RV64I-NEXT: addiw a1, a1, 819
; RV64I-NEXT: slli a2, a1, 32
; RV64I-NEXT: add a1, a1, a2
; RV64I-NEXT: and a2, a0, a1
; RV64I-NEXT: srli a0, a0, 2
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: add a0, a2, a0
; RV64I-NEXT: srli a1, a0, 4
; RV64I-NEXT: add a0, a0, a1
; RV64I-NEXT: lui a1, 61681
; RV64I-NEXT: addiw a1, a1, -241
; RV64I-NEXT: slli a2, a1, 32
; RV64I-NEXT: add a1, a1, a2
; RV64I-NEXT: and a0, a0, a1
; RV64I-NEXT: lui a1, 4112
; RV64I-NEXT: addiw a1, a1, 257
; RV64I-NEXT: slli a2, a1, 32
; RV64I-NEXT: add a1, a1, a2
; RV64I-NEXT: call __muldi3
; RV64I-NEXT: srli a0, a0, 56
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
; RV64I-NEXT: .LBB5_2:
; RV64I-NEXT: li a0, 64
; RV64I-NEXT: ret
;
; RV64XTHEADBB-LABEL: ctiz_i64:
; RV64XTHEADBB:    # %bb.0:

```

```

; RV64XTHEADBB-NEXT:
    th.ff1 a0, a0
; RV64XTHEADBB-NEXT:  ret
    %1 = call i64 @llvm.ctlz.i64(i64 %a, i1 false)
    ret i64 %1
}

declare i32 @llvm.cttz.i32(i32, i1)

define signext i32 @cttz_i32(i32 signext %a) nounwind {
; RV64I-LABEL: cttz_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  beqz a0, .LBB6_2
; RV64I-NEXT:  # %bb.1: # %cond.false
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  negw a1, a0
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  lui a1, 30667
; RV64I-NEXT:  addiw a1, a1, 1329
; RV64I-NEXT:  call __muldi3
; RV64I-NEXT:  srlw a0, a0, 27
; RV64I-NEXT:  lui a1, %hi(.LCPI6_0)
; RV64I-NEXT:  addi a1, a1, %lo(.LCPI6_0)
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  lbu a0, 0(a0)
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
; RV64I-NEXT:  .LBB6_2:
; RV64I-NEXT:  li a0, 32
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: cttz_i32:
; RV64XTHEADBB:  #
    %bb.0:
; RV64XTHEADBB-NEXT:  beqz a0, .LBB6_2
; RV64XTHEADBB-NEXT:  # %bb.1: # %cond.false
; RV64XTHEADBB-NEXT:  addi sp, sp, -16
; RV64XTHEADBB-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64XTHEADBB-NEXT:  negw a1, a0
; RV64XTHEADBB-NEXT:  and a0, a0, a1
; RV64XTHEADBB-NEXT:  lui a1, 30667
; RV64XTHEADBB-NEXT:  addiw a1, a1, 1329
; RV64XTHEADBB-NEXT:  call __muldi3
; RV64XTHEADBB-NEXT:  srlw a0, a0, 27
; RV64XTHEADBB-NEXT:  lui a1, %hi(.LCPI6_0)
; RV64XTHEADBB-NEXT:  addi a1, a1, %lo(.LCPI6_0)

```

```

; RV64XTHEADBB-NEXT:  add a0, a1, a0
; RV64XTHEADBB-NEXT:  lbu a0, 0(a0)
; RV64XTHEADBB-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64XTHEADBB-NEXT:  addi sp, sp, 16
; RV64XTHEADBB-NEXT:  ret
; RV64XTHEADBB-NEXT:  .LBB6_2:
; RV64XTHEADBB-NEXT:  li a0, 32
; RV64XTHEADBB-NEXT:  ret
; RV64ZBB-LABEL: cttz_i32:
; RV64ZBB:      # %bb.0:
; RV64ZBB-NEXT:  ctzw a0, a0
; RV64ZBB-NEXT:  ret
%1 = call i32 @llvm.cttz.i32(i32 %a, i1 false)
ret i32 %1
}

```

```

define
  signext i32 @cttz_zero_undef_i32(i32 signext %a) nounwind {
; RV64I-LABEL: cttz_zero_undef_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  negw a1, a0
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  lui a1, 30667
; RV64I-NEXT:  addiw a1, a1, 1329
; RV64I-NEXT:  call __muldi3
; RV64I-NEXT:  srliw a0, a0, 27
; RV64I-NEXT:  lui a1, %hi(.LCPI7_0)
; RV64I-NEXT:  addi a1, a1, %lo(.LCPI7_0)
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  lbu a0, 0(a0)
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: cttz_zero_undef_i32:
; RV64XTHEADBB:      # %bb.0:
; RV64XTHEADBB-NEXT:  addi sp, sp, -16
; RV64XTHEADBB-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64XTHEADBB-NEXT:  negw a1, a0
; RV64XTHEADBB-NEXT:  and a0, a0, a1
; RV64XTHEADBB-NEXT:  lui a1, 30667
; RV64XTHEADBB-NEXT:  addiw a1, a1, 1329
; RV64XTHEADBB-NEXT:
  call __muldi3
; RV64XTHEADBB-NEXT:  srliw a0, a0, 27
; RV64XTHEADBB-NEXT:  lui a1, %hi(.LCPI7_0)

```

```

; RV64XTHEADBB-NEXT:  addi a1, a1, %lo(.LCPI7_0)
; RV64XTHEADBB-NEXT:  add a0, a1, a0
; RV64XTHEADBB-NEXT:  lbu a0, 0(a0)
; RV64XTHEADBB-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64XTHEADBB-NEXT:  addi sp, sp, 16
; RV64XTHEADBB-NEXT:  ret
%1 = call i32 @llvm.cttz.i32(i32 %a, i1 true)
ret i32 %1
}

```

```

define signext i32 @findFirstSet_i32(i32 signext %a) nounwind {

```

```

; RV64I-LABEL: findFirstSet_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  sd s0, 0(sp) # 8-byte Folded Spill
; RV64I-NEXT:  mv s0, a0
; RV64I-NEXT:  negw a0, a0
; RV64I-NEXT:  and a0, s0, a0
; RV64I-NEXT:  lui a1, 30667
; RV64I-NEXT:  addiw a1, a1, 1329
; RV64I-NEXT:  call __muldi3
; RV64I-NEXT:  srliw a0, a0, 27
; RV64I-NEXT:  lui a1, %hi(.LCPI8_0)
; RV64I-NEXT:  addi a1, a1, %lo(.LCPI8_0)
; RV64I-NEXT:
    add a0, a1, a0
; RV64I-NEXT:  lbu a0, 0(a0)
; RV64I-NEXT:  snez a1, s0
; RV64I-NEXT:  addi a1, a1, -1
; RV64I-NEXT:  or a0, a1, a0
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  ld s0, 0(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: findFirstSet_i32:
; RV64XTHEADBB:      # %bb.0:
; RV64XTHEADBB-NEXT:  addi sp, sp, -16
; RV64XTHEADBB-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64XTHEADBB-NEXT:  sd s0, 0(sp) # 8-byte Folded Spill
; RV64XTHEADBB-NEXT:  mv s0, a0
; RV64XTHEADBB-NEXT:  negw a0, a0
; RV64XTHEADBB-NEXT:  and a0, s0, a0
; RV64XTHEADBB-NEXT:  lui a1, 30667
; RV64XTHEADBB-NEXT:  addiw a1, a1, 1329
; RV64XTHEADBB-NEXT:  call __muldi3
; RV64XTHEADBB-NEXT:  srliw a0, a0, 27

```

```

; RV64XTHEADBB-NEXT: lui a1, %hi(.LCPI8_0)
; RV64XTHEADBB-NEXT: addi a1, a1, %lo(.LCPI8_0)
; RV64XTHEADBB-NEXT: add a0, a1, a0
; RV64XTHEADBB-NEXT: lbu a0, 0(a0)
; RV64XTHEADBB-NEXT:
    snez a1, s0
; RV64XTHEADBB-NEXT: addi a1, a1, -1
; RV64XTHEADBB-NEXT: or a0, a1, a0
; RV64XTHEADBB-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64XTHEADBB-NEXT: ld s0, 0(sp) # 8-byte Folded Reload
; RV64XTHEADBB-NEXT: addi sp, sp, 16
; RV64XTHEADBB-NEXT: ret
%1 = call i32 @llvm.cttz.i32(i32 %a, i1 true)
%2 = icmp eq i32 %a, 0
%3 = select i1 %2, i32 -1, i32 %1
ret i32 %3
}

```

```

define signext i32 @ffs_i32(i32 signext %a) nounwind {

```

```

; RV64I-LABEL: ffs_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT: sd s0, 0(sp) # 8-byte Folded Spill
; RV64I-NEXT: mv s0, a0
; RV64I-NEXT: negw a0, a0
; RV64I-NEXT: and a0, s0, a0
; RV64I-NEXT: lui a1, 30667
; RV64I-NEXT: addiw a1, a1, 1329
; RV64I-NEXT: call __muldi3
; RV64I-NEXT: srliw a0, a0, 27
; RV64I-NEXT: lui a1, %hi(.LCPI9_0)
; RV64I-NEXT: addi a1, a1, %lo(.LCPI9_0)
; RV64I-NEXT: add a0, a1, a0
; RV64I-NEXT:
    lbu a0, 0(a0)
; RV64I-NEXT: addi a0, a0, 1
; RV64I-NEXT: seqz a1, s0
; RV64I-NEXT: addi a1, a1, -1
; RV64I-NEXT: and a0, a1, a0
; RV64I-NEXT: slli a0, a0, 32
; RV64I-NEXT: srli a0, a0, 32
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: ld s0, 0(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
;
; RV64XTHEADBB-LABEL: ffs_i32:

```

```

; RV64XTHEADBB:    # %bb.0:
; RV64XTHEADBB-NEXT:  addi sp, sp, -16
; RV64XTHEADBB-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64XTHEADBB-NEXT:  sd s0, 0(sp) # 8-byte Folded Spill
; RV64XTHEADBB-NEXT:  mv s0, a0
; RV64XTHEADBB-NEXT:  negw a0, a0
; RV64XTHEADBB-NEXT:  and a0, s0, a0
; RV64XTHEADBB-NEXT:  lui a1, 30667
; RV64XTHEADBB-NEXT:  addiw a1, a1, 1329
; RV64XTHEADBB-NEXT:  call __muldi3
; RV64XTHEADBB-NEXT:  srliw a0, a0, 27
; RV64XTHEADBB-NEXT:  lui a1, %hi(.LCPI9_0)
; RV64XTHEADBB-NEXT:  addi a1, a1, %lo(.LCPI9_0)
; RV64XTHEADBB-NEXT:  add a0, a1, a0
;
RV64XTHEADBB-NEXT:  lbu a0, 0(a0)
; RV64XTHEADBB-NEXT:  addi a0, a0, 1
; RV64XTHEADBB-NEXT:  seqz a1, s0
; RV64XTHEADBB-NEXT:  addi a1, a1, -1
; RV64XTHEADBB-NEXT:  and a0, a1, a0
; RV64XTHEADBB-NEXT:  slli a0, a0, 32
; RV64XTHEADBB-NEXT:  srli a0, a0, 32
; RV64XTHEADBB-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64XTHEADBB-NEXT:  ld s0, 0(sp) # 8-byte Folded Reload
; RV64XTHEADBB-NEXT:  addi sp, sp, 16
; RV64XTHEADBB-NEXT:  ret
%1 = call i32 @llvm.cttz.i32(i32 %a, i1 true)
%2 = add i32 %1, 1
%3 = icmp eq i32 %a, 0
%4 = select i1 %3, i32 0, i32 %2
ret i32 %4
}

```

```
declare i64 @llvm.cttz.i64(i64, i1)
```

```

define i64 @cttz_i64(i64 %a) nounwind {
; RV64I-LABEL: cttz_i64:
; RV64I:    # %bb.0:
; RV64I-NEXT:  beqz a0, .LBB10_2
; RV64I-NEXT:  # %bb.1: # %cond.false
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  neg a1, a0
; RV64I-NEXT:  and a0, a0, a1
; RV64I-NEXT:  lui a1, %hi(.LCPI10_0)
; RV64I-NEXT:
    ld a1, %lo(.LCPI10_0)(a1)
; RV64I-NEXT:  call __muldi3

```

```

; RV64I-NEXT: srli a0, a0, 58
; RV64I-NEXT: lui a1, %hi(.LCPI10_1)
; RV64I-NEXT: addi a1, a1, %lo(.LCPI10_1)
; RV64I-NEXT: add a0, a1, a0
; RV64I-NEXT: lbu a0, 0(a0)
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
; RV64I-NEXT: .LBB10_2:
; RV64I-NEXT: li a0, 64
; RV64I-NEXT: ret
;
; RV64XTHEADBB-LABEL: cttz_i64:
; RV64XTHEADBB: # %bb.0:
; RV64XTHEADBB-NEXT: beqz a0, .LBB10_2
; RV64XTHEADBB-NEXT: # %bb.1: # %cond.false
; RV64XTHEADBB-NEXT: addi a1, a0, -1
; RV64XTHEADBB-NEXT: not a0, a0
; RV64XTHEADBB-NEXT: and a0, a0, a1
; RV64XTHEADBB-NEXT: th.ff1 a0, a0
; RV64XTHEADBB-NEXT: li a1, 64
; RV64XTHEADBB-NEXT: sub a0, a1, a0
; RV64XTHEADBB-NEXT: ret
; RV64XTHEADBB-NEXT: .LBB10_2:
; RV64XTHEADBB-NEXT: li a0, 64
; RV64XTHEADBB-NEXT: ret
%1 = call i64 @llvm.cttz.i64(i64 %a, i1 false)
ret i64 %1
}

```

```

define signext
  i32 @sextb_i32(i32 signext %a) nounwind {
; RV64I-LABEL: sextb_i32:
; RV64I: # %bb.0:
; RV64I-NEXT: slli a0, a0, 56
; RV64I-NEXT: srai a0, a0, 56
; RV64I-NEXT: ret
;
; RV64XTHEADBB-LABEL: sextb_i32:
; RV64XTHEADBB: # %bb.0:
; RV64XTHEADBB-NEXT: th.ext a0, a0, 7, 0
; RV64XTHEADBB-NEXT: ret
%shl = shl i32 %a, 24
%shr = ashr exact i32 %shl, 24
ret i32 %shr
}

```

```

define i64 @sextb_i64(i64 %a) nounwind {

```



```

; RV64I-LABEL: sextb_i64:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 56
; RV64I-NEXT:  srai a0, a0, 56
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: sextb_i64:
; RV64XTHEADBB:    # %bb.0:
; RV64XTHEADBB-NEXT:  th.ext a0, a0, 7, 0
; RV64XTHEADBB-NEXT:  ret
%shl = shl i64 %a, 56
%shr = ashr exact i64 %shl, 56
ret i64 %shr
}

define signext i32 @sexth_i32(i32 signext %a) nounwind {
; RV64I-LABEL: sexth_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 48
; RV64I-NEXT:  srai a0, a0, 48
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL:
sexth_i32:
; RV64XTHEADBB:    # %bb.0:
; RV64XTHEADBB-NEXT:  th.ext a0, a0, 15, 0
; RV64XTHEADBB-NEXT:  ret
%shl = shl i32 %a, 16
%shr = ashr exact i32 %shl, 16
ret i32 %shr
}

define signext i32 @no_sexth_i32(i32 signext %a) nounwind {
; RV64I-LABEL: no_sexth_i32:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 17
; RV64I-NEXT:  sraiw a0, a0, 16
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: no_sexth_i32:
; RV64XTHEADBB:    # %bb.0:
; RV64XTHEADBB-NEXT:  slli a0, a0, 17
; RV64XTHEADBB-NEXT:  sraiw a0, a0, 16
; RV64XTHEADBB-NEXT:  ret
%shl = shl i32 %a, 17
%shr = ashr exact i32 %shl, 16
ret i32 %shr
}

```

```

define i64 @sexth_i64(i64 %a) nounwind {
; RV64I-LABEL: sexth_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 48
; RV64I-NEXT:  srai a0, a0, 48
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: sexth_i64:
; RV64XTHEADBB:  # %bb.0:
; RV64XTHEADBB-NEXT:  th.ext a0, a0, 15, 0
; RV64XTHEADBB-NEXT:  ret
%shl = shl i64 %a, 48
%shr = ashr
exact i64 %shl, 48
ret i64 %shr
}

```

```

define i64 @no_sexth_i64(i64 %a) nounwind {
; RV64I-LABEL: no_sexth_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 49
; RV64I-NEXT:  srai a0, a0, 48
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: no_sexth_i64:
; RV64XTHEADBB:  # %bb.0:
; RV64XTHEADBB-NEXT:  slli a0, a0, 49
; RV64XTHEADBB-NEXT:  srai a0, a0, 48
; RV64XTHEADBB-NEXT:  ret
%shl = shl i64 %a, 49
%shr = ashr exact i64 %shl, 48
ret i64 %shr
}

```

```

define i32 @zexth_i32(i32 %a) nounwind {
; RV64I-LABEL: zexth_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 48
; RV64I-NEXT:  srli a0, a0, 48
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: zexth_i32:
; RV64XTHEADBB:  # %bb.0:
; RV64XTHEADBB-NEXT:  th.extu a0, a0, 15, 0
; RV64XTHEADBB-NEXT:  ret
%and = and i32 %a, 65535
ret i32 %and

```

```

}

define i64 @zexth_i64(i64 %a) nounwind {
; RV64I-LABEL: zexth_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 48
; RV64I-NEXT:  srli a0, a0, 48
; RV64I-NEXT:
    ret
;
; RV64XTHEADBB-LABEL: zexth_i64:
; RV64XTHEADBB:  # %bb.0:
; RV64XTHEADBB-NEXT:  th.extu a0, a0, 15, 0
; RV64XTHEADBB-NEXT:  ret
    %and = and i64 %a, 65535
    ret i64 %and
}

define i64 @zext_bf_i64(i64 %a) nounwind {
; RV64I-LABEL: zext_bf_i64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 47
; RV64I-NEXT:  srli a0, a0, 48
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: zext_bf_i64:
; RV64XTHEADBB:  # %bb.0:
; RV64XTHEADBB-NEXT:  th.extu a0, a0, 16, 1
; RV64XTHEADBB-NEXT:  ret
    %1 = lshr i64 %a, 1
    %and = and i64 %1, 65535
    ret i64 %and
}

define i64 @zext_i64_srliw(i64 %a) nounwind {
; RV64I-LABEL: zext_i64_srliw:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srliw a0, a0, 16
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: zext_i64_srliw:
; RV64XTHEADBB:  # %bb.0:
; RV64XTHEADBB-NEXT:  srliw a0, a0, 16
; RV64XTHEADBB-NEXT:  ret
    %1 = lshr i64 %a, 16
    %and = and i64 %1, 65535
    ret i64 %and
}

```

```
declare i32 @llvm.bswap.i32(i32)
```

```
define signext
  i32 @bswap_i32(i32 signext %a) nounwind {
; RV64I-LABEL: bswap_i32:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srlw a1, a0, 8
; RV64I-NEXT:  lui a2, 16
; RV64I-NEXT:  addiw a2, a2, -256
; RV64I-NEXT:  and a1, a1, a2
; RV64I-NEXT:  srlw a3, a0, 24
; RV64I-NEXT:  or a1, a1, a3
; RV64I-NEXT:  and a2, a0, a2
; RV64I-NEXT:  sllw a2, a2, 8
; RV64I-NEXT:  sllw a0, a0, 24
; RV64I-NEXT:  or a0, a0, a2
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: bswap_i32:
; RV64XTHEADBB:  # %bb.0:
; RV64XTHEADBB-NEXT:  th.rev w a0, a0
; RV64XTHEADBB-NEXT:  ret
  %1 = tail call i32 @llvm.bswap.i32(i32 %a)
  ret i32 %1
}
```

; Similar to bswap_i32 but the result is not sign extended.

```
define void @bswap_i32_nosext(i32 signext %a, ptr %x) nounwind {
; RV64I-LABEL: bswap_i32_nosext:
; RV64I:      # %bb.0:
; RV64I-NEXT:  srlw a2, a0, 8
; RV64I-NEXT:  lui a3, 16
; RV64I-NEXT:  addi a3, a3, -256
; RV64I-NEXT:  and a2, a2, a3
; RV64I-NEXT:  srlw
a4, a0, 24
; RV64I-NEXT:  or a2, a2, a4
; RV64I-NEXT:  and a3, a0, a3
; RV64I-NEXT:  slli a3, a3, 8
; RV64I-NEXT:  slli a0, a0, 24
; RV64I-NEXT:  or a0, a0, a3
; RV64I-NEXT:  or a0, a0, a2
; RV64I-NEXT:  sw a0, 0(a1)
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: bswap_i32_nosext:
```

```

; RV64XTHEADBB:    # %bb.0:
; RV64XTHEADBB-NEXT:  th.rev a0, a0
; RV64XTHEADBB-NEXT:  sw a0, 0(a1)
; RV64XTHEADBB-NEXT:  ret
%1 = tail call i32 @llvm.bswap.i32(i32 %a)
store i32 %1, ptr %x
ret void
}

```

```

declare i64 @llvm.bswap.i64(i64)

```

```

define i64 @bswap_i64(i64 %a) {
; RV64I-LABEL: bswap_i64:
; RV64I:    # %bb.0:
; RV64I-NEXT:  srli a1, a0, 40
; RV64I-NEXT:  lui a2, 16
; RV64I-NEXT:  addiw a2, a2, -256
; RV64I-NEXT:  and a1, a1, a2
; RV64I-NEXT:  srli a3, a0, 56
; RV64I-NEXT:  or a1, a1, a3
; RV64I-NEXT:  srli a3, a0, 24
; RV64I-NEXT:  lui a4, 4080
; RV64I-NEXT:  and a3, a3, a4
; RV64I-NEXT:  srli a5, a0, 8
; RV64I-NEXT:  srliw a5, a5, 24
; RV64I-NEXT:  slli
a5, a5, 24
; RV64I-NEXT:  or a3, a5, a3
; RV64I-NEXT:  or a1, a3, a1
; RV64I-NEXT:  and a4, a0, a4
; RV64I-NEXT:  slli a4, a4, 24
; RV64I-NEXT:  srliw a3, a0, 24
; RV64I-NEXT:  slli a3, a3, 32
; RV64I-NEXT:  or a3, a4, a3
; RV64I-NEXT:  and a2, a0, a2
; RV64I-NEXT:  slli a2, a2, 40
; RV64I-NEXT:  slli a0, a0, 56
; RV64I-NEXT:  or a0, a0, a2
; RV64I-NEXT:  or a0, a0, a3
; RV64I-NEXT:  or a0, a0, a1
; RV64I-NEXT:  ret
;
; RV64XTHEADBB-LABEL: bswap_i64:
; RV64XTHEADBB:    # %bb.0:
; RV64XTHEADBB-NEXT:  th.rev a0, a0
; RV64XTHEADBB-NEXT:  ret
%1 = call i64 @llvm.bswap.i64(i64 %a)
ret i64 %1

```

```

}
; RUN: llc < %s -mtriple=s390x-linux-gnu -mcpu=zEC12 -verify-machineinstrs | FileCheck %s
;
; Test that early if conversion produces LOCR with operands of the right
; register classes.

define void @autogen_SD4739(ptr) {
; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
BB:
    %L34 = load i8, ptr %0
    %Cmp56 = icmp sgt i8 undef, %L34
    br label %CF246

CF246:                                ; preds = %CF246, %BB
    %S1163 = select i1 %Cmp56, i8 %L34, i8 undef
    br i1 undef, label %CF246, label %CF248

CF248:                                ; preds = %CF248, %CF246
    store i8 %S1163, ptr %0
    br label %CF248
}
; RUN: llc -march=hexagon -hexagon-hvx-widen=32 < %s | FileCheck %s

; Truncating a type-to-be-widenened to a legal type (v8i8).
; Check that this compiles successfully.
; CHECK-LABEL: f0:
; CHECK: dealloc_return

target datalayout = "e-m:e-p:32:32:32-a:0-n16:32-i64:64:64-i32:32:32-i16:16:16-i1:8:8-f32:32:32-f64:64:64-
v32:32:32-v64:64:64-v512:512:512-v1024:1024:1024-v2048:2048:2048"
target triple = "hexagon"

define dlllexport void @f0(ptr %a0) local_unnamed_addr #0 {
b0:
    %v0 = load i8, ptr undef, align 1
    %v1 = zext i8 %v0 to i16
    %v2 = add i16 0, %v1
    %v3 = icmp sgt i16 %v2, 1
    %v4 = select i1 %v3, i16 %v2, i16 1
    %v5 = udiv i16 -32768, %v4
    %v6 = zext i16 %v5 to i32
    %v7 = insertelement <8 x i32> undef, i32 %v6, i32 0
    %v8 = shufflevector <8 x i32> %v7, <8 x i32> undef, <8 x i32> zeroinitializer
    %v9 = load <8 x i16>, ptr undef, align 2
    %v10 = sext <8 x i16> %v9 to <8 x i32>
    %v11 = mul nsw <8 x i32> %v8, %v10
    %v12 = add nsw <8 x i32> %v11, <i32 16384, i32 16384, i32 16384,

```

```

i32 16384, i32 16384, i32 16384, i32 16384, i32 16384>
%v13 = lshr <8 x i32> %v12, <i32 15, i32 15, i32 15, i32 15, i32 15, i32 15, i32 15, i32 15>
%v14 = trunc <8 x i32> %v13 to <8 x i8>
%v15 = getelementptr inbounds i8, ptr %a0, i32 undef
store <8 x i8> %v14, ptr %v15, align 1
ret void
}

attributes #0 = { "target-features"="+hvx,+hvx-length128b" }
; RUN: llc -O3 -mtriple=powerpc-unknown-linux-gnu -mcpu=e500 -mattr=spe < %s | FileCheck %s

; PowerPC SPE is a rare in-tree target that has the FP_TO_SINT node marked
; as Legal.

; Verify that fptosi(42.1) isn't simplified when the rounding mode is
; unknown.
; Verify that no gross errors happen.
; CHECK-LABEL: @f20
; COMMON: cfdctsiz
define i32 @f20(double %a) strictfp {
entry:
    %result = call i32 @llvm.experimental.constrained.fptosi.i32.f64(double 42.1,
                                metadata !"fpexcept.strict")
                                strictfp
    ret i32 %result
}

@llvm.fp.env = thread_local global i8 zeroinitializer, section "llvm.metadata"
declare i32 @llvm.experimental.constrained.fptosi.i32.f64(double, metadata)
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```

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CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

; NOTE: Assertions have been autogenerated by utils/update_analyze_test_checks.py

; RUN: opt < %s -passes="print<cost-model>" 2>&1 -disable-output -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx2 | FileCheck %s --check-prefixes=VEC256,AVX

; RUN: opt < %s -passes="print<cost-model>" 2>&1 -disable-output -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+prefer-256-bit | FileCheck %s --check-prefixes=VEC256,AVX512VL256

; RUN: opt < %s -passes="print<cost-model>" 2>&1 -disable-output -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+prefer-256-bit | FileCheck %s --check-prefixes=AVX512VL512

; RUN: opt < %s -passes="print<cost-model>" 2>&1 -disable-output -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-prefixes=VEC256,SKX256

; RUN: opt < %s -passes="print<cost-model>" 2>&1 -disable-output -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,-prefer-256-bit | FileCheck %s --check-prefixes=SKX512

define

void @zext256() "min-legal-vector-width"="256" {

; AVX-LABEL: 'zext256'

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %A = zext <8 x i16> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %B = zext <8 x i32> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; AVX512VL256-LABEL: 'zext256'

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %A = zext <8 x i16> undef to <8 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>

; AVX512VL256-NEXT: Cost

Model: Found an estimated cost of 2 for instruction: %C = zext <16 x i8> undef to <16 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; AVX512VL512-LABEL: 'zext256'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>


```

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction:
%E = zext <32 x i8> undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'zext256'
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'zext256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated
cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = zext <8 x i16> undef to <8 x i64>
%B = zext <8 x i32> undef to <8 x i64>
%C = zext <16 x i8> undef to <16 x i32>
%D = zext <16 x i16> undef to <16 x i32>
%E = zext <32 x i8> undef to <32 x i16>
ret void
}

```

```

define void @zext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'zext512'
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %B = zext <8 x i32>
undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

```

```

;
; AVX512VL256-LABEL: 'zext512'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to
<8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to
<8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to
<16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to
<16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost
of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'zext512'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to
<16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to
<16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to
<32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'zext512'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8
x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'zext512'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16

```

```

x i16> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = zext <8 x i16> undef to <8 x i64>
%B = zext <8 x i32> undef to <8 x i64>
%C = zext <16 x i8> undef to <16 x i32>
%D = zext <16 x i16> undef to <16 x i32>
%E = zext <32 x i8> undef to <32 x i16>
ret void
}

define void @sext256() "min-legal-vector-width"="256" {
; AVX-LABEL: 'sext256'
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found
an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL256-LABEL: 'sext256'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %A = sext <8 x i8> undef to <8
x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = sext <8 x i16> undef to
<8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to
<8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = sext <16 x i8> undef to
<16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to
<16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef
to <32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'sext256'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8
x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to
<16 x i32>

```

```

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to
<16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to
<32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'sext256'
; SKX256-NEXT: Cost Model: Found an
estimated cost of 2 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'sext256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; SKX512-NEXT: Cost
Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

define void @sext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'sext512'
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found

```

```

an estimated cost of 4 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL256-LABEL: 'sext512'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8
x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to
<8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to
<8 x i64>
; AVX512VL256-NEXT:
Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to
<16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to
<32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'sext512'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8
x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to
<16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost
of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to
<32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'sext512'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x

```

```

i16>
; SKX256-NEXT: Cost
Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'sext512'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8>
undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

define void @trunc256() "min-legal-vector-width"="256" {
; VEC256-LABEL: 'trunc256'
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = trunc <8 x i64> undef to <8 x
i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %B = trunc <8 x i64> undef to <8 x
i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %C = trunc <8 x i64> undef to <8 x
i8>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = trunc <16 x i32> undef to <16 x
i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = trunc <16 x i32> undef to <16 x
i8>
; VEC256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %F = trunc <32 x i16> undef to <32 x
i8>
; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'trunc256'
;
AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = trunc <8 x i64> undef to
<8 x i32>

```

```

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = trunc <8 x i64> undef to
<8 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = trunc <8 x i64> undef to
<8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc <16 x i32> undef
to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %E = trunc <16 x i32> undef to
<16 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %F = trunc <32 x i16> undef to
<32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'trunc256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = trunc <8 x i64> undef to <8 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated
cost of 2 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = trunc <8 x i64> undef to <8 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc <16 x i32> undef to <16 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %E = trunc <16 x i32> undef to <16 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %F = trunc <32 x i16> undef to <32 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = trunc <8 x i64> undef to <8 x i32>
%B = trunc <8 x i64> undef to <8 x i16>
%C = trunc <8 x i64> undef to <8 x i8>
%D = trunc <16 x i32> undef to <16 x i16>
%E = trunc <16 x i32> undef to <16 x i8>
%F = trunc <32 x i16> undef to <32 x i8>
ret void
}

define i32 @zext256_vXi1() "min-legal-vector-width"="256" {
; AVX-LABEL: 'zext256_vXi1'
; AVX-NEXT: Cost Model: Found
an estimated cost of 1 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = zext <4 x i1> undef to <4 x
i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i64 = zext <8 x i1> undef to <8 x
i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = zext <2 x i1> undef to <2 x
i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = zext <4 x i1> undef to <4 x
i32>

```

```

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = zext <8 x i1> undef to <8 x
i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = zext <16 x i1> undef to <16 x
i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = zext <2 x i1> undef to <2 x
i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = zext <4 x i1> undef to <4 x
i16>
; AVX-NEXT:
  Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = zext <16 x i1> undef to <16 x
i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = zext <32 x i1> undef to <32 x
i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = zext <16 x i1> undef to <16 x
i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = zext <32 x i1> undef to <32 x
i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = zext <64 x i1> undef
to <64 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL256-LABEL: 'zext256_vXi1'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef
to <2 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef
to <4 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i64 = zext <8 x i1> undef
to <8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef
to <2 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef
to <4 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef
to <8 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = zext <16 x i1>
undef to <16 x i32>
; AVX512VL256-NEXT:
  Cost Model: Found an estimated cost of 5 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V4i16 = zext <4 x i1> undef
to <4 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i16 = zext <8 x i1> undef
to <8 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 12 for instruction: %V16i16 = zext <16 x i1>
undef to <16 x i16>

```



```

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %V32i16 = zext <32 x i1>
undef to <32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V2i8 = zext <2 x i1> undef to
<2 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V4i8 = zext <4 x i1> undef to
<4 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V8i8 = zext <8 x i1> undef to
<8 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated
cost of 12 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 25 for instruction: %V32i8 = zext <32 x i1>
undef to <32 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 50 for instruction: %V64i8 = zext <64 x i1>
undef to <64 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL512-LABEL: 'zext256_vXi1'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef
to <2 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef
to <4 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef
to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef
to <2 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of
2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef
to <8 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1>
undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i16 = zext <2 x i1> undef
to <2 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i16 = zext <4 x i1> undef
to <4 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i16 = zext <8 x i1> undef
to <8 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = zext <16 x i1>
undef to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i16 = zext <32 x i1>
undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i8
= zext <2 x i1> undef to <2 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i8 = zext <4 x i1> undef to
<4 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i8 = zext <8 x i1> undef to
<8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i8 = zext <16 x i1> undef

```

```

to <16 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i8 = zext <32 x i1> undef
to <32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 19 for instruction: %V64i8 = zext <64 x i1>
undef to <64 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX256-LABEL: 'zext256_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x
i64>
;
SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i64 = zext <8 x i1> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = zext <16 x i1> undef to
<16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction:
%V16i16 = zext <16 x i1> undef to <16 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V32i16 = zext <32 x i1> undef to
<32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x
i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x
i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x
i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16
x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32
x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i8 = zext <64 x i1> undef to <64
x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX512-LABEL: 'zext256_vXi1'

```

```

; SKX512-NEXT: Cost
Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1> undef to
<16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext
<4 x i1> undef to <4 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = zext <16 x i1> undef to
<16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i16 = zext <32 x i1> undef to
<32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16
x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32
x i8>
; SKX512-NEXT: Cost Model: Found an estimated
cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
%V2i64 = zext <2 x i1> undef to <2 x i64>
%V4i64 = zext <4 x i1> undef to <4 x i64>
%V8i64 = zext <8 x i1> undef to <8 x i64>

%V2i32 = zext <2 x i1> undef to <2 x i32>
%V4i32 = zext <4 x i1> undef to <4 x i32>
%V8i32 = zext <8 x i1> undef to <8 x i32>
%V16i32 = zext <16 x i1> undef to <16 x i32>

%V2i16 = zext <2 x i1> undef to <2 x i16>

```

```
%V4i16 = zext <4 x i1> undef to <4 x i16>
%V8i16 = zext <8 x i1> undef to <8 x i16>
%V16i16 = zext <16 x i1> undef to <16 x i16>
%V32i16 = zext <32 x i1> undef to <32 x i16>
```

```
%V2i8 = zext <2 x i1> undef to <2 x i8>
%V4i8 = zext <4 x i1> undef to <4 x i8>
%V8i8 = zext <8 x i1> undef to <8 x i8>
%V16i8 = zext <16 x i1> undef to <16 x i8>
%V32i8 = zext <32 x i1> undef to <32 x i8>
%V64i8 = zext <64 x i1> undef to <64 x i8>
```

```
ret i32 undef
}
```

```
define i32 @sext256_vXi1()
"min-legal-vector-width"="256" {
; AVX-LABEL: 'sext256_vXi1'
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost
of 4 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for
```

```

instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL256-LABEL: 'sext256_vXi1'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; AVX512VL256-NEXT:
  Cost Model: Found an estimated cost of 3 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction:
  %V4i16 = sext <4 x i1> undef to <4 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 20 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
;

```

AVX512VL256-NEXT: Cost Model: Found an estimated cost of 21 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 42 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; AVX512VL512-LABEL: 'sext256_vXi1'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 15 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>

; AVX512VL512-NEXT:

Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; SKX256-LABEL: 'sext256_vXi1'

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>

; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; SKX512-LABEL: 'sext256_vXi1'

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x

```

i64>
; SKX512-NEXT: Cost Model: Found an estimated
cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to
<16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x
i16>
; SKX512-NEXT: Cost Model:
Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to
<16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to
<32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = sext <4 x i1> undef to <4 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = sext <8 x i1> undef to <8 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16
x i8>
;
SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = sext <32 x i1> undef to <32
x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V64i8 = sext <64 x i1> undef to <64
x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
%i64 = sext i1 undef to i64
%V2i64 = sext <2 x i1> undef to <2 x i64>
%V4i64 = sext <4 x i1> undef to <4 x i64>
%V8i64 = sext <8 x i1> undef to <8 x i64>

%i32 = sext i1 undef to i32
%V2i32 = sext <2 x i1> undef to <2 x i32>

```



```
%V4i32 = sext <4 x i1> undef to <4 x i32>
%V8i32 = sext <8 x i1> undef to <8 x i32>
%V16i32 = sext <16 x i1> undef to <16 x i32>
```

```
%I16 = sext i1 undef to i16
%V2i16 = sext <2 x i1> undef to <2 x i16>
%V4i16 = sext <4 x i1> undef to <4 x i16>
%V8i16 = sext <8 x i1> undef to <8 x i16>
%V16i16 = sext <16 x i1> undef to <16 x i16>
%V32i16 = sext <32 x i1> undef to <32 x i16>
```

```
%I8 = sext i1 undef to i8
%V2i8 = sext <2
x i1> undef to <2 x i8>
%V4i8 = sext <4 x i1> undef to <4 x i8>
%V8i8 = sext <8 x i1> undef to <8 x i8>
%V16i8 = sext <16 x i1> undef to <16 x i8>
%V32i8 = sext <32 x i1> undef to <32 x i8>
%V64i8 = sext <64 x i1> undef to <64 x i8>
```

```
ret i32 undef
}
```

```
define i32 @trunc_vXi1() "min-legal-vector-width"="256" {
; AVX-LABEL: 'trunc_vXi1'
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to
<16 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i64 = trunc <32 x i64> undef to <32
x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V64i64
= trunc <64 x i64> undef to <64 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i32 = trunc <16 x i32> undef to <16
x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i32 = trunc <32 x i32> undef to <32
x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V64i32 = trunc <64 x i32> undef to <64
```

```

x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x
i1>
; AVX-NEXT: Cost Model: Found an estimated
cost of 0 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = trunc <16 x i16> undef to <16
x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i16 = trunc <32 x i16> undef to <32
x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V64i16 = trunc <64 x i16> undef to <64
x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x
i1>
; AVX-NEXT:
Cost Model: Found an estimated cost of 0 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL256-LABEL: 'trunc_vXi1'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64>
undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64>
undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64>
undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64>
undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i64 = trunc <32 x i64>
undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V64i64 = trunc <64 x i64>
undef to <64 x i1>
; AVX512VL256-NEXT: Cost Model:
Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32>
undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32>
undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = trunc <16 x i32>
undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V32i32 = trunc <32 x i32>
undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 16 for instruction: %V64i32 = trunc <64 x i32>

```

```

undef to <64 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = trunc <2 x i16>
undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = trunc <4 x i16>
undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an
estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i16 = trunc <16 x i16>
undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 16 for instruction: %V32i16 = trunc <32 x i16>
undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 32 for instruction: %V64i16 = trunc <64 x i16>
undef to <64 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = trunc <2 x i8> undef
to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = trunc <4 x i8> undef
to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = trunc <8 x i8> undef
to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i8 = trunc <16 x i8>
undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of
0 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V64i8 = trunc <64 x i8>
undef to <64 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL512-LABEL: 'trunc_vXi1'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64>
undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64>
undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = trunc <8 x i64>
undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64>
undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i64 = trunc <32 x i64>
undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction:
%V64i64 = trunc <64 x i64> undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32>
undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32>
undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32>
undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32>
undef to <16 x i1>

```

```

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V32i32 = trunc <32 x i32>
undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V64i32 = trunc <64 x i32>
undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = trunc <2 x i16>
undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction:
%V4i16 = trunc <4 x i16> undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16>
undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = trunc <16 x i16>
undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i16 = trunc <32 x i16>
undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V64i16 = trunc <64 x i16>
undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = trunc <2 x i8> undef
to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = trunc <4 x i8> undef
to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = trunc <8 x i8> undef
to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i8 = trunc <16 x
i8> undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i8 = trunc <32 x i8>
undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V64i8 = trunc <64 x i8>
undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX256-LABEL: 'trunc_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to
<16 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i64 = trunc <32 x i64> undef to
<32 x i1>
; SKX256-NEXT:
Cost Model: Found an estimated cost of 0 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8

```

```

x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = trunc <16 x i32> undef to
<16 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i32 = trunc <32 x i32> undef to
<32 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V64i32 = trunc <64 x i32> undef to
<64 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = trunc <2 x i16> undef to <2
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction:
%V4i16 = trunc <4 x i16> undef to <4 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = trunc <8 x i16> undef to <8
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = trunc <16 x i16> undef to
<16 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V32i16 = trunc <32 x i16> undef to
<32 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V64i16 = trunc <64 x i16> undef to
<64 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x
i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x
i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x
i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = trunc <16 x i8> undef to
<16 x i1>
; SKX256-NEXT:
Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i8 = trunc <64 x i8> undef to
<64 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX512-LABEL: 'trunc_vXi1'
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = trunc <8 x i64> undef to <8
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to
<16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i64 = trunc <32 x i64> undef to
<32 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction:
%V64i64 = trunc <64 x i64> undef to <64 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2
x i1>

```

```

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32> undef to
<16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i32 = trunc <32 x i32> undef to
<32 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V64i32 = trunc <64 x i32> undef to
<64 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = trunc <2 x i16> undef to <2
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = trunc <4 x i16> undef to <4
x i1>
;
SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = trunc <8 x i16> undef to <8
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = trunc <16 x i16> undef to
<16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i16 = trunc <32 x i16> undef to
<32 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i16 = trunc <64 x i16> undef to
<64 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x
i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x
i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x
i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = trunc <16 x i8> undef to
<16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for
instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = trunc <64 x i8> undef to
<64 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
%V2i64 = trunc <2 x i64> undef to <2 x i1>
%V4i64 = trunc <4 x i64> undef to <4 x i1>
%V8i64 = trunc <8 x i64> undef to <8 x i1>
%V16i64 = trunc <16 x i64> undef to <16 x i1>
%V32i64 = trunc <32 x i64> undef to <32 x i1>
%V64i64 = trunc <64 x i64> undef to <64 x i1>

%V2i32 = trunc <2 x i32> undef to <2 x i1>
%V4i32 = trunc <4 x i32> undef to <4 x i1>
%V8i32 = trunc <8 x i32> undef to <8 x i1>
%V16i32 = trunc <16 x i32> undef to <16 x i1>

```

%V32i32 = trunc <32 x i32> undef to <32 x i1>

%V64i32 = trunc <64 x i32> undef to <64 x i1>

%V2i16 = trunc <2 x i16> undef to <2 x i1>

%V4i16 = trunc <4 x i16> undef to <4 x i1>

%V8i16 = trunc <8 x i16> undef to <8 x i1>

%V16i16 = trunc <16 x i16> undef to
<16 x i1>

%V32i16 = trunc <32 x i16> undef to <32 x i1>

%V64i16 = trunc <64 x i16> undef to <64 x i1>

%V2i8 = trunc <2 x i8> undef to <2 x i1>

%V4i8 = trunc <4 x i8> undef to <4 x i1>

%V8i8 = trunc <8 x i8> undef to <8 x i1>

%V16i8 = trunc <16 x i8> undef to <16 x i1>

%V32i8 = trunc <32 x i8> undef to <32 x i1>

%V64i8 = trunc <64 x i8> undef to <64 x i1>

ret i32 undef

}

; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py

; RUN: llc -mtriple=riscv64 -mattr=+m -verify-machineinstrs < %s \

; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefix=RV64

;

; Get the actual value of the overflow bit.

;

define zeroext i1 @saddo1.i32(i32 signext %v1, i32 signext %v2, ptr %res) {

; RV64-LABEL: saddo1.i32:

; RV64: # %bb.0: # %entry

; RV64-NEXT: addw a3, a0, a1

; RV64-NEXT: slt a0, a3, a0

; RV64-NEXT: slti a1, a1, 0

; RV64-NEXT: xor a0, a1, a0

; RV64-NEXT: sw a3, 0(a2)

; RV64-NEXT: ret

entry:

%t = call {i32, i1} @llvm.sadd.with.overflow.i32(i32 %v1, i32 %v2)

%val = extractvalue {i32, i1} %t, 0

%obit = extractvalue {i32, i1} %t, 1

store i32 %val, ptr %res

ret i1 %obit

}

; Test the immediate version.

define zeroext i1 @saddo2.i32(i32 signext %v1, ptr %res) {

; RV64-LABEL: saddo2.i32:

; RV64: # %bb.0: # %entry

```

; RV64-NEXT:   addiw a2, a0, 4
; RV64-NEXT:   slt a0, a2, a0
; RV64-NEXT:
    sw a2, 0(a1)
; RV64-NEXT:   ret
entry:
%t = call {i32, i1} @llvm.sadd.with.overflow.i32(i32 %v1, i32 4)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

; Test negative immediates.
define zeroext i1 @saddo3.i32(i32 signext %v1, ptr %res) {
; RV64-LABEL: saddo3.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:   addiw a2, a0, -4
; RV64-NEXT:   slt a0, a2, a0
; RV64-NEXT:   xori a0, a0, 1
; RV64-NEXT:   sw a2, 0(a1)
; RV64-NEXT:   ret
entry:
%t = call {i32, i1} @llvm.sadd.with.overflow.i32(i32 %v1, i32 -4)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

; Test immediates that are too large to be encoded.
define zeroext i1 @saddo4.i32(i32 signext %v1, ptr %res) {
; RV64-LABEL: saddo4.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:   lui a2, 4096
; RV64-NEXT:   addi a2, a2, -1
; RV64-NEXT:   addw a2, a0, a2
; RV64-NEXT:   slt
a0, a2, a0
; RV64-NEXT:   sw a2, 0(a1)
; RV64-NEXT:   ret
entry:
%t = call {i32, i1} @llvm.sadd.with.overflow.i32(i32 %v1, i32 16777215)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

```



```

define zeroext i1 @saddo1.i64(i64 %v1, i64 %v2, ptr %res) {
; RV64-LABEL: saddo1.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  add a3, a0, a1
; RV64-NEXT:  slt a0, a3, a0
; RV64-NEXT:  slti a1, a1, 0
; RV64-NEXT:  xor a0, a1, a0
; RV64-NEXT:  sd a3, 0(a2)
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.sadd.with.overflow.i64(i64 %v1, i64 %v2)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
store i64 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @saddo2.i64(i64 %v1, ptr %res) {
; RV64-LABEL: saddo2.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  addi a2, a0, 4
; RV64-NEXT:  slt a0, a2, a0
; RV64-NEXT:  sd a2, 0(a1)
; RV64-NEXT:  ret
entry:
%t = call {i64, i1}
@llvm.sadd.with.overflow.i64(i64 %v1, i64 4)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
store i64 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @saddo3.i64(i64 %v1, ptr %res) {
; RV64-LABEL: saddo3.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  addi a2, a0, -4
; RV64-NEXT:  slt a0, a2, a0
; RV64-NEXT:  xori a0, a0, 1
; RV64-NEXT:  sd a2, 0(a1)
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.sadd.with.overflow.i64(i64 %v1, i64 -4)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
store i64 %val, ptr %res
ret i1 %obit
}

```

```

}

define zeroext i1 @uaddo.i32(i32 signext %v1, i32 signext %v2, ptr %res) {
; RV64-LABEL: uaddo.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  addw a1, a0, a1
; RV64-NEXT:  sltu a0, a1, a0
; RV64-NEXT:  sw a1, 0(a2)
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.uadd.with.overflow.i32(i32 %v1, i32 %v2)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32,
i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

define zeroext i1 @uaddo.i32.constant(i32 signext %v1, ptr %res) {
; RV64-LABEL: uaddo.i32.constant:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  addiw a2, a0, -2
; RV64-NEXT:  sltu a0, a2, a0
; RV64-NEXT:  sw a2, 0(a1)
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.uadd.with.overflow.i32(i32 %v1, i32 -2)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

define zeroext i1 @uaddo.i32.constant_one(i32 signext %v1, ptr %res) {
; RV64-LABEL: uaddo.i32.constant_one:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  addiw a2, a0, 1
; RV64-NEXT:  seqz a0, a2
; RV64-NEXT:  sw a2, 0(a1)
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.uadd.with.overflow.i32(i32 %v1, i32 1)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @uaddo.i64(i64 %v1, i64 %v2, ptr
%res) {
; RV64-LABEL: uaddo.i64:
; RV64:    # %bb.0: # %entry
; RV64-NEXT:  add a1, a0, a1
; RV64-NEXT:  sltu a0, a1, a0
; RV64-NEXT:  sd a1, 0(a2)
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.uadd.with.overflow.i64(i64 %v1, i64 %v2)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
store i64 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @uaddo.i64.constant_one(i64 %v1, ptr %res) {
; RV64-LABEL: uaddo.i64.constant_one:
; RV64:    # %bb.0: # %entry
; RV64-NEXT:  addi a2, a0, 1
; RV64-NEXT:  seqz a0, a2
; RV64-NEXT:  sd a2, 0(a1)
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.uadd.with.overflow.i64(i64 %v1, i64 1)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
store i64 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @ssubo1.i32(i32 signext %v1, i32 signext %v2, ptr %res) {
; RV64-LABEL: ssubo1.i32:
; RV64:    # %bb.0: # %entry
; RV64-NEXT:  sgtz a3, a1
; RV64-NEXT:  subw a1,
a0, a1
; RV64-NEXT:  slt a0, a1, a0
; RV64-NEXT:  xor a0, a3, a0
; RV64-NEXT:  sw a1, 0(a2)
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.ssub.with.overflow.i32(i32 %v1, i32 %v2)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @ssubo2.i32(i32 signext %v1, ptr %res) {
; RV64-LABEL: ssubo2.i32:
; RV64:    # %bb.0: # %entry
; RV64-NEXT:  addiw a2, a0, 4
; RV64-NEXT:  slt a0, a2, a0
; RV64-NEXT:  sw a2, 0(a1)
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.ssub.with.overflow.i32(i32 %v1, i32 -4)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

define zeroext i1 @ssubo.i64(i64 %v1, i64 %v2, ptr %res) {
; RV64-LABEL: ssubo.i64:
; RV64:    # %bb.0: # %entry
; RV64-NEXT:  sgtz a3, a1
; RV64-NEXT:  sub a1, a0, a1
; RV64-NEXT:  slt a0, a1, a0
; RV64-NEXT:  xor a0, a3, a0
; RV64-NEXT:  sd a1,
0(a2)
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.ssub.with.overflow.i64(i64 %v1, i64 %v2)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
store i64 %val, ptr %res
ret i1 %obit
}

define zeroext i1 @usubo.i32(i32 signext %v1, i32 signext %v2, ptr %res) {
; RV64-LABEL: usubo.i32:
; RV64:    # %bb.0: # %entry
; RV64-NEXT:  subw a1, a0, a1
; RV64-NEXT:  sltu a0, a0, a1
; RV64-NEXT:  sw a1, 0(a2)
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.usub.with.overflow.i32(i32 %v1, i32 %v2)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @usubo.i32.constant.rhs(i32 signext %v1, ptr %res) {
; RV64-LABEL: usubo.i32.constant.rhs:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  addiw a2, a0, 2
; RV64-NEXT:  sltu a0, a0, a2
; RV64-NEXT:  sw a2, 0(a1)
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.usub.with.overflow.i32(i32 %v1, i32 -2)

%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @usubo.i32.constant.lhs(i32 signext %v1, ptr %res) {
; RV64-LABEL: usubo.i32.constant.lhs:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  li a2, -2
; RV64-NEXT:  subw a2, a2, a0
; RV64-NEXT:  addi a0, a2, 1
; RV64-NEXT:  seqz a0, a0
; RV64-NEXT:  sw a2, 0(a1)
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.usub.with.overflow.i32(i32 -2, i32 %v1)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @usubo.i64(i64 %v1, i64 %v2, ptr %res) {
; RV64-LABEL: usubo.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  sub a1, a0, a1
; RV64-NEXT:  sltu a0, a0, a1
; RV64-NEXT:  sd a1, 0(a2)
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.usub.with.overflow.i64(i64 %v1, i64 %v2)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t,
1
store i64 %val, ptr %res
ret i1 %obit
}

```

```

}

define zeroext i1 @smulo.i32(i32 signext %v1, i32 signext %v2, ptr %res) {
; RV64-LABEL: smulo.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  mul a1, a0, a1
; RV64-NEXT:  srai a0, a1, 32
; RV64-NEXT:  sraiw a3, a1, 31
; RV64-NEXT:  xor a0, a0, a3
; RV64-NEXT:  snez a0, a0
; RV64-NEXT:  sw a1, 0(a2)
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.smul.with.overflow.i32(i32 %v1, i32 %v2)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @smulo2.i32(i32 signext %v1, ptr %res) {
; RV64-LABEL: smulo2.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  li a2, 13
; RV64-NEXT:  mul a2, a0, a2
; RV64-NEXT:  srai a0, a2, 32
; RV64-NEXT:  sraiw a3, a2, 31
; RV64-NEXT:  xor a0, a0, a3
; RV64-NEXT:  snez a0, a0
; RV64-NEXT:  sw a2, 0(a1)
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.smul.with.overflow.i32(i32 %v1, i32
13)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @smulo.i64(i64 %v1, i64 %v2, ptr %res) {
; RV64-LABEL: smulo.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  mulh a3, a0, a1
; RV64-NEXT:  mul a1, a0, a1
; RV64-NEXT:  srai a0, a1, 63
; RV64-NEXT:  xor a0, a3, a0
; RV64-NEXT:  snez a0, a0

```

```

; RV64-NEXT: sd a1, 0(a2)
; RV64-NEXT: ret
entry:
%t = call {i64, i1} @llvm.smul.with.overflow.i64(i64 %v1, i64 %v2)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
store i64 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @smulo2.i64(i64 %v1, ptr %res) {
; RV64-LABEL: smulo2.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT: li a2, 13
; RV64-NEXT: mulh a3, a0, a2
; RV64-NEXT: mul a2, a0, a2
; RV64-NEXT: srai a0, a2, 63
; RV64-NEXT: xor a0, a3, a0
; RV64-NEXT: snez a0, a0
; RV64-NEXT: sd a2, 0(a1)
; RV64-NEXT: ret
entry:
%t = call
{i64, i1} @llvm.smul.with.overflow.i64(i64 %v1, i64 13)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
store i64 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @umulo.i32(i32 signext %v1, i32 signext %v2, ptr %res) {
; RV64-LABEL: umulo.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT: slli a1, a1, 32
; RV64-NEXT: slli a0, a0, 32
; RV64-NEXT: mulhu a1, a0, a1
; RV64-NEXT: srai a0, a1, 32
; RV64-NEXT: snez a0, a0
; RV64-NEXT: sw a1, 0(a2)
; RV64-NEXT: ret
entry:
%t = call {i32, i1} @llvm.umul.with.overflow.i32(i32 %v1, i32 %v2)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
store i32 %val, ptr %res
ret i1 %obit
}

```

```

define zeroext i1 @umulo2.i32(i32 signext %v1, ptr %res) {
; RV64-LABEL: umulo2.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  li a2, 13
; RV64-NEXT:  slli a2, a2, 32
; RV64-NEXT:  slli a0, a0, 32
; RV64-NEXT:  mulhu a2, a0, a2
; RV64-NEXT:  srli a0, a2, 32
; RV64-NEXT:
    snez a0, a0
; RV64-NEXT:  sw a2, 0(a1)
; RV64-NEXT:  ret
entry:
    %t = call {i32, i1} @llvm.umul.with.overflow.i32(i32 %v1, i32 13)
    %val = extractvalue {i32, i1} %t, 0
    %obit = extractvalue {i32, i1} %t, 1
    store i32 %val, ptr %res
    ret i1 %obit
}

; Similar to umulo.i32, but storing the overflow and returning the result.
define signext i32 @umulo3.i32(i32 signext %0, i32 signext %1, ptr %2) {
; RV64-LABEL: umulo3.i32:
; RV64:      # %bb.0:
; RV64-NEXT:  slli a1, a1, 32
; RV64-NEXT:  slli a0, a0, 32
; RV64-NEXT:  mulhu a0, a0, a1
; RV64-NEXT:  srai a1, a0, 32
; RV64-NEXT:  snez a1, a1
; RV64-NEXT:  sext.w a0, a0
; RV64-NEXT:  sw a1, 0(a2)
; RV64-NEXT:  ret
    %4 = tail call { i32, i1 } @llvm.umul.with.overflow.i32(i32 %0, i32 %1)
    %5 = extractvalue { i32, i1 } %4, 1
    %6 = extractvalue { i32, i1 } %4, 0
    %7 = zext i1 %5 to i32
    store i32 %7, ptr %2, align 4
    ret i32 %6
}

define zeroext i1 @umulo.i64(i64 %v1, i64 %v2, ptr %res) {
; RV64-LABEL: umulo.i64:
;
    RV64:      # %bb.0: # %entry
; RV64-NEXT:  mulhu a3, a0, a1
; RV64-NEXT:  snez a3, a3
; RV64-NEXT:  mul a0, a0, a1
; RV64-NEXT:  sd a0, 0(a2)

```



```

; RV64-NEXT:  mv a0, a3
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.umul.with.overflow.i64(i64 %v1, i64 %v2)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
store i64 %val, ptr %res
ret i1 %obit
}

define zeroext i1 @umulo2.i64(i64 %v1, ptr %res) {
; RV64-LABEL: umulo2.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  li a3, 13
; RV64-NEXT:  mulhu a2, a0, a3
; RV64-NEXT:  snez a2, a2
; RV64-NEXT:  mul a0, a0, a3
; RV64-NEXT:  sd a0, 0(a1)
; RV64-NEXT:  mv a0, a2
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.umul.with.overflow.i64(i64 %v1, i64 13)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
store i64 %val, ptr %res
ret i1 %obit
}

;
; Check the use of the overflow bit in combination with a select instruction.
;
define i32 @saddo.select.i32(i32
signext %v1, i32 signext %v2) {
; RV64-LABEL: saddo.select.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  addw a2, a0, a1
; RV64-NEXT:  slt a2, a2, a0
; RV64-NEXT:  slti a3, a1, 0
; RV64-NEXT:  bne a3, a2, .LBB28_2
; RV64-NEXT: # %bb.1: # %entry
; RV64-NEXT:  mv a0, a1
; RV64-NEXT: .LBB28_2: # %entry
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.sadd.with.overflow.i32(i32 %v1, i32 %v2)
%obit = extractvalue {i32, i1} %t, 1
%ret = select i1 %obit, i32 %v1, i32 %v2

```

```

ret i32 %ret
}

define i1 @saddo.not.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL: saddo.not.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  addw a2, a0, a1
; RV64-NEXT:  slt a0, a2, a0
; RV64-NEXT:  slti a1, a1, 0
; RV64-NEXT:  xor a0, a1, a0
; RV64-NEXT:  xori a0, a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.sadd.with.overflow.i32(i32 %v1, i32 %v2)
%obit = extractvalue {i32, i1} %t, 1
%ret = xor i1 %obit, true
ret i1 %ret
}

define i64 @saddo.select.i64(i64
%v1, i64 %v2) {
; RV64-LABEL: saddo.select.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  add a2, a0, a1
; RV64-NEXT:  slt a2, a2, a0
; RV64-NEXT:  slti a3, a1, 0
; RV64-NEXT:  bne a3, a2, .LBB30_2
; RV64-NEXT:  # %bb.1: # %entry
; RV64-NEXT:  mv a0, a1
; RV64-NEXT:  .LBB30_2: # %entry
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.sadd.with.overflow.i64(i64 %v1, i64 %v2)
%obit = extractvalue {i64, i1} %t, 1
%ret = select i1 %obit, i64 %v1, i64 %v2
ret i64 %ret
}

define i1 @saddo.not.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: saddo.not.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  add a2, a0, a1
; RV64-NEXT:  slt a0, a2, a0
; RV64-NEXT:  slti a1, a1, 0
; RV64-NEXT:  xor a0, a1, a0
; RV64-NEXT:  xori a0, a0, 1
; RV64-NEXT:  ret
entry:

```

```

%t = call {i64, i1} @llvm.sadd.with.overflow.i64(i64 %v1, i64 %v2)
%obit = extractvalue {i64, i1} %t, 1
%ret = xor i1 %obit, true
ret i1 %ret
}

```

```

define i32 @uaddo.select.i32(i32 signext %v1,
i32 signext %v2) {
; RV64-LABEL: uaddo.select.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  addw a2, a0, a1
; RV64-NEXT:  bltu a2, a0, .LBB32_2
; RV64-NEXT:  # %bb.1: # %entry
; RV64-NEXT:  mv a0, a1
; RV64-NEXT:  .LBB32_2: # %entry
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.uadd.with.overflow.i32(i32 %v1, i32 %v2)
%obit = extractvalue {i32, i1} %t, 1
%ret = select i1 %obit, i32 %v1, i32 %v2
ret i32 %ret
}

```

```

define i1 @uaddo.not.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL: uaddo.not.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  addw a1, a0, a1
; RV64-NEXT:  sltu a0, a1, a0
; RV64-NEXT:  xori a0, a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.uadd.with.overflow.i32(i32 %v1, i32 %v2)
%obit = extractvalue {i32, i1} %t, 1
%ret = xor i1 %obit, true
ret i1 %ret
}

```

```

define i64 @uaddo.select.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: uaddo.select.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  add a2, a0, a1
; RV64-NEXT:
; RV64-NEXT:  bltu a2, a0, .LBB34_2
; RV64-NEXT:  # %bb.1: # %entry
; RV64-NEXT:  mv a0, a1
; RV64-NEXT:  .LBB34_2: # %entry
; RV64-NEXT:  ret
entry:

```

```

%t = call {i64, i1} @llvm.uadd.with.overflow.i64(i64 %v1, i64 %v2)
%obit = extractvalue {i64, i1} %t, 1
%ret = select i1 %obit, i64 %v1, i64 %v2
ret i64 %ret
}

```

```

define i1 @uaddo.not.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: uaddo.not.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  add a1, a0, a1
; RV64-NEXT:  sltu a0, a1, a0
; RV64-NEXT:  xori a0, a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.uadd.with.overflow.i64(i64 %v1, i64 %v2)
%obit = extractvalue {i64, i1} %t, 1
%ret = xor i1 %obit, true
ret i1 %ret
}

```

```

define i32 @ssubo.select.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL: ssubo.select.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  sgtz a2, a1
; RV64-NEXT:  subw a3, a0, a1
; RV64-NEXT:  slt a3, a3, a0
; RV64-NEXT:  bne a2, a3, .LBB36_2
; RV64-NEXT:  # %bb.1: # %entry
; RV64-NEXT:  mv a0,
a1
; RV64-NEXT:  .LBB36_2: # %entry
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.ssub.with.overflow.i32(i32 %v1, i32 %v2)
%obit = extractvalue {i32, i1} %t, 1
%ret = select i1 %obit, i32 %v1, i32 %v2
ret i32 %ret
}

```

```

define i1 @ssubo.not.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL: ssubo.not.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  sgtz a2, a1
; RV64-NEXT:  subw a1, a0, a1
; RV64-NEXT:  slt a0, a1, a0
; RV64-NEXT:  xor a0, a2, a0
; RV64-NEXT:  xori a0, a0, 1
; RV64-NEXT:  ret

```

```

entry:
    %t = call {i32, i1} @llvm.ssub.with.overflow.i32(i32 %v1, i32 %v2)
    %obit = extractvalue {i32, i1} %t, 1
    %ret = xor i1 %obit, true
    ret i1 %ret
}

```

```

define i64 @ssubo.select.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: ssubo.select.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  sgtz a2, a1
; RV64-NEXT:  sub a3, a0, a1
; RV64-NEXT:  slt a3, a3, a0
; RV64-NEXT:  bne a2, a3, .LBB38_2
; RV64-NEXT:  # %bb.1: # %entry
; RV64-NEXT:  mv a0, a1
; RV64-NEXT:
.LBB38_2: # %entry
; RV64-NEXT:  ret
entry:
    %t = call {i64, i1} @llvm.ssub.with.overflow.i64(i64 %v1, i64 %v2)
    %obit = extractvalue {i64, i1} %t, 1
    %ret = select i1 %obit, i64 %v1, i64 %v2
    ret i64 %ret
}

```

```

define i1 @ssub.not.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: ssub.not.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  sgtz a2, a1
; RV64-NEXT:  sub a1, a0, a1
; RV64-NEXT:  slt a0, a1, a0
; RV64-NEXT:  xor a0, a2, a0
; RV64-NEXT:  xori a0, a0, 1
; RV64-NEXT:  ret
entry:
    %t = call {i64, i1} @llvm.ssub.with.overflow.i64(i64 %v1, i64 %v2)
    %obit = extractvalue {i64, i1} %t, 1
    %ret = xor i1 %obit, true
    ret i1 %ret
}

```

```

define i32 @usubo.select.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL: usubo.select.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  subw a2, a0, a1
; RV64-NEXT:  bltu a0, a2, .LBB40_2
; RV64-NEXT:  # %bb.1: # %entry

```

```

; RV64-NEXT:  mv a0, a1
; RV64-NEXT:  .LBB40_2: # %entry
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.usub.with.overflow.i32(i32
%v1, i32 %v2)
%obit = extractvalue {i32, i1} %t, 1
%ret = select i1 %obit, i32 %v1, i32 %v2
ret i32 %ret
}

define i1 @usubo.not.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL: usubo.not.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  subw a1, a0, a1
; RV64-NEXT:  sltu a0, a0, a1
; RV64-NEXT:  xori a0, a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.usub.with.overflow.i32(i32 %v1, i32 %v2)
%obit = extractvalue {i32, i1} %t, 1
%ret = xor i1 %obit, true
ret i1 %ret
}

define i64 @usubo.select.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: usubo.select.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  sub a2, a0, a1
; RV64-NEXT:  bltu a0, a2, .LBB42_2
; RV64-NEXT:  # %bb.1: # %entry
; RV64-NEXT:  mv a0, a1
; RV64-NEXT:  .LBB42_2: # %entry
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.usub.with.overflow.i64(i64 %v1, i64 %v2)
%obit = extractvalue {i64, i1} %t, 1
%ret = select i1 %obit, i64 %v1, i64 %v2
ret i64 %ret
}

define
i1 @usubo.not.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: usubo.not.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  sub a1, a0, a1
; RV64-NEXT:  sltu a0, a0, a1
; RV64-NEXT:  xori a0, a0, 1

```

```
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.usub.with.overflow.i64(i64 %v1, i64 %v2)
%obit = extractvalue {i64, i1} %t, 1
%ret = xor i1 %obit, true
ret i1 %ret
}
```

```
define i32 @smulo.select.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL: smulo.select.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  mul a2, a0, a1
; RV64-NEXT:  srai a3, a2, 32
; RV64-NEXT:  sraiw a2, a2, 31
; RV64-NEXT:  bne a3, a2, .LBB44_2
; RV64-NEXT: # %bb.1: # %entry
; RV64-NEXT:  mv a0, a1
; RV64-NEXT: .LBB44_2: # %entry
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.smul.with.overflow.i32(i32 %v1, i32 %v2)
%obit = extractvalue {i32, i1} %t, 1
%ret = select i1 %obit, i32 %v1, i32 %v2
ret i32 %ret
}
```

```
define i1 @smulo.not.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL:
smulo.not.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  mul a0, a0, a1
; RV64-NEXT:  srai a1, a0, 32
; RV64-NEXT:  sraiw a0, a0, 31
; RV64-NEXT:  xor a0, a1, a0
; RV64-NEXT:  snez a0, a0
; RV64-NEXT:  xori a0, a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.smul.with.overflow.i32(i32 %v1, i32 %v2)
%obit = extractvalue {i32, i1} %t, 1
%ret = xor i1 %obit, true
ret i1 %ret
}
```

```
define i64 @smulo.select.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: smulo.select.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  mulh a2, a0, a1
```

```

; RV64-NEXT:  mul a3, a0, a1
; RV64-NEXT:  srai a3, a3, 63
; RV64-NEXT:  bne a2, a3, .LBB46_2
; RV64-NEXT:  # %bb.1: # %entry
; RV64-NEXT:  mv a0, a1
; RV64-NEXT:  .LBB46_2: # %entry
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.smul.with.overflow.i64(i64 %v1, i64 %v2)
%obit = extractvalue {i64, i1} %t, 1
%ret = select i1 %obit, i64 %v1, i64 %v2
ret i64 %ret
}

```

```

define i1 @smulo.not.i64(i64 %v1, i64 %v2) {
; RV64-LABEL:
smulo.not.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  mulh a2, a0, a1
; RV64-NEXT:  mul a0, a0, a1
; RV64-NEXT:  srai a0, a0, 63
; RV64-NEXT:  xor a0, a2, a0
; RV64-NEXT:  snez a0, a0
; RV64-NEXT:  xori a0, a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.smul.with.overflow.i64(i64 %v1, i64 %v2)
%obit = extractvalue {i64, i1} %t, 1
%ret = xor i1 %obit, true
ret i1 %ret
}

```

```

define i32 @umulo.select.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL: umulo.select.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  slli a2, a1, 32
; RV64-NEXT:  slli a3, a0, 32
; RV64-NEXT:  mulhu a2, a3, a2
; RV64-NEXT:  srai a2, a2, 32
; RV64-NEXT:  bnez a2, .LBB48_2
; RV64-NEXT:  # %bb.1: # %entry
; RV64-NEXT:  mv a0, a1
; RV64-NEXT:  .LBB48_2: # %entry
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.umul.with.overflow.i32(i32 %v1, i32 %v2)
%obit = extractvalue {i32, i1} %t, 1
%ret = select i1 %obit, i32 %v1, i32 %v2

```



```

ret i32 %ret
}

define
i1 @umulo.not.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL: umulo.not.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  slli a1, a1, 32
; RV64-NEXT:  slli a0, a0, 32
; RV64-NEXT:  mulhu a0, a0, a1
; RV64-NEXT:  srai a0, a0, 32
; RV64-NEXT:  snez a0, a0
; RV64-NEXT:  xori a0, a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.umul.with.overflow.i32(i32 %v1, i32 %v2)
%obit = extractvalue {i32, i1} %t, 1
%ret = xor i1 %obit, true
ret i1 %ret
}

define i64 @umulo.select.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: umulo.select.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  mulhu a2, a0, a1
; RV64-NEXT:  bnez a2, .LBB50_2
; RV64-NEXT:  # %bb.1: # %entry
; RV64-NEXT:  mv a0, a1
; RV64-NEXT:  .LBB50_2: # %entry
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.umul.with.overflow.i64(i64 %v1, i64 %v2)
%obit = extractvalue {i64, i1} %t, 1
%ret = select i1 %obit, i64 %v1, i64 %v2
ret i64 %ret
}

define i1 @umulo.not.i64(i64 %v1, i64 %v2)
{
; RV64-LABEL: umulo.not.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  mulhu a0, a0, a1
; RV64-NEXT:  snez a0, a0
; RV64-NEXT:  xori a0, a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.umul.with.overflow.i64(i64 %v1, i64 %v2)
%obit = extractvalue {i64, i1} %t, 1

```

```

%ret = xor i1 %obit, true
ret i1 %ret
}

;
; Check the use of the overflow bit in combination with a branch instruction.
;
define zeroext i1 @saddo.br.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL: saddo.br.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  addw a2, a0, a1
; RV64-NEXT:  slt a0, a2, a0
; RV64-NEXT:  slti a1, a1, 0
; RV64-NEXT:  beq a1, a0, .LBB52_2
; RV64-NEXT:  # %bb.1: # %overflow
; RV64-NEXT:  li a0, 0
; RV64-NEXT:  ret
; RV64-NEXT: .LBB52_2: # %continue
; RV64-NEXT:  li a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.sadd.with.overflow.i32(i32 %v1, i32 %v2)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
br i1
%obit, label %overflow, label %continue

overflow:
ret i1 false

continue:
ret i1 true
}

define zeroext i1 @saddo.br.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: saddo.br.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  add a2, a0, a1
; RV64-NEXT:  slt a0, a2, a0
; RV64-NEXT:  slti a1, a1, 0
; RV64-NEXT:  beq a1, a0, .LBB53_2
; RV64-NEXT:  # %bb.1: # %overflow
; RV64-NEXT:  li a0, 0
; RV64-NEXT:  ret
; RV64-NEXT: .LBB53_2: # %continue
; RV64-NEXT:  li a0, 1
; RV64-NEXT:  ret

```

```

entry:
    %t = call {i64, i1} @llvm.sadd.with.overflow.i64(i64 %v1, i64 %v2)
    %val = extractvalue {i64, i1} %t, 0
    %obit = extractvalue {i64, i1} %t, 1
    br i1 %obit, label %overflow, label %continue

```

```

overflow:
    ret i1 false

```

```

continue:
    ret i1 true
}

```

```

define zeroext i1 @uaddo.br.i32(i32 %v1, i32 %v2) {
; RV64-LABEL: uaddo.br.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  addw a1, a0, a1
; RV64-NEXT:  sext.w a0, a0
; RV64-NEXT:  bgeu a1, a0, .LBB54_2
; RV64-NEXT:  # %bb.1: # %overflow
;
; RV64-NEXT:  li a0, 0
; RV64-NEXT:  ret
; RV64-NEXT:  .LBB54_2: # %continue
; RV64-NEXT:  li a0, 1
; RV64-NEXT:  ret
entry:
    %t = call {i32, i1} @llvm.uadd.with.overflow.i32(i32 %v1, i32 %v2)
    %val = extractvalue {i32, i1} %t, 0
    %obit = extractvalue {i32, i1} %t, 1
    br i1 %obit, label %overflow, label %continue

```

```

overflow:
    ret i1 false

```

```

continue:
    ret i1 true
}

```

```

define zeroext i1 @uaddo.br.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: uaddo.br.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  add a1, a0, a1
; RV64-NEXT:  bgeu a1, a0, .LBB55_2
; RV64-NEXT:  # %bb.1: # %overflow
; RV64-NEXT:  li a0, 0
; RV64-NEXT:  ret
; RV64-NEXT:  .LBB55_2: # %continue

```

```

; RV64-NEXT:  li a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.uadd.with.overflow.i64(i64 %v1, i64 %v2)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
br i1 %obit, label %overflow, label %continue

overflow:
ret i1 false

continue:
ret i1 true
}

```

```

define zeroext i1 @ssubo.br.i32(i32
signext %v1, i32 signext %v2) {
; RV64-LABEL: ssubo.br.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  sgtz a2, a1
; RV64-NEXT:  subw a1, a0, a1
; RV64-NEXT:  slt a0, a1, a0
; RV64-NEXT:  beq a2, a0, .LBB56_2
; RV64-NEXT: # %bb.1: # %overflow
; RV64-NEXT:  li a0, 0
; RV64-NEXT:  ret
; RV64-NEXT: .LBB56_2: # %continue
; RV64-NEXT:  li a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.ssub.with.overflow.i32(i32 %v1, i32 %v2)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
br i1 %obit, label %overflow, label %continue

overflow:
ret i1 false

continue:
ret i1 true
}

```

```

define zeroext i1 @ssubo.br.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: ssubo.br.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  sgtz a2, a1
; RV64-NEXT:  sub a1, a0, a1
; RV64-NEXT:  slt a0, a1, a0

```

```

; RV64-NEXT: beq a2, a0, .LBB57_2
; RV64-NEXT: # %bb.1: # %overflow
; RV64-NEXT: li a0, 0
; RV64-NEXT: ret
; RV64-NEXT: .LBB57_2: # %continue
;
RV64-NEXT: li a0, 1
; RV64-NEXT: ret
entry:
%t = call {i64, i1} @llvm.ssub.with.overflow.i64(i64 %v1, i64 %v2)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
br i1 %obit, label %overflow, label %continue

overflow:
ret i1 false

continue:
ret i1 true
}

define zeroext i1 @usubo.br.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL: usubo.br.i32:
; RV64:    # %bb.0: # %entry
; RV64-NEXT: subw a1, a0, a1
; RV64-NEXT: bgeu a0, a1, .LBB58_2
; RV64-NEXT: # %bb.1: # %overflow
; RV64-NEXT: li a0, 0
; RV64-NEXT: ret
; RV64-NEXT: .LBB58_2: # %continue
; RV64-NEXT: li a0, 1
; RV64-NEXT: ret
entry:
%t = call {i32, i1} @llvm.usub.with.overflow.i32(i32 %v1, i32 %v2)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
br i1 %obit, label %overflow, label %continue

overflow:
ret i1 false

continue:
ret i1 true
}

define zeroext i1 @usubo.br.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: usubo.br.i64:
;

```

```

RV64:    # %bb.0: # %entry
; RV64-NEXT:  sub a1, a0, a1
; RV64-NEXT:  bgeu a0, a1, .LBB59_2
; RV64-NEXT:  # %bb.1: # %overflow
; RV64-NEXT:  li a0, 0
; RV64-NEXT:  ret
; RV64-NEXT:  .LBB59_2: # %continue
; RV64-NEXT:  li a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.usub.with.overflow.i64(i64 %v1, i64 %v2)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
br i1 %obit, label %overflow, label %continue

overflow:
ret i1 false

continue:
ret i1 true
}

define zeroext i1 @smulo.br.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL: smulo.br.i32:
; RV64:    # %bb.0: # %entry
; RV64-NEXT:  mul a0, a0, a1
; RV64-NEXT:  srai a1, a0, 32
; RV64-NEXT:  sraiw a0, a0, 31
; RV64-NEXT:  beq a1, a0, .LBB60_2
; RV64-NEXT:  # %bb.1: # %overflow
; RV64-NEXT:  li a0, 0
; RV64-NEXT:  ret
; RV64-NEXT:  .LBB60_2: # %continue
; RV64-NEXT:  li a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i32, i1} @llvm.smul.with.overflow.i32(i32
%v1, i32 %v2)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
br i1 %obit, label %overflow, label %continue

overflow:
ret i1 false

continue:
ret i1 true
}

```

```

define zeroext i1 @smulo.br.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: smulo.br.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  mulh a2, a0, a1
; RV64-NEXT:  mul a0, a0, a1
; RV64-NEXT:  srai a0, a0, 63
; RV64-NEXT:  beq a2, a0, .LBB61_2
; RV64-NEXT:  # %bb.1: # %overflow
; RV64-NEXT:  li a0, 0
; RV64-NEXT:  ret
; RV64-NEXT: .LBB61_2: # %continue
; RV64-NEXT:  li a0, 1
; RV64-NEXT:  ret
entry:
  %t = call {i64, i1} @llvm.smul.with.overflow.i64(i64 %v1, i64 %v2)
  %val = extractvalue {i64, i1} %t, 0
  %obit = extractvalue {i64, i1} %t, 1
  br i1 %obit, label %overflow, label %continue

overflow:
  ret i1 false

continue:
  ret i1 true
}

```

```

define zeroext i1 @smulo2.br.i64(i64 %v1) {
; RV64-LABEL: smulo2.br.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  li a1, -13
; RV64-NEXT:
  mulh a2, a0, a1
; RV64-NEXT:  mul a0, a0, a1
; RV64-NEXT:  srai a0, a0, 63
; RV64-NEXT:  beq a2, a0, .LBB62_2
; RV64-NEXT:  # %bb.1: # %overflow
; RV64-NEXT:  li a0, 0
; RV64-NEXT:  ret
; RV64-NEXT: .LBB62_2: # %continue
; RV64-NEXT:  li a0, 1
; RV64-NEXT:  ret
entry:
  %t = call {i64, i1} @llvm.smul.with.overflow.i64(i64 %v1, i64 -13)
  %val = extractvalue {i64, i1} %t, 0
  %obit = extractvalue {i64, i1} %t, 1
  br i1 %obit, label %overflow, label %continue

```

```

overflow:
ret i1 false

continue:
ret i1 true
}

define zeroext i1 @umulo.br.i32(i32 signext %v1, i32 signext %v2) {
; RV64-LABEL: umulo.br.i32:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  slli a1, a1, 32
; RV64-NEXT:  slli a0, a0, 32
; RV64-NEXT:  mulhu a0, a0, a1
; RV64-NEXT:  srai a0, a0, 32
; RV64-NEXT:  beqz a0, .LBB63_2
; RV64-NEXT: # %bb.1: # %overflow
; RV64-NEXT:  li a0, 0
; RV64-NEXT:  ret
; RV64-NEXT: .LBB63_2: # %continue
; RV64-NEXT:  li a0, 1
; RV64-NEXT:  ret
entry:
%t = call
{i32, i1} @llvm.umul.with.overflow.i32(i32 %v1, i32 %v2)
%val = extractvalue {i32, i1} %t, 0
%obit = extractvalue {i32, i1} %t, 1
br i1 %obit, label %overflow, label %continue

overflow:
ret i1 false

continue:
ret i1 true
}

define zeroext i1 @umulo.br.i64(i64 %v1, i64 %v2) {
; RV64-LABEL: umulo.br.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  mulhu a0, a0, a1
; RV64-NEXT:  beqz a0, .LBB64_2
; RV64-NEXT: # %bb.1: # %overflow
; RV64-NEXT:  li a0, 0
; RV64-NEXT:  ret
; RV64-NEXT: .LBB64_2: # %continue
; RV64-NEXT:  li a0, 1
; RV64-NEXT:  ret
entry:
%t = call {i64, i1} @llvm.umul.with.overflow.i64(i64 %v1, i64 %v2)

```



```

%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
br i1 %obit, label %overflow, label %continue

overflow:
ret i1 false

continue:
ret i1 true
}

define zeroext i1 @umulo2.br.i64(i64 %v1) {
; RV64-LABEL: umulo2.br.i64:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  add a1, a0, a0
; RV64-NEXT:  bgeu a1, a0,
.LBB65_2
; RV64-NEXT: # %bb.1: # %overflow
; RV64-NEXT: li a0, 0
; RV64-NEXT: ret
; RV64-NEXT: .LBB65_2: # %continue
; RV64-NEXT: li a0, 1
; RV64-NEXT: ret
entry:
%t = call {i64, i1} @llvm.umul.with.overflow.i64(i64 %v1, i64 2)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
br i1 %obit, label %overflow, label %continue

overflow:
ret i1 false

continue:
ret i1 true
}

define zeroext i1 @uaddo.i64.constant(i64 %v1, ptr %res) {
; RV64-LABEL: uaddo.i64.constant:
; RV64:      # %bb.0: # %entry
; RV64-NEXT: addi a2, a0, 2
; RV64-NEXT: sltu a0, a2, a0
; RV64-NEXT: sd a2, 0(a1)
; RV64-NEXT: ret
entry:
%t = call {i64, i1} @llvm.uadd.with.overflow.i64(i64 %v1, i64 2)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
store i64 %val, ptr %res

```

```

ret i1 %obit
}

define zeroext i1 @uaddo.i64.constant_2048(i64 %v1, ptr %res) {
; RV64-LABEL: uaddo.i64.constant_2048:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:
    addi a2, a0, 2047
; RV64-NEXT:  addi a2, a2, 1
; RV64-NEXT:  sltu a0, a2, a0
; RV64-NEXT:  sd a2, 0(a1)
; RV64-NEXT:  ret
entry:
    %t = call {i64, i1} @llvm.uadd.with.overflow.i64(i64 %v1, i64 2048)
    %val = extractvalue {i64, i1} %t, 0
    %obit = extractvalue {i64, i1} %t, 1
    store i64 %val, ptr %res
    ret i1 %obit
}

define zeroext i1 @uaddo.i64.constant_2049(i64 %v1, ptr %res) {
; RV64-LABEL: uaddo.i64.constant_2049:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  addi a2, a0, 2047
; RV64-NEXT:  addi a2, a2, 2
; RV64-NEXT:  sltu a0, a2, a0
; RV64-NEXT:  sd a2, 0(a1)
; RV64-NEXT:  ret
entry:
    %t = call {i64, i1} @llvm.uadd.with.overflow.i64(i64 %v1, i64 2049)
    %val = extractvalue {i64, i1} %t, 0
    %obit = extractvalue {i64, i1} %t, 1
    store i64 %val, ptr %res
    ret i1 %obit
}

define i64 @uaddo.i64.constant_setcc_on_overflow_flag(ptr %p) {
; RV64-LABEL: uaddo.i64.constant_setcc_on_overflow_flag:
; RV64:      # %bb.0: # %entry
; RV64-NEXT:  ld a1, 0(a0)
;
    RV64-NEXT:  addi a0, a1, 2
; RV64-NEXT:  bltu a0, a1, .LBB69_2
; RV64-NEXT:  # %bb.1: # %IfOverflow
; RV64-NEXT:  li a0, 0
; RV64-NEXT:  .LBB69_2: # %IfNoOverflow
; RV64-NEXT:  ret
entry:

```

```

%v1 = load i64, ptr %p
%t = call {i64, i1} @llvm.uadd.with.overflow.i64(i64 %v1, i64 2)
%val = extractvalue {i64, i1} %t, 0
%obit = extractvalue {i64, i1} %t, 1
br i1 %obit, label %IfNoOverflow, label %IfOverflow
IfOverflow:
ret i64 0
IfNoOverflow:
ret i64 %val
}

```

```

declare {i32, i1} @llvm.sadd.with.overflow.i32(i32, i32) nounwind readnone
declare {i64, i1} @llvm.sadd.with.overflow.i64(i64, i64) nounwind readnone
declare {i32, i1} @llvm.uadd.with.overflow.i32(i32, i32) nounwind readnone
declare {i64, i1} @llvm.uadd.with.overflow.i64(i64, i64) nounwind readnone
declare {i32, i1} @llvm.ssub.with.overflow.i32(i32, i32) nounwind readnone
declare {i64, i1} @llvm.ssub.with.overflow.i64(i64, i64) nounwind readnone
declare {i32, i1} @llvm.usub.with.overflow.i32(i32, i32) nounwind readnone
declare
  {i64, i1} @llvm.usub.with.overflow.i64(i64, i64) nounwind readnone
declare {i32, i1} @llvm.smul.with.overflow.i32(i32, i32) nounwind readnone
declare {i64, i1} @llvm.smul.with.overflow.i64(i64, i64) nounwind readnone
declare {i32, i1} @llvm.umul.with.overflow.i32(i32, i32) nounwind readnone
declare {i64, i1} @llvm.umul.with.overflow.i64(i64, i64) nounwind readnone

```

=====

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2cc784086c8a087e4008cc9f558624bd

add_llvm_library(llvmPluginObjectContainerBSDArchive PLUGIN
ObjectContainerBSDArchive.cpp

LINK_LIBS

llvmCore

llvmHost

llvmSymbol

LINK_COMPONENTS

Support

)

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```
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck -check-prefix=RV64I %s
; RUN: llc -mtriple=riscv64 -mattr=+m -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck -check-prefix=RV64IM %s
```

```
define i32 @udiv(i32 %a, i32 %b) nounwind {
; RV64I-LABEL: udiv:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  slli a1, a1, 32
; RV64I-NEXT:  srli a1, a1, 32
; RV64I-NEXT:  call __udivdi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: udiv:
```



```

; RV64IM:    # %bb.0:
; RV64IM-NEXT:  divuw a0, a0, a1
; RV64IM-NEXT:  ret
%1 = udiv i32 %a, %b
ret i32 %1
}

define i32 @udiv_constant(i32 %a) nounwind {
; RV64I-LABEL:
udiv_constant:
; RV64I:    # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a0, a0, 32
; RV64I-NEXT:  li a1, 5
; RV64I-NEXT:  call __udivdi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: udiv_constant:
; RV64IM:    # %bb.0:
; RV64IM-NEXT:  slli a0, a0, 32
; RV64IM-NEXT:  lui a1, 838861
; RV64IM-NEXT:  addi a1, a1, -819
; RV64IM-NEXT:  slli a1, a1, 32
; RV64IM-NEXT:  mulhu a0, a0, a1
; RV64IM-NEXT:  srli a0, a0, 34
; RV64IM-NEXT:  ret
%1 = udiv i32 %a, 5
ret i32 %1
}

define i32 @udiv_pow2(i32 %a) nounwind {
; RV64I-LABEL: udiv_pow2:
; RV64I:    # %bb.0:
; RV64I-NEXT:  srliw a0, a0, 3
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: udiv_pow2:
; RV64IM:    # %bb.0:
; RV64IM-NEXT:  srliw a0, a0, 3
; RV64IM-NEXT:  ret
%1 = udiv i32 %a, 8
ret i32 %1
}

```

```

define i32 @udiv_constant_lhs(i32
    %a) nounwind {
; RV64I-LABEL: udiv_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a0, a0, 32
; RV64I-NEXT:  srli a1, a0, 32
; RV64I-NEXT:  li a0, 10
; RV64I-NEXT:  call __udivdi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: udiv_constant_lhs:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  li a1, 10
; RV64IM-NEXT:  divuw a0, a1, a0
; RV64IM-NEXT:  ret
    %1 = udiv i32 10, %a
    ret i32 %1
}

```

```

define i64 @udiv64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: udiv64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  tail __udivdi3
;
; RV64IM-LABEL: udiv64:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  divu a0, a0, a1
; RV64IM-NEXT:  ret
    %1 = udiv i64 %a, %b
    ret i64 %1
}

```

```

define i64 @udiv64_constant(i64 %a) nounwind {
; RV64I-LABEL: udiv64_constant:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 5
; RV64I-NEXT:
    tail __udivdi3
;
; RV64IM-LABEL: udiv64_constant:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  lui a1, 838861
; RV64IM-NEXT:  addiw a1, a1, -819
; RV64IM-NEXT:  slli a2, a1, 32

```

```

; RV64IM-NEXT:  add a1, a1, a2
; RV64IM-NEXT:  mulhu a0, a0, a1
; RV64IM-NEXT:  srli a0, a0, 2
; RV64IM-NEXT:  ret
%1 = udiv i64 %a, 5
ret i64 %1
}

```

```

define i64 @udiv64_constant_lhs(i64 %a) nounwind {
; RV64I-LABEL: udiv64_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT:  mv a1, a0
; RV64I-NEXT:  li a0, 10
; RV64I-NEXT:  tail __udivdi3
;
; RV64IM-LABEL: udiv64_constant_lhs:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  li a1, 10
; RV64IM-NEXT:  divu a0, a1, a0
; RV64IM-NEXT:  ret
%1 = udiv i64 10, %a
ret i64 %1
}

```

```

define i8 @udiv8(i8 %a, i8 %b) nounwind {
; RV64I-LABEL: udiv8:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  andi a0, a0, 255
; RV64I-NEXT:  andi a1, a1, 255
; RV64I-NEXT:  call
__udivdi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: udiv8:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  andi a1, a1, 255
; RV64IM-NEXT:  andi a0, a0, 255
; RV64IM-NEXT:  divuw a0, a0, a1
; RV64IM-NEXT:  ret
%1 = udiv i8 %a, %b
ret i8 %1
}

```

```

define i8 @udiv8_constant(i8 %a) nounwind {

```

```

; RV64I-LABEL: udiv8_constant:
; RV64I:    # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  andi a0, a0, 255
; RV64I-NEXT:  li a1, 5
; RV64I-NEXT:  call __udivdi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: udiv8_constant:
; RV64IM:    # %bb.0:
; RV64IM-NEXT:  andi a0, a0, 255
; RV64IM-NEXT:  li a1, 205
; RV64IM-NEXT:  mul a0, a0, a1
; RV64IM-NEXT:  srliw a0, a0, 10
; RV64IM-NEXT:  ret
%1 = udiv i8 %a, 5
ret i8 %1
}

```

```

define i8 @udiv8_pow2(i8 %a) nounwind
{
; RV64I-LABEL: udiv8_pow2:
; RV64I:    # %bb.0:
; RV64I-NEXT:  slli a0, a0, 56
; RV64I-NEXT:  srli a0, a0, 59
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: udiv8_pow2:
; RV64IM:    # %bb.0:
; RV64IM-NEXT:  slli a0, a0, 56
; RV64IM-NEXT:  srli a0, a0, 59
; RV64IM-NEXT:  ret
%1 = udiv i8 %a, 8
ret i8 %1
}

```

```

define i8 @udiv8_constant_lhs(i8 %a) nounwind {
; RV64I-LABEL: udiv8_constant_lhs:
; RV64I:    # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  andi a1, a0, 255
; RV64I-NEXT:  li a0, 10
; RV64I-NEXT:  call __udivdi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload

```

```

; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: udiv8_constant_lhs:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  andi a0, a0, 255
; RV64IM-NEXT:  li a1, 10
; RV64IM-NEXT:  divuw a0, a1, a0
; RV64IM-NEXT:  ret
%1 = udiv i8 10, %a
ret i8 %1
}

define i16 @udiv16(i16 %a, i16 %b) nounwind {
; RV64I-LABEL: udiv16:
;
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  lui a2, 16
; RV64I-NEXT:  addiw a2, a2, -1
; RV64I-NEXT:  and a0, a0, a2
; RV64I-NEXT:  and a1, a1, a2
; RV64I-NEXT:  call __udivdi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: udiv16:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  lui a2, 16
; RV64IM-NEXT:  addi a2, a2, -1
; RV64IM-NEXT:  and a1, a1, a2
; RV64IM-NEXT:  and a0, a0, a2
; RV64IM-NEXT:  divuw a0, a0, a1
; RV64IM-NEXT:  ret
%1 = udiv i16 %a, %b
ret i16 %1
}

define i16 @udiv16_constant(i16 %a) nounwind {
; RV64I-LABEL: udiv16_constant:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a0, a0, 48
; RV64I-NEXT:  srli a0, a0, 48
; RV64I-NEXT:  li a1, 5

```

```

; RV64I-NEXT:  call __udivdi3
; RV64I-NEXT:  ld ra, 8(sp)
; # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: udiv16_constant:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  lui a1, 52429
; RV64IM-NEXT:  slli a1, a1, 4
; RV64IM-NEXT:  slli a0, a0, 48
; RV64IM-NEXT:  mulhu a0, a0, a1
; RV64IM-NEXT:  srliw a0, a0, 18
; RV64IM-NEXT:  ret
%1 = udiv i16 %a, 5
ret i16 %1
}

define i16 @udiv16_pow2(i16 %a) nounwind {
; RV64I-LABEL: udiv16_pow2:
; RV64I:      # %bb.0:
; RV64I-NEXT:  slli a0, a0, 48
; RV64I-NEXT:  srli a0, a0, 51
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: udiv16_pow2:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  slli a0, a0, 48
; RV64IM-NEXT:  srli a0, a0, 51
; RV64IM-NEXT:  ret
%1 = udiv i16 %a, 8
ret i16 %1
}

define i16 @udiv16_constant_lhs(i16 %a) nounwind {
; RV64I-LABEL: udiv16_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a0, a0, 48
; RV64I-NEXT:  srli a1, a0, 48
; RV64I-NEXT:
;   li a0, 10
; RV64I-NEXT:  call __udivdi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;

```

```

; RV64IM-LABEL: udiv16_constant_lhs:
; RV64IM:      # %bb.0:
; RV64IM-NEXT: slli a0, a0, 48
; RV64IM-NEXT: srli a0, a0, 48
; RV64IM-NEXT: li a1, 10
; RV64IM-NEXT: divuw a0, a1, a0
; RV64IM-NEXT: ret
%1 = udiv i16 10, %a
ret i16 %1
}

```

```

define i32 @sdiv(i32 %a, i32 %b) nounwind {
; RV64I-LABEL: sdiv:
; RV64I:      # %bb.0:
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT: sext.w a0, a0
; RV64I-NEXT: sext.w a1, a1
; RV64I-NEXT: call __divdi3
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
;
; RV64IM-LABEL: sdiv:
; RV64IM:      # %bb.0:
; RV64IM-NEXT: divw a0, a0, a1
; RV64IM-NEXT: ret
%1 = sdiv i32 %a, %b
ret i32 %1
}

```

```

define i32 @sdiv_constant(i32 %a) nounwind {
; RV64I-LABEL: sdiv_constant:
;
; RV64I:      # %bb.0:
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT: sext.w a0, a0
; RV64I-NEXT: li a1, 5
; RV64I-NEXT: call __divdi3
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
;
; RV64IM-LABEL: sdiv_constant:
; RV64IM:      # %bb.0:
; RV64IM-NEXT: sext.w a0, a0
; RV64IM-NEXT: lui a1, 419430

```

```

; RV64IM-NEXT:  addiw a1, a1, 1639
; RV64IM-NEXT:  mul a0, a0, a1
; RV64IM-NEXT:  srli a1, a0, 63
; RV64IM-NEXT:  srai a0, a0, 33
; RV64IM-NEXT:  addw a0, a0, a1
; RV64IM-NEXT:  ret
%1 = sdiv i32 %a, 5
ret i32 %1
}

```

```

define i32 @sdiv_pow2(i32 %a) nounwind {
; RV64I-LABEL: sdiv_pow2:
; RV64I:      # %bb.0:
; RV64I-NEXT:  sraiw a1, a0, 31
; RV64I-NEXT:  srliw a1, a1, 29
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  sraiw a0, a0, 3
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: sdiv_pow2:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  sraiw a1, a0,
31
; RV64IM-NEXT:  srliw a1, a1, 29
; RV64IM-NEXT:  add a0, a0, a1
; RV64IM-NEXT:  sraiw a0, a0, 3
; RV64IM-NEXT:  ret
%1 = sdiv i32 %a, 8
ret i32 %1
}

```

```

define i32 @sdiv_pow2_2(i32 %a) nounwind {
; RV64I-LABEL: sdiv_pow2_2:
; RV64I:      # %bb.0:
; RV64I-NEXT:  sraiw a1, a0, 31
; RV64I-NEXT:  srliw a1, a1, 16
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  sraiw a0, a0, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: sdiv_pow2_2:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  sraiw a1, a0, 31
; RV64IM-NEXT:  srliw a1, a1, 16
; RV64IM-NEXT:  add a0, a0, a1
; RV64IM-NEXT:  sraiw a0, a0, 16
; RV64IM-NEXT:  ret
%1 = sdiv i32 %a, 65536

```



```

ret i32 %1
}

define i32 @sdiv_constant_lhs(i32 %a) nounwind {
; RV64I-LABEL: sdiv_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  sext.w a1, a0
; RV64I-NEXT:  li a0, -10
; RV64I-NEXT:  call __divdi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded
Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: sdiv_constant_lhs:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  li a1, -10
; RV64IM-NEXT:  divw a0, a1, a0
; RV64IM-NEXT:  ret
%1 = sdiv i32 -10, %a
ret i32 %1
}

define i64 @sdiv64(i64 %a, i64 %b) nounwind {
; RV64I-LABEL: sdiv64:
; RV64I:      # %bb.0:
; RV64I-NEXT:  tail __divdi3
;
; RV64IM-LABEL: sdiv64:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  div a0, a0, a1
; RV64IM-NEXT:  ret
%1 = sdiv i64 %a, %b
ret i64 %1
}

define i64 @sdiv64_constant(i64 %a) nounwind {
; RV64I-LABEL: sdiv64_constant:
; RV64I:      # %bb.0:
; RV64I-NEXT:  li a1, 5
; RV64I-NEXT:  tail __divdi3
;
; RV64IM-LABEL: sdiv64_constant:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  lui a1, %hi(.LCPI21_0)
; RV64IM-NEXT:  ld a1, %lo(.LCPI21_0)(a1)

```

```

; RV64IM-NEXT:  mulh a0, a0, a1
; RV64IM-NEXT:  srli a1, a0, 63
; RV64IM-NEXT:  srai a0, a0, 1
; RV64IM-NEXT:  add a0, a0, a1
; RV64IM-NEXT:  ret
%1 = sdiv i64 %a,
5
ret i64 %1
}

```

```

define i64 @sdiv64_constant_lhs(i64 %a) nounwind {
; RV64I-LABEL: sdiv64_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT:  mv a1, a0
; RV64I-NEXT:  li a0, 10
; RV64I-NEXT:  tail __divdi3
;
; RV64IM-LABEL: sdiv64_constant_lhs:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  li a1, 10
; RV64IM-NEXT:  div a0, a1, a0
; RV64IM-NEXT:  ret
%1 = sdiv i64 10, %a
ret i64 %1
}

```

; Although this sdiv has two sexti32 operands, it shouldn't compile to divw on
; RV64M as that wouldn't produce the correct result for e.g. INT_MIN/-1.

```

define i64 @sdiv64_sext_operands(i32 %a, i32 %b) nounwind {
; RV64I-LABEL: sdiv64_sext_operands:
; RV64I:      # %bb.0:
; RV64I-NEXT:  sext.w a0, a0
; RV64I-NEXT:  sext.w a1, a1
; RV64I-NEXT:  tail __divdi3
;
; RV64IM-LABEL: sdiv64_sext_operands:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  sext.w a0, a0
; RV64IM-NEXT:  sext.w a1, a1
; RV64IM-NEXT:  div a0, a0, a1
; RV64IM-NEXT:  ret
%1 = sext i32 %a to i64
%2 = sext i32 %b to
i64
%3 = sdiv i64 %1, %2
ret i64 %3
}

```

```

define i8 @sdiv8(i8 %a, i8 %b) nounwind {
; RV64I-LABEL: sdiv8:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a1, a1, 24
; RV64I-NEXT:  sraiw a1, a1, 24
; RV64I-NEXT:  slli a0, a0, 24
; RV64I-NEXT:  sraiw a0, a0, 24
; RV64I-NEXT:  call __divdi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: sdiv8:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  slli a1, a1, 24
; RV64IM-NEXT:  sraiw a1, a1, 24
; RV64IM-NEXT:  slli a0, a0, 24
; RV64IM-NEXT:  sraiw a0, a0, 24
; RV64IM-NEXT:  divw a0, a0, a1
; RV64IM-NEXT:  ret
%1 = sdiv i8 %a, %b
ret i8 %1
}

```

```

define i8 @sdiv8_constant(i8 %a) nounwind {
; RV64I-LABEL: sdiv8_constant:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a0, a0, 24
; RV64I-NEXT:
; RV64I-NEXT:  sraiw a0, a0, 24
; RV64I-NEXT:  li a1, 5
; RV64I-NEXT:  call __divdi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: sdiv8_constant:
; RV64IM:      # %bb.0:
; RV64IM-NEXT:  slli a0, a0, 24
; RV64IM-NEXT:  sraiw a0, a0, 24
; RV64IM-NEXT:  li a1, 103
; RV64IM-NEXT:  mul a0, a0, a1
; RV64IM-NEXT:  sraiw a1, a0, 9

```

```

; RV64IM-NEXT:  slli a0, a0, 48
; RV64IM-NEXT:  srli a0, a0, 63
; RV64IM-NEXT:  addw a0, a1, a0
; RV64IM-NEXT:  ret
%1 = sdiv i8 %a, 5
ret i8 %1
}

```

```

define i8 @sdiv8_pow2(i8 %a) nounwind {
; RV64I-LABEL: sdiv8_pow2:
; RV64I:      # %bb.0:
; RV64I-NEXT: slli a1, a0, 24
; RV64I-NEXT: sraiw a1, a1, 24
; RV64I-NEXT: slli a1, a1, 49
; RV64I-NEXT: srli a1, a1, 61
; RV64I-NEXT: add a0, a0, a1
; RV64I-NEXT: slli a0, a0, 24
; RV64I-NEXT: sraiw a0, a0, 27
; RV64I-NEXT: ret
;
; RV64IM-LABEL: sdiv8_pow2:
; RV64IM:     # %bb.0:
; RV64IM-NEXT: slli a1, a0,
24
; RV64IM-NEXT: sraiw a1, a1, 24
; RV64IM-NEXT: slli a1, a1, 49
; RV64IM-NEXT: srli a1, a1, 61
; RV64IM-NEXT: add a0, a0, a1
; RV64IM-NEXT: slli a0, a0, 24
; RV64IM-NEXT: sraiw a0, a0, 27
; RV64IM-NEXT: ret
%1 = sdiv i8 %a, 8
ret i8 %1
}

```

```

define i8 @sdiv8_constant_lhs(i8 %a) nounwind {
; RV64I-LABEL: sdiv8_constant_lhs:
; RV64I:      # %bb.0:
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT: slli a0, a0, 24
; RV64I-NEXT: sraiw a1, a0, 24
; RV64I-NEXT: li a0, -10
; RV64I-NEXT: call __divdi3
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
;

```

```

; RV64IM-LABEL: sdiv8_constant_lhs:
; RV64IM:      # %bb.0:
; RV64IM-NEXT: slli a0, a0, 24
; RV64IM-NEXT: sraiw a0, a0, 24
; RV64IM-NEXT: li a1, -10
; RV64IM-NEXT: divw a0, a1, a0
; RV64IM-NEXT: ret
%1 = sdiv i8 -10, %a
ret i8 %1
}

define i16 @sdiv16(i16 %a, i16 %b) nounwind {
; RV64I-LABEL:
sdiv16:
; RV64I:      # %bb.0:
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT: slli a1, a1, 16
; RV64I-NEXT: sraiw a1, a1, 16
; RV64I-NEXT: slli a0, a0, 16
; RV64I-NEXT: sraiw a0, a0, 16
; RV64I-NEXT: call __divdi3
; RV64I-NEXT: ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
;
; RV64IM-LABEL: sdiv16:
; RV64IM:      # %bb.0:
; RV64IM-NEXT: slli a1, a1, 16
; RV64IM-NEXT: sraiw a1, a1, 16
; RV64IM-NEXT: slli a0, a0, 16
; RV64IM-NEXT: sraiw a0, a0, 16
; RV64IM-NEXT: divw a0, a0, a1
; RV64IM-NEXT: ret
%1 = sdiv i16 %a, %b
ret i16 %1
}

define i16 @sdiv16_constant(i16 %a) nounwind {
; RV64I-LABEL: sdiv16_constant:
; RV64I:      # %bb.0:
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT: slli a0, a0, 16
; RV64I-NEXT: sraiw a0, a0, 16
; RV64I-NEXT: li a1, 5
; RV64I-NEXT: call __divdi3
; RV64I-NEXT:

```

```

    ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: sdiv16_constant:
; RV64IM:      # %bb.0:
; RV64IM-NEXT: slli a0, a0, 16
; RV64IM-NEXT: sraiw a0, a0, 16
; RV64IM-NEXT: lui a1, 6
; RV64IM-NEXT: addi a1, a1, 1639
; RV64IM-NEXT: mul a0, a0, a1
; RV64IM-NEXT: srliw a1, a0, 31
; RV64IM-NEXT: sraiw a0, a0, 17
; RV64IM-NEXT: addw a0, a0, a1
; RV64IM-NEXT: ret
%1 = sdiv i16 %a, 5
ret i16 %1
}

define i16 @sdiv16_pow2(i16 %a) nounwind {
; RV64I-LABEL: sdiv16_pow2:
; RV64I:      # %bb.0:
; RV64I-NEXT: slli a1, a0, 16
; RV64I-NEXT: sraiw a1, a1, 16
; RV64I-NEXT: slli a1, a1, 33
; RV64I-NEXT: srli a1, a1, 61
; RV64I-NEXT: add a0, a0, a1
; RV64I-NEXT: slli a0, a0, 16
; RV64I-NEXT: sraiw a0, a0, 19
; RV64I-NEXT: ret
;
; RV64IM-LABEL: sdiv16_pow2:
; RV64IM:      # %bb.0:
; RV64IM-NEXT: slli a1, a0, 16
; RV64IM-NEXT: sraiw a1, a1, 16
; RV64IM-NEXT: slli a1, a1, 33
;
RV64IM-NEXT: srli a1, a1, 61
; RV64IM-NEXT: add a0, a0, a1
; RV64IM-NEXT: slli a0, a0, 16
; RV64IM-NEXT: sraiw a0, a0, 19
; RV64IM-NEXT: ret
%1 = sdiv i16 %a, 8
ret i16 %1
}

define i16 @sdiv16_constant_lhs(i16 %a) nounwind {
; RV64I-LABEL: sdiv16_constant_lhs:

```

```

; RV64I:    # %bb.0:
; RV64I-NEXT:  addi sp, sp, -16
; RV64I-NEXT:  sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT:  slli a0, a0, 16
; RV64I-NEXT:  sraiw a1, a0, 16
; RV64I-NEXT:  li a0, -10
; RV64I-NEXT:  call __divdi3
; RV64I-NEXT:  ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT:  addi sp, sp, 16
; RV64I-NEXT:  ret
;
; RV64IM-LABEL: sdiv16_constant_lhs:
; RV64IM:    # %bb.0:
; RV64IM-NEXT:  slli a0, a0, 16
; RV64IM-NEXT:  sraiw a0, a0, 16
; RV64IM-NEXT:  li a1, -10
; RV64IM-NEXT:  divw a0, a1, a0
; RV64IM-NEXT:  ret
%1 = sdiv i16 -10, %a
ret i16 %1
}

```

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck -check-prefix=RV64I %s

; Check indexed and unindexed, sext, zext and anyext loads

```
define dso_local i64 @lb(ptr %a) nounwind {  
; RV64I-LABEL: lb:  
; RV64I:      # %bb.0:  
; RV64I-NEXT: lb a1, 1(a0)  
; RV64I-NEXT: lbu zero, 0(a0)  
; RV64I-NEXT: mv a0, a1  
; RV64I-NEXT: ret  
%1 = getelementptr i8, ptr %a, i32 1  
%2 = load i8, ptr %1  
%3 = sext i8 %2 to i64  
; the unused load will produce an anyext for selection  
%4 = load volatile i8, ptr %a  
ret i64 %3  
}
```

```

define dso_local i64 @lh(ptr %a) nounwind {
; RV64I-LABEL: lh:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lh a1, 4(a0)
; RV64I-NEXT:  lh zero, 0(a0)
; RV64I-NEXT:  mv a0, a1
; RV64I-NEXT:  ret
%1 = getelementptr i16, ptr %a, i32 2
%2 = load i16, ptr %1
%3 = sext i16 %2 to i64
; the unused load will produce an anyext for selection
%4 = load volatile i16, ptr %a
ret i64 %3
}

```

```

define dso_local i64 @lw(ptr %a) nounwind {
; RV64I-LABEL: lw:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lw a1, 12(a0)
; RV64I-NEXT:  lw zero, 0(a0)
; RV64I-NEXT:  mv a0, a1
; RV64I-NEXT:  ret
%1 = getelementptr i32, ptr %a, i32 3
%2 = load i32, ptr %1
%3 = sext i32 %2 to i64
; the unused load will produce an anyext for selection
%4 = load volatile i32, ptr %a
ret i64 %3
}

```

```

define dso_local i64 @lbu(ptr %a) nounwind {
; RV64I-LABEL: lbu:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lbu a1, 4(a0)
; RV64I-NEXT:  lbu a0, 0(a0)
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  ret
%1 = getelementptr i8, ptr %a, i32 4
%2 = load i8, ptr %1
%3 = zext i8 %2 to i64
%4 = load volatile i8, ptr %a
%5 = zext i8 %4 to i64
%6 = add i64 %3, %5
ret i64 %6
}

```

```

define dso_local i64 @lhu(ptr %a) nounwind {

```

```

; RV64I-LABEL: lhu:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lhu a1, 10(a0)
; RV64I-NEXT:  lhu a0, 0(a0)
; RV64I-NEXT:
    add a0, a1, a0
; RV64I-NEXT:  ret
%1 = getelementptr i16, ptr %a, i32 5
%2 = load i16, ptr %1
%3 = zext i16 %2 to i64
%4 = load volatile i16, ptr %a
%5 = zext i16 %4 to i64
%6 = add i64 %3, %5
ret i64 %6
}

```

```

define dso_local i64 @lwu(ptr %a) nounwind {
; RV64I-LABEL: lwu:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lwu a1, 24(a0)
; RV64I-NEXT:  lwu a0, 0(a0)
; RV64I-NEXT:  add a0, a1, a0
; RV64I-NEXT:  ret
%1 = getelementptr i32, ptr %a, i32 6
%2 = load i32, ptr %1
%3 = zext i32 %2 to i64
%4 = load volatile i32, ptr %a
%5 = zext i32 %4 to i64
%6 = add i64 %3, %5
ret i64 %6
}

```

; 64-bit loads and stores

```

define dso_local i64 @ld(ptr %a) nounwind {
; RV64I-LABEL: ld:
; RV64I:      # %bb.0:
; RV64I-NEXT:  ld a1, 80(a0)
; RV64I-NEXT:  ld zero, 0(a0)
; RV64I-NEXT:  mv a0, a1
; RV64I-NEXT:  ret
%1 = getelementptr i64, ptr %a, i32 10
%2 = load i64, ptr %1
%3 = load volatile i64, ptr %a
ret i64 %2
}

```

```

define dso_local void @sd(ptr %a, i64 %b)

```



```

nounwind {
; RV64I-LABEL: sd:
; RV64I:    # %bb.0:
; RV64I-NEXT:  sd a1, 0(a0)
; RV64I-NEXT:  sd a1, 88(a0)
; RV64I-NEXT:  ret
store i64 %b, ptr %a
%1 = getelementptr i64, ptr %a, i32 11
store i64 %b, ptr %1
ret void
}

; Check load and store to an i1 location
define dso_local i64 @load_sext_zext_anyext_i1(ptr %a) nounwind {
; RV64I-LABEL: load_sext_zext_anyext_i1:
; RV64I:    # %bb.0:
; RV64I-NEXT:  lbu a1, 1(a0)
; RV64I-NEXT:  lbu a2, 2(a0)
; RV64I-NEXT:  lbu zero, 0(a0)
; RV64I-NEXT:  sub a0, a2, a1
; RV64I-NEXT:  ret
; sextload i1
%1 = getelementptr i1, ptr %a, i32 1
%2 = load i1, ptr %1
%3 = sext i1 %2 to i64
; zextload i1
%4 = getelementptr i1, ptr %a, i32 2
%5 = load i1, ptr %4
%6 = zext i1 %5 to i64
%7 = add i64 %3, %6
; extload i1 (anyext). Produced as the load is unused.
%8 = load volatile i1, ptr %a
ret i64 %7
}

define dso_local i16 @load_sext_zext_anyext_i1_i16(ptr %a) nounwind {
; RV64I-LABEL: load_sext_zext_anyext_i1_i16:
;
; RV64I:    # %bb.0:
; RV64I-NEXT:  lbu a1, 1(a0)
; RV64I-NEXT:  lbu a2, 2(a0)
; RV64I-NEXT:  lbu zero, 0(a0)
; RV64I-NEXT:  subw a0, a2, a1
; RV64I-NEXT:  ret
; sextload i1
%1 = getelementptr i1, ptr %a, i32 1
%2 = load i1, ptr %1
%3 = sext i1 %2 to i16

```

```

; zextload i1
%4 = getelementptr i1, ptr %a, i32 2
%5 = load i1, ptr %4
%6 = zext i1 %5 to i16
%7 = add i16 %3, %6
; extload i1 (anyext). Produced as the load is unused.
%8 = load volatile i1, ptr %a
ret i16 %7
}

```

```

; Check load and store to a global
@G = dso_local global i64 0

```

```

define dso_local i64 @ld_sd_global(i64 %a) nounwind {
; RV64I-LABEL: ld_sd_global:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a2, %hi(G)
; RV64I-NEXT:  ld a1, %lo(G)(a2)
; RV64I-NEXT:  addi a3, a2, %lo(G)
; RV64I-NEXT:  sd a0, %lo(G)(a2)
; RV64I-NEXT:  ld zero, 72(a3)
; RV64I-NEXT:  sd a0, 72(a3)
; RV64I-NEXT:  mv a0, a1
; RV64I-NEXT:  ret
%1 = load volatile i64, ptr @G
store i64 %a, ptr @G
%2 = getelementptr
i64, ptr @G, i64 9
%3 = load volatile i64, ptr %2
store i64 %a, ptr %2
ret i64 %1
}

```

```

define i64 @lw_near_local(ptr %a) {
; RV64I-LABEL: lw_near_local:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi a0, a0, 2047
; RV64I-NEXT:  ld a0, 9(a0)
; RV64I-NEXT:  ret
%1 = getelementptr inbounds i64, ptr %a, i64 257
%2 = load volatile i64, ptr %1
ret i64 %2
}

```

```

define void @st_near_local(ptr %a, i64 %b) {
; RV64I-LABEL: st_near_local:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi a0, a0, 2047

```

```

; RV64I-NEXT:  sd a1, 9(a0)
; RV64I-NEXT:  ret
%1 = getelementptr inbounds i64, ptr %a, i64 257
store i64 %b, ptr %1
ret void
}

define i64 @lw_sw_near_local(ptr %a, i64 %b) {
; RV64I-LABEL: lw_sw_near_local:
; RV64I:      # %bb.0:
; RV64I-NEXT:  addi a2, a0, 2047
; RV64I-NEXT:  ld a0, 9(a2)
; RV64I-NEXT:  sd a1, 9(a2)
; RV64I-NEXT:  ret
%1 = getelementptr inbounds i64, ptr %a, i64 257
%2 = load volatile i64, ptr %1
store i64 %b, ptr %1
ret i64 %2
}

define
i64 @lw_far_local(ptr %a) {
; RV64I-LABEL: lw_far_local:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a1, 8
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ld a0, -8(a0)
; RV64I-NEXT:  ret
%1 = getelementptr inbounds i64, ptr %a, i64 4095
%2 = load volatile i64, ptr %1
ret i64 %2
}

define void @st_far_local(ptr %a, i64 %b) {
; RV64I-LABEL: st_far_local:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a2, 8
; RV64I-NEXT:  add a0, a0, a2
; RV64I-NEXT:  sd a1, -8(a0)
; RV64I-NEXT:  ret
%1 = getelementptr inbounds i64, ptr %a, i64 4095
store i64 %b, ptr %1
ret void
}

define i64 @lw_sw_far_local(ptr %a, i64 %b) {
; RV64I-LABEL: lw_sw_far_local:
; RV64I:      # %bb.0:

```

```

; RV64I-NEXT:  lui a2, 8
; RV64I-NEXT:  add a2, a0, a2
; RV64I-NEXT:  ld a0, -8(a2)
; RV64I-NEXT:  sd a1, -8(a2)
; RV64I-NEXT:  ret
%1 = getelementptr inbounds i64, ptr %a, i64 4095
%2 = load volatile i64, ptr %1
store i64 %b, ptr %1
ret i64 %2
}

```

```

; Make sure we don't fold the addiw
into the load offset. The sign extend of the
; addiw is required.
define i64 @lw_really_far_local(ptr %a) {
; RV64I-LABEL: lw_really_far_local:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a1, 524288
; RV64I-NEXT:  addiw a1, a1, -2048
; RV64I-NEXT:  add a0, a0, a1
; RV64I-NEXT:  ld a0, 0(a0)
; RV64I-NEXT:  ret
%1 = getelementptr inbounds i64, ptr %a, i64 268435200
%2 = load volatile i64, ptr %1
ret i64 %2
}

```

```

; Make sure we don't fold the addiw into the store offset. The sign extend of
; the addiw is required.
define void @st_really_far_local(ptr %a, i64 %b) {
; RV64I-LABEL: st_really_far_local:
; RV64I:      # %bb.0:
; RV64I-NEXT:  lui a2, 524288
; RV64I-NEXT:  addiw a2, a2, -2048
; RV64I-NEXT:  add a0, a0, a2
; RV64I-NEXT:  sd a1, 0(a0)
; RV64I-NEXT:  ret
%1 = getelementptr inbounds i64, ptr %a, i64 268435200
store i64 %b, ptr %1
ret void
}

```

```

; Make sure we don't fold the addiw into the load/store offset. The sign extend
; of the addiw is required.
define
i64 @lw_sw_really_far_local(ptr %a, i64 %b) {
; RV64I-LABEL: lw_sw_really_far_local:
; RV64I:      # %bb.0:

```

```
; RV64I-NEXT: lui a2, 524288
; RV64I-NEXT: addiw a2, a2, -2048
; RV64I-NEXT: add a2, a0, a2
; RV64I-NEXT: ld a0, 0(a2)
; RV64I-NEXT: sd a1, 0(a2)
; RV64I-NEXT: ret
%1 = getelementptr inbounds i64, ptr %a, i64 268435200
%2 = load volatile i64, ptr %1
store i64 %b, ptr %1
ret i64 %2
}
```

```
%struct.quux = type { i32, [0 x i8] }
```

```
; Make sure we don't remove the addi and fold the C from
; (add (addi FrameIndex, C), X) into the store address.
; FrameIndex cannot be the operand of an ADD. We must keep the ADDI.
define void @addi_fold_crash(i64 %arg) nounwind {
; RV64I-LABEL: addi_fold_crash:
; RV64I:      # %bb.0: # %bb
; RV64I-NEXT: addi sp, sp, -16
; RV64I-NEXT: sd ra, 8(sp) # 8-byte Folded Spill
; RV64I-NEXT: addi a1, sp, 4
; RV64I-NEXT: add a0, a1, a0
; RV64I-NEXT: sb zero, 0(a0)
; RV64I-NEXT: mv a0, a1
; RV64I-NEXT: call snork
; RV64I-NEXT:
    ld ra, 8(sp) # 8-byte Folded Reload
; RV64I-NEXT: addi sp, sp, 16
; RV64I-NEXT: ret
bb:
%tmp = alloca %struct.quux, align 8
%tmp1 = getelementptr inbounds %struct.quux, ptr %tmp, i64 0, i32 1
%tmp2 = getelementptr inbounds %struct.quux, ptr %tmp, i64 0, i32 1, i64 %arg
store i8 0, ptr %tmp2, align 1
call void @snork(ptr %tmp1)
ret void
}
```

```
declare void @snork(ptr)
```

```
; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature --
scrub-attributes
```

```
; RUN: opt -S -passes=argpromotion < %s | FileCheck %s
```

```
; Test that we only promote arguments when the caller/callee have compatible
```

```
; function attributes.
```

```
target triple = "x86_64-unknown-linux-gnu"
```

```

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr %arg, ptr
readonly %arg1) #0 {
; CHECK-LABEL: define {{^[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; CHECK-SAME: (ptr [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT:   store <8 x i64> [[ARG1_VAL]], ptr [[ARG]]
; CHECK-NEXT:   ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
}

```

```

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr %arg) #0 {
; CHECK-LABEL: define {{^[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
; CHECK-SAME:
(ptr [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT:   [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:   [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:   call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT:   [[TMP_VAL:%.*]] = load <8 x i64>, ptr [[TMP]]
; CHECK-NEXT:   call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT:   [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT:   store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CHECK-NEXT:   ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}

```

```

; This should promote
define
internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr %arg, ptr readonly
%arg1) #1 {
; CHECK-LABEL: define {{^[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:

```

```

; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], ptr [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr %arg) #1 {
; CHECK-LABEL: define {{^[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, ptr [[TMP]]
; CHECK-NEXT: call fastcc
void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr [[TMP2]], <8 x i64>
[[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr %arg, ptr
readonly %arg1) #1 {
; CHECK-LABEL: define {{^[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]],
ptr [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void

```

```

}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr %arg) #0 {
; CHECK-LABEL: define {{^[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, ptr [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align
32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr %arg, ptr
readonly %arg1) #0 {
; CHECK-LABEL: define {{^[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (ptr [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], ptr [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr %arg) #1 {
; CHECK-LABEL: define {{^[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (ptr [[ARG:%.*]])
; CHECK-NEXT:
bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

```



```

; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, ptr [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}

```

; This should not promote

```

define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr
%arg, ptr readonly %arg1) #1 {
; CHECK-LABEL: define {{{^@}+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]], ptr readonly [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1]]
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
}

```

```

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr %arg) #2 {
; CHECK-LABEL: define {{{^@}+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr
[[TMP2]], ptr [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CHECK-NEXT: ret void
;

```

```

bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr %arg, ptr
readonly %arg1) #2 {
; CHECK-LABEL: define {{{^@}+}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]], ptr readonly [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1]]
; CHECK-NEXT: store <8 x i64>
[[TMP]], ptr [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr %arg) #1 {
; CHECK-LABEL: define {{{^@}+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr
[[TMP2]], ptr [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64
32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2

```

```
ret void
}
```

; This should promote

```
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr %arg, ptr readonly
%arg1) #3 {
; CHECK-LABEL: define {{[^@]++}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], ptr [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
}
```

```
define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr %arg) #4 {
; CHECK-LABEL: define {{[^@]++}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:
[[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, ptr [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}
```

; This should promote

```
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr %arg, ptr readonly
%arg1) #4 {
;
```

```

CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT:   store <8 x i64> [[ARG1_VAL]], ptr [[ARG]]
; CHECK-NEXT:   ret void
;
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
}

```

```

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr %arg) #3 {
; CHECK-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT:   [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:   [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:   call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT:   [[TMP_VAL:%.*]] = load <8 x i64>, ptr [[TMP]]
; CHECK-NEXT:   call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT:   [[TMP4:%.*]] = load
<8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT:   store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CHECK-NEXT:   ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}

```

; If the arguments are scalar, its ok to promote.

```

define internal i32 @scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr %X, ptr %Y)
#2 {
; CHECK-LABEL: define
{{[^@]+}}@scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (i32 [[X_VAL:%.*]], i32 [[Y_VAL:%.*]])
; CHECK-NEXT:   [[C:%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
; CHECK-NEXT:   ret i32 [[C]]
;
%A = load i32, ptr %X
%B = load i32, ptr %Y

```

```

%C = add i32 %A, %B
ret i32 %C
}

```

```

define i32 @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr
%B) #2 {
; CHECK-LABEL: define {{[^@]+}}@scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[B:%.*]])
; CHECK-NEXT: [[A:%.*]] = alloca i32
; CHECK-NEXT: store i32 1, ptr [[A]]
; CHECK-NEXT: [[A_VAL:%.*]] = load i32, ptr [[A]]
; CHECK-NEXT: [[B_VAL:%.*]] = load i32, ptr [[B]]
; CHECK-NEXT: [[C:%.*]] = call i32
@scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32 [[A_VAL]], i32 [[B_VAL]])
; CHECK-NEXT: ret i32 [[C]]
;
%A = alloca i32
store i32 1, ptr %A
%C = call i32 @scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr %A, ptr %B)
ret i32 %C
}

```

; If the arguments are scalar, its ok to promote.

```

define internal i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr %X, ptr %Y)
#2 {
; CHECK-LABEL: define
{{[^@]+}}@scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (i32 [[X_VAL:%.*]],
i32 [[Y_VAL:%.*]])
; CHECK-NEXT: [[C:%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
; CHECK-NEXT: ret i32 [[C]]
;
%A = load i32, ptr %X
%B = load i32, ptr %Y
%C = add i32 %A, %B
ret i32 %C
}

```

```

define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr %B) #2 {
; CHECK-LABEL: define {{[^@]+}}@scalar_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (ptr [[B:%.*]])
; CHECK-NEXT: [[A:%.*]] = alloca i32
; CHECK-NEXT: store i32 1, ptr [[A]]
; CHECK-NEXT: [[A_VAL:%.*]] = load i32, ptr [[A]]
; CHECK-NEXT: [[B_VAL:%.*]] = load i32, ptr [[B]]
; CHECK-NEXT: [[C:%.*]] = call i32
@scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32 [[A_VAL]], i32 [[B_VAL]])
; CHECK-NEXT: ret i32 [[C]]

```

```

;
%A = alloca i32
store i32 1, ptr %A
%C = call i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr %A, ptr %B)
ret i32 %C
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0.i64(ptr
nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512"
"prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256"
"prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=riscv64 -mattr=+zbc -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefix=RV64ZBC-ZBKC
; RUN: llc -mtriple=riscv64 -mattr=+zbkc -verify-machineinstrs < %s \
; RUN: -riscv-experimental-rv64-legal-i32 | FileCheck %s -check-prefix=RV64ZBC-ZBKC

declare i64 @llvm.riscv.clmul.i64(i64 %a, i64 %b)

define i64 @clmul64(i64 %a, i64 %b) nounwind {
; RV64ZBC-ZBKC-LABEL: clmul64:
; RV64ZBC-ZBKC:      # %bb.0:
; RV64ZBC-ZBKC-NEXT:  clmul a0, a0, a1
; RV64ZBC-ZBKC-NEXT:  ret
%tmp = call i64 @llvm.riscv.clmul.i64(i64 %a, i64 %b)
ret i64 %tmp
}

declare i64 @llvm.riscv.clmulh.i64(i64 %a, i64 %b)

define i64 @clmul64h(i64 %a, i64 %b) nounwind {
; RV64ZBC-ZBKC-LABEL: clmul64h:
; RV64ZBC-ZBKC:      # %bb.0:
; RV64ZBC-ZBKC-NEXT:  clmulh a0, a0, a1
; RV64ZBC-ZBKC-NEXT:  ret
%tmp = call i64 @llvm.riscv.clmulh.i64(i64 %a, i64 %b)
ret i64 %tmp

```

```

}

declare
i32 @llvm.riscv.clmul.i32(i32 %a, i32 %b)

define signext i32 @clmul32(i32 signext %a, i32 signext %b) nounwind {
; RV64ZBC-ZBKC-LABEL: clmul32:
; RV64ZBC-ZBKC:      # %bb.0:
; RV64ZBC-ZBKC-NEXT:  clmul a0, a0, a1
; RV64ZBC-ZBKC-NEXT:  sext.w a0, a0
; RV64ZBC-ZBKC-NEXT:  ret
%tmp = call i32 @llvm.riscv.clmul.i32(i32 %a, i32 %b)
ret i32 %tmp
}

declare i32 @llvm.riscv.clmulh.i32(i32 %a, i32 %b)

define signext i32 @clmul32h(i32 signext %a, i32 signext %b) nounwind {
; RV64ZBC-ZBKC-LABEL: clmul32h:
; RV64ZBC-ZBKC:      # %bb.0:
; RV64ZBC-ZBKC-NEXT:  slli a1, a1, 32
; RV64ZBC-ZBKC-NEXT:  slli a0, a0, 32
; RV64ZBC-ZBKC-NEXT:  clmulh a0, a0, a1
; RV64ZBC-ZBKC-NEXT:  srai a0, a0, 32
; RV64ZBC-ZBKC-NEXT:  ret
%tmp = call i32 @llvm.riscv.clmulh.i32(i32 %a, i32 %b)
ret i32 %tmp
}

; FIXME: We could avoid the slli instructions by using clmul+srai since the
; inputs are zero extended.
define signext i32 @clmul32h_zext(i32 zeroext %a, i32 zeroext %b) nounwind {
;
RV64ZBC-ZBKC-LABEL: clmul32h_zext:
; RV64ZBC-ZBKC:      # %bb.0:
; RV64ZBC-ZBKC-NEXT:  slli a1, a1, 32
; RV64ZBC-ZBKC-NEXT:  slli a0, a0, 32
; RV64ZBC-ZBKC-NEXT:  clmulh a0, a0, a1
; RV64ZBC-ZBKC-NEXT:  srai a0, a0, 32
; RV64ZBC-ZBKC-NEXT:  ret
%tmp = call i32 @llvm.riscv.clmulh.i32(i32 %a, i32 %b)
ret i32 %tmp
}

```

1.27 openssl 1.1.1q

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lib/erl/src/Makefile.am

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For the aclocal/ax_boost_base.m4 and contrib/fb303/aclocal/ax_boost_base.m4

components:

```
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#
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```

For the lib/nodejs/lib/thrift/json_parse.js:

```
/*
  json_parse.js
  2015-05-02
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  */
(By Douglas Crockford <douglas@crockford.com>)
```

For lib/cpp/src/thrift/windows/SocketPair.cpp

```
/* socketpair.c
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 */
```

For lib/py/compat/win32/stdint.h

```
// ISO C9x compliantstdint.h for Microsoft Visual Studio
// Based on ISO/IEC 9899:TC2 Committee draft (May 6, 2005) WG14/N1124
//
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//
////////////////////////////////////
```

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in t_html_generator.h

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*

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*

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For t_cl_generator.cc

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1.30 protobuf 3.21.6

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* Small patch to handle trailing slashes in --proto_path flag.

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* Small patch to fix Python CallMethod().

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* Small optimizations to Python serialization.

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* VI syntax highlighting tweaks.

* Fix compiler to not make output executable.

Dilip Joseph <dilip.antony.joseph@gmail.com>

* Heuristic detection of sub-messages when printing unknown fields in text format.

Brian Atkinson <nairb774@gmail.com>

* Added @Override annotation to generated Java code where appropriate.

Vincent Choiniere <Choiniere.Vincent@hydro.qc.ca>

* Tru64 support.

Monty Taylor <monty.taylor@gmail.com>

- * Solaris 10 + Sun Studio fixes.

Alek Storm <alek.storm@gmail.com>

- * Slicing support for repeated scalar fields for the Python API.

Oleg Smolsky <oleg.smolsky@gmail.com>

- * MS Visual Studio error format option.
- * Detect unordered_map in stl_hash.m4.

Brian Olson <brianolson@google.com>

- * gzip/zlib I/O support.

Michael Poole <mdpoole@troilus.org>

- * Fixed warnings about generated constructors not explicitly initializing all fields (only present with certain compiler settings).
- * Added generation of field number constants.

Wink Saville <wink@google.com>

- * Fixed initialization ordering problem in logging code.

Will Pierce <willp@nuclei.com>

- * Small patch improving performance of in Python serialization.

Alexandre Vassalotti <alexandre@peadrop.com>

- * Emacs mode for Protocol Buffers (editors/protobuf-mode.el).

Scott Stafford <scott.stafford@gmail.com>

- * Added Swap(), SwapElements(), and RemoveLast() to Reflection interface.

Alexander Melnikov <alm@sibmail.ru>

- * HPUX support.

Oliver Jowett <oliver.jowett@gmail.com>

- * Detect whether zlib is new enough in configure script.
- * Fixes for Solaris 10 32/64-bit confusion.

Evan Jones <evanj@mit.edu>

- * Optimize Java serialization code when writing a small message to a stream.
- * Optimize Java serialization of strings so that UTF-8 encoding happens only once per string per serialization call.
- * Clean up some Java warnings.
- * Fix bug with permanent callbacks that delete themselves when run.

Michael Kucharski <m.kucharski@gmail.com>

- * Added CodedInputStream.getTotalBytesRead().

Kacper Kowalik <xarthisius.kk@gmail.com>

- * Fixed m4/acx_pthread.m4 problem for some Linux distributions.

William Orr <will@worrbase.com>

- * Fixed detection of sched_yield on Solaris.
- * Added atomicops for Solaris

Andrew Paprocki <andrew@ishiboo.com>

- * Fixed minor IBM xLC compiler build issues
- * Added atomicops for AIX (POWER)

Nipunn Koorapati <nipunn1313@gmail.com>

- * Provide a type alias field ValueType on EnumTypeWrapper
- * Match service argument names to abstract interface

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1.31 Iz4 1.9.4

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Upstream-Name: liblz4

Upstream-Contact: Yann Collet <Cyan4973@github.com>

Source: <https://github.com/lz4/lz4>

Files: *

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1.36 swingx-all 1.6.5

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 * $Id: DefaultUserNameStore.java 4147 2012-02-01 17:13:24Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/auth/DefaultUserNameStore.java

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/*
 * $Id: AbstractTreeTableModel.java 3780 2010-09-09 16:17:41Z kschaefe $
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/treetable/AbstractTreeTableModel.java

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```
/*
 * $Id: Targetable.java 3972 2011-03-17 20:31:58Z kschaefe $
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/action/Targetable.java

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 * $Id: ToolTipHighlighter.java 3676 2010-04-26 15:42:26Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/ToolTipHighlighter.java
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/*
* $Id: JXHeader.java 4147 2012-02-01 17:13:24Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXHeader.java
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```

/*
* $Id: GradientTrackRenderer.java 4082 2011-11-15 18:39:43Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/color/GradientTrackRenderer.java
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/*
 * \$Id: IconValue.java 3298 2009-03-11 13:51:25Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/IconValue.java
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/*
 * $Id: ShadowRenderer.java 4082 2011-11-15 18:39:43Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/graphics/ShadowRenderer.java

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```

/*
 * $Id: WrappingProvider.java 3927 2011-02-22 16:34:11Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/WrappingProvider.java

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/*

* \$Id: TreeTableCellEditor.java 3990 2011-03-31 13:41:08Z kleopatra \$

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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/treetable/TreeTableCellEditor.java

No license file was found, but licenses were detected in source scan.

/*

* \$Id: CellContext.java 3778 2010-09-07 10:10:49Z kleopatra \$

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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/CellContext.java

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/*

* \$Id: GaussianBlurFilter.java 4219 2012-08-07 04:11:12Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/image/GaussianBlurFilter.java

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/*

```

* $Id: BusyPainter.java 4156 2012-02-02 19:54:38Z kschaefe $
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*/

```

Found in path(s):

```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/BusyPainter.java

```

No license file was found, but licenses were detected in source scan.

/swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/resources/TipOfTheDay24.gif: binary file matches

Found in path(s):

```

* /bin/grep

```

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```

/*

```

```

* $Id: TreeTableNode.java 3927 2011-02-22 16:34:11Z kleopatra $
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*/

Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/treetable/TreeTableNode.java

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/*

* \$Id: JXRadioGroup.java 4158 2012-02-03 18:29:40Z kschaefe \$

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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXRadioGroup.java

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/*

* \$Id: JXImagePanel.java 4017 2011-05-10 21:00:48Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXImagePanel.java
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/*
* \$Id: TreeRolloverController.java 3100 2008-10-14 22:33:10Z rah003 \$
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/rollover/TreeRolloverController.java
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/*
* \$Id: UIDependent.java 4028 2011-06-03 19:32:19Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/UIDependent.java
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/*
 * \$Id: DefaultTreeTableModel.java 3780 2010-09-09 16:17:41Z kschaefe \$
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/treetable/DefaultTreeTableModel.java
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/*
 * \$Id: BasicTitledPanelUI.java 3927 2011-02-22 16:34:11Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/BasicTitledPanelUI.java
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```
/*
 * $Id: JDBCLoginService.java 4147 2012-02-01 17:13:24Z kschaefe $
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/auth/JDBCLoginService.java
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```
/*
 * $Id: JAASLoginService.java 4147 2012-02-01 17:13:24Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/auth/JAASLoginService.java
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/*
* $Id: JXHyperlink.java 4162 2012-02-08 16:21:35Z kschaefe $
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```

Found in path(s):

```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXHyperlink.java

```


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```
/*
 * $Id: AbstractHighlighter.java 3927 2011-02-22 16:34:11Z kleopatra $
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```

Found in path(s):

```
*/swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/AbstractHighlighter.java
```

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```
/*
 * $Id: DefaultXTreeCellRenderer.java 3304 2009-03-20 15:11:25Z kleopatra $
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*/

Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/tree/DefaultXTreeCellRenderer.java

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/*

* \$Id: JXTableHeader.java 3960 2011-03-15 19:36:53Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXTableHeader.java

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/*

* \$Id: NumberEditorNumberFormat.java 3781 2010-09-15 08:33:52Z kleopatra \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/table/NumberEditorNumberFormat.java
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* \$Id: OpenBrowserAction.java 3972 2011-03-17 20:31:58Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/action/OpenBrowserAction.java
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* \$Id: CalendarCellContext.java 3286 2009-03-10 12:13:43Z kleopatra \$
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```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/CalendarCellContext.java
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```

```

/*
* $Id: package-info.java 4146 2012-01-25 19:40:05Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/package-info.java
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/*
* $Id: JXFindBar.java 4147 2012-02-01 17:13:24Z kschaefe $
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXFindBar.java

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/*
 * $Id: LabelProvider.java 3100 2008-10-14 22:33:10Z rah003 $
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/LabelProvider.java

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```
/*
 * $Id: TipOfTheDayModel.java 542 2005-10-10 18:03:15Z rbair $
 *
 */
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/tips/TipOfTheDayModel.java
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 * \$Id: WindowsClassicLookAndFeelAddons.java 4092 2011-11-30 18:04:36Z kschaefe \$
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/windows/WindowsClassicLookAndFeelAddons.java

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```
/*
 * $Id: AreaEffect.java 3241 2009-02-01 21:18:40Z rah003 $
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```

Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/effects/AreaEffect.java

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```
/*
 * $Id: AlphaPainter.java 4147 2012-02-01 17:13:24Z kschaefe $
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```

Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/AlphaPainter.java

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/*

* \$Id: HeaderUI.java 1422 2006-09-25 23:06:11Z rbair \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/HeaderUI.java

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/*

* \$Id: BasicStatusBarUI.java 3927 2011-02-22 16:34:11Z kleopatra \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/BasicStatusBarUI.java

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/*

* \$Id: LookAndFeelAddons.java 4250 2012-11-13 18:15:34Z kschaefe \$

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/*

* \$Id: PainterPaint.java 4082 2011-11-15 18:39:43Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/PainterPaint.java
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* \$Id: ComboBoxCellEditor.java 4051 2011-07-19 20:17:05Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/autocomplete/ComboBoxCellEditor.java
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/*
* \$Id: JXMonthView.java 4147 2012-02-01 17:13:24Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXMonthView.java
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 * \$Id: DatePickerFormatter.java 3140 2008-12-16 15:09:09Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/calendar/DatePickerFormatter.java
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/*
 * \$Id: InnerShadowPathEffect.java 1837 2007-03-15 22:44:22Z josh \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/effects/InnerShadowPathEffect.java
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```

/*
* $Id: TitledPanelAddon.java 3288 2009-03-10 14:36:28Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/TitledPanelAddon.java
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```

/*
* $Id: DefaultSplitPaneModel.java 3100 2008-10-14 22:33:10Z rah003 $
*

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/multisplitpane/DefaultSplitPaneModel.java
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 * \$Id: CalendarUtils.java 3916 2011-01-12 10:21:58Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/calendar/CalendarUtils.java

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/*
 * $Id: TreeModelSupport.java 3100 2008-10-14 22:33:10Z rah003 $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/tree/TreeModelSupport.java

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/*
 * $Id: DropShadowBorder.java 4147 2012-02-01 17:13:24Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/border/DropShadowBorder.java

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* \$Id: NimbusLookAndFeelAddons.java 4092 2011-11-30 18:04:36Z kschaefe \$

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/*

* \$Id: TreeSearchable.java 4178 2012-06-20 08:52:11Z kleopatra \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/search/TreeSearchable.java
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* \$Id: GlossyTaskPaneUI.java 3448 2009-08-19 08:12:23Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/misc/GlossyTaskPaneUI.java
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* \$Id: package-info.java 3972 2011-03-17 20:31:58Z kschaefe \$
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* \$Id: TipOfTheDayUI.java 542 2005-10-10 18:03:15Z rbair \$
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* \$Id: StringValues.java 3927 2011-02-22 16:34:11Z kleopatra \$
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/StringValues.java

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/*
 * $Id: CheckBoxProvider.java 3152 2008-12-23 18:12:39Z kschaefe $
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/*
 * $Id: ErrorSupport.java 3840 2010-10-09 03:25:17Z kschaefe $
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/auth/KeyChain.java

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```

/*
 * $Id: LinkModelAction.java 3927 2011-02-22 16:34:11Z kleopatra $
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```

Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/hyperlink/LinkModelAction.java

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/*

* \$Id: ActionFactory.java 3972 2011-03-17 20:31:58Z kschaefe \$

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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/action/ActionFactory.java

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/*

* \$Id: RolloverRenderer.java 3100 2008-10-14 22:33:10Z rah003 \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/rollover/RolloverRenderer.java

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/*

* \$Id: AbstractLayoutPainter.java 4079 2011-11-15 16:05:13Z kschaefe \$

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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/AbstractLayoutPainter.java

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/*

* \$Id: OS.java 4088 2011-11-17 19:53:49Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/util/OS.java
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/*
* \$Id: ColumnControlButton.java 4065 2011-08-19 13:28:26Z kleopatra \$
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/table/ColumnControlButton.java
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/*
* \$Id: ResetDTCRCColorHighlighter.java 3100 2008-10-14 22:33:10Z rah003 \$
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/ResetDTCRColorHighlighter.java

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```
/*
 * $Id: ImagePainter.java 4261 2012-11-19 18:38:46Z kschaefe $
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Found in path(s):

- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/ImagePainter.java

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```
/*
 * $Id: WindowsClassicTaskPaneUI.java 3448 2009-08-19 08:12:23Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/windows/WindowsClassicTaskPaneUI.java
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```

/*
* $Id: ErrorReporter.java 3166 2009-01-02 13:27:18Z rah003 $
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```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/error/ErrorReporter.java
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```

/*
* $Id: LinkModel.java 2951 2008-06-17 10:07:49Z kleopatra $
*

```

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Found in path(s):

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/hyperlink/LinkModel.java
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```

/*
* $Id: Contract.java 4028 2011-06-03 19:32:19Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/util/Contract.java
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```

/*
 * $Id: JXList.java 4158 2012-02-03 18:29:40Z kschaefe $
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Found in path(s):

```
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXList.java
```

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```

/*
 * $Id: Painters.java 3590 2010-01-12 19:19:45Z kschaefe $
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```
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/Painters.java
```

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```
/*
 * $Id: TipOfTheDayAddon.java 2474 2007-11-21 17:32:04Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/TipOfTheDayAddon.java

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```
/*
 * $Id: MetalStatusBarUI.java 3472 2009-08-27 13:12:42Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/metal/MetalStatusBarUI.java

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/*

* \$Id: DefaultListRenderer.java 3779 2010-09-07 18:01:55Z kschaefe \$

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/*

* \$Id: AbstractHyperlinkAction.java 3484 2009-09-03 15:55:34Z kleopatra \$

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* \$Id: BasicMonthViewUI.java 3927 2011-02-22 16:34:11Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/BasicMonthViewUI.java
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/TableHeaderAddon.java
 *
 /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/synth/SynthUtils.java
 * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/core/LazyActionMap.java
 * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/AlignmentHighlighter.java
 * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/sort/DefaultSortController.java
 * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/TableAddon.java
 * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/LookAndFeelUtils.java
 * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/core/BasicXListUI.java
 * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/sort/StringValueRegistry.java

```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/table/StrictNumberFormatter.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/core/BasicTransferable.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/search/PatternMatcher.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/synth/SynthUI.java
*
/swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/text/StrictNumberFormatter.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/table/NumberFormatExt.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/sort/TableSortController.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/sort/StringValueProvider.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/nimbus/NimbusTaskPaneUI.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/EnabledHighlighter.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/event/TreeExpansionBroadcaster.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/sort/RowFilters.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/synth/SynthXListUI.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/synth/XRegion.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/hyperlink/HyperlinkAction.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/table/TableRowHeightController.java
*
/swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/text/NumberFormatExt.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/core/ListSortUI.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/ScrollableSizeHint.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/sort/ListSortController.java
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```

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```

Found in path(s):

```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/combobox/MapComboBoxModel.java

```


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```
/*
 * $Id: DefaultTipOfTheDayModel.java 3927 2011-02-22 16:34:11Z kleopatra $
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Found in path(s):

```
*/swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/tips/DefaultTipOfTheDayModel.java
```

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```
/*
 * $Id: DateSpan.java 542 2005-10-10 18:03:15Z rbair $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/calendar/DateSpan.java

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/*

* \$Id: JXDialog.java 4172 2012-04-17 14:54:00Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXDialog.java

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/*

* \$Id: package-info.java 4028 2011-06-03 19:32:19Z kschaefe \$

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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/motif/package-info.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/linux/package-info.java
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/*
* \$Id: MutableTreeTableNode.java 3927 2011-02-22 16:34:11Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/treetable/MutableTreeTableNode.java
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/*
* \$Id: HyperlinkProvider.java 3927 2011-02-22 16:34:11Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/HyperlinkProvider.java
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/*
* \$Id: ErrorPaneAddon.java 3475 2009-08-28 08:30:47Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/ErrorPaneAddon.java
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/*
* \$Id: EnumComboBoxModel.java 3475 2009-08-28 08:30:47Z kleopatra \$
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/combobox/EnumComboBoxModel.java

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```
/*
 * $Id: JXTipOfTheDay.java 4147 2012-02-01 17:13:24Z kschaefe $
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXTipOfTheDay.java

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```
/*
 * $Id: PinstripePainter.java 4259 2012-11-14 20:07:00Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/PinstripePainter.java
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/*
 * \$Id: DateSelectionListener.java 3100 2008-10-14 22:33:10Z rah003 \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/event/DateSelectionListener.java
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/*
 * $Id: DatePickerAddon.java 3100 2008-10-14 22:33:10Z rah003 $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/DatePickerAddon.java

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/*
 * $Id: ColumnControlIcon.java 3927 2011-02-22 16:34:11Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/icon/ColumnControlIcon.java

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/*

* \$Id: JVM.java 4236 2012-08-13 17:32:35Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/util/JVM.java

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/*

* \$Id: HyperlinkAddon.java 3745 2010-08-06 03:02:52Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/HyperlinkAddon.java

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* \$Id: AbstractRenderer.java 3927 2011-02-22 16:34:11Z kleopatra \$

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/*

* \$Id: LoginPaneAddon.java 3033 2008-08-12 05:05:44Z rah003 \$

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* \$Id: MultiThumbSliderAddon.java 3100 2008-10-14 22:33:10Z rah003 \$
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/*
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/image/FastBlurFilter.java

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 * \$Id: AbstractMutableTreeTableNode.java 3780 2010-09-09 16:17:41Z kschaefe \$
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/*
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```
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/treetable/SimpleFileSystemModel.java
```

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```

/*
 * $Id: BasicMultiThumbSliderUI.java 3927 2011-02-22 16:34:11Z kleopatra $
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Found in path(s):

```
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/BasicMultiThumbSliderUI.java
```

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```
/*
```

```

* $Id: EyeDropperColorChooserPanel.java 4082 2011-11-15 18:39:43Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/color/EyeDropperColorChooserPanel.java
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```

```

/*
* $Id: Thumb.java 3259 2009-02-17 21:06:19Z kschaefe $
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```

Found in path(s):

```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/multislider/Thumb.java

```

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```
/*
 * $Id: FileSystemModel.java 3927 2011-02-22 16:34:11Z kleopatra $
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 */
```

Found in path(s):

`/swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/treetable/FileSystemModel.java`

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```
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 * $Id: TableRolloverController.java 3641 2010-04-01 10:48:43Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/rollover/TableRolloverController.java

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/*

* \$Id: AbstractFilter.java 3863 2010-10-26 02:53:32Z kschaefe \$

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/*

* \$Id: MetalTaskPaneUI.java 3448 2009-08-19 08:12:23Z kleopatra \$

```

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/metal/MetalTaskPaneUI.java
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```

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* $Id: BasicHyperlinkUI.java 3927 2011-02-22 16:34:11Z kleopatra $
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Found in path(s):

```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/BasicHyperlinkUI.java

```

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```
/*
 * $Id: DefaultMultiThumbModel.java 3935 2011-03-02 19:06:41Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/multislider/DefaultMultiThumbModel.java

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```
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 * $Id: UserPermissions.java 542 2005-10-10 18:03:15Z rbair $
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/*

* \$Id: BorderHighlighter.java 3100 2008-10-14 22:33:10Z rah003 \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/BorderHighlighter.java

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* \$Id: ColorHighlighter.java 4082 2011-11-15 18:39:43Z kschaefe \$

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* \$Id: ListAdaptor.java 4045 2011-07-19 18:39:17Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/autocomplete/ListAdaptor.java
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* \$Id: JXEditorPane.java 4147 2012-02-01 17:13:24Z kschaefe \$
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 * $Id: ShapeUtils.java 4082 2011-11-15 18:39:43Z kschaefe $
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* $Id: AbstractPainter.java 4082 2011-11-15 18:39:43Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/AbstractPainter.java
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```

/*
* $Id: PainterAware.java 3472 2009-08-27 13:12:42Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/CalendarHeaderHandler.java

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* \$Id: AutoComplete.java 4051 2011-07-19 20:17:05Z kschaefe \$

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* \$Id: BooleanValue.java 3100 2008-10-14 22:33:10Z rah003 \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/search/SearchFactory.java
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/*
* \$Id: MatteBorderExt.java 4147 2012-02-01 17:13:24Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/border/MatteBorderExt.java
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/*
* \$Id: WindowsStatusBarUI.java 3472 2009-08-27 13:12:42Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/windows/WindowsStatusBarUI.java
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```
/*
 * $Id: TableColumnModelExt.java 3927 2011-02-22 16:34:11Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/table/TableColumnModelExt.java
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```
/*
 * $Id: JXTitledPanel.java 4260 2012-11-14 20:59:08Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXTitledPanel.java
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```
/*
 * $Id: MacOSXErrorPaneUI.java 3475 2009-08-28 08:30:47Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/macosex/MacOSXErrorPaneUI.java
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```

/*
 * $Id: PainterIcon.java 3927 2011-02-22 16:34:11Z kleopatra $
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/icon/PainterIcon.java

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```

/*
 * $Id: PainterHighlighter.java 3927 2011-02-22 16:34:11Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/PainterHighlighter.java

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/*

* \$Id: TargetableAction.java 3972 2011-03-17 20:31:58Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/action/TargetableAction.java

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* \$Id: JXRootPane.java 4147 2012-02-01 17:13:24Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXRootPane.java

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* \$Id: MattePainter.java 4147 2012-02-01 17:13:24Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/MattePainter.java

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/*

* \$Id: package-info.java 4084 2011-11-15 18:53:49Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/util/package-info.java

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/*
* \$Id: InnerGlowPathEffect.java 1837 2007-03-15 22:44:22Z josh \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/effects/InnerGlowPathEffect.java

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/*
* \$Id: TextCrossingPainter.java 3100 2008-10-14 22:33:10Z rah003 \$
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/TextCrossingPainter.java

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 * $Id: StackBlurFilter.java 4082 2011-11-15 18:39:43Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/image/StackBlurFilter.java

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* \$Id: BasicTaskPaneUI.java 4260 2012-11-14 20:59:08Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/BasicTaskPaneUI.java

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* \$Id: EmptyIcon.java 3927 2011-02-22 16:34:11Z kleopatra \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/icon/EmptyIcon.java
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* \$Id: MacOSXPopupLocationFix.java 4019 2011-05-11 16:52:30Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/autocomplete/workarounds/MacOSXPopupLocationFix.java
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/*
* \$Id: ComboBoxAdaptor.java 4051 2011-07-19 20:17:05Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/autocomplete/ComboBoxAdaptor.java
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```

/*
 * $Id: AbstractDateSelectionModel.java 3927 2011-02-22 16:34:11Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/calendar/AbstractDateSelectionModel.java
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/*
 * $Id: WindowsTaskPaneUI.java 3448 2009-08-19 08:12:23Z kleopatra $
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/windows/WindowsTaskPaneUI.java

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/*
 * $Id: package-info.java 3167 2009-01-02 13:28:04Z rah003 $
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/table/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/treetable/package-info.java

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/event/EventListenerMap.java

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 * $Id: TipLoader.java 542 2005-10-10 18:03:15Z rbair $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/tips/TipLoader.java

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/*

* \$Id: TrackRenderer.java 3100 2008-10-14 22:33:10Z rah003 \$

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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/multislider/TrackRenderer.java

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/*

* \$Id: SimpleLoginService.java 3475 2009-08-28 08:30:47Z kleopatra \$

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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/auth/SimpleLoginService.java
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/*
* \$Id: LoginEvent.java 648 2005-11-30 05:21:56Z rbair \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/auth/LoginEvent.java
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/*
* \$Id: package-info.java 3165 2009-01-02 13:26:07Z rah003 \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/event/package-info.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/multisplitpane/package-info.java
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/icon/package-info.java
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/*
* \$Id: ErrorListener.java 2979 2008-07-08 01:32:06Z kschaefe \$
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/error/ErrorListener.java
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* \$Id: TreeCellContext.java 3424 2009-07-30 10:53:39Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/TreeCellContext.java
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```

```

/*
* $Id: AbstractAreaEffect.java 4082 2011-11-15 18:39:43Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/effects/AbstractAreaEffect.java
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```

```

/*
* $Id: ActionManager.java 3972 2011-03-17 20:31:58Z kschaefe $
*

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/action/ActionManager.java
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```
/*
 * $Id: ColorTintFilter.java 4082 2011-11-15 18:39:43Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/image/ColorTintFilter.java
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* \$Id: JXTitledSeparator.java 4147 2012-02-01 17:13:24Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXTitledSeparator.java
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/*
* \$Id: package-info.java 3100 2008-10-14 22:33:10Z rah003 \$
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/autocomplete/workarounds/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/image/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/beans/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/macosex/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/color/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/misc/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/calendar/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/graphics/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/auth/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/multislider/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/windows/package-info.java
- *
- /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/combobox/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/nimbus/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/metal/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/error/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/tree/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/border/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/effects/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/package-info.java
- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/geom/package-info.java

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 * $Id: JXTaskPane.java 4260 2012-11-14 20:59:08Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXTaskPane.java
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/*
 * $Id: PatternPredicate.java 3927 2011-02-22 16:34:11Z kleopatra $
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 * $Id: ComponentAdapter.java 4158 2012-02-03 18:29:40Z kschaefe $
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 * \$Id: Utilities.java 4084 2011-11-15 18:53:49Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/util/Utilities.java
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* $Id: CalendarAdapter.java 3877 2010-11-03 11:36:33Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/CalendarAdapter.java

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* $Id: SwingXUtilities.java 4262 2012-11-19 18:40:10Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/SwingXUtilities.java

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* \$Id: AbstractAreaPainter.java 4082 2011-11-15 18:39:43Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/graphics/ColorUtilities.java

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/*

* \$Id: TitledPanelUI.java 997 2006-04-11 20:51:31Z rbair \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/TitledPanelUI.java

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/*

* \$Id: FontHighlighter.java 1164 2009-11-03 04:22:00Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/FontHighlighter.java

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/*

* \$Id: PainterUIResource.java 4046 2011-07-19 18:45:40Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/PainterUIResource.java

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/*

* \$Id: Searchable.java 2948 2008-06-16 15:02:14Z kleopatra \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/search/Searchable.java
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* \$Id: ShapeUIResource.java 4028 2011-06-03 19:32:19Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/ShapeUIResource.java
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* \$Id: ErrorPaneUI.java 3105 2008-10-16 21:09:43Z rah003 \$
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 * \$Id: AbstractSerializableBean.java 4088 2011-11-17 19:53:49Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/beans/AbstractSerializableBean.java
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 * \$Id: PatternModel.java 3472 2009-08-27 13:12:42Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/search/PatternModel.java
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```

/*
* $Id: JXLabel.java 4225 2012-08-07 15:37:57Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXLabel.java
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/*
* $Id: ServerAction.java 3972 2011-03-17 20:31:58Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/action/ServerAction.java
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/*
 * $Id: ThumbListener.java 3100 2008-10-14 22:33:10Z rah003 $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/multislider/ThumbListener.java
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```
/*
```

```

* $Id: VerticalLayout.java 4147 2012-02-01 17:13:24Z kschaefe $
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```
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/VerticalLayout.java
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/*
* $Id: StackLayout.java 3793 2010-09-28 05:15:02Z kschaefe $
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```
* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/StackLayout.java
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/*
 * $Id: TableColumnModelExtListener.java 1395 2006-09-14 14:40:12Z kleopatra $
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*/swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/event/TableColumnModelExtListener.java
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/*
 * $Id: JXRendererHyperlink.java 3235 2009-02-01 15:01:07Z rah003 $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/JXRendererHyperlink.java

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* \$Id: JXApplet.java 4175 2012-05-30 16:57:33Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXApplet.java

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/*

* \$Id: ColumnFactory.java 3554 2009-11-06 09:07:55Z kleopatra \$

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/*
 * $Id: TargetManager.java 3972 2011-03-17 20:31:58Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/action/TargetManager.java
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 * $Id: JXStatusBar.java 4147 2012-02-01 17:13:24Z kschaefe $
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 * $Id: MacOSXLookAndFeelAddons.java 4092 2011-11-30 18:04:36Z kschaefe $
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/windows/WindowsLookAndFeelAddons.java

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 * $Id: EditorPaneLinkVisitor.java 3927 2011-02-22 16:34:11Z kleopatra $
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/hyperlink/EditorPaneLinkVisitor.java

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 * $Id: DefaultTableRenderer.java 3927 2011-02-22 16:34:11Z kleopatra $
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/*
 * \$Id: LoginAdapter.java 603 2005-11-11 23:05:18Z rbair \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/auth/LoginAdapter.java
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* $Id: DefaultTableColumnModelExt.java 3975 2011-03-28 14:05:29Z kleopatra $
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```

Found in path(s):

```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/table/DefaultTableColumnModelExt.java
No license file was found, but licenses were detected in source scan.

```

```

/*
* $Id: Star2D.java 3863 2010-10-26 02:53:32Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/geom/Star2D.java
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* \$Id: MappedValues.java 3882 2010-11-05 09:24:37Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/MappedValues.java
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/*
* \$Id: DatePickerUI.java 3100 2008-10-14 22:33:10Z rah003 \$
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/DatePickerUI.java

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```
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 * $Id: PasswordStore.java 3343 2009-05-25 00:33:12Z kschaefe $
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/auth/PasswordStore.java

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```
/*
 * $Id: CompoundPainter.java 4156 2012-02-02 19:54:38Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/CompoundPainter.java
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 * \$Id: DatePickerCellEditor.java 3927 2011-02-22 16:34:11Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/table/DatePickerCellEditor.java
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/*
 * $Id: TableColumnExt.java 3927 2011-02-22 16:34:11Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/table/TableColumnExt.java

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```

/*
 * $Id: ListSearchable.java 3166 2009-01-02 13:27:18Z rah003 $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/search/ListSearchable.java

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/*

* \$Id: DefaultTip.java 3927 2011-02-22 16:34:11Z kleopatra \$

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* \$Id: MotifLookAndFeelAddons.java 4092 2011-11-30 18:04:36Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/motif/MotifLookAndFeelAddons.java
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/*

* \$Id: ThumbDataEvent.java 3475 2009-08-28 08:30:47Z kleopatra \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/multislider/ThumbDataEvent.java
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/*

* \$Id: BasicLoginPaneUI.java 4082 2011-11-15 18:39:43Z kschaefe \$

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* \$Id: ListRolloverController.java 3707 2010-07-08 19:19:25Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/rollover/ListRolloverController.java
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* \$Id: Painter.java 3860 2010-10-26 01:14:53Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/Painter.java
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/*
 * \$Id: BasicHeaderUI.java 3927 2011-02-22 16:34:11Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/BasicHeaderUI.java
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 * \$Id: SearchPredicate.java 3927 2011-02-22 16:34:11Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/SearchPredicate.java
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```

/*
* $Id: AbstractMultiThumbModel.java 3259 2009-02-17 21:06:19Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/multislider/AbstractMultiThumbModel.java
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```

/*
* $Id: WrappingIconPanel.java 4252 2012-11-13 18:37:17Z kschaefe $
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 * \$Id: RepaintManagerX.java 4249 2012-11-13 18:12:49Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/RepaintManagerX.java

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`/swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/search/AbstractSearchable.java`

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 * $Id: PaintUtils.java 4193 2012-06-27 19:42:05Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/util/PaintUtils.java

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* \$Id: HighlightPredicate.java 3935 2011-03-02 19:06:41Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/HighlightPredicate.java

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* \$Id: UIManagerExt.java 4028 2011-06-03 19:32:19Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/calendar/SingleDaySelectionModel.java
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```
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Found in path(s):

- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/MultiThumbSliderUI.java

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```
/*
 * $Id: BoundAction.java 3972 2011-03-17 20:31:58Z kschaefe $
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Found in path(s):

- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/action/BoundAction.java

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```
/*
 * $Id: HorizontalLayout.java 4147 2012-02-01 17:13:24Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/HorizontalLayout.java
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```
/*
 * $Id: DateSelectionEvent.java 3272 2009-02-25 11:06:37Z kleopatra $
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/event/DateSelectionEvent.java
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```
/*
 * $Id: ThumbRenderer.java 3100 2008-10-14 22:33:10Z rah003 $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/multislider/ThumbRenderer.java

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* \$Id: BlendComposite.java 4011 2011-05-05 16:19:34Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/graphics/BlendComposite.java

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* \$Id: ActionContainerFactory.java 3980 2011-03-28 20:24:46Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/action/ActionContainerFactory.java

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* \$Id: JXCollapseablePane.java 4265 2012-11-28 18:15:57Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXCollapsiblePane.java

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/*
* $Id: BasicBusyLabelUI.java 3927 2011-02-22 16:34:11Z kleopatra $
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```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/BasicBusyLabelUI.java

```

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/*
* $Id: AutoCompleteComboBoxEditor.java 4045 2011-07-19 18:39:17Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/autocomplete/AutoCompleteComboBoxEditor.java
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/*
 * $Id: CompositeAction.java 3972 2011-03-17 20:31:58Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/action/CompositeAction.java
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/*
 * $Id: TaskPaneUI.java 2365 2007-11-01 13:38:15Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/TaskPaneUI.java
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```

/*
* $Id: ListCellContext.java 3424 2009-07-30 10:53:39Z kleopatra $
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```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/ListCellContext.java

```

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```
/*
 * $Id: AbstractAutoCompleteAdaptor.java 4045 2011-07-19 18:39:17Z kschaefe $
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```
*/swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/autocomplete/AbstractAutoCompleteAdaptor.java
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/*
 * $Id: ListRolloverProducer.java 3296 2009-03-11 12:06:01Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/rollover/ListRolloverProducer.java

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* \$Id: JRendererLabel.java 4222 2012-08-07 10:23:08Z kleopatra \$

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* \$Id: IconHighlighter.java 4192 2012-06-27 19:20:56Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/IconHighlighter.java

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* \$Id: ListComboBoxModel.java 3935 2011-03-02 19:06:41Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/StringValue.java
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 * $Id: Morphing2D.java 3863 2010-10-26 02:53:32Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/geom/Morphing2D.java

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/*

* \$Id: ShadingColorHighlighter.java 3100 2008-10-14 22:33:10Z rah003 \$

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```

Found in path(s):

```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/border/IconBorder.java

```

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```

/*
* $Id: DefaultsList.java 4047 2011-07-19 18:51:12Z kschaefe $
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```

Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/DefaultsList.java

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/*

* \$Id: JXImageView.java 4248 2012-11-13 18:12:08Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXImageView.java

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/*

* \$Id: AbstractActionExt.java 4158 2012-02-03 18:29:40Z kschaefe \$

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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/action/AbstractActionExt.java

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/*

* \$Id: NeonBorderEffect.java 3829 2010-10-07 02:01:20Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/effects/NeonBorderEffect.java

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* \$Id: JXTaskPaneContainer.java 4226 2012-08-07 16:09:19Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXTaskPaneContainer.java
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/*
* \$Id: Highlighter.java 3100 2008-10-14 22:33:10Z rah003 \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/Highlighter.java
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* \$Id: ForwardingRepaintManager.java 3690 2010-05-03 17:55:44Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/ForwardingRepaintManager.java
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* \$Id: MacOSXStatusBarUI.java 3475 2009-08-28 08:30:47Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/macosex/MacOSXStatusBarUI.java
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/*
* \$Id: DaySelectionModel.java 3927 2011-02-22 16:34:11Z kleopatra \$
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Found in path(s):

- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/calendar/DaySelectionModel.java

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```
/*
 * $Id: ColumnControlButtonAddon.java 3100 2008-10-14 22:33:10Z rah003 $
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/ColumnControlButtonAddon.java

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*/
/*
* @(#)DragRecognitionSupport.java
* 1.2 05/11/17
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/core/DragRecognitionSupport.java
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```

/*
* $Id: TextPainter.java 4147 2012-02-01 17:13:24Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/TextPainter.java

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/*

* \$Id: StatusBarUI.java 3246 2009-02-04 15:43:14Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/StatusBarUI.java

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/*

* \$Id: WindowsTipOfTheDayUI.java 3927 2011-02-22 16:34:11Z kleopatra \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/windows/WindowsTipOfTheDayUI.java
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```
/*
 * $Id: RectanglePainter.java 4147 2012-02-01 17:13:24Z kschaefe $
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/RectanglePainter.java
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```
/*
 * $Id: DateUtils.java 3100 2008-10-14 22:33:10Z rah003 $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/calendar/DateUtils.java

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/*

* \$Id: JXPanel.java 4264 2012-11-27 19:44:18Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXPanel.java

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/*

* \$Id: AutoCompleteDocument.java 4051 2011-07-19 20:17:05Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/autocomplete/AutoCompleteDocument.java
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```

/*
* $Id: DefaultTreeRenderer.java 3927 2011-02-22 16:34:11Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/DefaultTreeRenderer.java
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```

/*
* $Id: ErrorLevel.java 1557 2006-11-10 17:02:53Z rbair $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/error/ErrorLevel.java
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```

/*
* $Id: TableRolloverProducer.java 3296 2009-03-11 12:06:01Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/rollover/TableRolloverProducer.java
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```

/*
* $Id: JXTree.java 4166 2012-02-15 15:21:04Z kleopatra $

```

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXTree.java
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```

/*
* $Id: TaskPaneContainerUI.java 2363 2007-10-31 13:24:06Z kschaefe $
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Found in path(s):

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/TaskPaneContainerUI.java

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`/swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/graphics/ReflectionRenderer.java`

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```
/*
 * $Id: BasicErrorPaneUI.java 3927 2011-02-22 16:34:11Z kleopatra $
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```

Found in path(s):

```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/BasicErrorPaneUI.java
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```

```

/*
* $Id: ErrorEvent.java 2979 2008-07-08 01:32:06Z kschaefe $
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```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/error/ErrorEvent.java
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```

/*
* $Id: WindowUtils.java 4084 2011-11-15 18:53:49Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/util/WindowUtils.java

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 * \$Id: TableSearchable.java 3194 2009-01-21 11:39:19Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/search/TableSearchable.java

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/*

```

* $Id: MonthViewUI.java 3100 2008-10-14 22:33:10Z rah003 $
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```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/MonthViewUI.java
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```

```

/*
* $Id: GradientThumbRenderer.java 4082 2011-11-15 18:39:43Z kschaefe $
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```

Found in path(s):

```

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/color/GradientThumbRenderer.java

```

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```
/*
 * $Id: StatusBarAddon.java 3475 2009-08-28 08:30:47Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/StatusBarAddon.java

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```
/*
 * $Id: MetalLookAndFeelAddons.java 4092 2011-11-30 18:04:36Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/metal/MetalLookAndFeelAddons.java

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/*

* \$Id: ShadowPathEffect.java 1837 2007-03-15 22:44:22Z joshy \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/effects/ShadowPathEffect.java

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/*

* \$Id: BusyLabelUI.java 3964 2011-03-17 19:12:29Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/BusyLabelUI.java
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* \$Id: JXGradientChooser.java 4147 2012-02-01 17:13:24Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXGradientChooser.java
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* \$Id: BasicLookAndFeelAddons.java 4034 2011-07-19 17:18:03Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/BasicLookAndFeelAddons.java
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 * \$Id: BasicCalendarHeaderHandler.java 3927 2011-02-22 16:34:11Z kleopatra \$
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 * \$Id: TaskPaneAddon.java 3622 2010-02-25 04:34:55Z kschaefe \$
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 * $Id: TreeTableModel.java 2476 2007-11-25 15:52:59Z kschaefe $
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/*
 * $Id: TranslucentRepaintManager.java 2476 2007-11-25 15:52:59Z kschaefe $
```

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/TranslucentRepaintManager.java
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* $Id: DefaultDateSelectionModel.java 3927 2011-02-22 16:34:11Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/calendar/DefaultDateSelectionModel.java

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 * $Id: LoginListener.java 3707 2010-07-08 19:19:25Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/auth/LoginListener.java

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 * $Id: BasicTipOfTheDayUI.java 3927 2011-02-22 16:34:11Z kleopatra $
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* \$Id: DefaultXTreeCellEditor.java 3927 2011-02-22 16:34:11Z kleopatra \$

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* \$Id: NumberEditorExt.java 3927 2011-02-22 16:34:11Z kleopatra \$

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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/UIColorHighlighterAddon.java

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```
/*
 * $Id: JXComboBox.java 4158 2012-02-03 18:29:40Z kschaefe $
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Found in path(s):

- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXComboBox.java

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```
/*
 * $Id: CheckerboardPainter.java 4147 2012-02-01 17:13:24Z kschaefe $
 *
```

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/CheckerboardPainter.java
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/*
 * \$Id: GradientPreviewPanel.java 4082 2011-11-15 18:39:43Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/color/GradientPreviewPanel.java

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```
/*
 * $Id: ObjectToStringConverter.java 4045 2011-07-19 18:39:17Z kschaefe $
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```

Found in path(s):

`/swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/autocomplete/ObjectToStringConverter.java`

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```
/*
 * $Id: GlossPainter.java 4147 2012-02-01 17:13:24Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/GlossPainter.java

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/*

* \$Id: DefaultVisuals.java 3778 2010-09-07 10:10:49Z kleopatra \$

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/*

* \$Id: MultiThumbModel.java 3259 2009-02-17 21:06:19Z kschaefe \$

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* \$Id: JXFindPanel.java 4158 2012-02-03 18:29:40Z kschaefe \$
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 * $Id: JXTable.java 4266 2012-12-05 16:34:37Z kleopatra $
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 * $Id: JXSearchPanel.java 4158 2012-02-03 18:29:40Z kschaefe $
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 * $Id: GraphicsUtilities.java 4193 2012-06-27 19:42:05Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/util/GraphicsUtilities.java

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/JXFrame.java

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* \$Id: JXButton.java 4257 2012-11-14 17:08:20Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/ShapePainter.java
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* \$Id: ColumnControlPopup.java 4065 2011-08-19 13:28:26Z kleopatra \$
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 * $Id: TreeRolloverProducer.java 4190 2012-06-27 19:01:06Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/rollover/TreeRolloverProducer.java
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 * $Id: JXMultiThumbSlider.java 4147 2012-02-01 17:13:24Z kschaefe $
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 * \$Id: WindowsClassicStatusBarUI.java 3472 2009-08-27 13:12:42Z kleopatra \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/windows/WindowsClassicStatusBarUI.java

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*/swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/action/ToggleActionPropertyChangeListener.java
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* \$Id: JRendererCheckBox.java 4229 2012-08-08 15:27:09Z kleopatra \$

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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/JRendererCheckBox.java

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/*

* \$Id: TextComponentAdaptor.java 4045 2011-07-19 18:39:17Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/autocomplete/TextComponentAdaptor.java

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/*

* \$Id: package-info.java 3933 2011-03-02 19:02:29Z kschaefe \$

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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/package-info.java
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/*
* \$Id: AutoCompleteStyledDocument.java 4045 2011-07-19 18:39:17Z kschaefe \$
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/autocomplete/AutoCompleteStyledDocument.java
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/*
* \$Id: RolloverProducer.java 3982 2011-03-30 12:27:31Z kleopatra \$
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Found in path(s):

- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/rollover/RolloverProducer.java

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```
/*
 * $Id: HeaderAddon.java 2474 2007-11-21 17:32:04Z kschaefe $
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```

Found in path(s):

- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/HeaderAddon.java

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```
/*
 * $Id: SortController.java 3498 2009-09-10 09:35:40Z kleopatra $
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/sort/SortController.java
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```
/*
 * $Id: ComponentAddOn.java 4028 2011-06-03 19:32:19Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/ComponentAddOn.java
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```
/*
 * $Id: AbstractBean.java 4088 2011-11-17 19:53:49Z kschaefe $
```

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 */
 /**
 * <p>
 * A convenience class from which to extend all non-visual AbstractBeans. It
 * manages the PropertyChange notification system, making it relatively trivial
 * to add support for property change events in getters/setters.
 * </p>
 *
 * <p>
 * A non-visual java bean is a Java class that conforms to the AbstractBean
 * patterns to allow visual manipulation of the bean's properties and event
 * handlers at design-time.
 * </p>
 *
 * <p>
 * Here is a simple example bean that contains one property, foo, and the proper
 * pattern for implementing property change notification:
 *
 * <pre><code>
 * public class ABean extends AbstractBean {
 * private String foo;
 *
 * public void setFoo(String newFoo) {
 * String old = getFoo();
 * this.foo = newFoo;
 * firePropertyChange("<quot;foo<quot;"; old, getFoo());
 * }
 *
 * public String getFoo() {
 * return foo;
 * }
 * }
 * </pre></code>

```

*   }
* }
* </code></pre>
*
* </p>
*
* <p>
* You will notice
* that "getFoo()" is used in the setFoo method rather than
* accessing "foo" directly for the gets. This is done intentionally so that if
* a subclass overrides getFoo() to return, for instance, a constant value the
* property change notification system will continue to work properly.
* </p>
*
* <p>
* The firePropertyChange method takes into account the old value and the new
* value. Only if the two differ will it fire a property change event. So you
* can be assured from the above code fragment that a property change event will
* only occur if old is indeed different from getFoo()
* </p>
*
* <p>
* <code>AbstractBean</code> also supports vetoable
* {@link PropertyChangeEvent} events. These events are similar to
* <code>PropertyChange</code> events, except a special exception can be used
* to veto changing the property. For example, perhaps the property is changing
* from "fred" to "red", but a listener deems that "red" is unacceptable. In
* this case, the listener
* can fire a veto exception and the property must
* remain "fred". For example:
*
* <pre><code>
* public class ABean extends AbstractBean {
*     private String foo;
*
*     public void setFoo(String newFoo) throws PropertyVetoException {
*         String old = getFoo();
*         this.foo = newFoo;
*         fireVetoableChange(&quot;foo&quot;, old, getFoo());
*     }
*     public String getFoo() {
*         return foo;
*     }
* }
*
* public class Tester {
*     public static void main(String... args) {
*         try {

```


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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/BasicDatePickerUI.java

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```
/*
 * $Id: CompoundHighlighter.java 3927 2011-02-22 16:34:11Z kleopatra $
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- * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/decorator/CompoundHighlighter.java

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/*
 * $Id: FormatStringValue.java 3927 2011-02-22 16:34:11Z kleopatra $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/FormatStringValue.java
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 * \$Id: CalendarRenderingHandler.java 3166 2009-01-02 13:27:18Z rah003 \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/basic/CalendarRenderingHandler.java
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/*
 * $Id: IconValues.java 3927 2011-02-22 16:34:11Z kleopatra $
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```

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/renderer/IconValues.java

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```

/*
 * $Id: WeakEventListenerList.java 3190 2009-01-20 17:47:52Z kschaefe $
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```


Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/event/WeakEventListenerList.java

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/*

* \$Id: LinuxLookAndFeelAddons.java 4092 2011-11-30 18:04:36Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/linux/LinuxLookAndFeelAddons.java

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/*

* \$Id: GlowPathEffect.java 1837 2007-03-15 22:44:22Z josh \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/painter/effects/GlowPathEffect.java

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/*

* \$Id: ThumbDataListener.java 957 2006-03-29 02:44:44Z rbair \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/multislider/ThumbDataListener.java

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/*

* \$Id: RolloverController.java 3967 2011-03-17 19:18:47Z kschaefe \$

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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/rollover/RolloverController.java
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* \$Id: DateSelectionModel.java 3100 2008-10-14 22:33:10Z rah003 \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/calendar/DateSelectionModel.java
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/*
* \$Id: BusyLabelAddon.java 2565 2008-01-03 19:08:32Z rah003 \$
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Found in path(s):

* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/BusyLabelAddon.java
 * /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/XListAddon.java
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 * \$Id: DefaultMutableTreeTableNode.java 3780 2010-09-09 16:17:41Z kschaefe \$
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/treetable/DefaultMutableTreeTableNode.java
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/*
 * \$Id: TaskPaneContainerAddon.java 3500 2009-09-10 10:28:24Z kleopatra \$
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 * $Id: UserNameStore.java 1387 2006-09-11 22:37:44Z rbair $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/auth/UserNameStore.java
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```
/*
 * $Id: MultiSplitLayout.java 4238 2012-08-28 17:56:36Z kschaefe $
 *
```

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```
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 * $Id: AbstractPatternPanel.java 3927 2011-02-22 16:34:11Z kleopatra $
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```
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 * $Id: JXErrorPane.java 4158 2012-02-03 18:29:40Z kschaefe $
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```
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 * $Id: AbstractComponentAddon.java 4047 2011-07-19 18:51:12Z kschaefe $
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* /swingx-all-1-6-5-sources-1-jar/org/jdesktop/swingx/plaf/AbstractComponentAddon.java

1.37 openssl 3.1.1

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Version 2, June 1991

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[This is the first released version of the library GPL. It is numbered 2 because it goes with version 2 of the ordinary GPL.]

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1.40 libxml2 2.11.4

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1.41 zlib 1.2.13

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1.42 xz 5.4.4

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1.44 file 5.40

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1.45 util-linux 2.16.840

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```
NR START  END SECTORS SIZE NAME UUID
1  32 7679   7648 3.7M   8f8378c0-01
2 7680 16383   8704 4.3M   8f8378c0-02
5 7936 12799   4864 2.4M
6 12544 16127   3584 1.8M
```

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```
#!/usr/bin/env bash
# MIT licenses will each have a unique MD5 sum since they contain a unique copyright.
# This script will read the license file into memory, strip out the copyright, and then
# generate an MD5 that is not unique and can be matched against a known MIT MD5 sum.
set -e

calculate_md5_sum() {
    local FILE="$1"

    # Read the contents of the file into a variable
    local raw_license_text=$(<"$FILE")

    # Convert to lowercase
    local lowercase_license_text="${raw_license_text,,}"

    # Remove anything before the beginning of the license
    local stripped_license_text=$(awk '/permission is hereby granted,/{p=1} p' <<< "$lowercase_license_text")

    # Replace line breaks (Windows or Linux) with a single space
    local replaced_linebreaks=$(tr "r\n" ' ' <<< "$stripped_license_text")

    # Replace multiple spaces with a single space
```

```

local normalized_license_text=$(tr -s ' ' <<< "$replaced_linebreaks")

# Strip away any non-printable, non-whitespace characters
local clean_unprintable_license_text=$(tr
-cd '[:print:][:space:]' <<< "$normalized_license_text")

# Remove punctuation and special characters
local clean_license_text=$(echo "$clean_unprintable_license_text" | sed 's/[^a-zA-Z ]//g')

# Calculate the MD5 sum of the cleaned license text
local MD5SUM=$(echo -n "$clean_license_text" | md5sum | awk '{print $1}')

# Output the MD5 sum
echo "$MD5SUM"
}

# Check if the FILE argument is provided
if [ -z "$1" ]; then
    echo "Please provide a FILE as an argument."
    exit 1
fi

# Invoke the function with the provided FILE argument
calculate_md5_sum "$1"
WEV @@ WEV[B "1
x ?"U@,5 @mISmIN<GimCN7g1u|E
43mI,5WEV @@ WEV @mImImIAmImImI0mImImI*mImI
A0mImImI...
lost+found...

;9GimCN7g

!"#$%&'()*+,-
./0123456789;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~

!"#$%&'()*+,-
./0123456789;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~

!"#$%&'()*+,-
./0123456789;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~

!"#$%&'()*+,-
./0123456789;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz{|}~WEV @@
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1.46 d-bus 1.12.24

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 * Version 1.1 1 Aug 2013 Mark Adler
 */
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at revision 3a0bb77429bd3a61596f5e8a3172445844342120

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%% winjs version 4.4.0 (<https://github.com/winjs/winjs>)

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```

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```
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```

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<signature of Ty Coon>, 1 April 1989
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1.61 sqlite 3.45.1

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```
/*
** CAPI3REF: Configuration Options
** KEYWORDS: {configuration option}
**
** These constants are the available integer configuration options that
** can be passed as the first argument to the [sqlite3_config()] interface.
**
** Most of the configuration options for sqlite3_config()
** will only work if invoked prior to [sqlite3_initialize()] or after
** [sqlite3_shutdown()]. The few exceptions to this rule are called
** "anytime configuration options".
** ^Calling [sqlite3_config()] with a first argument that is not an
** anytime configuration option in between calls to [sqlite3_initialize()] and
** [sqlite3_shutdown()] is a no-op that returns SQLITE_MISUSE.
**
** The set of anytime configuration options can change (by insertions
** and/or deletions) from one release of SQLite to the next.
** As of SQLite version 3.42.0, the complete set of anytime configuration
```

** options is:

- **
- ** SQLITE_CONFIG_LOG
- **
- ** SQLITE_CONFIG_PCACHE_HDRSZ
- **
- **

** New configuration options may be added in future releases of SQLite.

** Existing configuration options might be discontinued. Applications

** should check the return code from [sqlite3_config()] to make sure that

** the call worked. The [sqlite3_config()] interface will return a

** non-zero [error code] if a discontinued or unsupported configuration option

** is invoked.

**

** <dl>

** [[SQLITE_CONFIG_SINGLETHREAD]] <dt>SQLITE_CONFIG_SINGLETHREAD</dt>

** <dd>There are no arguments to this option. ^This option sets the

** [threading mode] to Single-thread. In other words, it disables

** all mutexing and puts SQLite into a mode where it can only be used

** by a single thread. ^If SQLite is compiled with

** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then

** it is not possible to change the [threading mode] from its default

** value of Single-thread and so [sqlite3_config()] will return

** [SQLITE_ERROR] if called

with the SQLITE_CONFIG_SINGLETHREAD

** configuration option.</dd>

**

** [[SQLITE_CONFIG_MULTITHREAD]] <dt>SQLITE_CONFIG_MULTITHREAD</dt>

** <dd>There are no arguments to this option. ^This option sets the

** [threading mode] to Multi-thread. In other words, it disables

** mutexing on [database connection] and [prepared statement] objects.

** The application is responsible for serializing access to

** [database connections] and [prepared statements]. But other mutexes

** are enabled so that SQLite will be safe to use in a multi-threaded

** environment as long as no two threads attempt to use the same

** [database connection] at the same time. ^If SQLite is compiled with

** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then

** it is not possible to set the Multi-thread [threading mode] and

** [sqlite3_config()] will return [SQLITE_ERROR] if called with the

** SQLITE_CONFIG_MULTITHREAD configuration option.</dd>

**

** [[SQLITE_CONFIG_SERIALIZED]] <dt>SQLITE_CONFIG_SERIALIZED</dt>

**

<dd>There are no arguments to this option. ^This option sets the

** [threading mode] to Serialized. In other words, this option enables

** all mutexes including the recursive

** mutexes on [database connection] and [prepared statement] objects.

** In this mode (which is the default when SQLite is compiled with

** [SQLITE_THREADSafe=1]) the SQLite library will itself serialize access
 ** to [database connections] and [prepared statements] so that the
 ** application is free to use the same [database connection] or the
 ** same [prepared statement] in different threads at the same time.
 ** ^If SQLite is compiled with
 ** the [SQLITE_THREADSafe | SQLITE_THREADSafe=0] compile-time option then
 ** it is not possible to set the Serialized [threading mode] and
 ** [sqlite3_config()] will return [SQLITE_ERROR] if called with the
 ** SQLITE_CONFIG_SERIALIZED configuration option.</dd>
 **
 ** [[SQLITE_CONFIG_MALLOC]] <dt>SQLITE_CONFIG_MALLOC</dt>
 ** <dd> ^The SQLITE_CONFIG_MALLOC option
 takes a single argument which is
 ** a pointer to an instance of the [sqlite3_mem_methods] structure.
 ** The argument specifies
 ** alternative low-level memory allocation routines to be used in place of
 ** the memory allocation routines built into SQLite.)^ ^SQLite makes
 ** its own private copy of the content of the [sqlite3_mem_methods] structure
 ** before the [sqlite3_config()] call returns.</dd>
 **
 ** [[SQLITE_CONFIG_GETMALLOC]] <dt>SQLITE_CONFIG_GETMALLOC</dt>
 ** <dd> ^The SQLITE_CONFIG_GETMALLOC option takes a single argument which
 ** is a pointer to an instance of the [sqlite3_mem_methods] structure.
 ** The [sqlite3_mem_methods]
 ** structure is filled with the currently defined memory allocation routines.)^
 ** This option can be used to overload the default memory allocation
 ** routines with a wrapper that simulations memory allocation failure or
 ** tracks memory usage, for example. </dd>
 **
 ** [[SQLITE_CONFIG_SMALL_MALLOC]] <dt>SQLITE_CONFIG_SMALL_MALLOC</dt>
 ** <dd> ^The SQLITE_CONFIG_SMALL_MALLOC
 option takes single argument of
 ** type int, interpreted as a boolean, which if true provides a hint to
 ** SQLite that it should avoid large memory allocations if possible.
 ** SQLite will run faster if it is free to make large memory allocations,
 ** but some application might prefer to run slower in exchange for
 ** guarantees about memory fragmentation that are possible if large
 ** allocations are avoided. This hint is normally off.
 ** </dd>
 **
 ** [[SQLITE_CONFIG_MEMSTATUS]] <dt>SQLITE_CONFIG_MEMSTATUS</dt>
 ** <dd> ^The SQLITE_CONFIG_MEMSTATUS option takes single argument of type int,
 ** interpreted as a boolean, which enables or disables the collection of
 ** memory allocation statistics. ^When memory allocation statistics are
 ** disabled, the following SQLite interfaces become non-operational:
 **
 ** [sqlite3_hard_heap_limit64()]
 ** [sqlite3_memory_used()]

```

** <li> [sqlite3_memory_highwater()]
** <li> [sqlite3_soft_heap_limit64()]
**
    <li> [sqlite3_status64()]
** </ul>)^
** ^Memory allocation statistics are enabled by default unless SQLite is
** compiled with [SQLITE_DEFAULT_MEMSTATUS]=0 in which case memory
** allocation statistics are disabled by default.
** </dd>
**
** [[SQLITE_CONFIG_SCRATCH]] <dt>SQLITE_CONFIG_SCRATCH</dt>
** <dd> The SQLITE_CONFIG_SCRATCH option is no longer used.
** </dd>
**
** [[SQLITE_CONFIG_PAGECACHE]] <dt>SQLITE_CONFIG_PAGECACHE</dt>
** <dd> ^The SQLITE_CONFIG_PAGECACHE option specifies a memory pool
** that SQLite can use for the database page cache with the default page
** cache implementation.
** This configuration option is a no-op if an application-defined page
** cache implementation is loaded using the [SQLITE_CONFIG_PCACHE2].
** ^There are three arguments to SQLITE_CONFIG_PAGECACHE: A pointer to
** 8-byte aligned memory (pMem), the size of each page cache line (sz),
** and the number of cache lines (N).
** The sz argument should be the size of the largest database page
** (a power
    of two between 512 and 65536) plus some extra bytes for each
** page header. ^The number of extra bytes needed by the page header
** can be determined using [SQLITE_CONFIG_PCACHE_HDRSZ].
** ^It is harmless, apart from the wasted memory,
** for the sz parameter to be larger than necessary. The pMem
** argument must be either a NULL pointer or a pointer to an 8-byte
** aligned block of memory of at least sz*N bytes, otherwise
** subsequent behavior is undefined.
** ^When pMem is not NULL, SQLite will strive to use the memory provided
** to satisfy page cache needs, falling back to [sqlite3_malloc()] if
** a page cache line is larger than sz bytes or if all of the pMem buffer
** is exhausted.
** ^If pMem is NULL and N is non-zero, then each database connection
** does an initial bulk allocation for page cache memory
** from [sqlite3_malloc()] sufficient for N cache lines if N is positive or
** of -1024*N bytes if N is negative, . ^If additional
** page cache memory is needed beyond
    what is provided by the initial
** allocation, then SQLite goes to [sqlite3_malloc()] separately for each
** additional cache line. </dd>
**
** [[SQLITE_CONFIG_HEAP]] <dt>SQLITE_CONFIG_HEAP</dt>
** <dd> ^The SQLITE_CONFIG_HEAP option specifies a static memory buffer

```


** that SQLite will use for all of its dynamic memory allocation needs
 ** beyond those provided for by [SQLITE_CONFIG_PAGECACHE].
 ** ^The SQLITE_CONFIG_HEAP option is only available if SQLite is compiled
 ** with either [SQLITE_ENABLE_MEMSYS3] or [SQLITE_ENABLE_MEMSYS5] and returns
 ** [SQLITE_ERROR] if invoked otherwise.
 ** ^There are three arguments to SQLITE_CONFIG_HEAP:
 ** An 8-byte aligned pointer to the memory,
 ** the number of bytes in the memory buffer, and the minimum allocation size.
 ** ^If the first pointer (the memory pointer) is NULL, then SQLite reverts
 ** to using its default memory allocator (the system malloc() implementation),
 ** undoing any prior invocation of [SQLITE_CONFIG_MALLOC]. ^If the
 ** memory pointer
 is not NULL then the alternative memory
 ** allocator is engaged to handle all of SQLites memory allocation needs.
 ** The first pointer (the memory pointer) must be aligned to an 8-byte
 ** boundary or subsequent behavior of SQLite will be undefined.
 ** The minimum allocation size is capped at 2**12. Reasonable values
 ** for the minimum allocation size are 2**5 through 2**8.</dd>
 **
 ** [[SQLITE_CONFIG_MUTEX]] <dt>SQLITE_CONFIG_MUTEX</dt>
 ** <dd> ^The SQLITE_CONFIG_MUTEX option takes a single argument which is a
 ** pointer to an instance of the [sqlite3_mutex_methods] structure.
 ** The argument specifies alternative low-level mutex routines to be used
 ** in place the mutex routines built into SQLite.)^ ^SQLite makes a copy of
 ** the content of the [sqlite3_mutex_methods] structure before the call to
 ** [sqlite3_config()] returns. ^If SQLite is compiled with
 ** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
 ** the entire mutexing subsystem is omitted from the
 build and hence calls to
 ** [sqlite3_config()] with the SQLITE_CONFIG_MUTEX configuration option will
 ** return [SQLITE_ERROR].</dd>
 **
 ** [[SQLITE_CONFIG_GETMUTEX]] <dt>SQLITE_CONFIG_GETMUTEX</dt>
 ** <dd> ^The SQLITE_CONFIG_GETMUTEX option takes a single argument which
 ** is a pointer to an instance of the [sqlite3_mutex_methods] structure. The
 ** [sqlite3_mutex_methods]
 ** structure is filled with the currently defined mutex routines.)^
 ** This option can be used to overload the default mutex allocation
 ** routines with a wrapper used to track mutex usage for performance
 ** profiling or testing, for example. ^If SQLite is compiled with
 ** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
 ** the entire mutexing subsystem is omitted from the build and hence calls to
 ** [sqlite3_config()] with the SQLITE_CONFIG_GETMUTEX configuration option will
 ** return [SQLITE_ERROR].</dd>
 **
 ** [[SQLITE_CONFIG_LOOKASIDE]] <dt>SQLITE_CONFIG_LOOKASIDE</dt>
 ** <dd> ^The SQLITE_CONFIG_LOOKASIDE

option takes two arguments that determine

- ** the default size of lookaside memory on each [database connection].
- ** The first argument is the
- ** size of each lookaside buffer slot and the second is the number of
- ** slots allocated to each database connection.)^ ^(SQLITE_CONFIG_LOOKASIDE
- ** sets the <i>default</i> lookaside size. The [SQLITE_DBCONFIG_LOOKASIDE]
- ** option to [sqlite3_db_config()] can be used to change the lookaside
- ** configuration on individual connections.)^ </dd>
- **
- ** [[SQLITE_CONFIG_PCACHE2]] <dt>SQLITE_CONFIG_PCACHE2</dt>
- ** <dd> ^(The SQLITE_CONFIG_PCACHE2 option takes a single argument which is
- ** a pointer to an [sqlite3_pcache_methods2] object. This object specifies
- ** the interface to a custom page cache implementation.)^
- ** ^SQLite makes a copy of the [sqlite3_pcache_methods2] object.</dd>
- **
- ** [[SQLITE_CONFIG_GETPCACHE2]] <dt>SQLITE_CONFIG_GETPCACHE2</dt>
- ** <dd> ^(The SQLITE_CONFIG_GETPCACHE2 option takes a single argument which
- ** is
- ** a pointer to an [sqlite3_pcache_methods2] object. SQLite copies of
- ** the current page cache implementation into that object.)^ </dd>
- **
- ** [[SQLITE_CONFIG_LOG]] <dt>SQLITE_CONFIG_LOG</dt>
- ** <dd> The SQLITE_CONFIG_LOG option is used to configure the SQLite
- ** global [error log].
- ** (^The SQLITE_CONFIG_LOG option takes two arguments: a pointer to a
- ** function with a call signature of void (*)(void*,int,const char*),
- ** and a pointer to void. ^If the function pointer is not NULL, it is
- ** invoked by [sqlite3_log()] to process each logging event. ^If the
- ** function pointer is NULL, the [sqlite3_log()] interface becomes a no-op.
- ** ^The void pointer that is the second argument to SQLITE_CONFIG_LOG is
- ** passed through as the first parameter to the application-defined logger
- ** function whenever that function is invoked. ^The second parameter to
- ** the logger function is a copy of the first parameter to the corresponding
- ** [sqlite3_log()] call and is intended to be a [result code] or
- ** an
- ** [extended result code]. ^The third parameter passed to the logger is
- ** log message after formatting via [sqlite3_snprintf()].
- ** The SQLite logging interface is not reentrant; the logger function
- ** supplied by the application must not invoke any SQLite interface.
- ** In a multi-threaded application, the application-defined logger
- ** function must be threadsafe. </dd>
- **
- ** [[SQLITE_CONFIG_URI]] <dt>SQLITE_CONFIG_URI
- ** <dd>^(The SQLITE_CONFIG_URI option takes a single argument of type int.
- ** If non-zero, then URI handling is globally enabled. If the parameter is zero,
- ** then URI handling is globally disabled.)^ ^If URI handling is globally
- ** enabled, all filenames passed to [sqlite3_open()], [sqlite3_open_v2()],
- ** [sqlite3_open16()] or

** specified as part of [ATTACH] commands are interpreted as URIs, regardless
 ** of whether or not the [SQLITE_OPEN_URI] flag is set when the database
 ** connection is opened. ^If it is globally disabled, filenames are
 ** only interpreted as
 URIs if the SQLITE_OPEN_URI flag is set when the
 ** database connection is opened. ^By default, URI handling is globally
 ** disabled. The default value may be changed by compiling with the
 ** [SQLITE_USE_URI] symbol defined.)^
 **
 ** [[SQLITE_CONFIG_COVERING_INDEX_SCAN]] <dt>SQLITE_CONFIG_COVERING_INDEX_SCAN
 ** <dd>^The SQLITE_CONFIG_COVERING_INDEX_SCAN option takes a single integer
 ** argument which is interpreted as a boolean in order to enable or disable
 ** the use of covering indices for full table scans in the query optimizer.
 ** ^The default setting is determined
 ** by the [SQLITE_ALLOW_COVERING_INDEX_SCAN] compile-time option, or is "on"
 ** if that compile-time option is omitted.
 ** The ability to disable the use of covering indices for full table scans
 ** is because some incorrectly coded legacy applications might malfunction
 ** when the optimization is enabled. Providing the ability to
 ** disable the optimization allows the older, buggy application code to work
 ** without change
 even with newer versions of SQLite.
 **
 ** [[SQLITE_CONFIG_PCACHE]] [[SQLITE_CONFIG_GETPCACHE]]
 ** <dt>SQLITE_CONFIG_PCACHE and SQLITE_CONFIG_GETPCACHE
 ** <dd> These options are obsolete and should not be used by new code.
 ** They are retained for backwards compatibility but are now no-ops.
 ** </dd>
 **
 ** [[SQLITE_CONFIG_SQLLOG]]
 ** <dt>SQLITE_CONFIG_SQLLOG
 ** <dd>This option is only available if sqlite is compiled with the
 ** [SQLITE_ENABLE_SQLLOG] pre-processor macro defined. The first argument should
 ** be a pointer to a function of type void(*)(void*,sqlite3*,const char*, int).
 ** The second should be of type (void*). The callback is invoked by the library
 ** in three separate circumstances, identified by the value passed as the
 ** fourth parameter. If the fourth parameter is 0, then the database connection
 ** passed as the second argument has just been opened. The third argument
 ** points to a buffer containing the name of the main database file. If the
 ** fourth parameter is 1,
 then the SQL statement that the third parameter
 ** points to has just been executed. Or, if the fourth parameter is 2, then
 ** the connection being passed as the second parameter is being closed. The
 ** third parameter is passed NULL In this case. An example of using this
 ** configuration option can be seen in the "test_sqllog.c" source file in
 ** the canonical SQLite source tree.</dd>
 **
 ** [[SQLITE_CONFIG_MMAP_SIZE]]

**** <dt>SQLITE_CONFIG_MMAP_SIZE**
**** <dd>^SQLITE_CONFIG_MMAP_SIZE takes two 64-bit integer (sqlite3_int64) values**
**** that are the default mmap size limit (the default setting for**
**** [PRAGMA mmap_size]) and the maximum allowed mmap size limit.**
**** ^The default setting can be overridden by each database connection using**
**** either the [PRAGMA mmap_size] command, or by using the**
**** [SQLITE_FCNTL_MMAP_SIZE] file control. ^The maximum allowed mmap size**
**** will be silently truncated if necessary so that it does not exceed the**
**** compile-time maximum mmap size set by the**
**** [SQLITE_MAX_MMAP_SIZE]**
compile-time option.)^
**** ^If either argument to this option is negative, then that argument is**
**** changed to its compile-time default.**

**** [[SQLITE_CONFIG_WIN32_HEAPSIZE]]**
**** <dt>SQLITE_CONFIG_WIN32_HEAPSIZE**
**** <dd>^The SQLITE_CONFIG_WIN32_HEAPSIZE option is only available if SQLite is**
**** compiled for Windows with the [SQLITE_WIN32_MALLOC] pre-processor macro**
**** defined. ^SQLITE_CONFIG_WIN32_HEAPSIZE takes a 32-bit unsigned integer value**
**** that specifies the maximum size of the created heap.**

**** [[SQLITE_CONFIG_PCACHE_HDRSZ]]**
**** <dt>SQLITE_CONFIG_PCACHE_HDRSZ**
**** <dd>^The SQLITE_CONFIG_PCACHE_HDRSZ option takes a single parameter which**
**** is a pointer to an integer and writes into that integer the number of extra**
**** bytes per page required for each page in [SQLITE_CONFIG_PAGECACHE].**
**** The amount of extra space required can change depending on the compiler,**
**** target platform, and SQLite version.**

**** [[SQLITE_CONFIG_PMASZ]]**
**** <dt>SQLITE_CONFIG_PMASZ**
**** <dd>^The**
SQLITE_CONFIG_PMASZ option takes a single parameter which
**** is an unsigned integer and sets the "Minimum PMA Size" for the multithreaded**
**** sorter to that integer. The default minimum PMA Size is set by the**
**** [SQLITE_SORTER_PMASZ] compile-time option. New threads are launched**
**** to help with sort operations when multithreaded sorting**
**** is enabled (using the [PRAGMA threads] command) and the amount of content**
**** to be sorted exceeds the page size times the minimum of the**
**** [PRAGMA cache_size] setting and this value.**

**** [[SQLITE_CONFIG_STMTJRNL_SPILL]]**
**** <dt>SQLITE_CONFIG_STMTJRNL_SPILL**
**** <dd>^The SQLITE_CONFIG_STMTJRNL_SPILL option takes a single parameter which**
**** becomes the [statement journal] spill-to-disk threshold.**
**** [Statement journals] are held in memory until their size (in bytes)**
**** exceeds this threshold, at which point they are written to disk.**
**** Or if the threshold is -1, statement journals are always held**

** exclusively in memory.
 ** Since many statement journals
 never become large, setting the spill
 ** threshold to a value such as 64KiB can greatly reduce the amount of
 ** I/O required to support statement rollback.
 ** The default value for this setting is controlled by the
 ** [SQLITE_STMTJRNL_SPILL] compile-time option.
 **
 ** [[SQLITE_CONFIG_SORTERREF_SIZE]]
 ** <dt>SQLITE_CONFIG_SORTERREF_SIZE
 ** <dd>The SQLITE_CONFIG_SORTERREF_SIZE option accepts a single parameter
 ** of type (int) - the new value of the sorter-reference size threshold.
 ** Usually, when SQLite uses an external sort to order records according
 ** to an ORDER BY clause, all fields required by the caller are present in the
 ** sorted records. However, if SQLite determines based on the declared type
 ** of a table column that its values are likely to be very large - larger
 ** than the configured sorter-reference size threshold - then a reference
 ** is stored in each sorted record and the required column values loaded
 ** from the database as records are returned in sorted order.
 The default
 ** value for this option is to never use this optimization. Specifying a
 ** negative value for this option restores the default behavior.
 ** This option is only available if SQLite is compiled with the
 ** [SQLITE_ENABLE_SORTER_REFERENCES] compile-time option.
 **
 ** [[SQLITE_CONFIG_MEMDB_MAXSIZE]]
 ** <dt>SQLITE_CONFIG_MEMDB_MAXSIZE
 ** <dd>The SQLITE_CONFIG_MEMDB_MAXSIZE option accepts a single parameter
 ** [sqlite3_int64] parameter which is the default maximum size for an in-memory
 ** database created using [sqlite3_deserialize()]. This default maximum
 ** size can be adjusted up or down for individual databases using the
 ** [SQLITE_FCNTL_SIZE_LIMIT] [sqlite3_file_control|file-control]. If this
 ** configuration setting is never used, then the default maximum is determined
 ** by the [SQLITE_MEMDB_DEFAULT_MAXSIZE] compile-time option. If that
 ** compile-time option is not set, then the default maximum is 1073741824.
 ** </dd>
 */
 /*
 ** The "printf" code that follows dates
 from the 1980's. It is in
 ** the public domain.
 **

 **
 ** This file contains code for a set of "printf"-like routines. These
 ** routines format strings much like the printf() from the standard C
 ** library, though the implementation here has enhancements to support
 ** SQLite.

```

*/
/*
** 2004 May 22
**
** The author disclaims copyright to this source code. In place of
** a legal notice, here is a blessing:
**
** May you do good and not evil.
** May you find forgiveness for yourself and forgive others.
** May you share freely, never taking more than you give.
**
*****
**
** This file contains the VFS implementation for unix-like operating systems
** include Linux, MacOSX, *BSD, QNX, VxWorks, AIX, HPUX, and others.
**
** There are actually several different VFS implementations in this file.
** The differences are in the way that file
locking is done. The default
** implementation uses Posix Advisory Locks. Alternative implementations
** use flock(), dot-files, various proprietary locking schemas, or simply
** skip locking all together.
**
** This source file is organized into divisions where the logic for various
** subfunctions is contained within the appropriate division. PLEASE
** KEEP THE STRUCTURE OF THIS FILE INTACT. New code should be placed
** in the correct division and should be clearly labelled.
**
** The layout of divisions is as follows:
**
** * General-purpose declarations and utility functions.
** * Unique file ID logic used by VxWorks.
** * Various locking primitive implementations (all except proxy locking):
**   + for Posix Advisory Locks
**   + for no-op locks
**   + for dot-file locks
**   + for flock() locking
**   + for named semaphore locks (VxWorks only)
**   + for AFP filesystem locks (MacOSX only)
** * sqlite3_file methods not associated with locking.
**
**   * Definitions of sqlite3_io_methods objects for all locking
**     methods plus "finder" functions for each locking method.
** * sqlite3_vfs method implementations.
** * Locking primitives for the proxy uber-locking-method. (MacOSX only)
** * Definitions of sqlite3_vfs objects for all locking methods
**   plus implementations of sqlite3_os_init() and sqlite3_os_end().
*/

```

```
/*
** Return a pointer to the "temporary page" buffer held internally
** by the pager. This is a buffer that is big enough to hold the
** entire content of a database page. This buffer is used internally
** during rollback and will be overwritten whenever a rollback
** occurs. But other modules are free to use it too, as long as
** no rollbacks are happening.
**/
```

Found in path(s):

* /sqlite-amalgamation-3450100-zip/sqlite-amalgamation-3450100/sqlite3.c

No license file was found, but licenses were detected in source scan.

```
/*
** 2022-11-18
**
** The author disclaims copyright to this source code. In place of
** a legal notice, here is a blessing:
**
** May you do good and not evil.
** May you find forgiveness for yourself and forgive others.
** May you share freely, never taking more than you give.
**
*****
**
** This is a SQLite extension for converting in either direction
** between a (binary) blob and base64 text. Base64 can transit a
** sane USASCII channel unmolested. It also plays nicely in CSV or
** written as TCL brace-enclosed literals or SQL string literals,
** and can be used unmodified in XML-like documents.
**
** This is an independent implementation of conversions specified in
** RFC 4648, done on the above date by the author (Larry Brasfield)
** who thereby has the right to put this into the public domain.
**
** The conversions meet RFC 4648 requirements,
** provided that this
** C source specifies that line-feeds are included in the encoded
** data to limit visible line lengths to 72 characters and to
** terminate any encoded blob having non-zero length.
**
** Length limitations are not imposed except that the runtime
** SQLite string or blob length limits are respected. Otherwise,
** any length binary sequence can be represented and recovered.
** Generated base64 sequences, with their line-feeds included,
** can be concatenated; the result converted back to binary will
** be the concatenation of the represented binary sequences.
**
```

```

** This SQLite3 extension creates a function, base64(x), which
** either: converts text x containing base64 to a returned blob;
** or converts a blob x to returned text containing base64. An
** error will be thrown for other input argument types.
**
** This code relies on UTF-8 encoding only with respect to the
** meaning of the first 128 (7-bit) codes matching that of USASCII.
** It will fail miserably
if somehow made to try to convert EBCDIC.
** Because it is table-driven, it could be enhanced to handle that,
** but the world and SQLite have moved on from that anachronism.
**
** To build the extension:
** Set shell variable SQDIR=<your favorite SQLite checkout directory>
** *Nix: gcc -O2 -shared -I$SQDIR -fPIC -o base64.so base64.c
** OSX: gcc -O2 -dynamiclib -fPIC -I$SQDIR -o base64.dylib base64.c
** Win32: gcc -O2 -shared -I$SQDIR% -o base64.dll base64.c
** Win32: cl /Os -I$SQDIR% base64.c -link -dll -out:base64.dll
*/
/*
** 2022-11-16
**
** The author disclaims copyright to this source code. In place of
** a legal notice, here is a blessing:
**
** May you do good and not evil.
** May you find forgiveness for yourself and forgive others.
** May you share freely, never taking more than you give.
**
*****
**
** This is a utility for converting binary to base85 or vice-versa.
** It can be built as a standalone
program or an SQLite3 extension.
**
** Much like base64 representations, base85 can be sent through a
** sane USASCII channel unmolested. It also plays nicely in CSV or
** written as TCL brace-enclosed literals or SQL string literals.
** It is not suited for unmodified use in XML-like documents.
**
** The encoding used resembles Ascii85, but was devised by the author
** (Larry Brasfield) before Mozilla, Adobe, ZMODEM or other Ascii85
** variant sources existed, in the 1984 timeframe on a VAX mainframe.
** Further, this is an independent implementation of a base85 system.
** Hence, the author has rightfully put this into the public domain.
**
** Base85 numerals are taken from the set of 7-bit USASCII codes,
** excluding control characters and Space ! " ' ( ) { | } ~ Del

```



```

** in code order representing digit values 0 to 84 (base 10.)
**
** Groups of 4 bytes, interpreted as big-endian 32-bit values,
** are represented as 5-digit base85 numbers with MS to LS digit
** order. Groups
  of 1-3 bytes are represented with 2-4 digits,
** still big-endian but 8-24 bit values. (Using big-endian yields
** the simplest transition to byte groups smaller than 4 bytes.
** These byte groups can also be considered base-256 numbers.)
** Groups of 0 bytes are represented with 0 digits and vice-versa.
** No pad characters are used; Encoded base85 numeral sequence
** (aka "group") length maps 1-to-1 to the decoded binary length.
**
** Any character not in the base85 numeral set delimits groups.
** When base85 is streamed or stored in containers of indefinite
** size, newline is used to separate it into sub-sequences of no
** more than 80 digits so that fgets() can be used to read it.
**
** Length limitations are not imposed except that the runtime
** SQLite string or blob length limits are respected. Otherwise,
** any length binary sequence can be represented and recovered.
** Base85 sequences can be concatenated by separating them with
** a non-base85 character; the conversion to binary
  will then
** be the concatenation of the represented binary sequences.

** The standalone program either converts base85 on stdin to create
** a binary file or converts a binary file to base85 on stdout.
** Read or make it blurt its help for invocation details.
**
** The SQLite3 extension creates a function, base85(x), which will
** either convert text base85 to a blob or a blob to text base85
** and return the result (or throw an error for other types.)
** Unless built with OMIT_BASE85_CHECKER defined, it also creates a
** function, is_base85(t), which returns 1 iff the text t contains
** nothing other than base85 numerals and whitespace, or 0 otherwise.
**
** To build the extension:
** Set shell variable SQDIR=<your favorite SQLite checkout directory>
** and variable OPTS to -DOMIT_BASE85_CHECKER if is_base85() unwanted.
** *Nix: gcc -O2 -shared -I$SQDIR $OPTS -fPIC -o base85.so base85.c
** OSX: gcc -O2 -dynamiclib -fPIC -I$SQDIR $OPTS -o base85.dylib base85.c
** Win32: gcc -O2
  -shared -I%SQDIR% %OPTS% -o base85.dll base85.c
** Win32: cl /Os -I%SQDIR% %OPTS% base85.c -link -dll -out:base85.dll
**
** To build the standalone program, define PP symbol BASE85_STANDALONE. Eg.
** *Nix or OSX: gcc -O2 -DBASE85_STANDALONE base85.c -o base85

```

```

** Win32: gcc -O2 -DBASE85_STANDALONE -o base85.exe base85.c
** Win32: cl /Os /MD -DBASE85_STANDALONE base85.c
*/
/* This will be more informative in a later version. */

```

Found in path(s):

```

*/sqlite-amalgamation-3450100-zip/sqlite-amalgamation-3450100/shell.c
No license file was found, but licenses were detected in source scan.

```

```

/*
** CAPI3REF: Configuration Options
** KEYWORDS: {configuration option}
**
** These constants are the available integer configuration options that
** can be passed as the first argument to the [sqlite3_config()] interface.
**
** Most of the configuration options for sqlite3_config()
** will only work if invoked prior to [sqlite3_initialize()] or after
** [sqlite3_shutdown()]. The few exceptions to this rule are called
** "anytime configuration options".
** ^Calling [sqlite3_config()] with a first argument that is not an
** anytime configuration option in between calls to [sqlite3_initialize()] and
** [sqlite3_shutdown()] is a no-op that returns SQLITE_MISUSE.
**
** The set of anytime configuration options can change (by insertions
** and/or deletions) from one release of SQLite to the next.
** As of SQLite version 3.42.0, the complete set of anytime configuration
** options is:
** <ul>
** <li>SQLITE_CONFIG_LOG
**
** <li>SQLITE_CONFIG_PCACHE_HDRSZ
** </ul>
**
** New configuration options may be added in future releases of SQLite.
** Existing configuration options might be discontinued. Applications
** should check the return code from [sqlite3_config()] to make sure that
** the call worked. The [sqlite3_config()] interface will return a
** non-zero [error code] if a discontinued or unsupported configuration option
** is invoked.
**
** <dl>
** [[SQLITE_CONFIG_SINGLETHREAD]] <dt>SQLITE_CONFIG_SINGLETHREAD</dt>
** <dd>There are no arguments to this option. ^This option sets the
** [threading mode] to Single-thread. In other words, it disables
** all mutexing and puts SQLite into a mode where it can only be used
** by a single thread. ^If SQLite is compiled with
** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then

```

** it is not possible to change the [threading mode] from its default
 ** value of Single-thread and so [sqlite3_config()] will return
 ** [SQLITE_ERROR] if called
 with the SQLITE_CONFIG_SINGLETHREAD
 ** configuration option.</dd>
 **
 ** [[SQLITE_CONFIG_MULTITHREAD]] <dt>SQLITE_CONFIG_MULTITHREAD</dt>
 ** <dd>There are no arguments to this option. ^This option sets the
 ** [threading mode] to Multi-thread. In other words, it disables
 ** mutexing on [database connection] and [prepared statement] objects.
 ** The application is responsible for serializing access to
 ** [database connections] and [prepared statements]. But other mutexes
 ** are enabled so that SQLite will be safe to use in a multi-threaded
 ** environment as long as no two threads attempt to use the same
 ** [database connection] at the same time. ^If SQLite is compiled with
 ** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
 ** it is not possible to set the Multi-thread [threading mode] and
 ** [sqlite3_config()] will return [SQLITE_ERROR] if called with the
 ** SQLITE_CONFIG_MULTITHREAD configuration option.</dd>
 **
 ** [[SQLITE_CONFIG_SERIALIZED]] <dt>SQLITE_CONFIG_SERIALIZED</dt>
 **
 <dd>There are no arguments to this option. ^This option sets the
 ** [threading mode] to Serialized. In other words, this option enables
 ** all mutexes including the recursive
 ** mutexes on [database connection] and [prepared statement] objects.
 ** In this mode (which is the default when SQLite is compiled with
 ** [SQLITE_THREADSAFE=1]) the SQLite library will itself serialize access
 ** to [database connections] and [prepared statements] so that the
 ** application is free to use the same [database connection] or the
 ** same [prepared statement] in different threads at the same time.
 ** ^If SQLite is compiled with
 ** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
 ** it is not possible to set the Serialized [threading mode] and
 ** [sqlite3_config()] will return [SQLITE_ERROR] if called with the
 ** SQLITE_CONFIG_SERIALIZED configuration option.</dd>
 **
 ** [[SQLITE_CONFIG_MALLOC]] <dt>SQLITE_CONFIG_MALLOC</dt>
 ** <dd> ^The SQLITE_CONFIG_MALLOC option
 takes a single argument which is
 ** a pointer to an instance of the [sqlite3_mem_methods] structure.
 ** The argument specifies
 ** alternative low-level memory allocation routines to be used in place of
 ** the memory allocation routines built into SQLite.)^ ^SQLite makes
 ** its own private copy of the content of the [sqlite3_mem_methods] structure
 ** before the [sqlite3_config()] call returns.</dd>
 **
 ** [[SQLITE_CONFIG_GETMALLOC]] <dt>SQLITE_CONFIG_GETMALLOC</dt>

** <dd> ^The SQLITE_CONFIG_GETMALLOC option takes a single argument which
 ** is a pointer to an instance of the [sqlite3_mem_methods] structure.
 ** The [sqlite3_mem_methods]
 ** structure is filled with the currently defined memory allocation routines.)^
 ** This option can be used to overload the default memory allocation
 ** routines with a wrapper that simulations memory allocation failure or
 ** tracks memory usage, for example. </dd>
 **
 ** [[SQLITE_CONFIG_SMALL_MALLOC]] <dt>SQLITE_CONFIG_SMALL_MALLOC</dt>
 ** <dd> ^The SQLITE_CONFIG_SMALL_MALLOC
 option takes single argument of
 ** type int, interpreted as a boolean, which if true provides a hint to
 ** SQLite that it should avoid large memory allocations if possible.
 ** SQLite will run faster if it is free to make large memory allocations,
 ** but some application might prefer to run slower in exchange for
 ** guarantees about memory fragmentation that are possible if large
 ** allocations are avoided. This hint is normally off.
 ** </dd>
 **
 ** [[SQLITE_CONFIG_MEMSTATUS]] <dt>SQLITE_CONFIG_MEMSTATUS</dt>
 ** <dd> ^The SQLITE_CONFIG_MEMSTATUS option takes single argument of type int,
 ** interpreted as a boolean, which enables or disables the collection of
 ** memory allocation statistics. ^When memory allocation statistics are
 ** disabled, the following SQLite interfaces become non-operational:
 **
 ** [sqlite3_hard_heap_limit64()]
 ** [sqlite3_memory_used()]
 ** [sqlite3_memory_highwater()]
 ** [sqlite3_soft_heap_limit64()]
 **
 [sqlite3_status64()]
 **)^
 ** ^Memory allocation statistics are enabled by default unless SQLite is
 ** compiled with [SQLITE_DEFAULT_MEMSTATUS]=0 in which case memory
 ** allocation statistics are disabled by default.
 ** </dd>
 **
 ** [[SQLITE_CONFIG_SCRATCH]] <dt>SQLITE_CONFIG_SCRATCH</dt>
 ** <dd> The SQLITE_CONFIG_SCRATCH option is no longer used.
 ** </dd>
 **
 ** [[SQLITE_CONFIG_PAGECACHE]] <dt>SQLITE_CONFIG_PAGECACHE</dt>
 ** <dd> ^The SQLITE_CONFIG_PAGECACHE option specifies a memory pool
 ** that SQLite can use for the database page cache with the default page
 ** cache implementation.
 ** This configuration option is a no-op if an application-defined page
 ** cache implementation is loaded using the [SQLITE_CONFIG_PCACHE2].
 ** ^There are three arguments to SQLITE_CONFIG_PAGECACHE: A pointer to

** 8-byte aligned memory (pMem), the size of each page cache line (sz),
 ** and the number of cache lines (N).
 ** The sz argument should be the size of the largest database page
 ** (a power
 of two between 512 and 65536) plus some extra bytes for each
 ** page header. ^The number of extra bytes needed by the page header
 ** can be determined using [SQLITE_CONFIG_PCACHE_HDRSZ].
 ** ^It is harmless, apart from the wasted memory,
 ** for the sz parameter to be larger than necessary. The pMem
 ** argument must be either a NULL pointer or a pointer to an 8-byte
 ** aligned block of memory of at least sz*N bytes, otherwise
 ** subsequent behavior is undefined.
 ** ^When pMem is not NULL, SQLite will strive to use the memory provided
 ** to satisfy page cache needs, falling back to [sqlite3_malloc()] if
 ** a page cache line is larger than sz bytes or if all of the pMem buffer
 ** is exhausted.
 ** ^If pMem is NULL and N is non-zero, then each database connection
 ** does an initial bulk allocation for page cache memory
 ** from [sqlite3_malloc()] sufficient for N cache lines if N is positive or
 ** of -1024*N bytes if N is negative, . ^If additional
 ** page cache memory is needed beyond
 what is provided by the initial
 ** allocation, then SQLite goes to [sqlite3_malloc()] separately for each
 ** additional cache line. </dd>
 **
 ** [[SQLITE_CONFIG_HEAP]] <dt>SQLITE_CONFIG_HEAP</dt>
 ** <dd> ^The SQLITE_CONFIG_HEAP option specifies a static memory buffer
 ** that SQLite will use for all of its dynamic memory allocation needs
 ** beyond those provided for by [SQLITE_CONFIG_PAGECACHE].
 ** ^The SQLITE_CONFIG_HEAP option is only available if SQLite is compiled
 ** with either [SQLITE_ENABLE_MEMSYS3] or [SQLITE_ENABLE_MEMSYS5] and returns
 ** [SQLITE_ERROR] if invoked otherwise.
 ** ^There are three arguments to SQLITE_CONFIG_HEAP:
 ** An 8-byte aligned pointer to the memory,
 ** the number of bytes in the memory buffer, and the minimum allocation size.
 ** ^If the first pointer (the memory pointer) is NULL, then SQLite reverts
 ** to using its default memory allocator (the system malloc() implementation),
 ** undoing any prior invocation of [SQLITE_CONFIG_MALLOC]. ^If the
 ** memory pointer
 is not NULL then the alternative memory
 ** allocator is engaged to handle all of SQLites memory allocation needs.
 ** The first pointer (the memory pointer) must be aligned to an 8-byte
 ** boundary or subsequent behavior of SQLite will be undefined.
 ** The minimum allocation size is capped at 2**12. Reasonable values
 ** for the minimum allocation size are 2**5 through 2**8.</dd>
 **
 ** [[SQLITE_CONFIG_MUTEX]] <dt>SQLITE_CONFIG_MUTEX</dt>
 ** <dd> ^The SQLITE_CONFIG_MUTEX option takes a single argument which is a

** pointer to an instance of the [sqlite3_mutex_methods] structure.
 ** The argument specifies alternative low-level mutex routines to be used
 ** in place the mutex routines built into SQLite.)^ ^SQLite makes a copy of
 ** the content of the [sqlite3_mutex_methods] structure before the call to
 ** [sqlite3_config()] returns. ^If SQLite is compiled with
 ** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
 ** the entire mutexing subsystem is omitted from the
 build and hence calls to
 ** [sqlite3_config()] with the SQLITE_CONFIG_MUTEX configuration option will
 ** return [SQLITE_ERROR].</dd>
 **
 ** [[SQLITE_CONFIG_GETMUTEX]] <dt>SQLITE_CONFIG_GETMUTEX</dt>
 ** <dd> ^The SQLITE_CONFIG_GETMUTEX option takes a single argument which
 ** is a pointer to an instance of the [sqlite3_mutex_methods] structure. The
 ** [sqlite3_mutex_methods]
 ** structure is filled with the currently defined mutex routines.)^
 ** This option can be used to overload the default mutex allocation
 ** routines with a wrapper used to track mutex usage for performance
 ** profiling or testing, for example. ^If SQLite is compiled with
 ** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
 ** the entire mutexing subsystem is omitted from the build and hence calls to
 ** [sqlite3_config()] with the SQLITE_CONFIG_GETMUTEX configuration option will
 ** return [SQLITE_ERROR].</dd>
 **
 ** [[SQLITE_CONFIG_LOOKASIDE]] <dt>SQLITE_CONFIG_LOOKASIDE</dt>
 ** <dd> ^The SQLITE_CONFIG_LOOKASIDE
 option takes two arguments that determine
 ** the default size of lookaside memory on each [database connection].
 ** The first argument is the
 ** size of each lookaside buffer slot and the second is the number of
 ** slots allocated to each database connection.)^ ^The SQLITE_CONFIG_LOOKASIDE
 ** sets the <i>default</i> lookaside size. The [SQLITE_DBCONFIG_LOOKASIDE]
 ** option to [sqlite3_db_config()] can be used to change the lookaside
 ** configuration on individual connections.)^ </dd>
 **
 ** [[SQLITE_CONFIG_PCACHE2]] <dt>SQLITE_CONFIG_PCACHE2</dt>
 ** <dd> ^The SQLITE_CONFIG_PCACHE2 option takes a single argument which is
 ** a pointer to an [sqlite3_pcache_methods2] object. This object specifies
 ** the interface to a custom page cache implementation.)^
 ** ^SQLite makes a copy of the [sqlite3_pcache_methods2] object.</dd>
 **
 ** [[SQLITE_CONFIG_GETPCACHE2]] <dt>SQLITE_CONFIG_GETPCACHE2</dt>
 ** <dd> ^The SQLITE_CONFIG_GETPCACHE2 option takes a single argument which
 ** is
 a pointer to an [sqlite3_pcache_methods2] object. SQLite copies of
 ** the current page cache implementation into that object.)^ </dd>
 **
 ** [[SQLITE_CONFIG_LOG]] <dt>SQLITE_CONFIG_LOG</dt>

** <dd> The SQLITE_CONFIG_LOG option is used to configure the SQLite
 ** global [error log].
 ** (^The SQLITE_CONFIG_LOG option takes two arguments: a pointer to a
 ** function with a call signature of void(*)(void*,int,const char*),
 ** and a pointer to void. ^If the function pointer is not NULL, it is
 ** invoked by [sqlite3_log()] to process each logging event. ^If the
 ** function pointer is NULL, the [sqlite3_log()] interface becomes a no-op.
 ** ^The void pointer that is the second argument to SQLITE_CONFIG_LOG is
 ** passed through as the first parameter to the application-defined logger
 ** function whenever that function is invoked. ^The second parameter to
 ** the logger function is a copy of the first parameter to the corresponding
 ** [sqlite3_log()] call and is intended to be a [result code] or
 an
 ** [extended result code]. ^The third parameter passed to the logger is
 ** log message after formatting via [sqlite3_snprintf()].
 ** The SQLite logging interface is not reentrant; the logger function
 ** supplied by the application must not invoke any SQLite interface.
 ** In a multi-threaded application, the application-defined logger
 ** function must be threadsafe. </dd>
 **
 ** [[SQLITE_CONFIG_URI]] <dt>SQLITE_CONFIG_URI
 ** <dd>^(The SQLITE_CONFIG_URI option takes a single argument of type int.
 ** If non-zero, then URI handling is globally enabled. If the parameter is zero,
 ** then URI handling is globally disabled.)^ ^If URI handling is globally
 ** enabled, all filenames passed to [sqlite3_open()], [sqlite3_open_v2()],
 ** [sqlite3_open16()] or
 ** specified as part of [ATTACH] commands are interpreted as URIs, regardless
 ** of whether or not the [SQLITE_OPEN_URI] flag is set when the database
 ** connection is opened. ^If it is globally disabled, filenames are
 ** only interpreted as
 URIs if the SQLITE_OPEN_URI flag is set when the
 ** database connection is opened. ^By default, URI handling is globally
 ** disabled. The default value may be changed by compiling with the
 ** [SQLITE_USE_URI] symbol defined.)^
 **
 ** [[SQLITE_CONFIG_COVERING_INDEX_SCAN]] <dt>SQLITE_CONFIG_COVERING_INDEX_SCAN
 ** <dd>^The SQLITE_CONFIG_COVERING_INDEX_SCAN option takes a single integer
 ** argument which is interpreted as a boolean in order to enable or disable
 ** the use of covering indices for full table scans in the query optimizer.
 ** ^The default setting is determined
 ** by the [SQLITE_ALLOW_COVERING_INDEX_SCAN] compile-time option, or is "on"
 ** if that compile-time option is omitted.
 ** The ability to disable the use of covering indices for full table scans
 ** is because some incorrectly coded legacy applications might malfunction
 ** when the optimization is enabled. Providing the ability to
 ** disable the optimization allows the older, buggy application code to work
 ** without change

even with newer versions of SQLite.

**

** [[SQLITE_CONFIG_PCACHE]] [[SQLITE_CONFIG_GETPCACHE]]

** <dt>SQLITE_CONFIG_PCACHE and SQLITE_CONFIG_GETPCACHE

** <dd> These options are obsolete and should not be used by new code.

** They are retained for backwards compatibility but are now no-ops.

** </dd>

**

** [[SQLITE_CONFIG_SQLLOG]]

** <dt>SQLITE_CONFIG_SQLLOG

** <dd>This option is only available if sqlite is compiled with the

** [SQLITE_ENABLE_SQLLOG] pre-processor macro defined. The first argument should

** be a pointer to a function of type void(*)(void*,sqlite3*,const char*, int).

** The second should be of type (void*). The callback is invoked by the library

** in three separate circumstances, identified by the value passed as the

** fourth parameter. If the fourth parameter is 0, then the database connection

** passed as the second argument has just been opened. The third argument

** points to a buffer containing the name of the main database file. If the

** fourth parameter is 1,

then the SQL statement that the third parameter

** points to has just been executed. Or, if the fourth parameter is 2, then

** the connection being passed as the second parameter is being closed. The

** third parameter is passed NULL In this case. An example of using this

** configuration option can be seen in the "test_sqllog.c" source file in

** the canonical SQLite source tree.</dd>

**

** [[SQLITE_CONFIG_MMAP_SIZE]]

** <dt>SQLITE_CONFIG_MMAP_SIZE

** <dd>^SQLITE_CONFIG_MMAP_SIZE takes two 64-bit integer (sqlite3_int64) values

** that are the default mmap size limit (the default setting for

** [PRAGMA mmap_size]) and the maximum allowed mmap size limit.

** ^The default setting can be overridden by each database connection using

** either the [PRAGMA mmap_size] command, or by using the

** [SQLITE_FCNTL_MMAP_SIZE] file control. ^The maximum allowed mmap size

** will be silently truncated if necessary so that it does not exceed the

** compile-time maximum mmap size set by the

** [SQLITE_MAX_MMAP_SIZE]

compile-time option.)^

** ^If either argument to this option is negative, then that argument is

** changed to its compile-time default.

**

** [[SQLITE_CONFIG_WIN32_HEAPSIZE]]

** <dt>SQLITE_CONFIG_WIN32_HEAPSIZE

** <dd>^The SQLITE_CONFIG_WIN32_HEAPSIZE option is only available if SQLite is

** compiled for Windows with the [SQLITE_WIN32_MALLOC] pre-processor macro

** defined. ^SQLITE_CONFIG_WIN32_HEAPSIZE takes a 32-bit unsigned integer value

** that specifies the maximum size of the created heap.

**

**** [[SQLITE_CONFIG_PCACHE_HDRSZ]]**
**** <dt>SQLITE_CONFIG_PCACHE_HDRSZ**
**** <dd>^The SQLITE_CONFIG_PCACHE_HDRSZ option takes a single parameter which**
**** is a pointer to an integer and writes into that integer the number of extra**
**** bytes per page required for each page in [SQLITE_CONFIG_PAGECACHE].**
**** The amount of extra space required can change depending on the compiler,**
**** target platform, and SQLite version.**

**** [[SQLITE_CONFIG_PMASZ]]**
**** <dt>SQLITE_CONFIG_PMASZ**
**** <dd>^The**
SQLITE_CONFIG_PMASZ option takes a single parameter which
**** is an unsigned integer and sets the "Minimum PMA Size" for the multithreaded**
**** sorter to that integer. The default minimum PMA Size is set by the**
**** [SQLITE_SORTER_PMASZ] compile-time option. New threads are launched**
**** to help with sort operations when multithreaded sorting**
**** is enabled (using the [PRAGMA threads] command) and the amount of content**
**** to be sorted exceeds the page size times the minimum of the**
**** [PRAGMA cache_size] setting and this value.**

**** [[SQLITE_CONFIG_STMTJRNL_SPILL]]**
**** <dt>SQLITE_CONFIG_STMTJRNL_SPILL**
**** <dd>^The SQLITE_CONFIG_STMTJRNL_SPILL option takes a single parameter which**
**** becomes the [statement journal] spill-to-disk threshold.**
**** [Statement journals] are held in memory until their size (in bytes)**
**** exceeds this threshold, at which point they are written to disk.**
**** Or if the threshold is -1, statement journals are always held**
**** exclusively in memory.**
**** Since many statement journals**
never become large, setting the spill
**** threshold to a value such as 64KiB can greatly reduce the amount of**
**** I/O required to support statement rollback.**
**** The default value for this setting is controlled by the**
**** [SQLITE_STMTJRNL_SPILL] compile-time option.**

**** [[SQLITE_CONFIG_SORTERREF_SIZE]]**
**** <dt>SQLITE_CONFIG_SORTERREF_SIZE**
**** <dd>The SQLITE_CONFIG_SORTERREF_SIZE option accepts a single parameter**
**** of type (int) - the new value of the sorter-reference size threshold.**
**** Usually, when SQLite uses an external sort to order records according**
**** to an ORDER BY clause, all fields required by the caller are present in the**
**** sorted records. However, if SQLite determines based on the declared type**
**** of a table column that its values are likely to be very large - larger**
**** than the configured sorter-reference size threshold - then a reference**
**** is stored in each sorted record and the required column values loaded**
**** from the database as records are returned in sorted order.**
The default
**** value for this option is to never use this optimization. Specifying a**

** negative value for this option restores the default behavior.
 ** This option is only available if SQLite is compiled with the
 ** [SQLITE_ENABLE_SORTER_REFERENCES] compile-time option.
 **
 ** [[SQLITE_CONFIG_MEMDB_MAXSIZE]]
 ** <dt>SQLITE_CONFIG_MEMDB_MAXSIZE
 ** <dd>The SQLITE_CONFIG_MEMDB_MAXSIZE option accepts a single parameter
 ** [sqlite3_int64] parameter which is the default maximum size for an in-memory
 ** database created using [sqlite3_deserialize()]. This default maximum
 ** size can be adjusted up or down for individual databases using the
 ** [SQLITE_FCNTL_SIZE_LIMIT] [sqlite3_file_control|file-control]. If this
 ** configuration setting is never used, then the default maximum is determined
 ** by the [SQLITE_MEMDB_DEFAULT_MAXSIZE] compile-time option. If that
 ** compile-time option is not set, then the default maximum is 1073741824.
 ** </dl>
 */

Found in path(s):

* /sqlite-amalgamation-3450100-zip/sqlite-amalgamation-3450100/sqlite3.h

1.62 tinyxml-2 2.5.3

1.62.1 Available under license :

No license file was found, but licenses were detected in source scan.

/*

www.sourceforge.net/projects/tinyxml

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distribution.

*/

Found in path(s):

* /tinyxml-2-5-3-tar-gz/tinyxml/tinyxmlparser.cpp

No license file was found, but licenses were detected in source scan.

/** @mainpage

<h1> TinyXML </h1>

TinyXML is a simple, small, C++ XML parser that can be easily integrated into other programs.

<h2> What it does. </h2>

In brief, TinyXML parses an XML document, and builds from that a Document Object Model (DOM) that can be read, modified, and saved.

XML stands for "eXtensible Markup Language." It allows you to create your own document markups. Where HTML does a very good job of marking documents for browsers, XML allows you to define any kind of document markup, for example a document that describes a "to do" list for an organizer application. XML is a very structured and convenient format. All those random file formats created to store application data can all be replaced with XML. One parser for everything.

The best place for the complete, correct, and quite frankly hard to read spec is at <http://www.w3.org/TR/2004/REC-xml-20040204/>.

An intro to XML

(that I really like) can be found at

<http://skew.org/xml/tutorial/>.

There are different ways to access and interact with XML data.

TinyXML uses a Document Object Model (DOM), meaning the XML data is parsed into a C++ objects that can be browsed and manipulated, and then written to disk or another output stream. You can also construct an XML document from scratch with C++ objects and write this to disk or another output stream.

TinyXML is designed to be easy and fast to learn. It is two headers and four cpp files. Simply add these to your project and off you go. There is an example file - xmltest.cpp - to get you started.

TinyXML is released under the ZLib license, so you can use it in open source or commercial code. The details

of the license are at the top of every source file.

TinyXML attempts to be a flexible parser, but with truly correct and compliant XML output. TinyXML should compile on any reasonably C++

compliant system. It does not rely on exceptions or RTTI. It can be compiled with or without STL support. TinyXML fully supports the UTF-8 encoding, and the first 64k character entities.

<h2> What it doesn't do. </h2>

TinyXML doesn't parse or use DTDs (Document Type Definitions) or XSLs (eXtensible Stylesheet Language.) There are other parsers out there (check out www.sourceforge.org, search for XML) that are much more fully featured. But they are also much bigger, take longer to set up in your project, have a higher learning curve, and often have a more restrictive license. If you are working with browsers or have more complete XML needs, TinyXML is not the parser for you.

The following DTD syntax will not parse at this time in TinyXML:

```
@verbatim
<!DOCTYPE Archiv [
<!ELEMENT Comment (#PCDATA)>
]>
@endverbatim
```

because TinyXML sees this as a !DOCTYPE node with an illegally embedded !ELEMENT node. This may be addressed in the future.

<h2> Tutorials. </h2>

For the impatient,
here is a tutorial to get you going. A great way to get started,
but it is worth your time to read this (very short) manual completely.

- @subpage tutorial0

<h2> Code Status. </h2>

TinyXML is mature, tested code. It is very stable. If you find bugs, please file a bug report on the sourceforge web site (www.sourceforge.net/projects/tinyxml). We'll get them straightened out as soon as possible.

There are some areas of improvement; please check sourceforge if you are interested in working on TinyXML.

<h2> Related Projects </h2>

TinyXML projects you may find useful! (Descriptions provided by the projects.)

 TinyXPath (<http://tinyxpath.sourceforge.net>). TinyXPath is a small footprint XPath syntax decoder, written in C++.

 TinyXML++ (<http://code.google.com/p/ticpp/>). TinyXML++ is a completely new interface to TinyXML that uses MANY of the C++ strengths. Templates, exceptions, and much better error handling.

<h2> Features </h2>

<h3> Using STL </h3>

TinyXML can be compiled to use or not use STL. When using STL, TinyXML uses the std::string class, and fully supports std::istream, std::ostream, operator<<, and operator>>. Many API methods have both 'const char*' and 'const std::string&' forms.

When STL support is compiled out, no STL files are included whatsoever. All the string classes are implemented by TinyXML itself. API methods all use the 'const char*' form for input.

Use the compile time #define:

TIXML_USE_STL

to compile one version or the other. This can be passed by the compiler, or set as the first line of "tinyxml.h".

Note: If compiling the test code in Linux, setting the environment variable TINYXML_USE_STL=YES/NO will control STL compilation. In the Windows project file, STL and non STL targets are provided. In your project, It's probably easiest to add the line "#define TIXML_USE_STL" as the first line of tinyxml.h.

<h3> UTF-8 </h3>

TinyXML supports UTF-8 allowing to manipulate XML files in any language.

TinyXML

also supports "legacy mode" - the encoding used before UTF-8 support and probably best described as "extended ascii".

Normally, TinyXML will try to detect the correct encoding and use it. However,

by setting the value of `TIXML_DEFAULT_ENCODING` in the header file, TinyXML can be forced to always use one encoding.

TinyXML will assume Legacy Mode until one of the following occurs:

 If the non-standard but common "UTF-8 lead bytes" (0xef 0xbb 0xbf) begin the file or data stream, TinyXML will read it as UTF-8.

 If the declaration tag is read, and it has an encoding="UTF-8", then TinyXML will read it as UTF-8.

 If the declaration tag is read, and it has no encoding specified, then TinyXML will read it as UTF-8.

 If the declaration tag is read, and it has an encoding="something else", then TinyXML will read it as Legacy Mode. In legacy mode, TinyXML will work as it did before. It's not clear what that mode does exactly, but old content should keep working.

 Until one of the above criteria is met, TinyXML runs in Legacy Mode.

What happens if the encoding is incorrectly set or detected? TinyXML will try to read and pass through text seen as improperly encoded. You may get some strange results or mangled characters. You may want to force TinyXML to the correct mode.

You may force TinyXML to Legacy Mode by using `LoadFile( TIXML_ENCODING_LEGACY )` or `LoadFile( filename, TIXML_ENCODING_LEGACY )`. You may force it to use legacy mode all the time by setting `TIXML_DEFAULT_ENCODING = TIXML_ENCODING_LEGACY`. Likewise, you may force it to `TIXML_ENCODING_UTF8` with the same technique.

For English users, using English XML, UTF-8 is the same as low-ASCII. You don't need to be aware of UTF-8 or change your code in any way. You can think of UTF-8 as a "superset" of ASCII.

UTF-8 is not a double byte format - but it is a standard encoding of Unicode!

TinyXML does not use or directly support `wchar`, `TCHAR`, or Microsoft's `_UNICODE` at this time.

It is common to see the term "Unicode" improperly refer to UTF-16, a wide byte encoding of unicode. This is a source of confusion.

For "high-ascii" languages - everything not English, pretty much - TinyXML can handle all languages, at the same time, as long as the XML is encoded in UTF-8. That can be a little tricky, older programs and operating systems tend to use the "default" or "traditional" code page. Many apps (and almost all modern ones) can output UTF-8, but older or stubborn (or just broken) ones still output text in the default code page.

For example, Japanese systems traditionally use SHIFT-JIS encoding.

Text encoded as SHIFT-JIS can not be read by TinyXML.

A good text editor can import SHIFT-JIS and then save as UTF-8.

The `<a href="http://skew.org/xml/tutorial/">Skew.org link</a>` does a great job covering the encoding issue.

The test file "utf8test.xml" is an XML containing English, Spanish, Russian, and Simplified Chinese. (Hopefully they are translated correctly). The file

"utf8test.gif" is a screen capture of the XML file, rendered in IE. Note that if you don't have the correct fonts (Simplified Chinese or Russian) on your system, you won't see output that matches the GIF file even if you can parse it correctly. Also note that (at least on my Windows machine) console output is in a Western code page, so that `Print()` or `printf()` cannot correctly display the file. This is not a bug in TinyXML - just an OS issue. No data is lost or destroyed by TinyXML. The console just doesn't render UTF-8.

<h3> Entities </h3>

TinyXML recognizes the pre-defined "character entities", meaning special characters. Namely:

```
@verbatim
&amp; &
&lt; <
&gt; >
&quot; "
&apos; '
@endverbatim
```

These are recognized when the XML document is read, and translated to there UTF-8 equivalents. For instance, text with the XML of:

```
@verbatim
Far & Away
@endverbatim
```

will have the `Value()` of "Far & Away" when queried from the `TiXmlText` object, and will be written

back to the XML stream/file as an ampersand. Older versions of TinyXML "preserved" character entities, but the newer versions will translate them into characters.

Additionally, any character can be specified by its Unicode code point:

The syntax `" "` or `" "` are both to the non-breaking space character.

<h3> Printing </h3>

TinyXML can print output in several different ways that all have strengths and limitations.

- `Print( FILE* )`. Output to a std-C stream, which includes all C files as well as `stdout`.
- "Pretty prints", but you don't have control over printing options.

- The output is streamed directly to the FILE object, so there is no memory overhead in the TinyXML code.
- used by Print() and SaveFile()
- operator<<. Output to a c++ stream.
- Integrates with standart C++ iostreams.
- Outputs in "network printing" mode without line breaks. Good for network transmission and moving XML between C++ objects, but hard for a human to read.
- TiXmlPrinter. Output to a std::string or memory buffer.
- API is less concise
- Future printing options will be put here.
- Printing may change slightly in future versions as it is refined and expanded.

<h3> Streams </h3>

With TIXML_USE_STL on TinyXML supports C++ streams (operator <<, >>) streams as well as C (FILE*) streams. There are some differences that you may need to be aware of.

C style output:

- based on FILE*
- the Print() and SaveFile() methods

Generates formatted output, with plenty of white space, intended to be as human-readable as possible. They are very fast, and tolerant of ill formed XML documents. For example, an XML document that contains 2 root elements and 2 declarations, will still print.

C style input:

- based on FILE*
- the Parse() and LoadFile() methods

A fast, tolerant read. Use whenever you don't need the C++ streams.

C++ style output:

- based on std::ostream
- operator<<

Generates condensed output, intended for network transmission rather than readability. Depending on your system's implementation of the ostream class, these may be somewhat slower. (Or may not.) Not tolerant of ill formed XML: a document should contain the correct one root element. Additional root level elements will not be streamed out.

C++ style input:

- based on std::istream
- operator>>

Reads XML from a stream, making it useful for network transmission. The tricky part is knowing when the XML document is complete, since there will almost certainly be other data in the stream. TinyXML will assume the XML data is complete after it reads the root element. Put another way, documents that are ill-constructed with more than one root element will not read correctly. Also note that operator>> is somewhat slower than Parse, due to both implementation of the STL and limitations of TinyXML.

<h3> White space </h3>

The world simply does not agree on whether white space should be kept, or condensed. For example, pretend the '_' is a space, and look at "Hello____world". HTML, and at least some XML parsers, will interpret this as "Hello_world". They condense white space. Some XML parsers do not, and will leave it as "Hello____world". (Remember to keep pretending the _ is a space.) Others suggest that __Hello__world__ should become Hello____world.

It's an issue that hasn't been resolved to my satisfaction. TinyXML supports the first 2 approaches. Call TiXmlBase::SetCondenseWhiteSpace(bool) to set the desired behavior. The default is to condense white space.

If you change the default, you should call TiXmlBase::SetCondenseWhiteSpace(bool) before making any calls to Parse XML data, and I don't recommend changing it after it has been set.

<h3> Handles </h3>

Where browsing an XML document in a robust way, it is important to check for null returns from method calls. An error safe implementation can generate a lot of code like:

```
@verbatim
TiXmlElement* root = document.FirstChildElement( "Document" );
if ( root )
{
    TiXmlElement* element = root->FirstChildElement( "Element" );
    if ( element
    )
    {
        TiXmlElement* child = element->FirstChildElement( "Child" );
        if ( child )
        {
            TiXmlElement* child2 = child->NextSiblingElement( "Child" );
            if ( child2 )
            {
                // Finally do something useful.
            }
        }
    }
}
```

@endverbatim

Handles have been introduced to clean this up. Using the TiXmlHandle class, the previous code reduces to:

```
@verbatim
TiXmlHandle docHandle( &document );
TiXmlElement* child2 = docHandle.FirstChild( "Document" ).FirstChild( "Element" ).Child( "Child", 1
).ToElement();
if ( child2 )
{
    // do something useful
}
@endverbatim
```

Which is much easier to deal with. See TiXmlHandle for more information.

<h3> Row and Column tracking </h3>

Being able to track nodes and attributes back to their origin location in source files can be very important for some applications. Additionally, knowing where parsing errors occurred in the original source can be very time saving.

TinyXML can track the row and column origin of all nodes and attributes in a text file. The TiXmlBase::Row() and TiXmlBase::Column() methods return the origin of the node in the source text. The correct tabs can be configured in TiXmlDocument::SetTabSize().

<h2> Using and Installing </h2>

To Compile and Run xmltest:

A Linux Makefile and a Windows Visual C++ .dsw file is provided. Simply compile and run. It will write the file demotest.xml to your disk and generate output on the screen. It also tests walking the DOM by printing out the number of nodes found using different techniques.

The Linux makefile is very generic and runs on many systems - it is currently tested on mingw and MacOSX. You do not need to run 'make depend'. The dependencies have been hard coded.

<h3>Windows project file for VC6</h3>

tinyxml: tinyxml library, non-STL

- tinyxmlSTL: tinyxml library, STL
- tinyXmlTest: test app, non-STL
- tinyXmlTestSTL: test app, STL

<h3>Makefile</h3>

At the top of the makefile you can set:

PROFILE, DEBUG, and TINYXML_USE_STL. Details (such that they are) are in the makefile.

In the tinyxml directory, type "make clean" then "make". The executable file 'xmltest' will be created.

<h3>To Use in an Application:</h3>

Add tinyxml.cpp, tinyxml.h, tinyxmlerror.cpp, tinyxmlparser.cpp, tinystr.cpp, and tinystr.h to your project or make file. That's it! It should compile on any reasonably compliant C++ system. You do not need to enable exceptions or RTTI for TinyXML.

<h2> How TinyXML works. </h2>

An example is probably the best way to go. Take:

```
@verbatim
<?xml version="1.0" standalone=no>
<!-- Our to do list data -->
<ToDo>
<Item priority="1"> Go to the <bold>Toy store!</bold></Item>
<Item priority="2"> Do bills</Item>
</ToDo>
@endverbatim
```

Its not much of a To Do list, but it will do. To read this file (say "demo.xml") you would create a document, and parse it in:

```
@verbatim
TiXmlDocument doc( "demo.xml" );
doc.LoadFile();
@endverbatim
```

And its ready to go. Now lets look at some lines and how they relate to the DOM.

```
@verbatim
```

```
<?xml version="1.0"
standalone=no>
@endverbatim
```

The first line is a declaration, and gets turned into the TiXmlDeclaration class. It will be the first child of the document node.

This is the only directive/special tag parsed by by TinyXML. Generally directive tags are stored in TiXmlUnknown so the commands wont be lost when it is saved back to disk.

```
@verbatim
<!-- Our to do list data -->
@endverbatim
```

A comment. Will become a TiXmlComment object.

```
@verbatim
<ToDo>
@endverbatim
```

The "ToDo" tag defines a TiXmlElement object. This one does not have any attributes, but does contain 2 other elements.

```
@verbatim
<Item priority="1">
@endverbatim
```

Creates another TiXmlElement which is a child of the "ToDo" element. This element has 1 attribute, with the name "priority" and the value "1".

```
@verbatim
Go to the
@endverbatim
```

A TiXmlText. This is a leaf node and cannot contain other nodes. It is a child of the "Item" TiXmlElement.

```
@verbatim
<bold>
@endverbatim
```

Another TiXmlElement, this one a child of the "Item" element.

Etc.

Looking at the entire object tree, you end up with:

```
@verbatim
TiXmlDocument    "demo.xml"
TiXmlDeclaration "version='1.0'" "standalone=no"
TiXmlComment     " Our to do list data"
TiXmlElement     "ToDo"
TiXmlElement     "Item" Attributes: priority = 1
TiXmlText        "Go to the "
TiXmlElement     "bold"
TiXmlText        "Toy store!"
TiXmlElement     "Item" Attributes: priority=2
TiXmlText        "Do bills"
@endverbatim
```

<h2> Documentation </h2>

The documentation is build with Doxygen, using the 'dox' configuration file.

<h2> License </h2>

TinyXML is released under the zlib license:

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3. This notice may not be removed or altered from any source distribution.

<h2> References </h2>

The World Wide Web Consortium is the definitive standard body for

XML, and there web pages contain huge amounts of information.

The definitive spec: <http://www.w3.org/TR/2004/REC-xml-20040204/>

I also recommend "XML Pocket Reference" by Robert Eckstein and published by OReilly...the book that got the whole thing started.

<h2> Contributors, Contacts, and a Brief History </h2>

Thanks very much to everyone who sends suggestions, bugs, ideas, and encouragement. It all helps, and makes this project fun. A special thanks to the contributors on the web pages that keep it lively.

So many people have sent in bugs and ideas, that rather than list here we try to give credit due in the "changes.txt" file.

TinyXML was originally written by Lee Thomason. (Often the "I" still in the documentation.) Lee reviews changes and releases new versions, with the help of Yves Berquin, Andrew Ellerton, and the tinyXml community.

We appreciate your suggestions, and would love to know if you use TinyXML. Hopefully you will enjoy it and find it useful. Please post questions, comments, file bugs, or contact us at:

www.sourceforge.net/projects/tinyxml

Lee Thomason, Yves Berquin, Andrew Ellerton
*/

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*

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* /tinyxml-2-5-3-tar-gz/tinyxml/docs/tinystl_8h-source.html

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* /tinyxml-2-5-3-tar-gz/tinyxml/tinyxml.h

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1.63 glog 0.6.0

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1.64 augeas 1.14.1

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1.65 yara 4.1.1

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* NCSA HTTPd Server
* Software Development Group
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Written by Adam Twiss (adam@zeus.co.uk). March 1996

Thanks to the following people for their input:

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*/

For the expat xml parser component:

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The End

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<?xml version="1.0" encoding="ISO-8859-1"?>

<!DOCTYPE html PUBLIC "-//W3C//DTD XHTML 1.0 Strict//EN" "http://www.w3.org/TR/xhtml1/DTD/xhtml1-strict.dtd">

<html xmlns="http://www.w3.org/1999/xhtml" lang="en" xml:lang="en"><head><!--

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX

X

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```
</div>
</div>
<div class="bottomlang">
<p><span>Available Languages: </span><a href="/en/license.html" title="English">&nbsp;en&nbsp;</a></p>
</div><div class="top"><a href="#page-header"></a></div><div
class="section"><h2><a id="comments_section" name="comments_section">Comments</a></h2><div
class="warning"><strong>Notice:</strong><br />This is not a Q&A section. Comments
placed here should be pointed towards suggestions on improving the documentation or server, and may be removed
again by our moderators if they are either implemented or considered invalid/off-topic. Questions on how to manage
the Apache HTTP Server should be directed at either our IRC channel, #httpd, on Freenode, or sent to our <a
href="http://httpd.apache.org/lists.html">mailing lists</a>.</div>
<script type="text/javascript"><!--><![CDATA[</script>
var comments_shortcode = 'httpd';
var comments_identifier = 'http://httpd.apache.org/docs/2.4/license.html';
(function(w, d) {
  if (w.location.hostname.toLowerCase() == "httpd.apache.org") {
    d.write('<div id="comments_thread"></div>');
    var s = d.createElement('script');
    s.type = 'text/javascript';
    s.async = true;
    s.src = 'https://comments.apache.org/show_comments.lua?site=' + comments_shortcode + '&page=' +
comments_identifier;
    (d.getElementsByTagName('head')[0] || d.getElementsByTagName('body')[0]).appendChild(s);
  }
  else {
    d.write('<div id="comments_thread">Comments are disabled for this page at the moment.</div>');
  }
})(window, document);
--><![></script></div><div id="footer">
<p class="apache">Copyright 2015 The Apache Software Foundation.<br />Licensed under the <a
href="http://www.apache.org/licenses/LICENSE-2.0">Apache License, Version 2.0</a>.</p>
<p class="menu"><a href="/mod/">Modules</a> | <a href="/mod/directives.html">Directives</a> | <a
href="http://wiki.apache.org/httpd/FAQ">FAQ</a> | <a href="/glossary.html">Glossary</a> | <a
href="/sitemap.html">Sitemap</a></p></div><script type="text/javascript"><!--><![CDATA[</script>
if (typeof(prettyPrint) !== 'undefined') {
  prettyPrint();
}
--><![></script>
</body></html>
```

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```
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#####  
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#####  
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1.67 sqlite 3.45.2

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```
/*
** CAPI3REF: Configuration Options
** KEYWORDS: {configuration option}
**
** These constants are the available integer configuration options that
** can be passed as the first argument to the [sqlite3_config()] interface.
**
** Most of the configuration options for sqlite3_config()
** will only work if invoked prior to [sqlite3_initialize()] or after
** [sqlite3_shutdown()]. The few exceptions to this rule are called
** "anytime configuration options".
** ^Calling [sqlite3_config()] with a first argument that is not an
** anytime configuration option in between calls to [sqlite3_initialize()] and
** [sqlite3_shutdown()] is a no-op that returns SQLITE_MISUSE.
**
** The set of anytime configuration options can change (by insertions
** and/or deletions) from one release of SQLite to the next.
** As of SQLite version 3.42.0, the complete set of anytime configuration
** options is:
** <ul>
** <li>SQLITE_CONFIG_LOG
**
** <li>SQLITE_CONFIG_PCACHE_HDRSZ
** </ul>
**
** New configuration options may be added in future releases of SQLite.
** Existing configuration options might be discontinued. Applications
** should check the return code from [sqlite3_config()] to make sure that
** the call worked. The [sqlite3_config()] interface will return a
** non-zero [error code] if a discontinued or unsupported configuration option
** is invoked.
**
** <dl>
** [[SQLITE_CONFIG_SINGLETHREAD]] <dt>SQLITE_CONFIG_SINGLETHREAD</dt>
** <dd>There are no arguments to this option. ^This option sets the
** [threading mode] to Single-thread. In other words, it disables
** all mutexing and puts SQLite into a mode where it can only be used
** by a single thread. ^If SQLite is compiled with
** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
** it is not possible to change the [threading mode] from its default
** value of Single-thread and so [sqlite3_config()] will return
** [SQLITE_ERROR] if called
** with the SQLITE_CONFIG_SINGLETHREAD
** configuration option.</dd>
**

```

SQLITE_CONFIG_MULTITHREAD <dt>SQLITE_CONFIG_MULTITHREAD</dt>
 <dd>There are no arguments to this option. ^This option sets the
 [threading mode] to Multi-thread. In other words, it disables
 mutexing on [database connection] and [prepared statement] objects.
 The application is responsible for serializing access to
 [database connections] and [prepared statements]. But other mutexes
 are enabled so that SQLite will be safe to use in a multi-threaded
 environment as long as no two threads attempt to use the same
 [database connection] at the same time. ^If SQLite is compiled with
 the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
 it is not possible to set the Multi-thread [threading mode] and
 [sqlite3_config()] will return [SQLITE_ERROR] if called with the
 SQLITE_CONFIG_MULTITHREAD configuration option.</dd>

SQLITE_CONFIG_SERIALIZED <dt>SQLITE_CONFIG_SERIALIZED</dt>
 <dd>There are no arguments to this option. ^This option sets the
 [threading mode] to Serialized. In other words, this option enables
 all mutexes including the recursive
 mutexes on [database connection] and [prepared statement] objects.
 In this mode (which is the default when SQLite is compiled with
 [SQLITE_THREADSAFE=1]) the SQLite library will itself serialize access
 to [database connections] and [prepared statements] so that the
 application is free to use the same [database connection] or the
 same [prepared statement] in different threads at the same time.
 ^If SQLite is compiled with
 the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
 it is not possible to set the Serialized [threading mode] and
 [sqlite3_config()] will return [SQLITE_ERROR] if called with the
 SQLITE_CONFIG_SERIALIZED configuration option.</dd>

SQLITE_CONFIG_MALLOC <dt>SQLITE_CONFIG_MALLOC</dt>
 <dd> ^The SQLITE_CONFIG_MALLOC option
 takes a single argument which is
 a pointer to an instance of the [sqlite3_mem_methods] structure.
 The argument specifies
 alternative low-level memory allocation routines to be used in place of
 the memory allocation routines built into SQLite.)^ ^SQLite makes
 its own private copy of the content of the [sqlite3_mem_methods] structure
 before the [sqlite3_config()] call returns.</dd>

SQLITE_CONFIG_GETMALLOC <dt>SQLITE_CONFIG_GETMALLOC</dt>
 <dd> ^The SQLITE_CONFIG_GETMALLOC option takes a single argument which
 is a pointer to an instance of the [sqlite3_mem_methods] structure.
 The [sqlite3_mem_methods]
 structure is filled with the currently defined memory allocation routines.)^
 This option can be used to overload the default memory allocation
 routines with a wrapper that simulations memory allocation failure or

** tracks memory usage, for example. </dd>
 **
 ** [[SQLITE_CONFIG_SMALL_MALLOC]] <dt>SQLITE_CONFIG_SMALL_MALLOC</dt>
 ** <dd> ^The SQLITE_CONFIG_SMALL_MALLOC
 option takes single argument of
 ** type int, interpreted as a boolean, which if true provides a hint to
 ** SQLite that it should avoid large memory allocations if possible.
 ** SQLite will run faster if it is free to make large memory allocations,
 ** but some application might prefer to run slower in exchange for
 ** guarantees about memory fragmentation that are possible if large
 ** allocations are avoided. This hint is normally off.
 ** </dd>
 **
 ** [[SQLITE_CONFIG_MEMSTATUS]] <dt>SQLITE_CONFIG_MEMSTATUS</dt>
 ** <dd> ^The SQLITE_CONFIG_MEMSTATUS option takes single argument of type int,
 ** interpreted as a boolean, which enables or disables the collection of
 ** memory allocation statistics. ^When memory allocation statistics are
 ** disabled, the following SQLite interfaces become non-operational:
 **
 ** [sqlite3_hard_heap_limit64()]
 ** [sqlite3_memory_used()]
 ** [sqlite3_memory_highwater()]
 ** [sqlite3_soft_heap_limit64()]
 **
 [sqlite3_status64()]
 **)^
 ** ^Memory allocation statistics are enabled by default unless SQLite is
 ** compiled with [SQLITE_DEFAULT_MEMSTATUS]=0 in which case memory
 ** allocation statistics are disabled by default.
 ** </dd>
 **
 ** [[SQLITE_CONFIG_SCRATCH]] <dt>SQLITE_CONFIG_SCRATCH</dt>
 ** <dd> The SQLITE_CONFIG_SCRATCH option is no longer used.
 ** </dd>
 **
 ** [[SQLITE_CONFIG_PAGECACHE]] <dt>SQLITE_CONFIG_PAGECACHE</dt>
 ** <dd> ^The SQLITE_CONFIG_PAGECACHE option specifies a memory pool
 ** that SQLite can use for the database page cache with the default page
 ** cache implementation.
 ** This configuration option is a no-op if an application-defined page
 ** cache implementation is loaded using the [SQLITE_CONFIG_PCACHE2].
 ** ^There are three arguments to SQLITE_CONFIG_PAGECACHE: A pointer to
 ** 8-byte aligned memory (pMem), the size of each page cache line (sz),
 ** and the number of cache lines (N).
 ** The sz argument should be the size of the largest database page
 ** (a power
 of two between 512 and 65536) plus some extra bytes for each
 ** page header. ^The number of extra bytes needed by the page header

** can be determined using [SQLITE_CONFIG_PCACHE_HDRSZ].
 ** ^It is harmless, apart from the wasted memory,
 ** for the sz parameter to be larger than necessary. The pMem
 ** argument must be either a NULL pointer or a pointer to an 8-byte
 ** aligned block of memory of at least sz*N bytes, otherwise
 ** subsequent behavior is undefined.
 ** ^When pMem is not NULL, SQLite will strive to use the memory provided
 ** to satisfy page cache needs, falling back to [sqlite3_malloc()] if
 ** a page cache line is larger than sz bytes or if all of the pMem buffer
 ** is exhausted.
 ** ^If pMem is NULL and N is non-zero, then each database connection
 ** does an initial bulk allocation for page cache memory
 ** from [sqlite3_malloc()] sufficient for N cache lines if N is positive or
 ** of -1024*N bytes if N is negative, . ^If additional
 ** page cache memory is needed beyond
 ** what is provided by the initial
 ** allocation, then SQLite goes to [sqlite3_malloc()] separately for each
 ** additional cache line. </dd>
 **
 ** [[SQLITE_CONFIG_HEAP]] <dt>SQLITE_CONFIG_HEAP</dt>
 ** <dd> ^The SQLITE_CONFIG_HEAP option specifies a static memory buffer
 ** that SQLite will use for all of its dynamic memory allocation needs
 ** beyond those provided for by [SQLITE_CONFIG_PAGECACHE].
 ** ^The SQLITE_CONFIG_HEAP option is only available if SQLite is compiled
 ** with either [SQLITE_ENABLE_MEMSYS3] or [SQLITE_ENABLE_MEMSYS5] and returns
 ** [SQLITE_ERROR] if invoked otherwise.
 ** ^There are three arguments to SQLITE_CONFIG_HEAP:
 ** An 8-byte aligned pointer to the memory,
 ** the number of bytes in the memory buffer, and the minimum allocation size.
 ** ^If the first pointer (the memory pointer) is NULL, then SQLite reverts
 ** to using its default memory allocator (the system malloc() implementation),
 ** undoing any prior invocation of [SQLITE_CONFIG_MALLOC]. ^If the
 ** memory pointer
 ** is not NULL then the alternative memory
 ** allocator is engaged to handle all of SQLites memory allocation needs.
 ** The first pointer (the memory pointer) must be aligned to an 8-byte
 ** boundary or subsequent behavior of SQLite will be undefined.
 ** The minimum allocation size is capped at 2**12. Reasonable values
 ** for the minimum allocation size are 2**5 through 2**8.</dd>
 **
 ** [[SQLITE_CONFIG_MUTEX]] <dt>SQLITE_CONFIG_MUTEX</dt>
 ** <dd> ^The SQLITE_CONFIG_MUTEX option takes a single argument which is a
 ** pointer to an instance of the [sqlite3_mutex_methods] structure.
 ** The argument specifies alternative low-level mutex routines to be used
 ** in place the mutex routines built into SQLite.)^ ^SQLite makes a copy of
 ** the content of the [sqlite3_mutex_methods] structure before the call to
 ** [sqlite3_config()] returns. ^If SQLite is compiled with
 ** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then

** the entire mutexing subsystem is omitted from the build and hence calls to
 ** [sqlite3_config()] with the SQLITE_CONFIG_MUTEX configuration option will
 ** return [SQLITE_ERROR].</dd>
 **
 ** [[SQLITE_CONFIG_GETMUTEX]] <dt>SQLITE_CONFIG_GETMUTEX</dt>
 ** <dd> ^(The SQLITE_CONFIG_GETMUTEX option takes a single argument which
 ** is a pointer to an instance of the [sqlite3_mutex_methods] structure. The
 ** [sqlite3_mutex_methods]
 ** structure is filled with the currently defined mutex routines.)^
 ** This option can be used to overload the default mutex allocation
 ** routines with a wrapper used to track mutex usage for performance
 ** profiling or testing, for example. ^If SQLite is compiled with
 ** the [SQLITE_THREADSafe | SQLITE_THREADSafe=0] compile-time option then
 ** the entire mutexing subsystem is omitted from the build and hence calls to
 ** [sqlite3_config()] with the SQLITE_CONFIG_GETMUTEX configuration option will
 ** return [SQLITE_ERROR].</dd>
 **
 ** [[SQLITE_CONFIG_LOOKASIDE]] <dt>SQLITE_CONFIG_LOOKASIDE</dt>
 ** <dd> ^(The SQLITE_CONFIG_LOOKASIDE
 option takes two arguments that determine
 ** the default size of lookaside memory on each [database connection].
 ** The first argument is the
 ** size of each lookaside buffer slot and the second is the number of
 ** slots allocated to each database connection.)^ ^(SQLITE_CONFIG_LOOKASIDE
 ** sets the <i>default</i> lookaside size. The [SQLITE_DBCONFIG_LOOKASIDE]
 ** option to [sqlite3_db_config()] can be used to change the lookaside
 ** configuration on individual connections.)^ </dd>
 **
 ** [[SQLITE_CONFIG_PCACHE2]] <dt>SQLITE_CONFIG_PCACHE2</dt>
 ** <dd> ^(The SQLITE_CONFIG_PCACHE2 option takes a single argument which is
 ** a pointer to an [sqlite3_pcache_methods2] object. This object specifies
 ** the interface to a custom page cache implementation.)^
 ** ^SQLite makes a copy of the [sqlite3_pcache_methods2] object.</dd>
 **
 ** [[SQLITE_CONFIG_GETPCACHE2]] <dt>SQLITE_CONFIG_GETPCACHE2</dt>
 ** <dd> ^(The SQLITE_CONFIG_GETPCACHE2 option takes a single argument which
 ** is
 a pointer to an [sqlite3_pcache_methods2] object. SQLite copies of
 ** the current page cache implementation into that object.)^ </dd>
 **
 ** [[SQLITE_CONFIG_LOG]] <dt>SQLITE_CONFIG_LOG</dt>
 ** <dd> The SQLITE_CONFIG_LOG option is used to configure the SQLite
 ** global [error log].
 ** (^The SQLITE_CONFIG_LOG option takes two arguments: a pointer to a
 ** function with a call signature of void(*)(void*,int,const char*),
 ** and a pointer to void. ^If the function pointer is not NULL, it is
 ** invoked by [sqlite3_log()] to process each logging event. ^If the

** function pointer is NULL, the [sqlite3_log()] interface becomes a no-op.
 ** ^The void pointer that is the second argument to SQLITE_CONFIG_LOG is
 ** passed through as the first parameter to the application-defined logger
 ** function whenever that function is invoked. ^The second parameter to
 ** the logger function is a copy of the first parameter to the corresponding
 ** [sqlite3_log()] call and is intended to be a [result code] or
 an
 ** [extended result code]. ^The third parameter passed to the logger is
 ** log message after formatting via [sqlite3_snprintf()].
 ** The SQLite logging interface is not reentrant; the logger function
 ** supplied by the application must not invoke any SQLite interface.
 ** In a multi-threaded application, the application-defined logger
 ** function must be threadsafe. </dd>
 **
 ** [[SQLITE_CONFIG_URI]] <dt>SQLITE_CONFIG_URI
 ** <dd>^(The SQLITE_CONFIG_URI option takes a single argument of type int.
 ** If non-zero, then URI handling is globally enabled. If the parameter is zero,
 ** then URI handling is globally disabled.)^ ^If URI handling is globally
 ** enabled, all filenames passed to [sqlite3_open()], [sqlite3_open_v2()],
 ** [sqlite3_open16()] or
 ** specified as part of [ATTACH] commands are interpreted as URIs, regardless
 ** of whether or not the [SQLITE_OPEN_URI] flag is set when the database
 ** connection is opened. ^If it is globally disabled, filenames are
 ** only interpreted as
 URIs if the SQLITE_OPEN_URI flag is set when the
 ** database connection is opened. ^By default, URI handling is globally
 ** disabled. The default value may be changed by compiling with the
 ** [SQLITE_USE_URI] symbol defined.)^
 **
 ** [[SQLITE_CONFIG_COVERING_INDEX_SCAN]] <dt>SQLITE_CONFIG_COVERING_INDEX_SCAN
 ** <dd>^The SQLITE_CONFIG_COVERING_INDEX_SCAN option takes a single integer
 ** argument which is interpreted as a boolean in order to enable or disable
 ** the use of covering indices for full table scans in the query optimizer.
 ** ^The default setting is determined
 ** by the [SQLITE_ALLOW_COVERING_INDEX_SCAN] compile-time option, or is "on"
 ** if that compile-time option is omitted.
 ** The ability to disable the use of covering indices for full table scans
 ** is because some incorrectly coded legacy applications might malfunction
 ** when the optimization is enabled. Providing the ability to
 ** disable the optimization allows the older, buggy application code to work
 ** without change
 even with newer versions of SQLite.
 **
 ** [[SQLITE_CONFIG_PCACHE]] [[SQLITE_CONFIG_GETPCACHE]]
 ** <dt>SQLITE_CONFIG_PCACHE and SQLITE_CONFIG_GETPCACHE
 ** <dd> These options are obsolete and should not be used by new code.
 ** They are retained for backwards compatibility but are now no-ops.
 ** </dd>

****** `[[SQLITE_CONFIG_SQLLOG]]`
****** `<dt>SQLITE_CONFIG_SQLLOG`
****** `<dd>`This option is only available if `sqlite` is compiled with the
****** `[SQLITE_ENABLE_SQLLOG]` pre-processor macro defined. The first argument should
****** be a pointer to a function of type `void(*)(void*,sqlite3*,const char*, int)`.
****** The second should be of type `(void*)`. The callback is invoked by the library
****** in three separate circumstances, identified by the value passed as the
****** fourth parameter. If the fourth parameter is 0, then the database connection
****** passed as the second argument has just been opened. The third argument
****** points to a buffer containing the name of the main database file. If the
****** fourth parameter is 1,
 then the SQL statement that the third parameter
****** points to has just been executed. Or, if the fourth parameter is 2, then
****** the connection being passed as the second parameter is being closed. The
****** third parameter is passed NULL In this case. An example of using this
****** configuration option can be seen in the "test_sqllog.c" source file in
****** the canonical SQLite source tree.`</dd>`

****** `[[SQLITE_CONFIG_MMAP_SIZE]]`
****** `<dt>SQLITE_CONFIG_MMAP_SIZE`
****** `<dd>`^`SQLITE_CONFIG_MMAP_SIZE` takes two 64-bit integer (`sqlite3_int64`) values
****** that are the default mmap size limit (the default setting for
****** `[PRAGMA mmap_size]`) and the maximum allowed mmap size limit.
****** ^The default setting can be overridden by each database connection using
****** either the `[PRAGMA mmap_size]` command, or by using the
****** `[SQLITE_FCNTL_MMAP_SIZE]` file control. ^The maximum allowed mmap size
****** will be silently truncated if necessary so that it does not exceed the
****** compile-time maximum mmap size set by the
****** `[SQLITE_MAX_MMAP_SIZE]`
 compile-time option.)^
****** ^If either argument to this option is negative, then that argument is
****** changed to its compile-time default.

****** `[[SQLITE_CONFIG_WIN32_HEAPSIZE]]`
****** `<dt>SQLITE_CONFIG_WIN32_HEAPSIZE`
****** `<dd>`^The `SQLITE_CONFIG_WIN32_HEAPSIZE` option is only available if SQLite is
****** compiled for Windows with the `[SQLITE_WIN32_MALLOC]` pre-processor macro
****** defined. ^`SQLITE_CONFIG_WIN32_HEAPSIZE` takes a 32-bit unsigned integer value
****** that specifies the maximum size of the created heap.

****** `[[SQLITE_CONFIG_PCACHE_HDRSZ]]`
****** `<dt>SQLITE_CONFIG_PCACHE_HDRSZ`
****** `<dd>`^The `SQLITE_CONFIG_PCACHE_HDRSZ` option takes a single parameter which
****** is a pointer to an integer and writes into that integer the number of extra
****** bytes per page required for each page in `[SQLITE_CONFIG_PAGECACHE]`.
****** The amount of extra space required can change depending on the compiler,
****** target platform, and SQLite version.

****** [[SQLITE_CONFIG_PMASZ]]
****** <dt>SQLITE_CONFIG_PMASZ
****** <dd>^The
 SQLITE_CONFIG_PMASZ option takes a single parameter which
****** is an unsigned integer and sets the "Minimum PMA Size" for the multithreaded
****** sorter to that integer. The default minimum PMA Size is set by the
****** [SQLITE_SORTER_PMASZ] compile-time option. New threads are launched
****** to help with sort operations when multithreaded sorting
****** is enabled (using the [PRAGMA threads] command) and the amount of content
****** to be sorted exceeds the page size times the minimum of the
****** [PRAGMA cache_size] setting and this value.

****** [[SQLITE_CONFIG_STMTJRNL_SPILL]]
****** <dt>SQLITE_CONFIG_STMTJRNL_SPILL
****** <dd>^The SQLITE_CONFIG_STMTJRNL_SPILL option takes a single parameter which
****** becomes the [statement journal] spill-to-disk threshold.
****** [Statement journals] are held in memory until their size (in bytes)
****** exceeds this threshold, at which point they are written to disk.
****** Or if the threshold is -1, statement journals are always held
****** exclusively in memory.
****** Since many statement journals
 never become large, setting the spill
****** threshold to a value such as 64KiB can greatly reduce the amount of
****** I/O required to support statement rollback.
****** The default value for this setting is controlled by the
****** [SQLITE_STMTJRNL_SPILL] compile-time option.

****** [[SQLITE_CONFIG_SORTERREF_SIZE]]
****** <dt>SQLITE_CONFIG_SORTERREF_SIZE
****** <dd>The SQLITE_CONFIG_SORTERREF_SIZE option accepts a single parameter
****** of type (int) - the new value of the sorter-reference size threshold.
****** Usually, when SQLite uses an external sort to order records according
****** to an ORDER BY clause, all fields required by the caller are present in the
****** sorted records. However, if SQLite determines based on the declared type
****** of a table column that its values are likely to be very large - larger
****** than the configured sorter-reference size threshold - then a reference
****** is stored in each sorted record and the required column values loaded
****** from the database as records are returned in sorted order.
 The default
****** value for this option is to never use this optimization. Specifying a
****** negative value for this option restores the default behavior.
****** This option is only available if SQLite is compiled with the
****** [SQLITE_ENABLE_SORTER_REFERENCES] compile-time option.

****** [[SQLITE_CONFIG_MEMDB_MAXSIZE]]
****** <dt>SQLITE_CONFIG_MEMDB_MAXSIZE
****** <dd>The SQLITE_CONFIG_MEMDB_MAXSIZE option accepts a single parameter


```

** [sqlite3_int64] parameter which is the default maximum size for an in-memory
** database created using [sqlite3_deserialize()]. This default maximum
** size can be adjusted up or down for individual databases using the
** [SQLITE_FCNTL_SIZE_LIMIT] [sqlite3_file_control|file-control]. If this
** configuration setting is never used, then the default maximum is determined
** by the [SQLITE_MEMDB_DEFAULT_MAXSIZE] compile-time option. If that
** compile-time option is not set, then the default maximum is 1073741824.
** </dl>
*/

```

Found in path(s):

* /sqlite-amalgamation-3450200-zip/sqlite-amalgamation-3450200/sqlite3.h
No license file was found, but licenses were detected in source scan.

```

/*
** 2022-11-18
**
** The author disclaims copyright to this source code. In place of
** a legal notice, here is a blessing:
**
**    May you do good and not evil.
**    May you find forgiveness for yourself and forgive others.
**    May you share freely, never taking more than you give.
**
*****
**
** This is a SQLite extension for converting in either direction
** between a (binary) blob and base64 text. Base64 can transit a
** sane USASCII channel unmolested. It also plays nicely in CSV or
** written as TCL brace-enclosed literals or SQL string literals,
** and can be used unmodified in XML-like documents.
**
** This is an independent implementation of conversions specified in
** RFC 4648, done on the above date by the author (Larry Brasfield)
** who thereby has the right to put this into the public domain.
**
** The conversions meet RFC 4648 requirements,
** provided that this
** C source specifies that line-feeds are included in the encoded
** data to limit visible line lengths to 72 characters and to
** terminate any encoded blob having non-zero length.
**
** Length limitations are not imposed except that the runtime
** SQLite string or blob length limits are respected. Otherwise,
** any length binary sequence can be represented and recovered.
** Generated base64 sequences, with their line-feeds included,
** can be concatenated; the result converted back to binary will
** be the concatenation of the represented binary sequences.

```

```

**
** This SQLite3 extension creates a function, base64(x), which
** either: converts text x containing base64 to a returned blob;
** or converts a blob x to returned text containing base64. An
** error will be thrown for other input argument types.
**
** This code relies on UTF-8 encoding only with respect to the
** meaning of the first 128 (7-bit) codes matching that of USASCII.
** It will fail miserably
if somehow made to try to convert EBCDIC.
** Because it is table-driven, it could be enhanced to handle that,
** but the world and SQLite have moved on from that anachronism.
**
** To build the extension:
** Set shell variable SQDIR=<your favorite SQLite checkout directory>
** *Nix: gcc -O2 -shared -I$SQDIR -fPIC -o base64.so base64.c
** OSX: gcc -O2 -dynamiclib -fPIC -I$SQDIR -o base64.dylib base64.c
** Win32: gcc -O2 -shared -I%SQDIR% -o base64.dll base64.c
** Win32: cl /Os -I%SQDIR% base64.c -link -dll -out:base64.dll
*/
/*
** 2022-11-16
**
** The author disclaims copyright to this source code. In place of
** a legal notice, here is a blessing:
**
** May you do good and not evil.
** May you find forgiveness for yourself and forgive others.
** May you share freely, never taking more than you give.
**
*****
**
** This is a utility for converting binary to base85 or vice-versa.
** It can be built as a standalone
program or an SQLite3 extension.
**
** Much like base64 representations, base85 can be sent through a
** sane USASCII channel unmolested. It also plays nicely in CSV or
** written as TCL brace-enclosed literals or SQL string literals.
** It is not suited for unmodified use in XML-like documents.
**
** The encoding used resembles Ascii85, but was devised by the author
** (Larry Brasfield) before Mozilla, Adobe, ZMODEM or other Ascii85
** variant sources existed, in the 1984 timeframe on a VAX mainframe.
** Further, this is an independent implementation of a base85 system.
** Hence, the author has rightfully put this into the public domain.
**
** Base85 numerals are taken from the set of 7-bit USASCII codes,

```

```

** excluding control characters and Space ! " ' ( ) { | } ~ Del
** in code order representing digit values 0 to 84 (base 10.)
**
** Groups of 4 bytes, interpreted as big-endian 32-bit values,
** are represented as 5-digit base85 numbers with MS to LS digit
** order. Groups
  of 1-3 bytes are represented with 2-4 digits,
** still big-endian but 8-24 bit values. (Using big-endian yields
** the simplest transition to byte groups smaller than 4 bytes.
** These byte groups can also be considered base-256 numbers.)
** Groups of 0 bytes are represented with 0 digits and vice-versa.
** No pad characters are used; Encoded base85 numeral sequence
** (aka "group") length maps 1-to-1 to the decoded binary length.
**
** Any character not in the base85 numeral set delimits groups.
** When base85 is streamed or stored in containers of indefinite
** size, newline is used to separate it into sub-sequences of no
** more than 80 digits so that fgets() can be used to read it.
**
** Length limitations are not imposed except that the runtime
** SQLite string or blob length limits are respected. Otherwise,
** any length binary sequence can be represented and recovered.
** Base85 sequences can be concatenated by separating them with
** a non-base85 character; the conversion to binary
  will then
** be the concatenation of the represented binary sequences.

** The standalone program either converts base85 on stdin to create
** a binary file or converts a binary file to base85 on stdout.
** Read or make it blurt its help for invocation details.
**
** The SQLite3 extension creates a function, base85(x), which will
** either convert text base85 to a blob or a blob to text base85
** and return the result (or throw an error for other types.)
** Unless built with OMIT_BASE85_CHECKER defined, it also creates a
** function, is_base85(t), which returns 1 iff the text t contains
** nothing other than base85 numerals and whitespace, or 0 otherwise.
**
** To build the extension:
** Set shell variable SQDIR=<your favorite SQLite checkout directory>
** and variable OPTS to -DOMIT_BASE85_CHECKER if is_base85() unwanted.
** *Nix: gcc -O2 -shared -I$SQDIR $OPTS -fPIC -o base85.so base85.c
** OSX: gcc -O2 -dynamiclib -fPIC -I$SQDIR $OPTS -o base85.dylib base85.c
** Win32: gcc -O2
  -shared -I$SQDIR% %OPTS% -o base85.dll base85.c
** Win32: cl /Os -I$SQDIR% %OPTS% base85.c -link -dll -out:base85.dll
**
** To build the standalone program, define PP symbol BASE85_STANDALONE. Eg.

```

```
** *Nix or OSX: gcc -O2 -DBASE85_STANDALONE base85.c -o base85
** Win32: gcc -O2 -DBASE85_STANDALONE -o base85.exe base85.c
** Win32: cl /Os /MD -DBASE85_STANDALONE base85.c
*/
/* This will be more informative in a later version. */
```

Found in path(s):

* /sqlite-amalgamation-3450200-zip/sqlite-amalgamation-3450200/shell.c

No license file was found, but licenses were detected in source scan.

```
/*
** CAPI3REF: Configuration Options
** KEYWORDS: {configuration option}
**
** These constants are the available integer configuration options that
** can be passed as the first argument to the [sqlite3_config()] interface.
**
** Most of the configuration options for sqlite3_config()
** will only work if invoked prior to [sqlite3_initialize()] or after
** [sqlite3_shutdown()]. The few exceptions to this rule are called
** "anytime configuration options".
** ^Calling [sqlite3_config()] with a first argument that is not an
** anytime configuration option in between calls to [sqlite3_initialize()] and
** [sqlite3_shutdown()] is a no-op that returns SQLITE_MISUSE.
**
** The set of anytime configuration options can change (by insertions
** and/or deletions) from one release of SQLite to the next.
** As of SQLite version 3.42.0, the complete set of anytime configuration
** options is:
** <ul>
** <li> SQLITE_CONFIG_LOG
**
** <li> SQLITE_CONFIG_PCACHE_HDRSZ
** </ul>
**
** New configuration options may be added in future releases of SQLite.
** Existing configuration options might be discontinued. Applications
** should check the return code from [sqlite3_config()] to make sure that
** the call worked. The [sqlite3_config()] interface will return a
** non-zero [error code] if a discontinued or unsupported configuration option
** is invoked.
**
** <dl>
** [[SQLITE_CONFIG_SINGLETHREAD]] <dt>SQLITE_CONFIG_SINGLETHREAD</dt>
** <dd>There are no arguments to this option. ^This option sets the
** [threading mode] to Single-thread. In other words, it disables
** all mutexing and puts SQLite into a mode where it can only be used
** by a single thread. ^If SQLite is compiled with
```

** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
 ** it is not possible to change the [threading mode] from its default
 ** value of Single-thread and so [sqlite3_config()] will return
 ** [SQLITE_ERROR] if called
 with the SQLITE_CONFIG_SINGLETHREAD
 configuration option.</dd>
 **
 ** [[SQLITE_CONFIG_MULTITHREAD]] <dt>SQLITE_CONFIG_MULTITHREAD</dt>
 ** <dd>There are no arguments to this option. ^This option sets the
 [threading mode] to Multi-thread. In other words, it disables
 mutexing on [database connection] and [prepared statement] objects.
 The application is responsible for serializing access to
 [database connections] and [prepared statements]. But other mutexes
 are enabled so that SQLite will be safe to use in a multi-threaded
 environment as long as no two threads attempt to use the same
 [database connection] at the same time. ^If SQLite is compiled with
 the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
 it is not possible to set the Multi-thread [threading mode] and
 [sqlite3_config()] will return [SQLITE_ERROR] if called with the
 SQLITE_CONFIG_MULTITHREAD configuration option.</dd>
 **
 ** [[SQLITE_CONFIG_SERIALIZED]] <dt>SQLITE_CONFIG_SERIALIZED</dt>
 **
 <dd>There are no arguments to this option. ^This option sets the
 [threading mode] to Serialized. In other words, this option enables
 all mutexes including the recursive
 mutexes on [database connection] and [prepared statement] objects.
 In this mode (which is the default when SQLite is compiled with
 [SQLITE_THREADSAFE=1]) the SQLite library will itself serialize access
 to [database connections] and [prepared statements] so that the
 application is free to use the same [database connection] or the
 same [prepared statement] in different threads at the same time.
 ^If SQLite is compiled with
 the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
 it is not possible to set the Serialized [threading mode] and
 [sqlite3_config()] will return [SQLITE_ERROR] if called with the
 SQLITE_CONFIG_SERIALIZED configuration option.</dd>
 **
 ** [[SQLITE_CONFIG_MALLOC]] <dt>SQLITE_CONFIG_MALLOC</dt>
 ** <dd> ^The SQLITE_CONFIG_MALLOC option
 takes a single argument which is
 a pointer to an instance of the [sqlite3_mem_methods] structure.
 The argument specifies
 alternative low-level memory allocation routines to be used in place of
 the memory allocation routines built into SQLite.)^ ^SQLite makes
 its own private copy of the content of the [sqlite3_mem_methods] structure
 before the [sqlite3_config()] call returns.</dd>
 **

SQLITE_CONFIG_GETMALLOC `<dt>SQLITE_CONFIG_GETMALLOC</dt>`
<dd> `^(The SQLITE_CONFIG_GETMALLOC option takes a single argument which`
is a pointer to an instance of the [sqlite3_mem_methods] structure.
The [sqlite3_mem_methods]
structure is filled with the currently defined memory allocation routines.)^
This option can be used to overload the default memory allocation
routines with a wrapper that simulations memory allocation failure or
tracks memory usage, for example. </dd>

SQLITE_CONFIG_SMALL_MALLOC `<dt>SQLITE_CONFIG_SMALL_MALLOC</dt>`
<dd> `^The SQLITE_CONFIG_SMALL_MALLOC`
option takes single argument of
type int, interpreted as a boolean, which if true provides a hint to
SQLite that it should avoid large memory allocations if possible.
SQLite will run faster if it is free to make large memory allocations,
but some application might prefer to run slower in exchange for
guarantees about memory fragmentation that are possible if large
allocations are avoided. This hint is normally off.
</dd>

SQLITE_CONFIG_MEMSTATUS `<dt>SQLITE_CONFIG_MEMSTATUS</dt>`
<dd> `^The SQLITE_CONFIG_MEMSTATUS option takes single argument of type int,`
interpreted as a boolean, which enables or disables the collection of
memory allocation statistics. ^When memory allocation statistics are
disabled, the following SQLite interfaces become non-operational:

** [sqlite3_hard_heap_limit64()]**
** [sqlite3_memory_used()]**
** [sqlite3_memory_highwater()]**
** [sqlite3_soft_heap_limit64()]**
** [sqlite3_status64()]**
)^
^Memory allocation statistics are enabled by default unless SQLite is
compiled with [SQLITE_DEFAULT_MEMSTATUS]=0 in which case memory
allocation statistics are disabled by default.
</dd>

SQLITE_CONFIG_SCRATCH `<dt>SQLITE_CONFIG_SCRATCH</dt>`
<dd> `The SQLITE_CONFIG_SCRATCH option is no longer used.`
</dd>

SQLITE_CONFIG_PAGECACHE `<dt>SQLITE_CONFIG_PAGECACHE</dt>`
<dd> `^The SQLITE_CONFIG_PAGECACHE option specifies a memory pool`
that SQLite can use for the database page cache with the default page
cache implementation.
This configuration option is a no-op if an application-defined page
cache implementation is loaded using the [SQLITE_CONFIG_PCACHE2].

** ^There are three arguments to SQLITE_CONFIG_PAGECACHE: A pointer to
 ** 8-byte aligned memory (pMem), the size of each page cache line (sz),
 ** and the number of cache lines (N).
 ** The sz argument should be the size of the largest database page
 ** (a power
 of two between 512 and 65536) plus some extra bytes for each
 ** page header. ^The number of extra bytes needed by the page header
 ** can be determined using [SQLITE_CONFIG_PCACHE_HDRSZ].
 ** ^It is harmless, apart from the wasted memory,
 ** for the sz parameter to be larger than necessary. The pMem
 ** argument must be either a NULL pointer or a pointer to an 8-byte
 ** aligned block of memory of at least sz*N bytes, otherwise
 ** subsequent behavior is undefined.
 ** ^When pMem is not NULL, SQLite will strive to use the memory provided
 ** to satisfy page cache needs, falling back to [sqlite3_malloc()] if
 ** a page cache line is larger than sz bytes or if all of the pMem buffer
 ** is exhausted.
 ** ^If pMem is NULL and N is non-zero, then each database connection
 ** does an initial bulk allocation for page cache memory
 ** from [sqlite3_malloc()] sufficient for N cache lines if N is positive or
 ** of -1024*N bytes if N is negative, . ^If additional
 ** page cache memory is needed beyond
 what is provided by the initial
 ** allocation, then SQLite goes to [sqlite3_malloc()] separately for each
 ** additional cache line. </dd>
 **
 ** [[SQLITE_CONFIG_HEAP]] <dt>SQLITE_CONFIG_HEAP</dt>
 ** <dd> ^The SQLITE_CONFIG_HEAP option specifies a static memory buffer
 ** that SQLite will use for all of its dynamic memory allocation needs
 ** beyond those provided for by [SQLITE_CONFIG_PAGECACHE].
 ** ^The SQLITE_CONFIG_HEAP option is only available if SQLite is compiled
 ** with either [SQLITE_ENABLE_MEMSYS3] or [SQLITE_ENABLE_MEMSYS5] and returns
 ** [SQLITE_ERROR] if invoked otherwise.
 ** ^There are three arguments to SQLITE_CONFIG_HEAP:
 ** An 8-byte aligned pointer to the memory,
 ** the number of bytes in the memory buffer, and the minimum allocation size.
 ** ^If the first pointer (the memory pointer) is NULL, then SQLite reverts
 ** to using its default memory allocator (the system malloc() implementation),
 ** undoing any prior invocation of [SQLITE_CONFIG_MALLOC]. ^If the
 ** memory pointer
 is not NULL then the alternative memory
 ** allocator is engaged to handle all of SQLites memory allocation needs.
 ** The first pointer (the memory pointer) must be aligned to an 8-byte
 ** boundary or subsequent behavior of SQLite will be undefined.
 ** The minimum allocation size is capped at 2**12. Reasonable values
 ** for the minimum allocation size are 2**5 through 2**8.</dd>
 **
 ** [[SQLITE_CONFIG_MUTEX]] <dt>SQLITE_CONFIG_MUTEX</dt>

** <dd> ^The SQLITE_CONFIG_MUTEX option takes a single argument which is a
 ** pointer to an instance of the [sqlite3_mutex_methods] structure.
 ** The argument specifies alternative low-level mutex routines to be used
 ** in place the mutex routines built into SQLite.)^ ^SQLite makes a copy of
 ** the content of the [sqlite3_mutex_methods] structure before the call to
 ** [sqlite3_config()] returns. ^If SQLite is compiled with
 ** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
 ** the entire mutexing subsystem is omitted from the
 build and hence calls to
 ** [sqlite3_config()] with the SQLITE_CONFIG_MUTEX configuration option will
 ** return [SQLITE_ERROR].</dd>
 **
 ** [[SQLITE_CONFIG_GETMUTEX]] <dt>SQLITE_CONFIG_GETMUTEX</dt>
 ** <dd> ^The SQLITE_CONFIG_GETMUTEX option takes a single argument which
 ** is a pointer to an instance of the [sqlite3_mutex_methods] structure. The
 ** [sqlite3_mutex_methods]
 ** structure is filled with the currently defined mutex routines.)^
 ** This option can be used to overload the default mutex allocation
 ** routines with a wrapper used to track mutex usage for performance
 ** profiling or testing, for example. ^If SQLite is compiled with
 ** the [SQLITE_THREADSAFE | SQLITE_THREADSAFE=0] compile-time option then
 ** the entire mutexing subsystem is omitted from the build and hence calls to
 ** [sqlite3_config()] with the SQLITE_CONFIG_GETMUTEX configuration option will
 ** return [SQLITE_ERROR].</dd>
 **
 ** [[SQLITE_CONFIG_LOOKASIDE]] <dt>SQLITE_CONFIG_LOOKASIDE</dt>
 ** <dd> ^The SQLITE_CONFIG_LOOKASIDE
 option takes two arguments that determine
 ** the default size of lookaside memory on each [database connection].
 ** The first argument is the
 ** size of each lookaside buffer slot and the second is the number of
 ** slots allocated to each database connection.)^ ^SQLITE_CONFIG_LOOKASIDE
 ** sets the <i>default</i> lookaside size. The [SQLITE_DBCONFIG_LOOKASIDE]
 ** option to [sqlite3_db_config()] can be used to change the lookaside
 ** configuration on individual connections.)^ </dd>
 **
 ** [[SQLITE_CONFIG_PCACHE2]] <dt>SQLITE_CONFIG_PCACHE2</dt>
 ** <dd> ^The SQLITE_CONFIG_PCACHE2 option takes a single argument which is
 ** a pointer to an [sqlite3_pcache_methods2] object. This object specifies
 ** the interface to a custom page cache implementation.)^
 ** ^SQLite makes a copy of the [sqlite3_pcache_methods2] object.</dd>
 **
 ** [[SQLITE_CONFIG_GETPCACHE2]] <dt>SQLITE_CONFIG_GETPCACHE2</dt>
 ** <dd> ^The SQLITE_CONFIG_GETPCACHE2 option takes a single argument which
 ** is
 a pointer to an [sqlite3_pcache_methods2] object. SQLite copies of
 ** the current page cache implementation into that object.)^ </dd>
 **

SQLITE_CONFIG_LOG `<dt>SQLITE_CONFIG_LOG</dt>`
<dd> The `SQLITE_CONFIG_LOG` option is used to configure the SQLite global [error log].
 ^The `SQLITE_CONFIG_LOG` option takes two arguments: a pointer to a function with a call signature of `void(*)(void*,int,const char*)`, and a pointer to void. ^If the function pointer is not NULL, it is invoked by `[sqlite3_log()]` to process each logging event. ^If the function pointer is NULL, the `[sqlite3_log()]` interface becomes a no-op.
 ^The void pointer that is the second argument to `SQLITE_CONFIG_LOG` is passed through as the first parameter to the application-defined logger function whenever that function is invoked. ^The second parameter to the logger function is a copy of the first parameter to the corresponding `[sqlite3_log()]` call and is intended to be a [result code] or an [extended result code]. ^The third parameter passed to the logger is log message after formatting via `[sqlite3_snprintf()]`.
 The SQLite logging interface is not reentrant; the logger function supplied by the application must not invoke any SQLite interface.
 In a multi-threaded application, the application-defined logger function must be threadsafe. **</dd>**

SQLITE_CONFIG_URI `<dt>SQLITE_CONFIG_URI`
<dd>^The `SQLITE_CONFIG_URI` option takes a single argument of type int. If non-zero, then URI handling is globally enabled. If the parameter is zero, then URI handling is globally disabled.)^ ^If URI handling is globally enabled, all filenames passed to `[sqlite3_open()]`, `[sqlite3_open_v2()]`, `[sqlite3_open16()]` or specified as part of `[ATTACH]` commands are interpreted as URIs, regardless of whether or not the `[SQLITE_OPEN_URI]` flag is set when the database connection is opened. ^If it is globally disabled, filenames are only interpreted as URIs if the `SQLITE_OPEN_URI` flag is set when the database connection is opened. ^By default, URI handling is globally disabled. The default value may be changed by compiling with the `[SQLITE_USE_URI]` symbol defined.)^

SQLITE_CONFIG_COVERING_INDEX_SCAN `<dt>SQLITE_CONFIG_COVERING_INDEX_SCAN`
<dd>^The `SQLITE_CONFIG_COVERING_INDEX_SCAN` option takes a single integer argument which is interpreted as a boolean in order to enable or disable the use of covering indices for full table scans in the query optimizer.
 ^The default setting is determined by the `[SQLITE_ALLOW_COVERING_INDEX_SCAN]` compile-time option, or is "on" if that compile-time option is omitted.
 The ability to disable the use of covering indices for full table scans is because some incorrectly coded legacy applications might malfunction when the optimization is enabled. Providing the ability to disable the optimization allows the older, buggy application code to work without change

even with newer versions of SQLite.

**

** [[SQLITE_CONFIG_PCACHE]] [[SQLITE_CONFIG_GETPCACHE]]

** <dt>SQLITE_CONFIG_PCACHE and SQLITE_CONFIG_GETPCACHE

** <dd> These options are obsolete and should not be used by new code.

** They are retained for backwards compatibility but are now no-ops.

** </dd>

**

** [[SQLITE_CONFIG_SQLLOG]]

** <dt>SQLITE_CONFIG_SQLLOG

** <dd>This option is only available if sqlite is compiled with the

** [SQLITE_ENABLE_SQLLOG] pre-processor macro defined. The first argument should

** be a pointer to a function of type void(*)(void*,sqlite3*,const char*, int).

** The second should be of type (void*). The callback is invoked by the library

** in three separate circumstances, identified by the value passed as the

** fourth parameter. If the fourth parameter is 0, then the database connection

** passed as the second argument has just been opened. The third argument

** points to a buffer containing the name of the main database file. If the

** fourth parameter is 1,

then the SQL statement that the third parameter

** points to has just been executed. Or, if the fourth parameter is 2, then

** the connection being passed as the second parameter is being closed. The

** third parameter is passed NULL In this case. An example of using this

** configuration option can be seen in the "test_sqllog.c" source file in

** the canonical SQLite source tree.</dd>

**

** [[SQLITE_CONFIG_MMAP_SIZE]]

** <dt>SQLITE_CONFIG_MMAP_SIZE

** <dd>^SQLITE_CONFIG_MMAP_SIZE takes two 64-bit integer (sqlite3_int64) values

** that are the default mmap size limit (the default setting for

** [PRAGMA mmap_size]) and the maximum allowed mmap size limit.

** ^The default setting can be overridden by each database connection using

** either the [PRAGMA mmap_size] command, or by using the

** [SQLITE_FCNTL_MMAP_SIZE] file control. ^The maximum allowed mmap size

** will be silently truncated if necessary so that it does not exceed the

** compile-time maximum mmap size set by the

** [SQLITE_MAX_MMAP_SIZE]

compile-time option.)^

** ^If either argument to this option is negative, then that argument is

** changed to its compile-time default.

**

** [[SQLITE_CONFIG_WIN32_HEAPSIZE]]

** <dt>SQLITE_CONFIG_WIN32_HEAPSIZE

** <dd>^The SQLITE_CONFIG_WIN32_HEAPSIZE option is only available if SQLite is

** compiled for Windows with the [SQLITE_WIN32_MALLOC] pre-processor macro

** defined. ^SQLITE_CONFIG_WIN32_HEAPSIZE takes a 32-bit unsigned integer value

** that specifies the maximum size of the created heap.

**

**** [[SQLITE_CONFIG_PCACHE_HDRSZ]]**
**** <dt>SQLITE_CONFIG_PCACHE_HDRSZ**
**** <dd>^The SQLITE_CONFIG_PCACHE_HDRSZ option takes a single parameter which**
**** is a pointer to an integer and writes into that integer the number of extra**
**** bytes per page required for each page in [SQLITE_CONFIG_PAGECACHE].**
**** The amount of extra space required can change depending on the compiler,**
**** target platform, and SQLite version.**

**** [[SQLITE_CONFIG_PMASZ]]**
**** <dt>SQLITE_CONFIG_PMASZ**
**** <dd>^The**
SQLITE_CONFIG_PMASZ option takes a single parameter which
**** is an unsigned integer and sets the "Minimum PMA Size" for the multithreaded**
**** sorter to that integer. The default minimum PMA Size is set by the**
**** [SQLITE_SORTER_PMASZ] compile-time option. New threads are launched**
**** to help with sort operations when multithreaded sorting**
**** is enabled (using the [PRAGMA threads] command) and the amount of content**
**** to be sorted exceeds the page size times the minimum of the**
**** [PRAGMA cache_size] setting and this value.**

**** [[SQLITE_CONFIG_STMTJRNL_SPILL]]**
**** <dt>SQLITE_CONFIG_STMTJRNL_SPILL**
**** <dd>^The SQLITE_CONFIG_STMTJRNL_SPILL option takes a single parameter which**
**** becomes the [statement journal] spill-to-disk threshold.**
**** [Statement journals] are held in memory until their size (in bytes)**
**** exceeds this threshold, at which point they are written to disk.**
**** Or if the threshold is -1, statement journals are always held**
**** exclusively in memory.**
**** Since many statement journals**
never become large, setting the spill
**** threshold to a value such as 64KiB can greatly reduce the amount of**
**** I/O required to support statement rollback.**
**** The default value for this setting is controlled by the**
**** [SQLITE_STMTJRNL_SPILL] compile-time option.**

**** [[SQLITE_CONFIG_SORTERREF_SIZE]]**
**** <dt>SQLITE_CONFIG_SORTERREF_SIZE**
**** <dd>The SQLITE_CONFIG_SORTERREF_SIZE option accepts a single parameter**
**** of type (int) - the new value of the sorter-reference size threshold.**
**** Usually, when SQLite uses an external sort to order records according**
**** to an ORDER BY clause, all fields required by the caller are present in the**
**** sorted records. However, if SQLite determines based on the declared type**
**** of a table column that its values are likely to be very large - larger**
**** than the configured sorter-reference size threshold - then a reference**
**** is stored in each sorted record and the required column values loaded**
**** from the database as records are returned in sorted order.**
The default
**** value for this option is to never use this optimization. Specifying a**

```

** negative value for this option restores the default behavior.
** This option is only available if SQLite is compiled with the
** [SQLITE_ENABLE_SORTER_REFERENCES] compile-time option.
**
** [[SQLITE_CONFIG_MEMDB_MAXSIZE]]
** <dt>SQLITE_CONFIG_MEMDB_MAXSIZE
** <dd>The SQLITE_CONFIG_MEMDB_MAXSIZE option accepts a single parameter
** [sqlite3_int64] parameter which is the default maximum size for an in-memory
** database created using [sqlite3_deserialize()]. This default maximum
** size can be adjusted up or down for individual databases using the
** [SQLITE_FCNTL_SIZE_LIMIT] [sqlite3_file_control|file-control]. If this
** configuration setting is never used, then the default maximum is determined
** by the [SQLITE_MEMDB_DEFAULT_MAXSIZE] compile-time option. If that
** compile-time option is not set, then the default maximum is 1073741824.
** </dd>
** /
/*
** The "printf" code that follows dates
** from the 1980's. It is in
** the public domain.
**
*****
**
** This file contains code for a set of "printf"-like routines. These
** routines format strings much like the printf() from the standard C
** library, though the implementation here has enhancements to support
** SQLite.
** /
/*
** 2004 May 22
**
** The author disclaims copyright to this source code. In place of
** a legal notice, here is a blessing:
**
**   May you do good and not evil.
**   May you find forgiveness for yourself and forgive others.
**   May you share freely, never taking more than you give.
**
*****
**
** This file contains the VFS implementation for unix-like operating systems
** include Linux, MacOSX, *BSD, QNX, VxWorks, AIX, HPUX, and others.
**
** There are actually several different VFS implementations in this file.
** The differences are in the way that file
** locking is done. The default
** implementation uses Posix Advisory Locks. Alternative implementations
** use flock(), dot-files, various proprietary locking schemas, or simply

```

```

** skip locking all together.
**
** This source file is organized into divisions where the logic for various
** subfunctions is contained within the appropriate division. PLEASE
** KEEP THE STRUCTURE OF THIS FILE INTACT. New code should be placed
** in the correct division and should be clearly labelled.
**
** The layout of divisions is as follows:
**
** * General-purpose declarations and utility functions.
** * Unique file ID logic used by VxWorks.
** * Various locking primitive implementations (all except proxy locking):
**   + for Posix Advisory Locks
**   + for no-op locks
**   + for dot-file locks
**   + for flock() locking
**   + for named semaphore locks (VxWorks only)
**   + for AFP filesystem locks (MacOSX only)
** * sqlite3_file methods not associated with locking.
**
**   * Definitions of sqlite3_io_methods objects for all locking
**     methods plus "finder" functions for each locking method.
**   * sqlite3_vfs method implementations.
**   * Locking primitives for the proxy uber-locking-method. (MacOSX only)
**   * Definitions of sqlite3_vfs objects for all locking methods
**     plus implementations of sqlite3_os_init() and sqlite3_os_end().
**/
/*
** Return a pointer to the "temporary page" buffer held internally
** by the pager. This is a buffer that is big enough to hold the
** entire content of a database page. This buffer is used internally
** during rollback and will be overwritten whenever a rollback
** occurs. But other modules are free to use it too, as long as
** no rollbacks are happening.
**/

```

Found in path(s):

* /sqlite-amalgamation-3450200-zip/sqlite-amalgamation-3450200/sqlite3.c

1.68 nghttp2 1.61.0

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nit Testing Framework

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- mrbgems/mruby-dir/src/Win/dirent.c: MIT-like license by Kevlin Henney

[src/readfloat.c]

strtod implementation.

author: Yasuhiro Matsumoto (@mattn)

license: public domain

The original code can be found in <https://github.com/mattn/strtod>

[src/fmt_fp.c]

The code in this function was inspired from Fred Bayer's pdouble.c. Since pdouble.c was released as Public Domain, I'm releasing this code as public domain as well.

Dave Hylands

The original code can be found in <https://github.com/dhylands/format-float>

[mrbgems/mruby-dir/src/Win/dirent.c] used only for Windows platform

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But that said, if there are any problems please get in touch.

set yrange [0:]

set terminal pngcairo font 'Sans, 8' lw 1 size 1400,1024

set xtics rotate by -45

set style histogram errorbars gap 2 lw 1

set style fill solid border -1

mruby-set

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1.69 log4cplus 2.0.7

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1.77 openssl 3.4.0

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1.79 mono.options 6.12.0.148

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Program	Directory

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<none yet>

```
; RUN: llc < %s -mtriple=s390x-linux-gnu -mcpu=zEC12 -verify-machineinstrs | FileCheck %s
;
; Test that early if conversion produces LOCR with operands of the right
; register classes.
```

```
define void @autogen_SD4739(i8*) {
; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
BB:
  %L34 = load i8, i8* %0
  %Cmp56 = icmp sgt i8 undef, %L34
  br label %CF246
```

```
CF246:                                ; preds = %CF246, %BB
```

```
%S1163 = select i1 %Cmp56, i8 %L34, i8 undef
```

```
br i1 undef, label %CF246, label %CF248
```

```
CF248:                                ; preds = %CF248, %CF246
```

```
store i8 %S1163, i8* %0
```

```
br label %CF248
```

```
}
```

```
UNRECOGNIZED LICENSE; MD5 sum: 84d87aa33afd1f9ee9aca3a71424
```

```
=====
```

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=====

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- * gettext

m4 source files used to probe features at build time: GPL

- * Benchmark Source Files

Logic.cs and zipmark.cs are GPL source files.

- * mono/docs/HtmlAgilityPack

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- * mcs/jay: 4-clause BSD licensed

- * mcs/class/I18N/mklist.sh, tools/cvt.sh: GNU GPLv2

Runtime Code

=====

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- * support/minizip: BSD license.

- * mono/utls/memcheck.h: BSD license, used on debug builds that use Valgrind.

- * mono/utls/freebsd-dwarf.h, freebsd-elf_common.h, freebsd-elf64.h freebsd-elf32.h: BSD license.

- * mono/utls/bsearch.c: BSD license.

- * mono/metadata/w32file-unix-glob.c, w32file-unix-glob.h: BSD license

Class Library code

=====

These are class libraries that can be loaded by your process:

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* mcs/class/Compat.ICSharpCode.SharpZipLib and
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Originates with the SharpDevelop project.

* mcs/class/System.Core/System/TimeZoneInfo.Android.cs

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From: james.newtonking@gmail.com [mailto:james.newtonking@gmail.com] On Behalf Of James Newton-King
Sent: Tuesday, June 05, 2007 6:36 AM
To: Konstantin Triger
Subject: Re: Support request by Konstantin Triger for Json.NET

Hey Kosta

I think it would be awesome to use Json.NET in Mono for System.Web.Extensions.

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I can waive that statement for you and Mono. Would that be acceptable?

Regards,
James

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*/
; RUN: llc -march=hexagon < %s
; REQUIRES: asserts

; The two loads based on %struct.0, loading two different data types
; cause LSR to assume type "void" for the memory type. This would then
; cause an assert in isLegalAddressingMode. Make sure we no longer crash.

target triple = "hexagon"

%struct.0 = type { i8*, i8, %union.anon.0 }
%union.anon.0 = type { i8* }

define hidden fastcc void @fred() unnamed_addr #0 {
entry:
br i1 undef, label %while.end, label %while.body.lr.ph

while.body.lr.ph:                                ; preds = %entry
br label %while.body

while.body:                                       ; preds = %exit.2, %while.body.lr.ph
%lsr.iv = phi %struct.0* [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
switch i32 undef, label %exit [
  i32 1, label %sw.bb.i
  i32 2, label %sw.bb3.i
]

```

```

sw.bb.i:                                ; preds = %while.body
unreachable

sw.bb3.i:                               ; preds = %while.body
unreachable

exit:
                                ; preds = %while.body
switch i32 undef, label %exit.2 [
  i32 1, label %sw.bb.i17
  i32 2, label %sw.bb3.i20
]

sw.bb.i17:                             ; preds = %exit
%0 = bitcast %struct.0* %lsr.iv to i32*
%1 = load i32, i32* %0, align 4
unreachable

sw.bb3.i20:                            ; preds = %exit
%2 = bitcast %struct.0* %lsr.iv to i8**
%3 = load i8*, i8** %2, align 4
unreachable

exit.2:                                ; preds = %exit
%cgep22 = getelementptr %struct.0, %struct.0* %lsr.iv, i32 1
br label %while.body

while.end:                              ; preds = %entry
ret void
}

```

attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }

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```
; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s
```

```
define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {  
; CHECK-LABEL: test_sitofp_fixed:
```

```
    ; First, extend each i32 to i64  
; CHECK-DAG: sshll2.2d [[BLOCK0_HI:v[0-9]+]], v0, #0  
; CHECK-DAG: sshll2.2d [[BLOCK1_HI:v[0-9]+]], v1, #0  
; CHECK-DAG: sshll2.2d [[BLOCK2_HI:v[0-9]+]], v2, #0  
; CHECK-DAG: sshll2.2d [[BLOCK3_HI:v[0-9]+]], v3, #0  
; CHECK-DAG: sshll.2d [[BLOCK0_LO:v[0-9]+]], v0, #0  
; CHECK-DAG: sshll.2d [[BLOCK1_LO:v[0-9]+]], v1, #0  
; CHECK-DAG: sshll.2d [[BLOCK2_LO:v[0-9]+]], v2, #0  
; CHECK-DAG: sshll.2d [[BLOCK3_LO:v[0-9]+]], v3, #0
```

```
    ; Next, convert each to double.  
; CHECK-DAG: scvtf.2d v0, [[BLOCK0_LO]]  
; CHECK-DAG: scvtf.2d v1, [[BLOCK0_HI]]  
; CHECK-DAG: scvtf.2d v2, [[BLOCK1_LO]]  
; CHECK-DAG: scvtf.2d v3, [[BLOCK1_HI]]  
; CHECK-DAG: scvtf.2d v4, [[BLOCK2_LO]]  
; CHECK-DAG: scvtf.2d v5, [[BLOCK2_HI]]  
; CHECK-DAG: scvtf.2d v6, [[BLOCK3_LO]]  
; CHECK-DAG: scvtf.2d v7, [[BLOCK3_HI]]
```

```
; CHECK: ret
%flt = sitofp <16 x i32>
%in to <16 x double>
%res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0,
double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0>
ret <16 x double> %res
}
```

; This one is small enough to satisfy isSimple, but still illegally large.

```
define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
```

```
; CHECK-LABEL: test_sitofp_fixed_shortish:
```

```
; CHECK-DAG: scvtf.2d v0, v0
```

```
; CHECK-DAG: scvtf.2d v1, v1
```

```
; CHECK: ret
```

```
%flt = sitofp <4 x i64> %in to <4 x double>
```

```
%res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
```

```
ret <4 x double> %res
```

```
}
```

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```
new XElement("TITLE", "The Tragedy of Hamlet, Prince of Denmark"),
```

```
new XElement("fm",
```

```
    new XElement("p", "Text placed in the public domain by Moby Lexical Tools, 1992."),
```

```
    new XElement("p", "SGML markup by Jon Bosak, 1992-1994."),
```

```
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```

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```

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Newtonsoft.Json 6.0.4

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/* zlib.h -- interface of the 'zlib' general purpose compression library
version 1.2.11, January 15th, 2017

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```
add_lldb_library(lldbPluginObjectContainerBSDArchive PLUGIN
ObjectContainerBSDArchive.cpp
```

```
LINK_LIBS
```

```
    lldbCore
```

```
    lldbHost
```

```
    lldbSymbol
```

```
LINK_COMPONENTS
```

```
    Support
```

```
)
```

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By Sean Eron Anderson
seander@cs.stanford.edu

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; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s

;

; D31946

; Check that we dont end up with the ""LLVM ERROR: Cannot select" error.

; Additionally ensure that the output code actually put fp128 values in SSE registers.

declare fp128 @llvm.fabs.f128(fp128)

declare fp128 @llvm.copysign.f128(fp128, fp128)

define fp128 @TestSelect(fp128 %a, fp128 %b) {

 %cmp = fcmp ogt fp128 %a, %b

 %sub = fsub fp128 %a, %b

 %res = select i1 %cmp, fp128 %sub, fp128 0xL00000000000000000000000000000000

 ret fp128 %res

; CHECK-LABEL: TestSelect:

; CHECK movaps 16(%rsp), %xmm1

; CHECK-NEXT callq __subtf3

; CHECK-NEXT testl %ebx, %ebx

; CHECK-NEXT jg .LBB0_2

; CHECK-NEXT # %bb.1:

; CHECK-NEXT movaps .LCPI0_0(%rip), %xmm0

; CHECK-NEXT .LBB0_2:

; CHECK-NEXT addq \$32, %rsp

; CHECK-NEXT popq %rbx

; CHECK-NEXT retq

}

define fp128 @TestFabs(fp128 %a) {

 %res = call fp128 @llvm.fabs.f128(fp128 %a)

 ret fp128 %res

; CHECK-LABEL: TestFabs:

;

 CHECK andps .LCPI1_0(%rip), %xmm0

; CHECK-NEXT retq

```

}

define fp128 @TestCopysign(fp128 %a, fp128 %b) {
    %res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
    ret fp128 %res
; CHECK-LABEL: TestCopysign:
; CHECK    andps .LCPI2_1(%rip), %xmm0
; CHECK-NEXT orps %xmm1, %xmm0
; CHECK-NEXT retq
}

define fp128 @TestFneg(fp128 %a) {
    %mul = fmul fp128 %a, %a
    %res = fsub fp128 0xL00000000000000008000000000000000, %mul
    ret fp128 %res
; CHECK-LABEL: TestFneg:
; CHECK    movaps %xmm0, %xmm1
; CHECK-NEXT callq __multf3
; CHECK-NEXT xorps .LCPI3_0(%rip), %xmm0
; CHECK-NEXT popq %rax
; CHECK-NEXT retq
}

```

1.80 gflags 2.2.2

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1.81 curl 8.11.0

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1.82 curl 8.10.1

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1.83 boost 1.84

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*/

#ifndef BOOST_PREDEF_OS_BSD_H

#define BOOST_PREDEF_OS_BSD_H

/* Special case: OSX will define BSD predefs if the sys/param.h

* header is included. We can guard against that, but only if we

* detect OSX first. Hence we will force include OSX detection

* before doing any BSD detection.

*/

#include <boost/predef/os/macos.h>

#include <boost/predef/version_number.h>

#include <boost/predef/make.h>

/* tag::reference[]

= `BOOST\_OS\_BSD`

http://en.wikipedia.org/wiki/Berkeley_Software_Distribution[BSD] operating system.

BSD has various branch operating systems possible and each detected individually. This detects the following variations and sets a specific version number macro to match:

* `BOOST\_OS\_BSD\_DRAGONFLY` http://en.wikipedia.org/wiki/DragonFly_BSD[DragonFly BSD]

* `BOOST\_OS\_BSD\_FREE` <http://en.wikipedia.org/wiki/Freebsd>[FreeBSD]

*

`BOOST\_OS\_BSD\_BSDI` <http://en.wikipedia.org/wiki/BSD/OS>[BSDi BSD/OS]

* `BOOST\_OS\_BSD\_NET` <http://en.wikipedia.org/wiki/Netbsd>[NetBSD]

* `BOOST\_OS\_BSD\_OPEN` <http://en.wikipedia.org/wiki/Openbsd>[OpenBSD]

NOTE: The general `BOOST\_OS\_BSD` is set in all cases to indicate some form of BSD. If the above variants is detected the corresponding macro is also set.

```

[options="header"]
|===
| {predef_symbol} | {predef_version}

| `BSD` | {predef_detection}
| `+_SYSTYPE_BSD+` | {predef_detection}

| `BSD4_2` | 4.2.0
| `BSD4_3` | 4.3.0
| `BSD4_4` | 4.4.0
| `BSD` | V.R.0
|===
*/ // end::reference[]

#include <boost/predef/os/bsd/bsdi.h>
#include <boost/predef/os/bsd/dragonfly.h>
#include <boost/predef/os/bsd/free.h>
#include <boost/predef/os/bsd/open.h>
#include <boost/predef/os/bsd/net.h>

#ifndef BOOST_OS_BSD
#define BOOST_OS_BSD BOOST_VERSION_NUMBER_NOT_AVAILABLE
#endif

#if !defined(BOOST_PREDEF_DETAIL_OS_DETECTED) && ( \
    defined(BSD) || \
    defined(_SYSTYPE_BSD) \
)
# undef BOOST_OS_BSD
# include <sys/param.h>
# if !defined(BOOST_OS_BSD) && defined(BSD4_4)
#   define BOOST_OS_BSD BOOST_VERSION_NUMBER(4,4,0)
# endif
# if !defined(BOOST_OS_BSD) && defined(BSD4_3)
#   define BOOST_OS_BSD BOOST_VERSION_NUMBER(4,3,0)
# endif
# if !defined(BOOST_OS_BSD) && defined(BSD4_2)
#   define BOOST_OS_BSD BOOST_VERSION_NUMBER(4,2,0)
# endif
# if !defined(BOOST_OS_BSD) && defined(BSD)
#   define BOOST_OS_BSD BOOST_PREDEF_MAKE_10_VVRR(BSD)
# endif
# if !defined(BOOST_OS_BSD)
#   define BOOST_OS_BSD BOOST_VERSION_NUMBER_AVAILABLE
# endif
#endif

```

```

#if BOOST_OS_BSD
# define BOOST_OS_BSD_AVAILABLE
# include <boost/predef/detail/os_detected.h>
#endif

#define BOOST_OS_BSD_NAME "BSD"

#endif

#include <boost/predef/os/bsd/bsdi.h>
#include <boost/predef/os/bsd/dragonfly.h>
#include <boost/predef/os/bsd/free.h>
#include <boost/predef/os/bsd/open.h>
#include <boost/predef/os/bsd/net.h>

#include <boost/predef/detail/test.h>
BOOST_PREDEF_DECLARE_TEST(BOOST_OS_BSD,BOOST_OS_BSD_NAME)

```

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Julian Seward, jseward@acm.org
bzip2/libbzip2 version 1.0.8 of 13 July 2019

////

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////

```
[#mpl]
# MPL Support, <boost/mp11/mpl.hpp>
:toc:
:toc-title:
:idprefix:
```

The header `<boost/mp11/mpl.hpp>`, when included, defines the necessary support infrastructure for `mp_list` and `std::tuple` to be valid link:../../../../libs/mpl[MPL] sequences.

NOTE: `mpl.hpp` is not included by `<boost/mp11.hpp>`.

It's also possible to only enable support for `mp_list` by including `<boost/mp11/mpl_list.hpp>`, and for `std::tuple` by including `<boost/mp11/mpl_tuple.hpp>`. This may be required because some libraries, such as Boost.Fusion, contain their own MPL support for `std::tuple`, which conflicts with Mp11's one.

.Converting an existing MPL Sequence into an `mp_list`
...

```
using L = mpl::copy<Sequence, mpl::back_inserter<mp11::mp_list<>>>::type;
...
```

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<html>

<head></head>

<body>

<h3>

Copyright Test

</h3>

<p class="copyright">

1963, 1964, 1965 Jane Doe

```
</p>
<p class="copyright">
  2018 Joe Blow, John Coe
</p>
<p class="copyright">
  1977, 1985 Someone else
</p>
</body>
</html>
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```
<?xml version="1.0" encoding="UTF-8"?>
<!DOCTYPE article PUBLIC "-//Boost/DTD BoostBook XML V1.0//EN"
"http://www.boost.org/tools/boostbook/dtd/boostbook.dtd">
<article id="copyright_test" last-revision="DEBUG MODE Date: 2000/12/20 12:00:00 $"
xmlns:xi="http://www.w3.org/2001/XInclude">
  <title>Copyright Test</title>
  <articleinfo>
    <copyright>
      <year>1963</year> <year>1964</year> <year>1965</year> <holder>Jane Doe</holder>
    </copyright>
    <copyright>
      <year>2018</year> <holder>Joe Blow, John Coe</holder>
    </copyright>
    <copyright>
      <year>1977</year> <year>1985</year> <holder>Someone else</holder>
    </copyright>
  </articleinfo>
</article>
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```

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