Cisco UCS Intel M8 Memory Guide

CISCO SYSTEMS
170 WEST TASMAN DR
SAN JOSE, CA, 95134
WWW.CISCO.COM

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CONTENTS

Introduction

The Intel M8 Memory guide provides the detailed specifications of the M8 memory DIMMs including:

- Memory DIMMs features
- Cisco PID's description
- Memory DIMMs guidelines, mixing rules and populations
- All M8 supported DIMM configurations

The Intel M8 Memory Guide document applies to the following Cisco Intel M8 generation servers:

- Intel M8 C220/C240 Racks servers
- Intel M8 X-series X210c/X410c Compute nodes

CHAPTER 1 MEMORY ORGANIZATION CAPABILITIES AND FEATURE

The *Table 1.0* and *Table 1.1* below describes the main memory DIMM and MRDIMM features supported on Cisco UCS Intel M8 servers.

Table 1.0 Main Memory Features for RDIMM

Intel M8 Memory DIMM Server Technologies	C220 M8	C240 M8	X210c M8	X410c M8
CPU Sockets	**1S or 2S**	**1S or 2S**	**1S or 2S**	**4S**
DDR5 memory clock speed	Intel® Xeon® 6 CPUs: Up to 6400 MT/s 1DPC; Up to 5200 MT/s 2DPC			
Operational voltage	1.1 Volts			
DRAM fab density	16Gb, 24Gb, and 32Gb			
DRAM DIMM type	RDIMM (Registered DDR5 DIMM)			
Memory DIMM organization	Eight memory DIMM channels per CPU; up to 2 DIMMs per channel			
Maximum number of DRAM DIMM per server	32 (2-Socket)			64 (4-Socket)
DRAM DIMM densities and ranks	16GB 1Rx8[1], 32GB 1Rx4, 48GB 1Rx4			N/A
	64GB 2Rx4, 96GB 2Rx4, 128GB 2Rx4, 256GB 4Rx4			
Maximum DRAM DIMMs system capacity	8TB (32x256GB)			16TB (64x256GB)

Notes:

1. SDDC and ADDDC RAS features are unsupported with x8 DIMMs. Therefore, 16GB 1Rx8 doesn't support SDDC and ADDDC RAS features.

NOTE: Intel® Xeon® 6 SKUs 6787P, 6781P, 6767P, 6761P, and 6747P support MRDIMM, Per Intel® Xeon® 6 documentation

Table 1.1 Main Memory Features for MRDIMM

Intel M8 Memory MRDIMM Server Technologies	C220 M8	C240 M8	X210c M8	X410c M8
CPU Sockets	**1S or 2S**	**1S or 2S**	**1S or 2S**	**4S**
DDR5 memory clock speed	Intel® Xeon® 6 CPUs: Up to 8000 MT/s 1DPC			N/A
Operational voltage	1.1 Volts			N/A
DRAM fab density	16Gb			N/A
MRDIMM type	MRDIMM (Multiplexed Rank DDR5 DIMM)			N/A
Memory MRDIMM organization	Eight MRDIMM channels per CPU; up to 1 DPC per channel			N/A
Maximum number of MRDIMM per server	16 (2-Socket)			N/A
MRDIMM densities and ranks	32GB 2Rx8, 64GB 2Rx4			N/A
Maximum MRDIMM system capacity	1TB (16x64GB)			N/A

Figure 1 2-socket memory organization

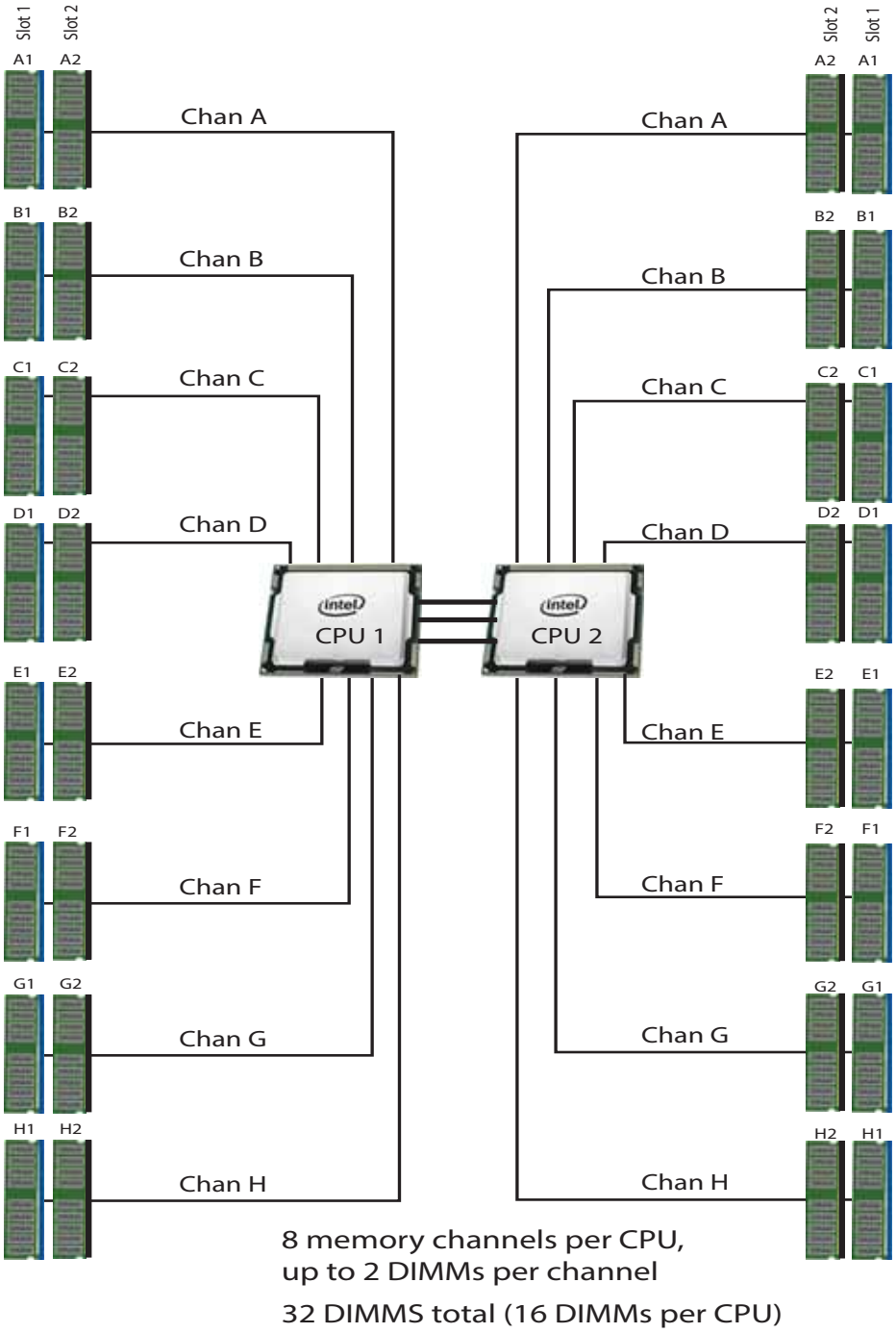
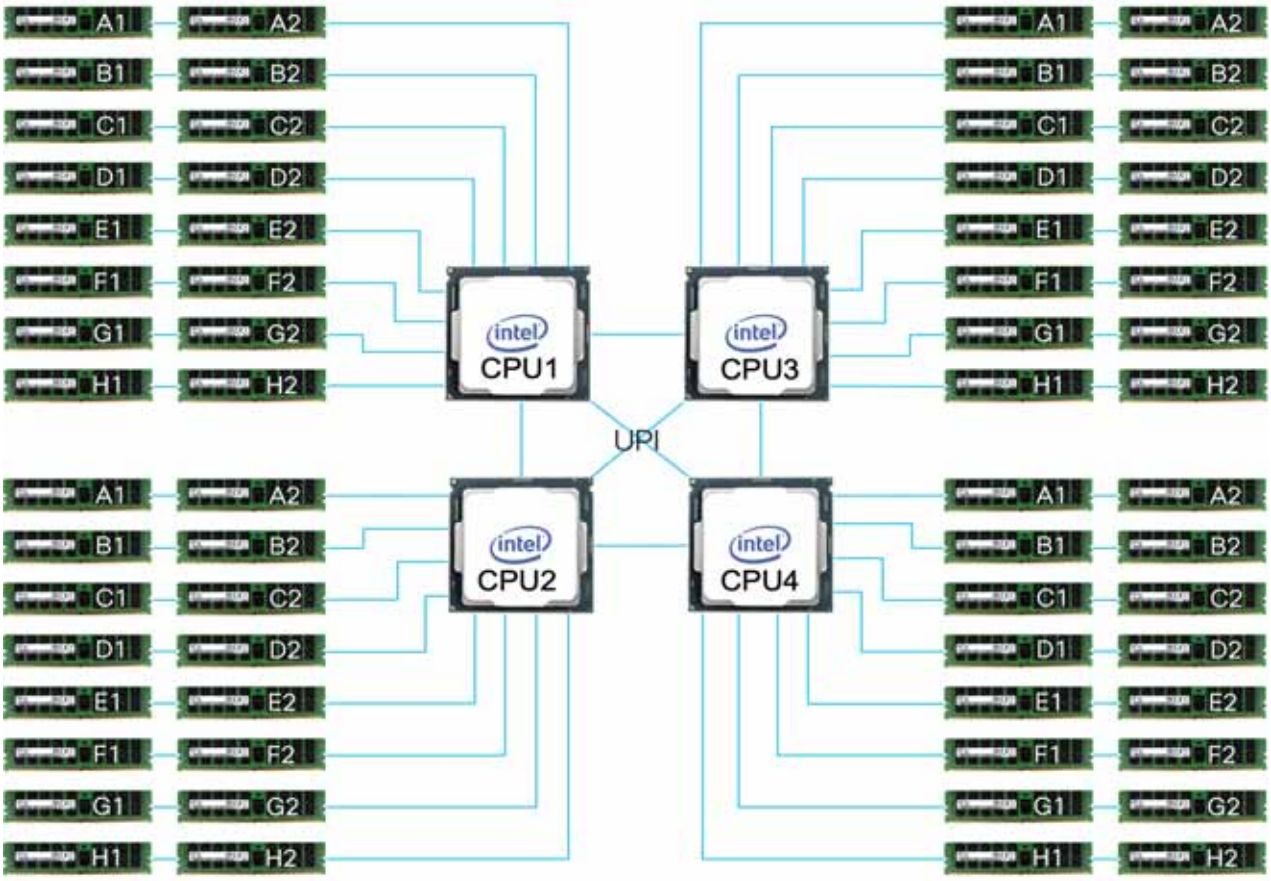


Figure 2 4-socket memory organization



CHAPTER 2 MEMORY OPTIONS

- The available memory devices for UCS and X-series M8 Servers are listed in *Table 2*.**0** and *Table 2*.**1**
- The memory PID decoder for Intel M8 Memory PIDs are shown in *Table 2*.**2**.

NOTE: Review the appropriate platform spec sheets for additional 256GB DIMM usage conditions.

CAUTION:

- On C240 M8, 256GB DIMMs cannot be combined with GPU cards and the ambient temperature shall be limited to a maximum of 28°C.
- On X210c M8, when populating 256GB DIMMs, the ambient temperature shall be limited to a maximum of 32°C.
- On X410c M8, when populating 256GB DIMMs, the ambient temperature shall be limited to a maximum of 32°C.

Table 2.0 Memory Options for UCS Intel M8 servers

Intel M8 Memory DIMM Densities & Cisco PIDs	Memory DIMM Description	C220 M8	C240 M8	X210c M8	X410c M8
DDR5-6400 MT/s Cisco Memory PIDs list					
16GB	16GB RDIMM 1Rx8 1.1Volts (16Gb)	UCS-MRX16G1RE5		UCSX-MRX16G1RE5	N/A
32GB	32GB RDIMM 1Rx4 1.1Volts (16Gb)	UCS-MRX32G1RE5		UCSX-MRX32G1RE5	N/A
48GB	48GB RDIMM 1Rx4 1.1Volts (24Gb)	UCS-MRX48G1RF5		UCSX-MRX48G1RF5	N/A
64GB	64GB RDIMM 2Rx4 1.1Volts (16Gb)	UCS-MRX64G2RE5		UCSX-MRX64G2RE5	
96GB	96GB RDIMM 2Rx4 1.1Volts (24Gb)	UCS-MRX96G2RF5		UCSX-MRX96G2RF5	
128GB	128GB RDIMM 2Rx4 1.1Volts (32Gb)	UCS-MR128G2RG5		UCSX-MR128G2RG5	
256GB	256GB RDIMM 4Rx4 1.1Volts (32Gb)	UCS-MR256G4RG5		UCSX-MR256G4RG5	

Table 2.1 MR (Multiplexed Rank) DIMMs Memory Options for UCS Intel M8 servers[1,2]

Intel M8 Memory DIMM Densities & Cisco PIDs[3]	Memory DIMM Description	C220 M8	C240 M8	X210c M8	X410c M8
DDR5 MRDIMM-8800 MT/s Cisco Memory PIDs list					
MRDIMM 32GB	32GB DDR5 MRDIMM 8800 2Rx8 (16Gb)	UCS-MCX32G2RE11		UCSX-MCX32G2RE11	N/A
MRDIMM 64GB	64GB DDR5 MRDIMM 8800 2Rx4 (16Gb)	UCS-MCX64G2RE11		UCSX-MCX64G2RE11	N/A

Notes:

1. MRDIMM Memory will operate at the maximum speed of the Intel® Xeon® 6 CPU memory controller, up to 8000 MT/s
2. Intel® Xeon® 6 SKUs 6787P, 6781P, 6767P, 6761P, and 6747P support MRDIMM, Per Intel® Xeon® 6 documentation
3. MRDIMM 32GB and 64GB will be available in Q2CY25

Table 2.2 Memory PID Decoder

Identifier#1	Identifier#2	Identifier#3	Identifier#4	Identifier#5	Identifier#6	Identifier#7
Cisco Product Family	**Memory DIMM Type**	**DIMM Capacity (GB)**	**DIMM Org. (Rank)**	**DDR Generation & DRAM Density**	**DIMM Speed (Mega Transfers per second)**	**Option/Spare DIMM**
UCS UCSX HCI	**MR**: RDIMM **MC**: MR (Multiplexed Rank) DIMM	X16G X32G X48G X64G X96G 128G 256G	**1R:** Single-Rank **2R:** Dual-rank **4R**: Quad-rank	**E:** DDR5/16Gb **F**: DDR5/24Gb **G**: DDR5/32Gb	5: 6400 MT/s 11: 8800 MT/s	**Blank:** Option **=:** Spare

CHAPTER 3 DRAM GUIDELINES

GOLDEN RULE: Memory on every CPU socket shall be configured identically. Therefore, the memory configuration of CPU-1 will be identical to CPU-2 for a 2-Socket system and identical to CPU-3 and CPU-4 for a 4-socket system. Unbalanced populations are unsupported.

- DIMM Count Rules:

Table 3.0 Allowed DIMM Count for 1-CPU and 2-CPU and 4-CPU[1]

Intel M8 Memory DIMM allowed counts	Memory DIMM description	1-CPU count	2-CPU count	4-CPU count
RDIMM				
16GB	16GB RDIMM 1Rx8	8	16	N/A
32GB	32GB RDIMM 1Rx4	8	16	N/A
48GB	48GB RDIMM 1Rx4	8	16	N/A
64GB	64GB RDIMM 2Rx4	4,8,16	8,16,32	16,32,64
96GB	96GB RDIMM 2Rx4	8,16	16,32	32,64
128GB	128GB RDIMM 2Rx4	8,16	16,32	32,64
256GB	256GB RDIMM 4Rx4	8,16	16,32	32,64
MRDIMM				
32GB	32GB MRDIMM 2Rx8	8	16	N/A
64GB	64GB MRDIMM 2Rx4	8	16	N/A

Notes:

1. See *Table 4*.**0** to *Table 4*.**3** for detailed populations and *Table 7*.**0** to *Table 7*.**1** for DIMM configurations.

- DIMM Population Rules:
  - Each channel has two memory slots (for example, channel A = slots A1 and A2). See **golden rule** above.
    - A channel can operate with one or two DIMMs installed.
    - If a channel has only one DIMM, populate slot 1 first (the blue slot).
  - When both CPUs are installed, populate the memory slots of each CPU identically. Fill the blue slots (slot 1) in the memory channels first according to the recommended DIMM populations in *Table 4*.**0**, *Table 4*.**1** **and** *Table 4*.**2**.

Table 4.0 Intel M8 DIMM population order for 16GB, 32GB, 48GB - 1DPC Only

# DIMMs per CPU	DIMM Population - 16GB, 32GB, 48GB (Intel® Xeon® 6 CPUs)[1]	
	Slot 1 (Blue)	Slot 2 (Black)
8	A1, B1, C1, D1, E1, F1, G1, H1	-

Notes:

1. Only 1 DPC supported by 16GB, 32GB, 48GB

Table 4.1 Intel M8 DIMM population order for 64GB - up to 2DPC

# DIMMs per CPU	DIMM Population - 64GB (Intel® Xeon® 6 CPUs)	
	Slot 1 (Blue)	Slot 2 (Black)
4	A1, C1, E1, G1	-
8	A1, B1, C1, D1, E1, F1, G1, H1	-
16	A1, B1, C1, D1, E1, F1, G1, H1	A2, B2, C2, D2, E2, F2, G2, H2

Table 4.2 Intel M8 DIMM population order for 96GB, 128GB, 256GB - up to 2DPC

# DIMMs per CPU	DIMM Population - 96GB, 128GB, 256GB (Intel® Xeon® 6 CPUs)	
	Slot 1 (Blue)	Slot 2 (Black)
8	A1, B1, C1, D1, E1, F1, G1, H1	-
16	A1, B1, C1, D1, E1, F1, G1, H1	A2, B2, C2, D2, E2, F2, G2, H2

Table 4.3 Intel M8 DIMM population order for MRDIMM 32GB, 64GB - 1DPC only

# MRDIMMs per CPU	MRDIMM Population - 32GB, 64GB (Intel® Xeon® 6 CPUs)[1]	
	Slot 1 (Blue)	Slot 2 (Black)
8	A1, B1, C1, D1, E1, F1, G1, H1	-

Notes:

1. Only 1 DPC supported by 32GB, 64GB MRDIMM.

- DIMM Mixing Rules:
  - All DIMMs must be all DDR5-6400 DIMMs or DDR5 MRDIMM-8800 DIMMs
  - When paired with Intel® Xeon® 6 CPUs, all MRDIMM memories must be Cisco DDR5 MRDIMM-8800 memory PIDs, although the memory will operate at the maximum speed of the Intel® Xeon® 6 CPUs memory controller, up to 8000 MT/s.
  - Higher rank DIMMs shall be populated on Slot 1
  - Mixing different DIMM densities in the same slot across channels is not supported. All populated slots of the same color must have the same DIMM density.
  - Mixing DDR5 MRDIMM-8800 and DDR5-6400 memory PIDs is not allowed
  - Mixing X4 and X8 DIMMs is not allowed
  - Mixing 16Gb or 32Gb DRAM based with 24Gb DRAM based DIMMs is not allowed. Therefore, 48GB and 96GB cannot be mixed with any other memory DIMMs
  - Mixing 16Gb or 24Gb DRAM based with 32Gb DRAM based DIMMs is not allowed. Therefore, 128GB 2Rx4 (32Gb) and 256GB 4Rx4 (32Gb) cannot be mixed with any other memory DIMMs
  - 16GB, 32GB, and 48GB supports 1 DIMM Per Channel (1DPC) only
  - 32GB and 64GB MRDIMM support 1 DIMM Per Channel (1DPC) only

- The DIMM mixing rules matrix is described in the *Table 5*.**0**, *Table 5*.**1**, *Table 5*.**2 and** *Table 5*.**3** below

Table 5.0 Supported DIMM mixing and population across 2 slots in each channel - 16Gb DRAM based DIMMs[1,2,3]

Channel Mixing		DIMM Slot 2 (Black)		
DIMM Slot 1 (Blue)		16GB	32GB	64GB
		1Rx8	1Rx4	2Rx4
16GB	1Rx8	No[4]	No	No
32GB	1Rx4	No	No[4]	No
64GB	2Rx4	No	No	Yes

Notes:

1. Mixing different DIMM densities in the same slot across channels is not supported.
2. All populated slots of the same color must have the same DIMM density.
3. 16Gb/32Gb/24Gb RDIMM mixing is not allowed.
4. 1 DPC only, per Intel® Xeon® 6 documentation

Table 5.1 Supported DIMM mixing and population across 2 slots in each channel - 32Gb DRAM based DIMMs[1,2,3]

Channel Mixing		DIMM Slot 2 (Black)	
DIMM Slot 1 (Blue)		128GB	256GB
		2Rx4	4Rx4
128GB	2Rx4	Yes	No
256GB	4Rx4	No	Yes

Notes:

1. 16Gb/32Gb/24Gb RDIMM mixing is not allowed.
2. 128GB and 256GB mixing within and across channel is not allowed.
3. 256GB supports 2 DPC only, Per Intel® Xeon® 6 documentation.

Table 5.2 Supported DIMM mixing and population across 2 slots in each channel - 24Gb DRAM based DIMMs[1,2,3]

Channel Mixing		DIMM Slot 2 (Black)	
DIMM Slot 1 (Blue)		48GB	96GB
		1Rx8	1Rx4
48GB	1Rx8	No[4]	No
96GB	1Rx4	No	Yes

Notes:

1. Mixing different DIMM densities in the same slot across channels is not supported.

2. All populated slots of the same color must have the same DIMM density.
3. 16Gb/32Gb/24Gb RDIMM mixing is not allowed.
4. 1 DPC only, per Intel® Xeon® 6 documentation.

Table 5.3 Supported DIMM mixing and population across 2 slots in each channel - MRDIMM[1,2]

Channel Mixing		DIMM Slot 2 (Black)	
DIMM Slot 1 (Blue)		32GB	64GB
		2Rx8	2Rx4
32GB	2Rx8	No	No
64GB	2Rx4	No	No

Notes:
1. 32GB and 64GB MRDIMM mixing within and across channel is not allowed.
2. 16Gb/32Gb/24Gb RDIMM mixing is not allowed.

- Memory Limitations:
  - Memory on every CPU socket shall be configured identically. See **golden rule from page 9**.
  - Refer to *Table 4.0, Table 4.1, Table 4.2, Table 5.0, Table 5.1*, *Table 5*.**2** **and** *Table 5.3*, for DIMM population and DIMM mixing rules.
  - Cisco memory from previous generation servers (DDR5-4800 and DDR5-5600) is not supported with the Intel M8 servers.
- For best performance, observe the following:
  - For optimum performance, populate at least one DIMM per memory channel per CPU. When one DIMM per channel is used, it must be populated in DIMM slot 1 (blue slot farthest away from the CPU) of a given channel.
  - The maximum 2 DPC speed is 6400 MT/s, refer to *Table 6*.**0** for the details.

Table 6.0 Maximum DIMM Memory Operating Frequency on Intel® Xeon® 6 CPUs.

Intel® Xeon® 6 CPU Memory Speed	1DPC	2DPC
	All RDIMMs	All RDIMMs
All Intel® Xeon® 6 SKUs	6400 MT/s	5200 MT/s

Table 6.1 Maximum MRDIMM Memory Operating Frequency on Intel® Xeon® 6 CPUs.

Intel® Xeon® 6 CPU Memory Speed	1DPC
	All MRDIMMs
Selected Intel® Xeon® 6 SKUs[1]	8000 MT/s

Notes:
1. Intel® Xeon® 6 SKUs 6787P, 6781P, 6767P, 6761P, and 6747P support MRDIMM, Per Intel® Xeon® 6 documentation

CHAPTER 4 SUPPORTED DRAM DIMM CONFIGURATIONS

Table 7.0 below shows the supported DIMM configurations with 4, 8, and 16 DIMMs per CPU.

Table 7.0 Supported DIMM Configurations for Intel® Xeon® 6 Scalable Processors

DDR5 Memory Total System Capacity			Capacity Per CPU (GB)		Total DIMMs Per CPU
1-CPU	**2-CPU**	**4-CPU**	**Blue Slots A1 to H1**	**Black Slots A2 to H2**	
16GB RDIMMs					
128GB	256GB	N/A	8x16GB	-	8
32GB RDIMMs					
256GB	512GB	N/A	8x32GB	-	8
48GB RDIMMs					
384GB	768GB	N/A	8x48GB	-	8
64GB RDIMMs					
256GB	512GB	1024GB	4x64GB	-	4
512GB	1024GB	2048GB	8x64GB	-	8
1024GB	2048GB	4096GB	8x64GB	8x64GB	16
96GB RDIMMs					
768GB	1536GB	3072GB	8x96GB	-	8
1536GB	3072GB	6144GB	8x96GB	8x96GB	16
128GB RDIMMs					
1024GB	2048GB	4096GB	8x128GB	-	8
2048GB	4096GB	8192GB	8x128GB	8x128GB	16
256GB RDIMMs					
2048GB	4096GB	8192GB	8x256GB	-	8
4096GB	8192GB	16384GB	8x256GB	8x256GB	16

Table 7.1 below shows the supported MRDIMM configurations with 4 and 8 MRDIMMs per CPU.

Table 7.1 Supported MRDIMM Configurations for Intel® Xeon® 6 Scalable Processors

DDR5 Memory Total System Capacity			Capacity Per CPU (GB)		Total MRDIMMs Per CPU
1-CPU	**2-CPU**	**4-CPU**	**Blue Slots A1 to H1**	**Black Slots A2 to H2**	
32GB MRDIMMs					
256GB	512GB	N/A	8x32GB	-	8
64GB MRDIMMs					
512GB	1024GB	N/A	8x64GB	-	8

NOTE:

- Review the appropriate platform spec sheets for additional 256GB DIMM usage conditions.
- MRDIMMs are available on all Intel M8 server models except X410c M8 compute node.

CHAPTER 5 INSTALLING a DIMM or DIMM BLANK

To install a DIMM or a DIMM blank into a slot on the blade server, follow these steps.

Procedure

Step 1 Open both DIMM connector latches.

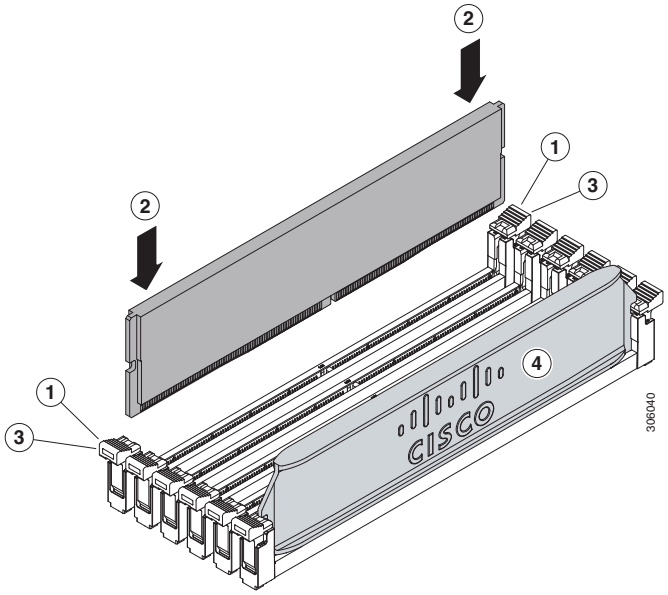
Step 2 Press evenly on both ends of the DIMM until it clicks into place in its slot

Note: Ensure that the notch in the DIMM aligns with the slot. If the notch is misaligned, it is possible to damage the DIMM, the slot, or both.

Step 3 Press the DIMM connector latches inward slightly to seat them fully.

Step 4 Populate all slots with a DIMM or DIMM blank. A slot cannot be empty.

Figure 3 Installing Memory



Change log

Please find the below table for the recent changes happened in the document.

Table 8 Change log

Publication Date	Revision
24/02/2025	Initial Memory Guide set up is completed
04/03/2025	Deleted 4x DIMM references for 48 and 96GB
27/03/2025	■ Moved 48 to not allowed, as 12 is no longer valid per CPU => 48 not allowed for 4-CPU servers ■ Added a note for 3.0 and 3.1 Tables
28/05/2025	■ removed table 3.1, and added information to the table 3. updated/improved table 3

Americas Headquarters
Cisco Systems, Inc.
San Jose, CA

Asia Pacific Headquarters
Cisco Systems (USA) Pte. Ltd.
Singapore

Europe Headquarters
Cisco Systems International BV Amsterdam,
The Netherlands

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