Cisco UCS C845A M8 AI Servers Memory Guide

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Introduction

The Cisco UCS C845A M8 AI Server Memory guide provides the detailed specifications of the M8 memory DIMMs including:

- Memory DIMMs features
- Cisco PID's description
- Memory DIMMs guidelines, mixing rules and populations
- All UCS C845A M8 supported DIMM configurations

The Cisco UCS C845A M8 AI Server Memory Guide document applies to the following Cisco UCS C845A M8 AI Server generation servers:

- UCS C845A M8 4RU MGX AI Servers

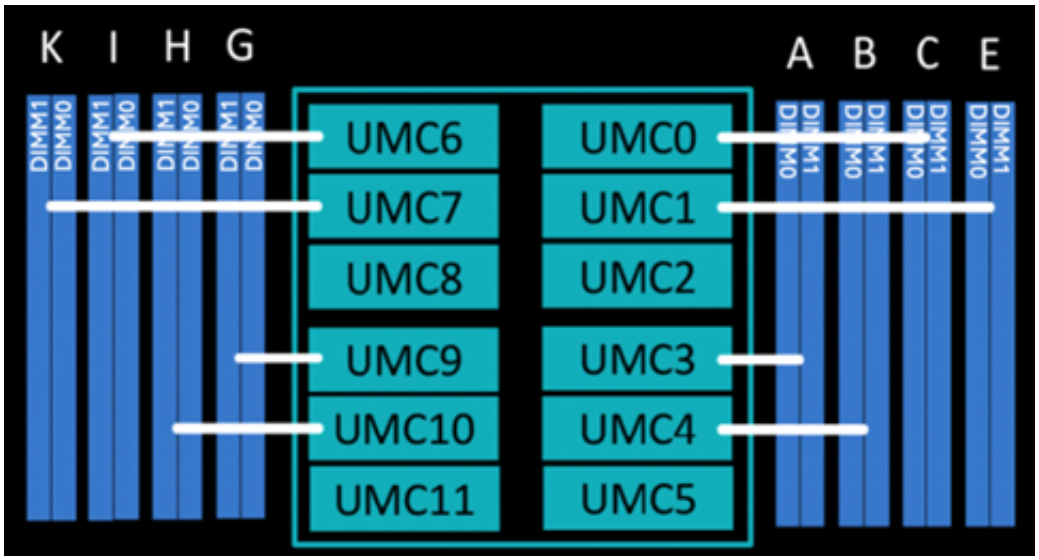
CHAPTER 1 MEMORY ORGANIZATION CAPABILITIES AND FEATURE

The *Table 1* below describes the main memory DIMM and MRDIMM features supported on Cisco UCS Cisco UCS C845A M8 AI servers.

Table 1 Main Memory Features

Cisco UCS C845A M8 AI Server Memory DIMM Server Technologies	C845A M8
CPU sockets	2S
DDR5 Memory clock speed	5th Gen. AMD EPYC CPUs: Up to 5200 MT/s 1DPC; Up to 4400 MT/s 2DPC
Operational voltage	1.1 Volts
DRAM Fab density	16Gb, 24Gb, and 32Gb
DRAM DIMM Type	RDIMM (Registered DDR5 DIMM)
Memory DIMM organization	Eight memory DIMM channels per CPU; up to 2 DIMMs per channel
Maximum number of DRAM DIMM per server	32 (2-Socket)
DRAM DIMM densities and Rank	32GB 1Rx4, 64GB 2Rx4, 96GB 2Rx4, 128GB 2Rx4
Maximum system Capacity	4TB (32x128GB)

Figure 1 8-channel Memory Organization



CHAPTER 2 MEMORY OPTIONS

■ The available memory devices for UCS C845A M8 AI Servers are listed in *Table 2*. The memory PID decoder for UCS C845A M8 AI Servers Memory PIDs are shown in *Table 3*

NOTE:

■ When paired with 5th Gen. AMD EPYC™ CPUs, all memory DIMMs must be Cisco DDR5-6400 memory PIDs, although the memory will operate at the maximum speed of the 5th Gen. AMD EPYC™ CPUs memory controller, up to 5200 MT/s.

Table 2 Memory Options for UCS M8 servers with 5th Gen. AMD EPYC™ CPUs

AMD M8 Memory DIMM Densities & Cisco PIDs	Memory DIMM Description	C845A M8
DDR5-6400MT/s Cisco Memory PIDs list - 5th Gen. AMD EPYC™ CPUs1[1]		
32GB[2]	32GB RDIMM 1Rx4 1.1Volts (16Gb)	CAI-MRX32G1RE5
64GB	64GB RDIMM 2Rx4 1.1Volts (16Gb)	CAI-MRX64G2RE5
96GB	96GB RDIMM 2Rx4 1.1Volts (24Gb)	CAI-MRX96G2RF5
128GB	128GB RDIMM 2Rx4 1.1Volts (32Gb)	CAI-MR128G2RG5

Notes:

1. Memory will operate at the maximum speed of the AMD 5th Gen. CPU memory controller, up to 5200 MT/s Check *Table 6* for details on 1DPC and 2 DPC maximum speed with 5th Gen. CPUs.
2. 32GB will be available post-FCS

Table 3 Memory PID Decoder

Identifier#1	Identifier#2	Identifier#3	Identifier#4	Identifier#5	Identifier#6	Identifier#7
Cisco Product Family	**Memory DIMM Type**	**DIMM Capacity (GB)**	**DIMM Org. (Rank)**	**DDR Generation & DRAM Density**	**DIMM Speed (Mega Transfers per second)**	**Option/Spare DIMM**
CAI	**MR:** RDIMM	X32G X64G X96G 128G	**1R:** Single-Rank **2R:** Dual-rank **4R**: Quad-rank	**E:** DDR5/16Gb **F**: DDR5/24Gb **G:** DDR5/32Gb	**5:** 6400 MT/s	**Blank:** Option =: Spare

CHAPTER 3 DRAM GUIDELINES

GOLDEN RULE: Memory on every CPU socket shall be configured identically. Therefore, the memory configuration of CPU-1 will be identical to CPU-2 for a 2-Socket system. Unbalanced populations are unsupported.

- DIMM Count Rules:

Table 4 Allowed DIMM Count for 1-CPU and 2-CPU[1]

Allowed DIMM Count rules	Minimum Count	Maximum Count	Allowed Count	Not Allowed Count
DIMM count for 1-CPU	1	16	1,2,4,6,8,12,16	3,5,7,9,10,11,13,14,15
DIMM count for 2-CPU	2	32	2,4,8,12,16,24,32	6,10,14,18,20,22,26,28,30

Notes:

1. Only 2-CPU system is configurable on UCS C845A M8 AI Servers.

- DIMM Population Rules:
  - When populating memory on a server powered by one or more 5th Gen. AMD EPYC™ CPUs:
    - All memory DIMMs must be RDIMM (32GB, 64GB, 96GB,128GB) module types.
    - When paired with 5th Gen. AMD EPYC™ CPUs, all memory DIMMs must be Cisco DDR5-6400 memory PIDs, although the memory will operate at the maximum speed of the 5th Gen. AMD EPYC™ CPUs memory controller, up to 5200 MT/s in a 2 DPC board design.
    - Use the same DIMM configuration for each processor socket, on a 2-socket configuration.
    - Each channel has two memory slots (for example, channel A = slots A0 and A1). See **golden rule** above.
      - A channel can operate with one or two DIMMs installed.
      - If a channel has only one DIMM, populate slot 1 first.
  - When both CPUs are installed, populate the memory slots of each CPU identically. Fill the slot 1 in the memory channels first according to the recommended DIMM populations *Table 5*
  - Balanced memory configurations maximize memory bandwidth by optimizing memory interleaving. To obtain a balanced memory configuration:
    - Populate each socket with 1, 2, 4, 6, 8, 12 or 16 memory channels.
    - Use the same memory configuration in all populated memory channels. No DIMM density mixing across channel or within channel (2DPC) is allowed.
    - Mixing DIMMs of different DRAM density within or across channel is not supported.

Table 5 M8 DIMM population order for 32GB, 64GB, 96GB, 128GB

#DIMMs per CPU	DIMM Population - 32GB, 64GB, 96GB, 128GB	
	Slot 1	Slot 0
1	A1	
2	A1, G1	
4	A1, C1, G1, I1	
6	A1, B1, C1, G1, H1, I1	
8	A1, B1, C1, E1, G1, H1, I1, K1	
12	A1, B1, C1, G1, H1, I1	A0, B0, C0, G0, H0, I0
16	A1, B1, C1, E1, G1, H1, I1, K1	A0, B0, C0, E0, G0, H0, I0, K0

- Memory Limitations:
  - Memory on every CPU socket shall be configured identically.
  - Refer to *Table 5* for DIMM population and DIMM mixing rules.
  - Cisco Memory DIMM PIDs used on M8 server models powered by 5th Gen. AMD EPYC™ CPUs are DDR5-6400 PIDs, although the memory will operate at the maximum speed of the 5th Gen. AMD EPYC™ CPUs memory controller, up to 5200 MT/s. Check *Table 6* for CPU SKUs definition and maximum memory speed.
- For best performance, observe the following:

Table 6 Maximum DIMM Memory Operating Frequency on 5th Gen. AMD EPYC™ CPUs

5th Gen. CPU Memory Speed on 2DPC board design	1DPC	2DPC
	All RDIMMs	All RDIMMs
RDIMM	5200 MT/s	4400 MT/s

CHAPTER 4 SUPPORTED DRAM DIMM CONFIGURATIONS

Table below shows the supported DIMM configurations with 1, 2, 4, 6, 8, 12, and 16 DIMMs per CPU

Table 7 Supported Memory Configurations for 5th Gen. AMD EPYC™ CPUs

DIMM Total System Capacity		Capacity Per CPU		Total DIMMs Per CPU
1-CPU	**2-CPU**	**Slots A1 to H1**	**Slots A0 to H0**	
32GB RDIMMs				
32 GB	64 GB	1x32GB	-	1
64 GB	128 GB	2x32GB	-	2
128 GB	256 GB	4x32GB	-	4
192 GB	384 GB	6x32GB	-	6
256 GB	512 GB	8x32GB	-	8
384 GB	768 GB	6x32GB	6x32GB	12
512 GB	1024 GB	8x32GB	8x32GB	16
64GB RDIMMs				
64 GB	128 GB	1x64GB		1
128 GB	256 GB	2x64GB		2
256 GB	512 GB	4x64GB		4
384 GB	768 GB	6x64GB		6
512 GB	1024 GB	8x64GB		8
768 GB	1536 GB	6x64GB	6x64GB	12
1024GB	2048GB	8x64GB	8x64GB	16
96GB RDIMMs				
96 GB	192 GB	1x96GB		1
192 GB	384 GB	2x96GB		2
384 GB	768 GB	4x96GB		4
576 GB	1152 GB	6x96GB		6
768 GB	1536 GB	8x96GB		8
1152 GB	2304 GB	6x96GB	6x96GB	12
1536GB	3072 GB	8x96GB	8x96GB	16

Table 7 Supported Memory Configurations for 5th Gen. AMD EPYC™ CPUs

128GB RDIMMs				
128 GB	256 GB	1x128GB		1
256 GB	512 GB	2x128GB		2
512 GB	1024 GB	4x128GB		4
768 GB	1536 GB	6x128GB		6
1024 GB	2048 GB	8x128GB		8
1536 GB	3072 GB	6x128GB	6x128GB	12
2048 GB	4096 GB	8x128GB	8x128GB	16

CHAPTER 5 INSTALLING a DIMM or DIMM BLANK

To install a DIMM or a DIMM blank into a slot on the blade server, follow these steps.

Procedure

Step 1 Open both DIMM connector latches.

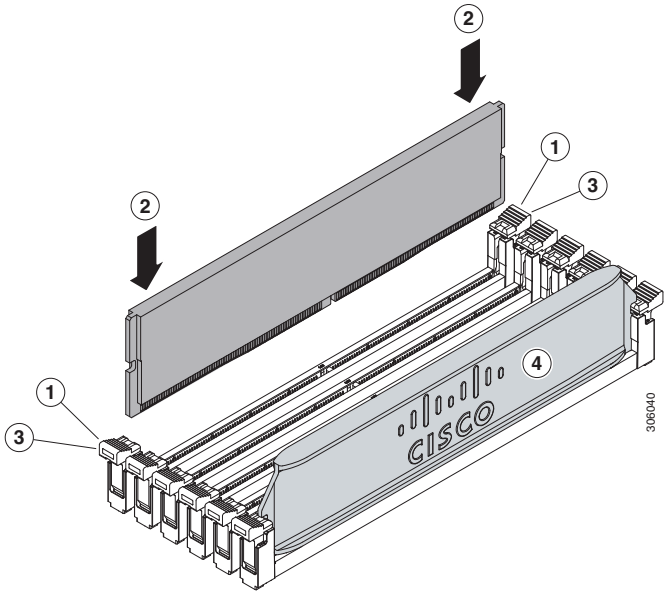
Step 2 Press evenly on both ends of the DIMM until it clicks into place in its slot

Note: Ensure that the notch in the DIMM aligns with the slot. If the notch is misaligned, it is possible to damage the DIMM, the slot, or both.

Step 3 Press the DIMM connector latches inward slightly to seat them fully.

Step 4 Populate all slots with a DIMM or DIMM blank. A slot cannot be empty.

Figure 2 Installing Memory



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