

Cisco Green Research Symposium

5 March 2008

**FPGA-based ASIC
Design and Verification**

Dejan Markovic

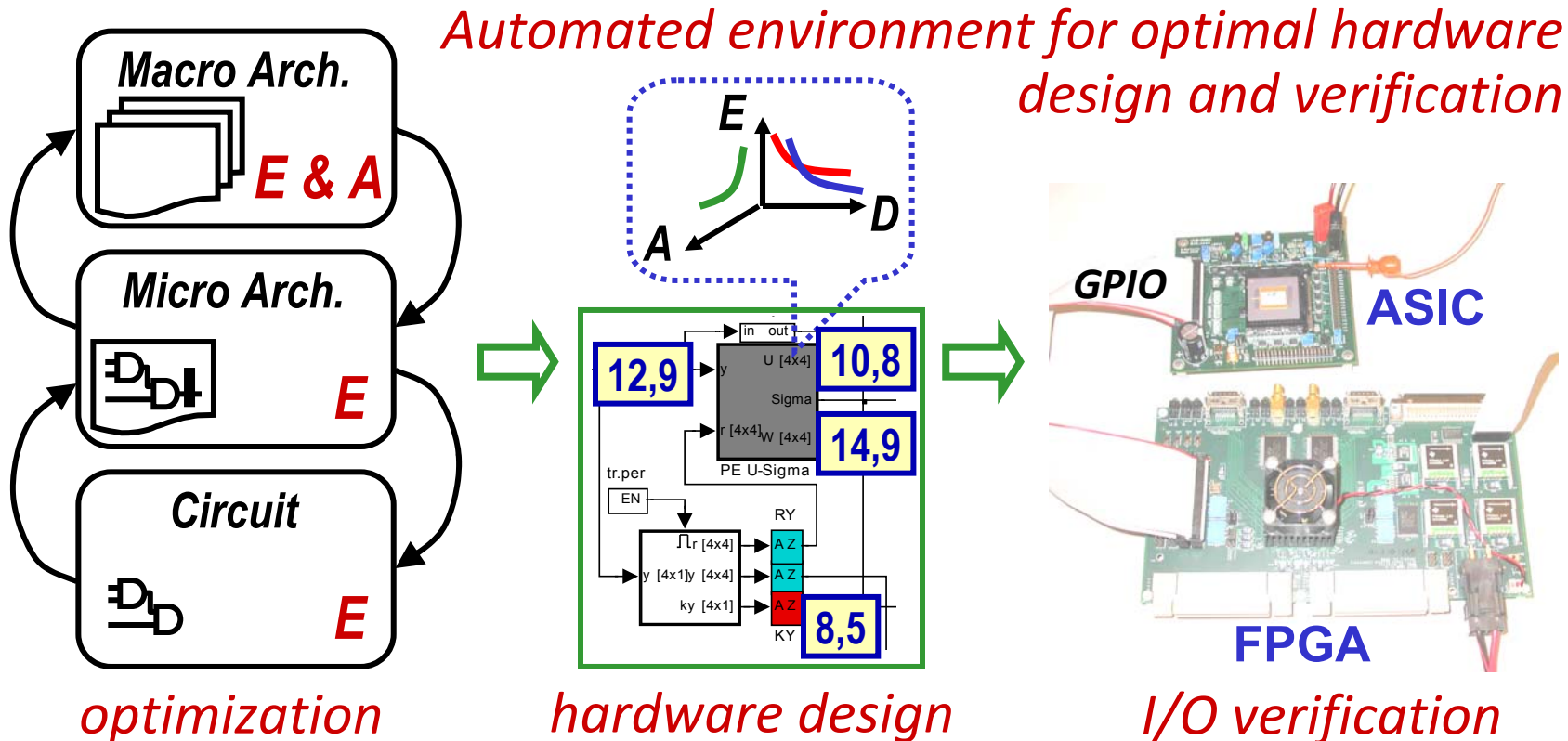
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The Issues I am Going to Address

- ◆ **Power efficiency = energy efficiency $\sim C \cdot V^2$**
- ◆ **Design complexity**
- ◆ **Design re-entry**
 - Algorithm (Matlab or C)
 - Fixed point description
 - RTL (behavioral, structural)
 - Test vectors for logic analysis
- ◆ **In this talk, I will demonstrate**
 - Power efficiency of 2.1GOPS/mW (90nm CMOS)
 - 70GOPS in 3.5mm²
 - FPGA-based design and verification

Optimization Approach

- ◆ Power efficiency: circuit-level (C,V)
- ◆ Performance and area: architectural techniques
- ◆ Unified Simulink description



Circuit-Level Optimization Framework

◆ Sensitivity based optimization

- Balance sensitivity to all variables
- Variables: gate size, V_{DD} , V_{TH}

$$\begin{aligned} &\text{minimize } Energy(V_{dd}, V_{th}, W) \\ &\text{subject to } Delay(V_{dd}, V_{th}, W) \leq D_{con} \end{aligned}$$

Constraints

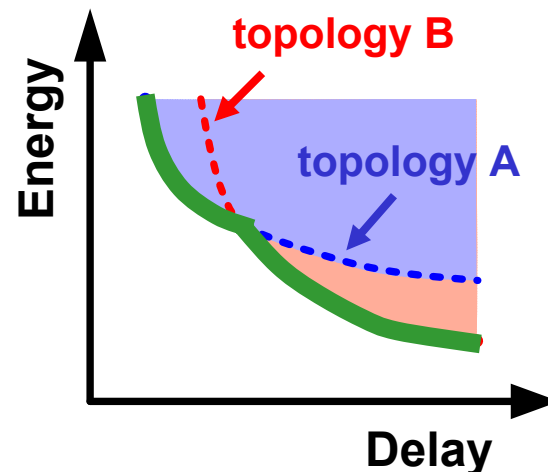
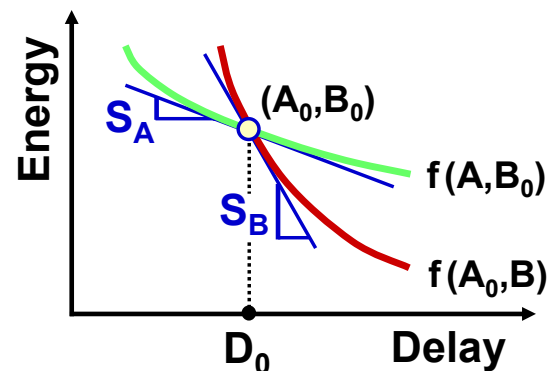
$$V_{dd}^{min} < V_{dd} < V_{dd}^{max}$$

$$V_{th}^{min} < V_{th} < V_{th}^{max}$$

$$W^{min} < W$$

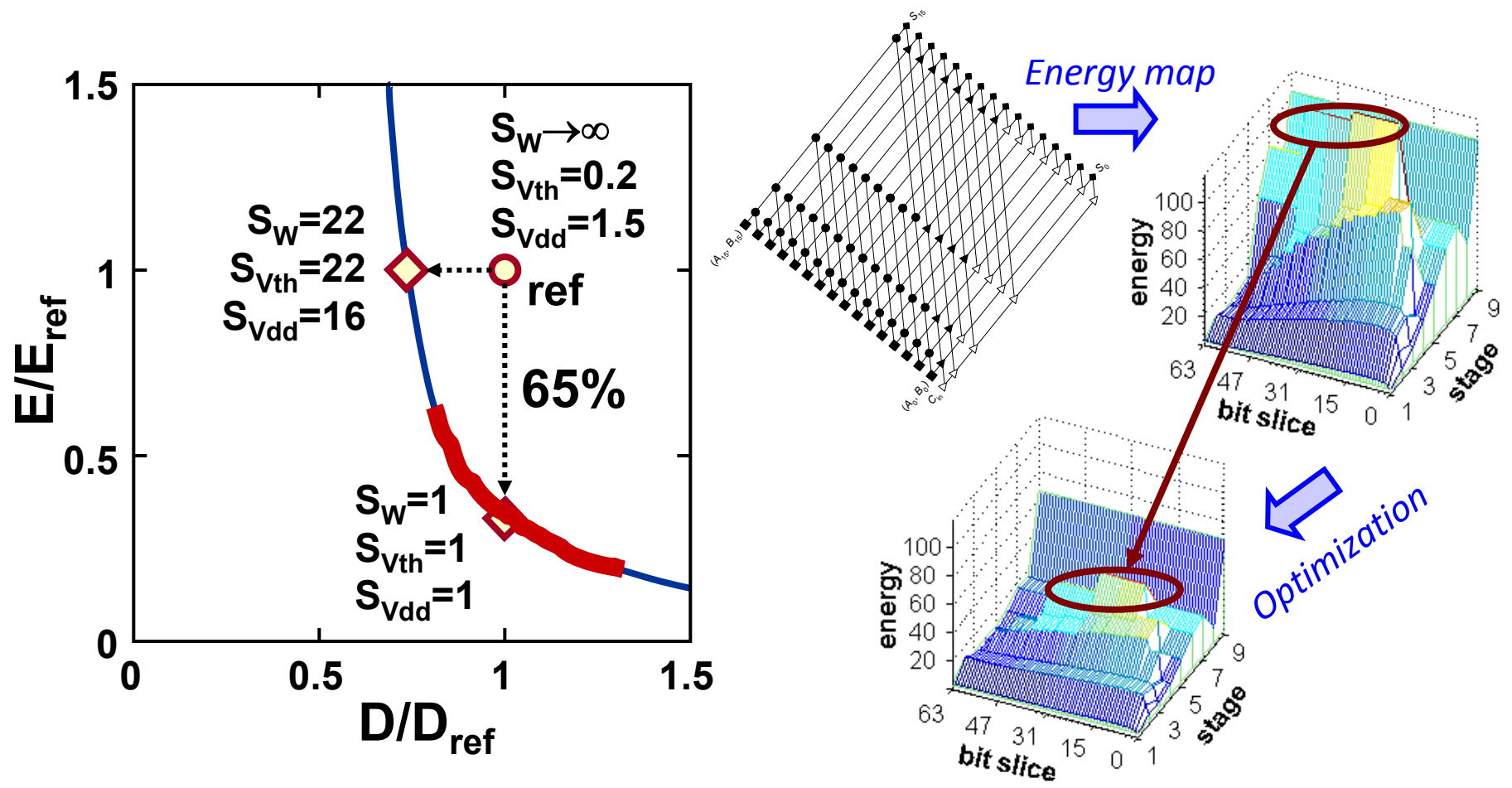
◆ Reference design

- D_{min} sizing @ V_{dd}^{max} , V_{th}^{ref}



Goal: find optimal E-D tradeoff for a datapath

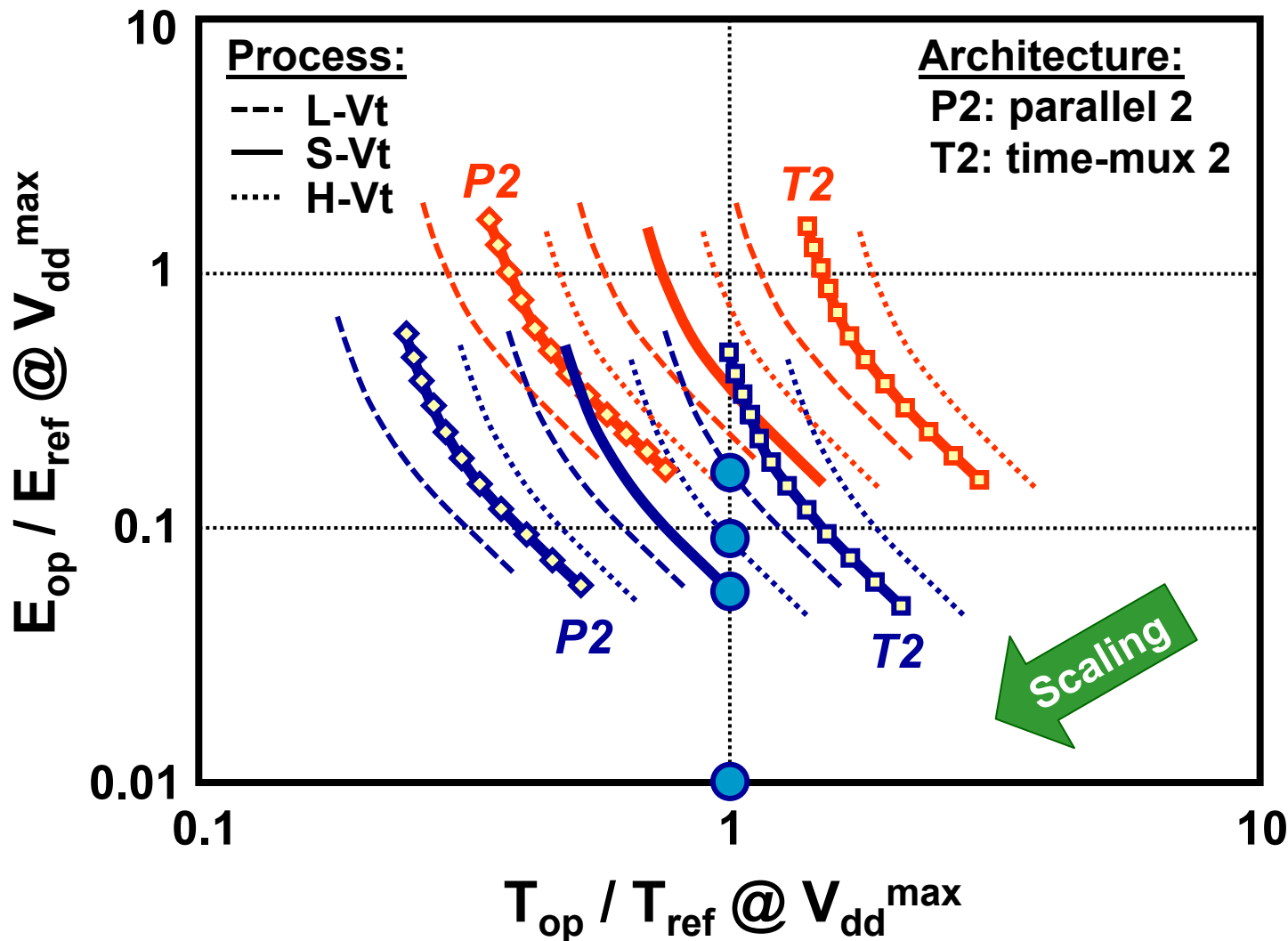
Circuit-Level Results: Tree Adder



[D. Markovic, V. Stojanovic, B. Nikolic, M.A. Horowitz, R.W. Brodersen, JSSC Aug'04]

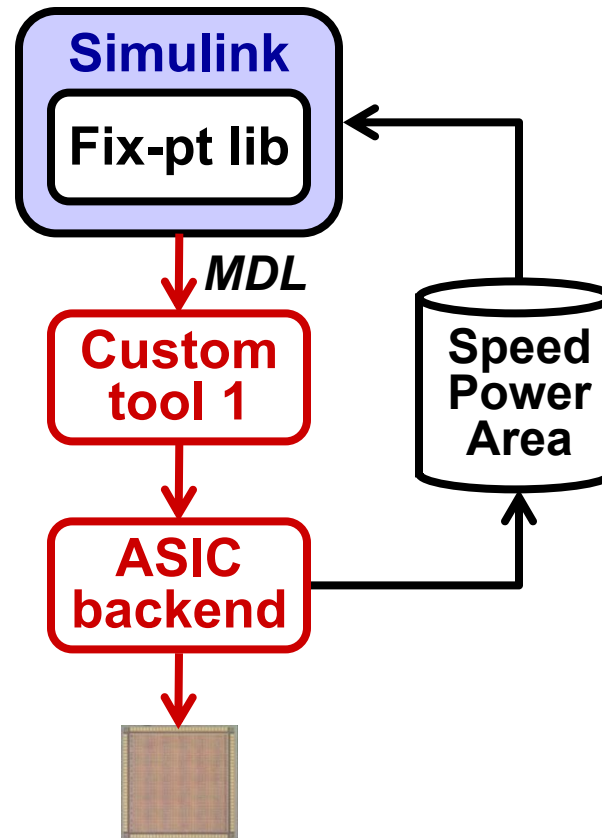
E-D space is the key for architecture optimization

Scaling Impacts Architecture



Simulink to Silicon Mapping

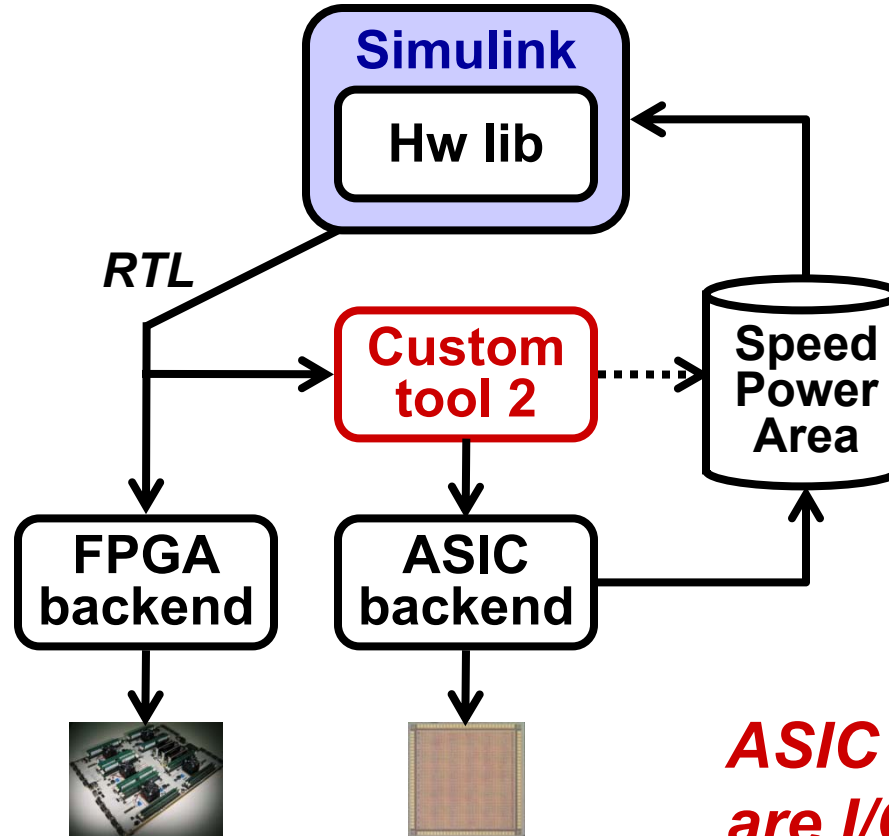
MDL to RTL conversion, automated P&R flow



[R. Davis et al., JSSC Mar'02]

Including FPGA Emulation

XSG hardware library, RTL translation scripts

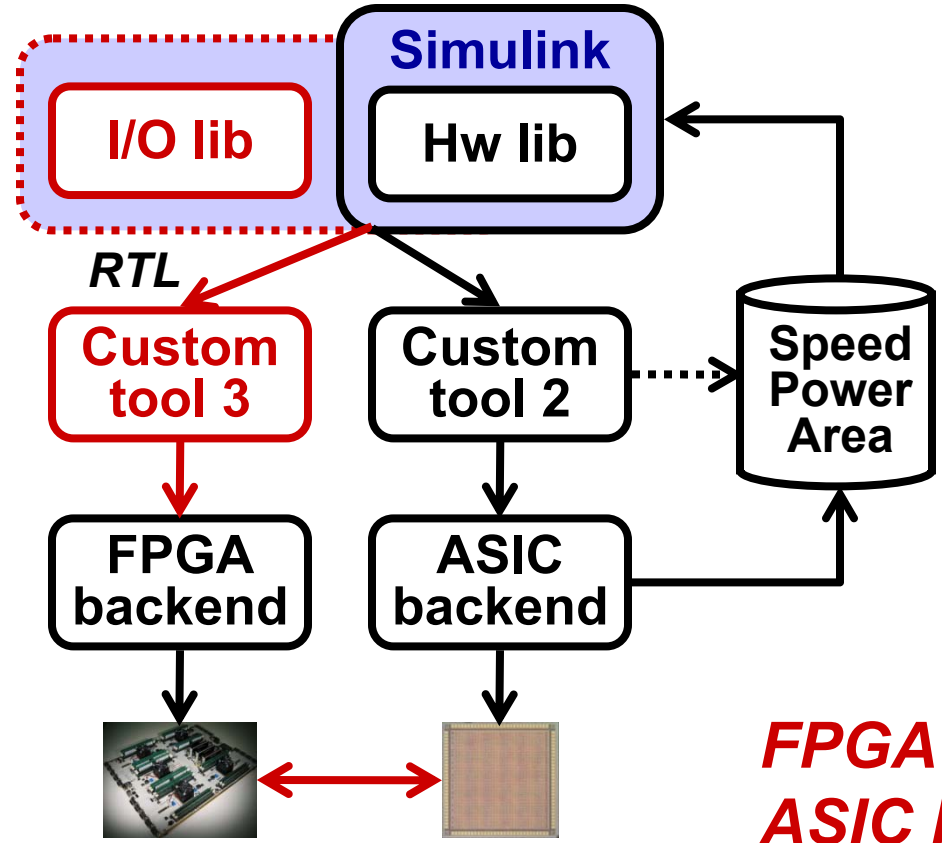


**ASIC and FPGA
are I/O equivalent**

[K. Kuusilinna et al., book chap. in SoC Revolution, KAP 2003]

Closing the Loop: I/O Verification

I/O hardware library, automated FPGA flow

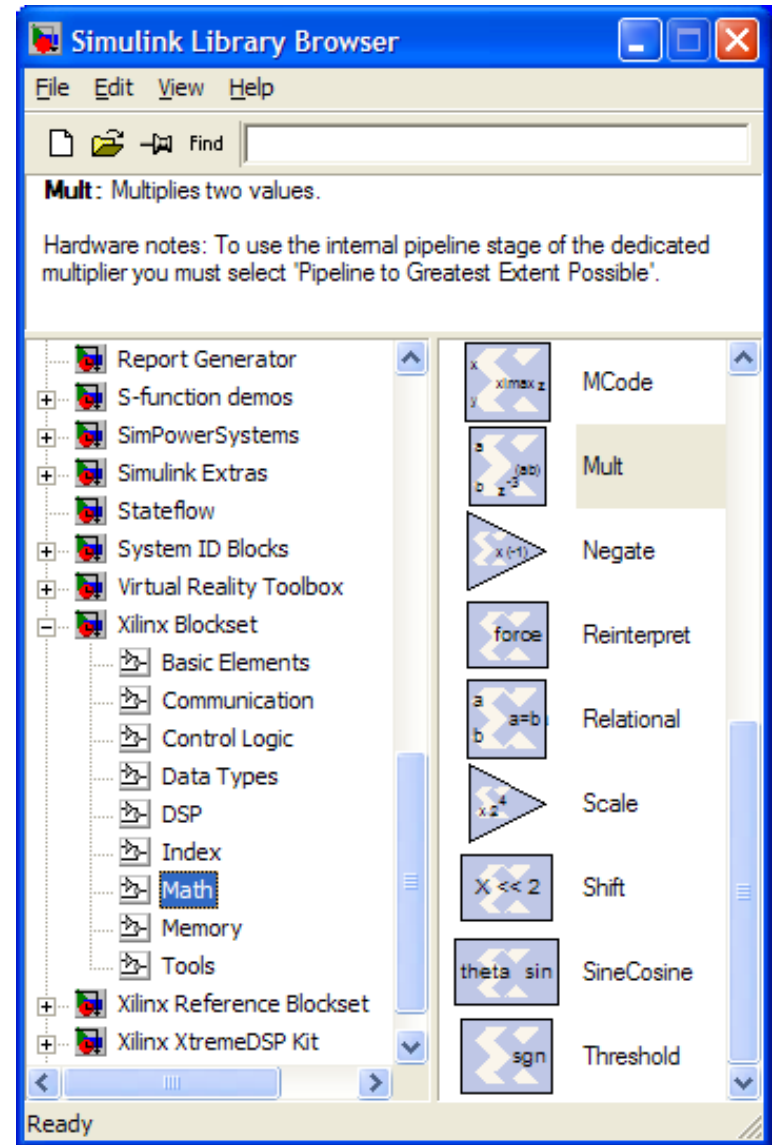


FPGA implements ASIC logic analysis

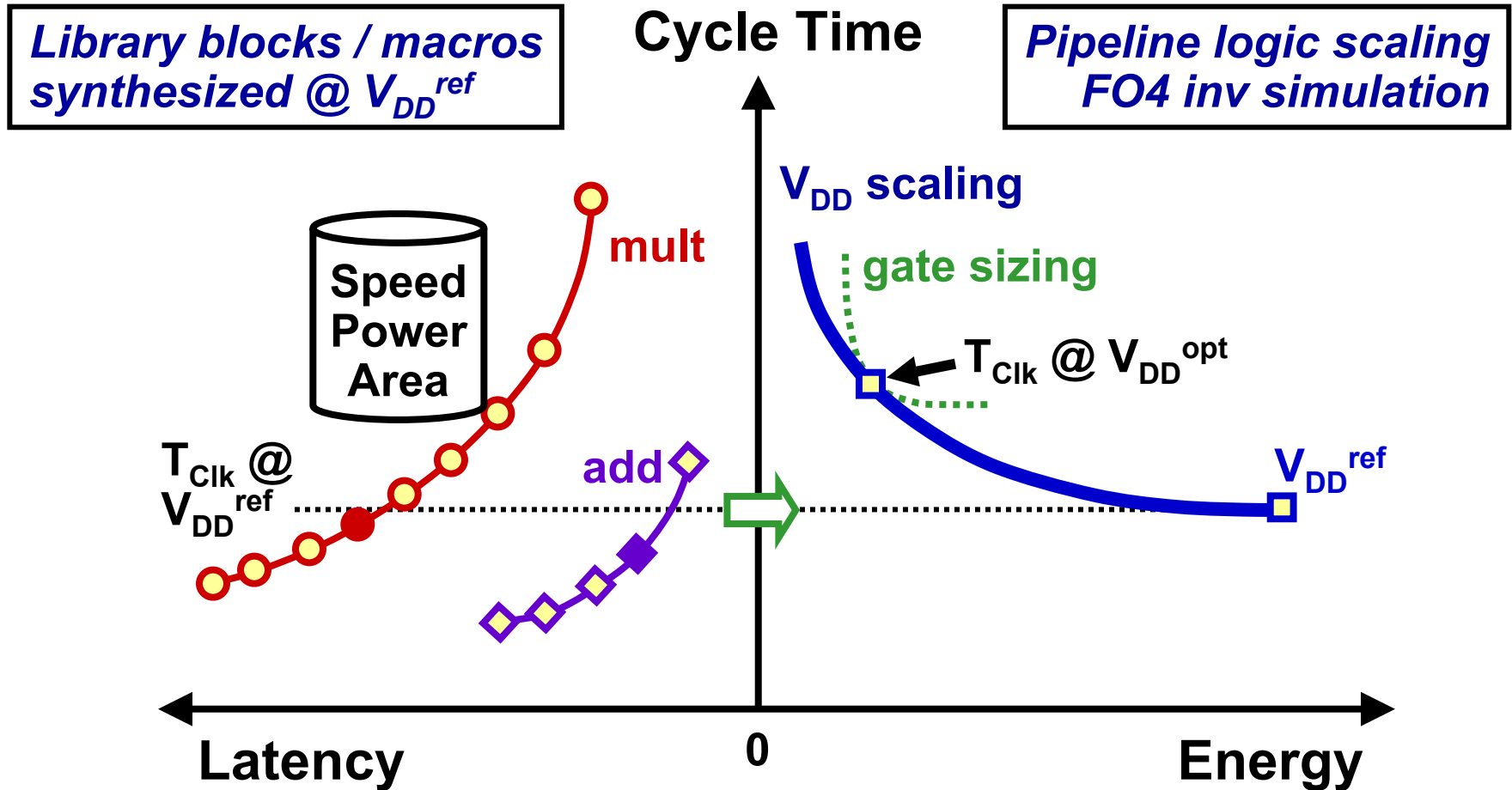
[D. Markovic, C. Chang, B. Richards, H. So, B. Nikolic, R.W. Brodersen, CICC'07]

Design Approach

- ◆ **Unified Simulink design environment**
 - Enter design once!
 - Algorithm verification
 - Macro-architecture
 - FPGA based ASIC debug
- ◆ **Hardware-equivalent Simulink blocks**
 - Add, mult, shift, mux...
 - Word-size, latency



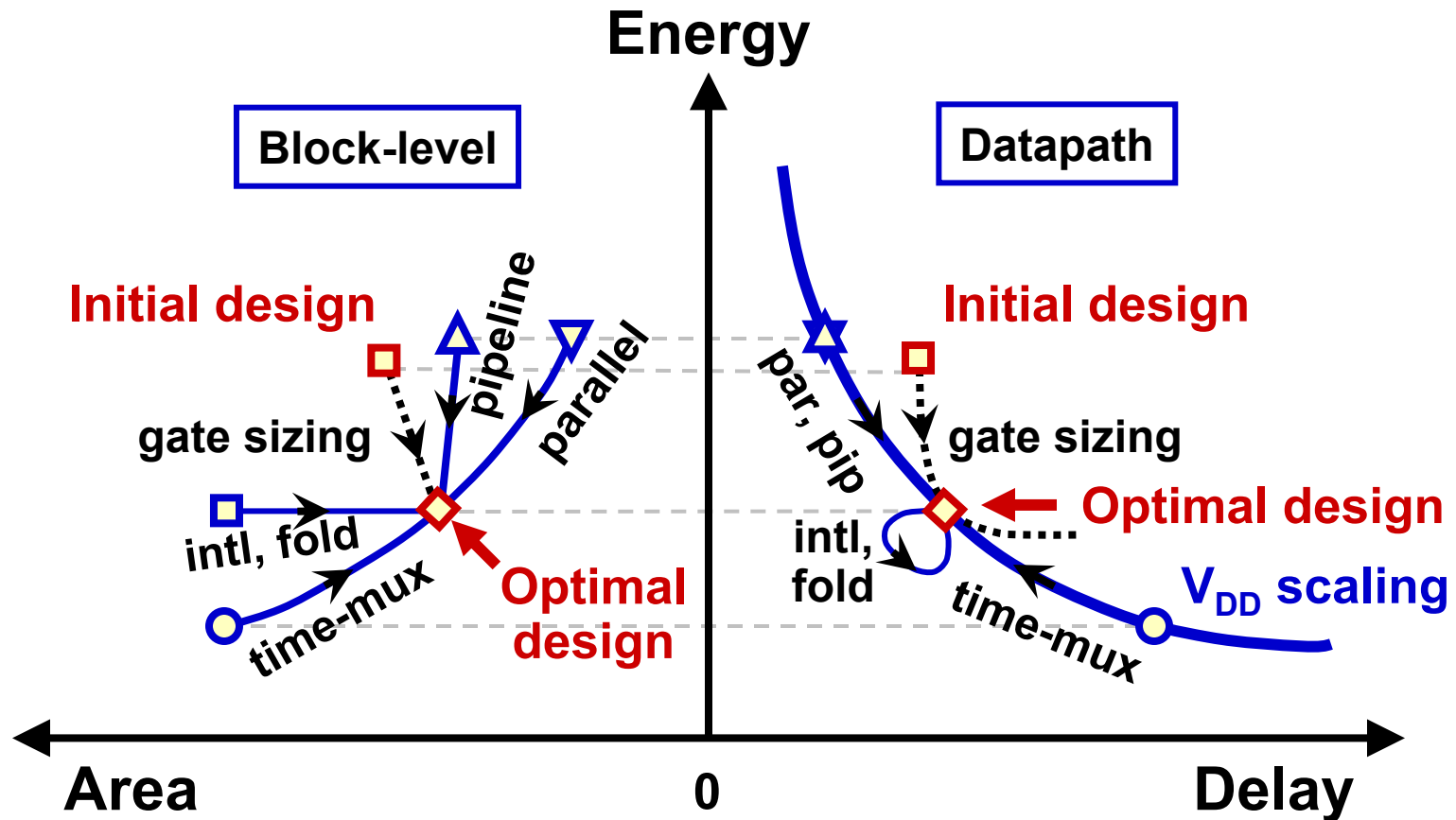
Block Characterization



Goal: balanced logic depth and E/D sensitivity

Methodology for Architecture Selection

- ◆ **Energy-Area-Delay space for architecture comparison**
 - Time-mux, parallelism, pipelining, V_{DD} scaling, sizing...



Example: 4x4 SVD Algorithm

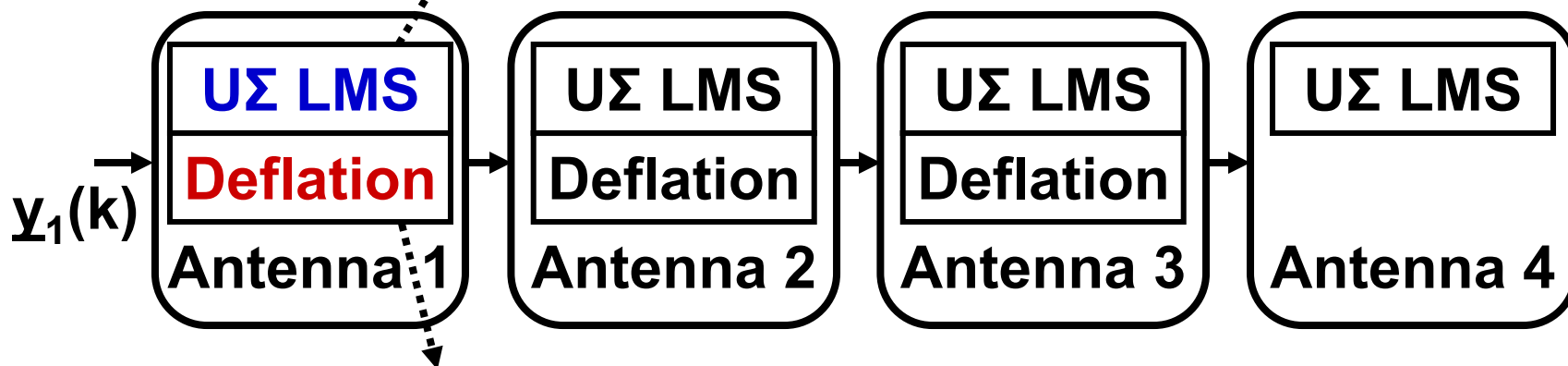
- ◆ This complexity is hard to optimize in RTL
 - 270 adders, 370 multipliers, 8 sqrt, 8 div
 - Recursive LMS-based algorithm (nested feedback loops)

$$\underline{\mathbf{w}}_i(k) = \underline{\mathbf{w}}_i(k-1) + \mu_i \cdot [\underline{\mathbf{y}}_i(k) \cdot \underline{\mathbf{y}}_i^\dagger(k) \cdot \underline{\mathbf{w}}_i(k-1) - \sigma_i^2(k-1) \cdot \underline{\mathbf{w}}_i(k-1)]$$

$$\sigma_i^2(k) = \underline{\mathbf{w}}_i^\dagger(k) \cdot \underline{\mathbf{w}}_i(k)$$

$$\underline{\mathbf{u}}_i(k) = \underline{\mathbf{w}}_i(k) / \sqrt{\sigma_i^2(k)}$$

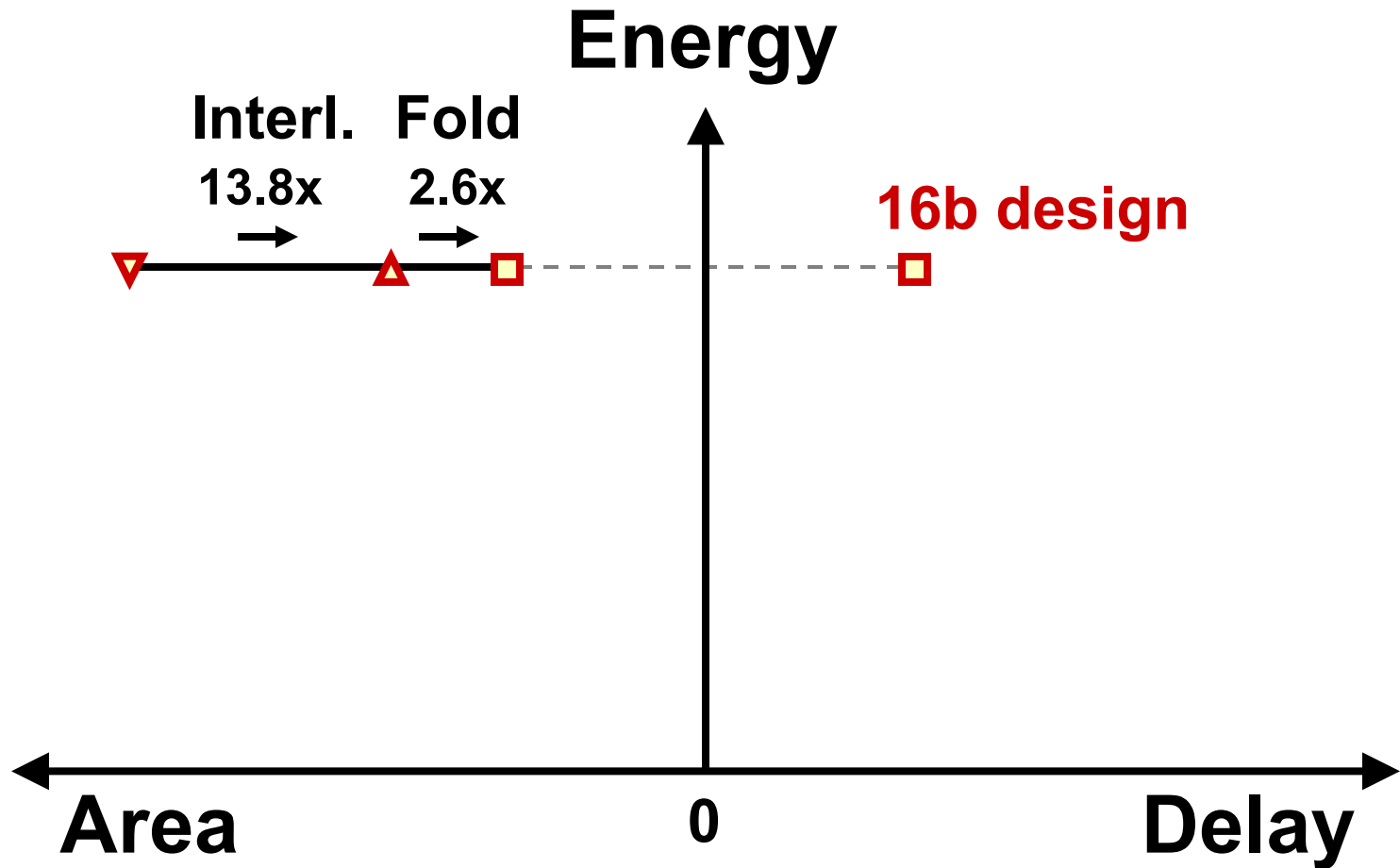
(i=1,2,3,4)



$$\underline{\mathbf{y}}_{i+1}(k) = \underline{\mathbf{y}}_i(k) - [\underline{\mathbf{w}}_i^\dagger(k) \cdot \underline{\mathbf{y}}_i(k) \cdot \underline{\mathbf{w}}_i(k)] / \sigma_i^2(k)$$

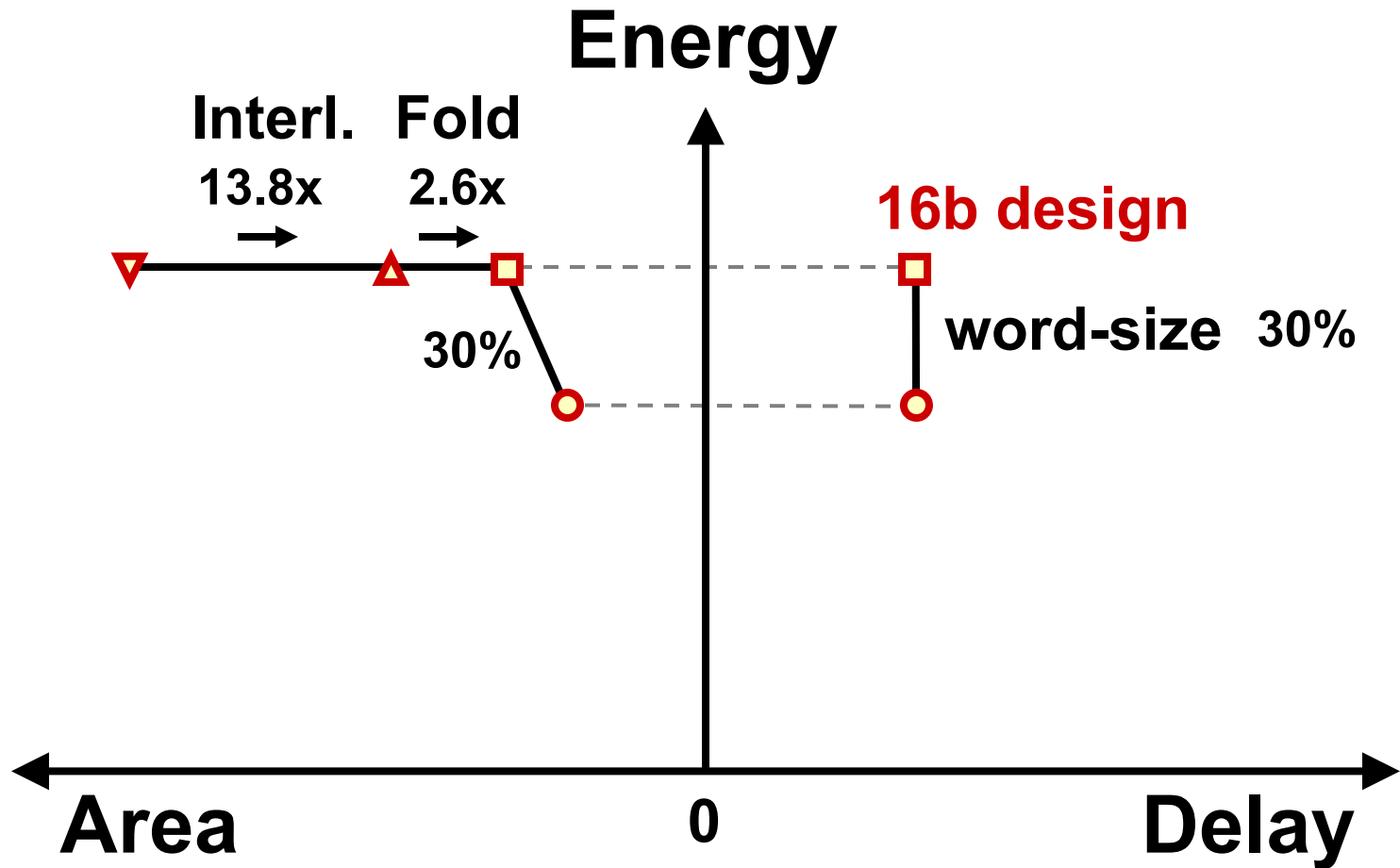
Energy/Area Optimization

- ◆ Starting point: fixed architecture



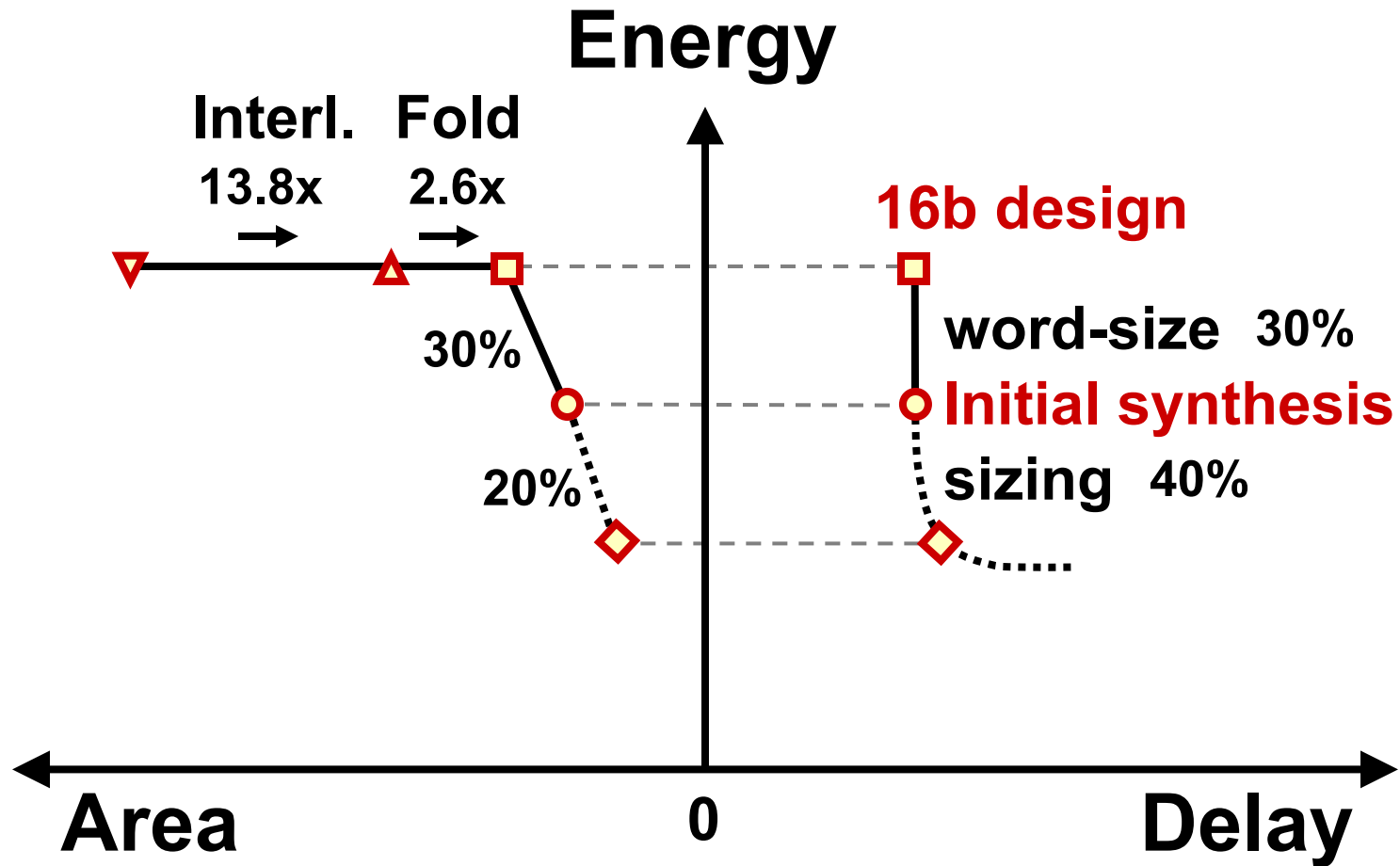
Energy/Area Optimization

- ◆ **Step 1: Word-length optimization**



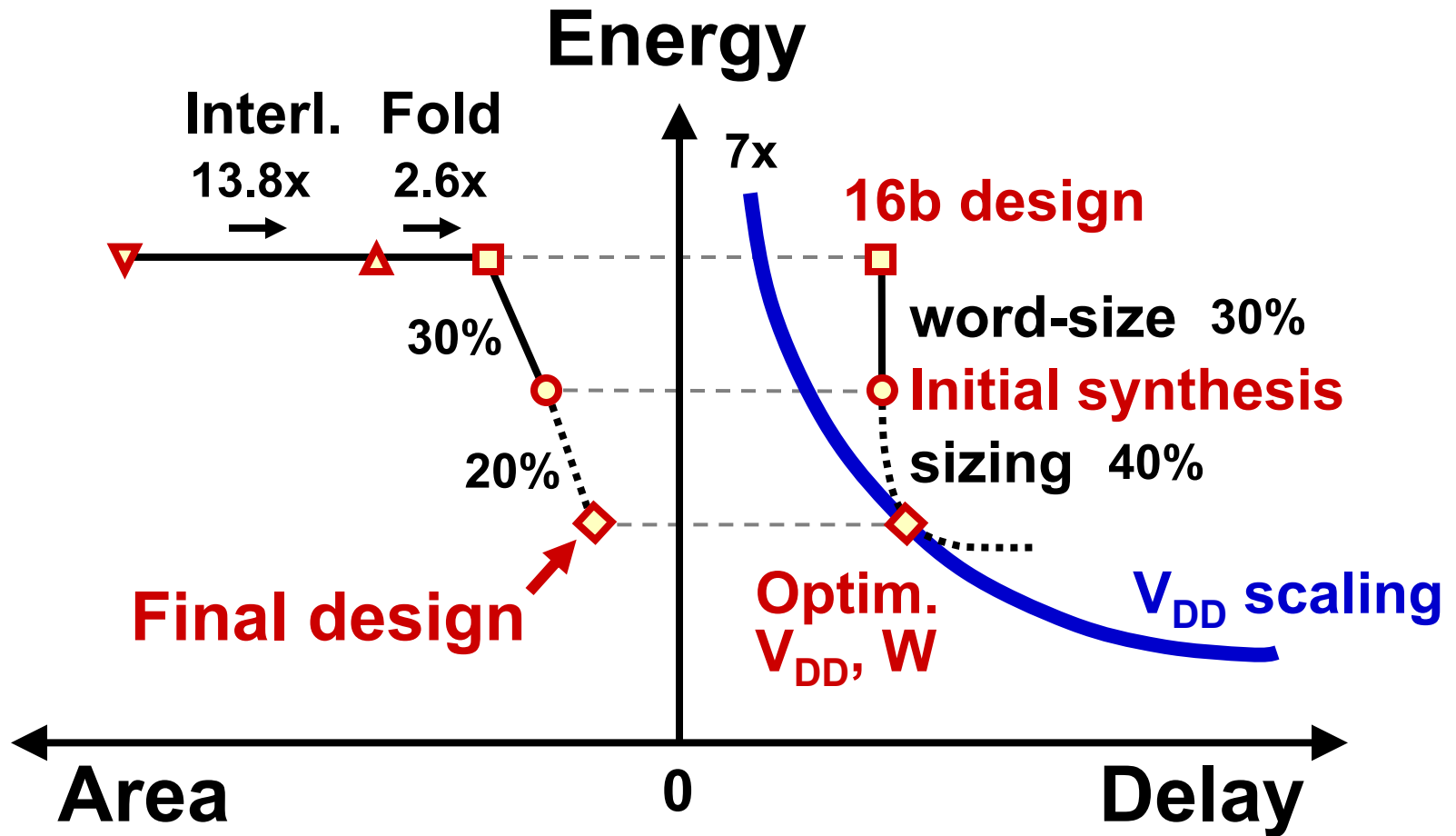
Energy/Area Optimization

- ◆ Step 2: Gate size & V_{DD} optimization



Energy/Area Optimization

- ◆ Step 2: Gate size & V_{DD} optimization



Hardware Results

◆ Result of Energy-Area-Performance Optimization



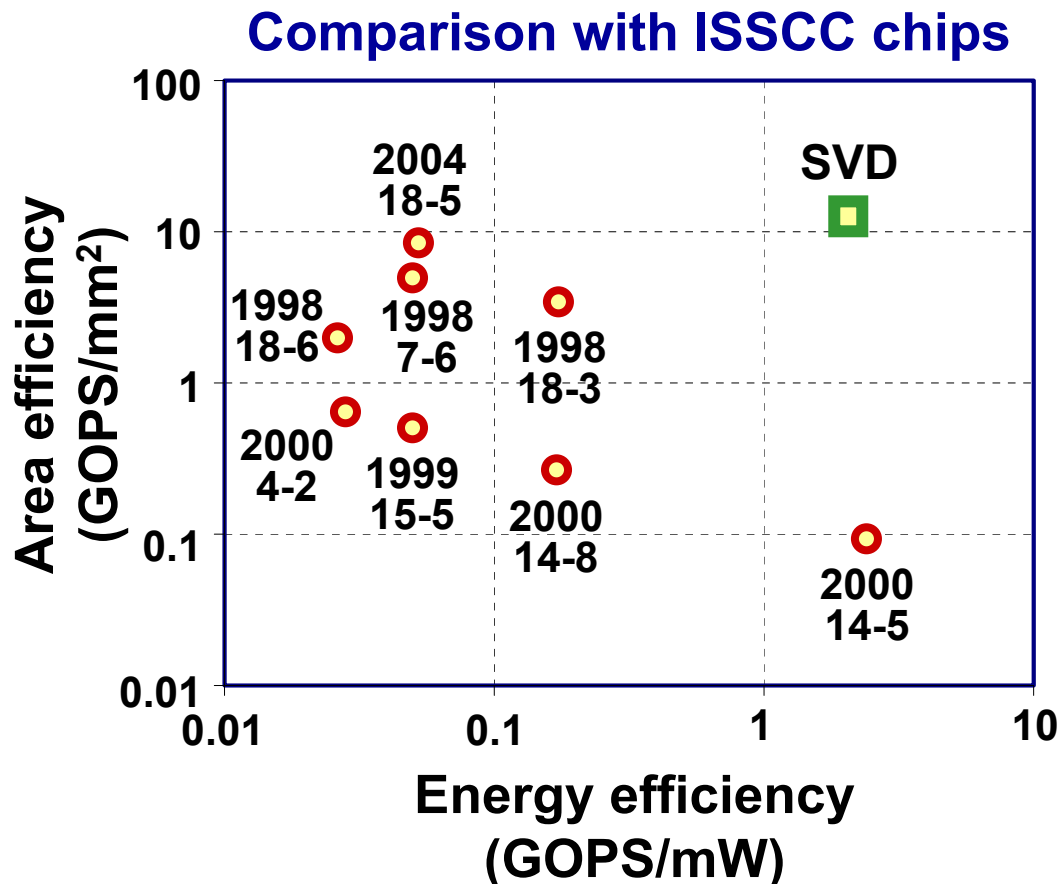
(90nm ST Micro)

◆ 2.1 GOPS/mW

- 70 GOPS @ 100MHz
- Power = 34mW

◆ 20 GOPS/mm²

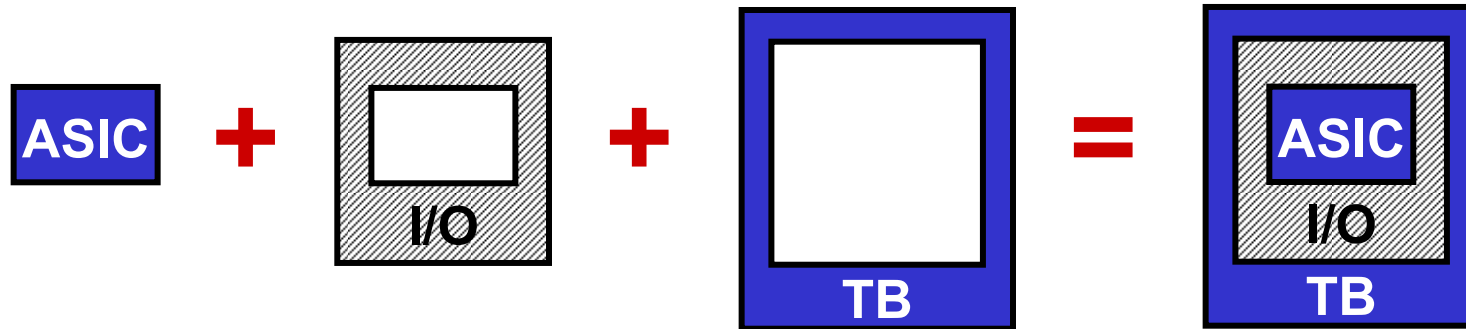
- 70 GOPS in 3.5mm²



[D. Markovic, B. Nikolic, R.W. Brodersen, JSSC Apr'07]

Functional test was performed with FPGA

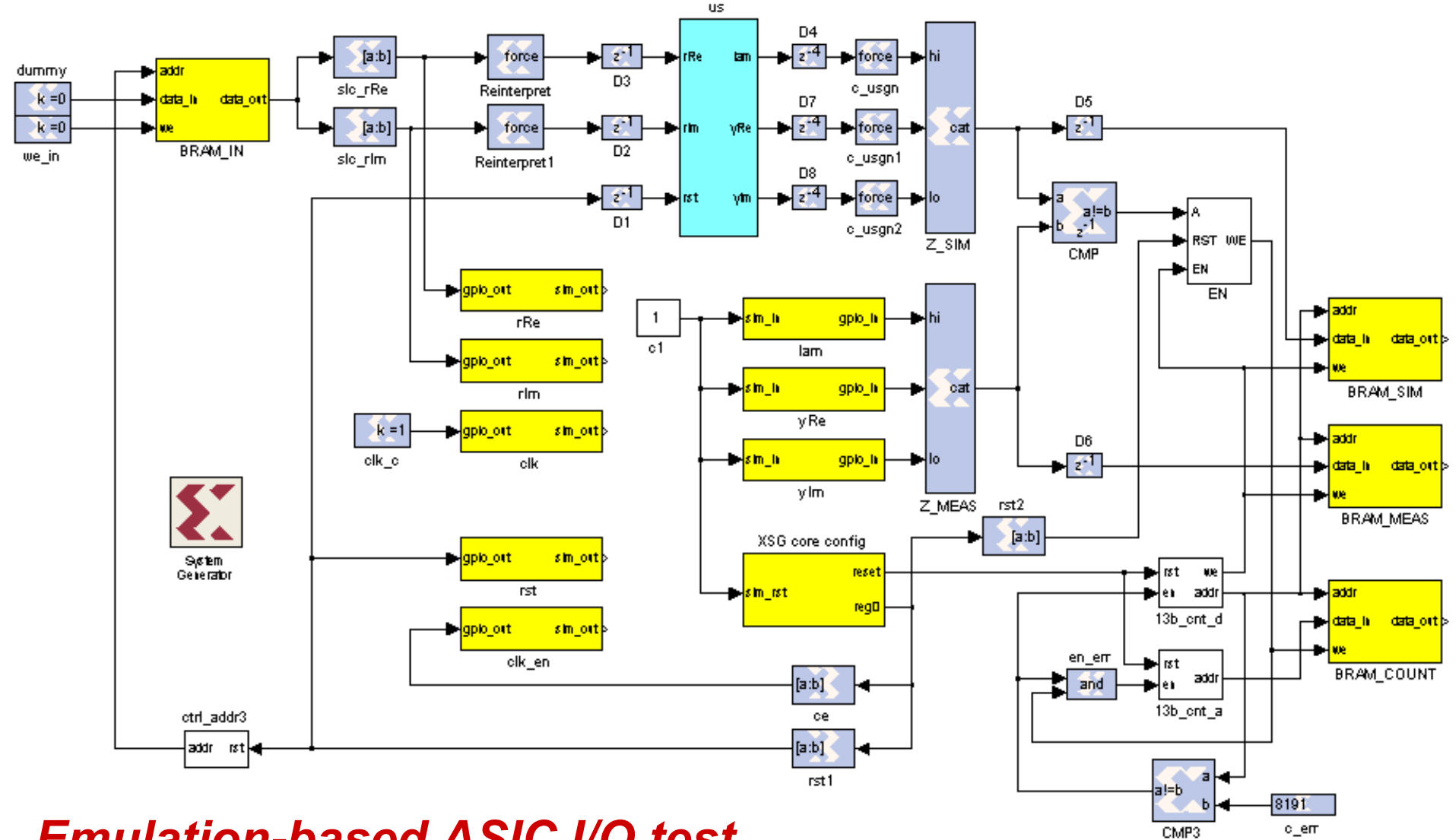
FPGA Based ASIC Verification



- ◆ **Goal: use Simulink testbench (TB) for ASIC verification**
 - Develop custom interface blocks (I/O)
 - Place I/O and ASIC RTL into TB model

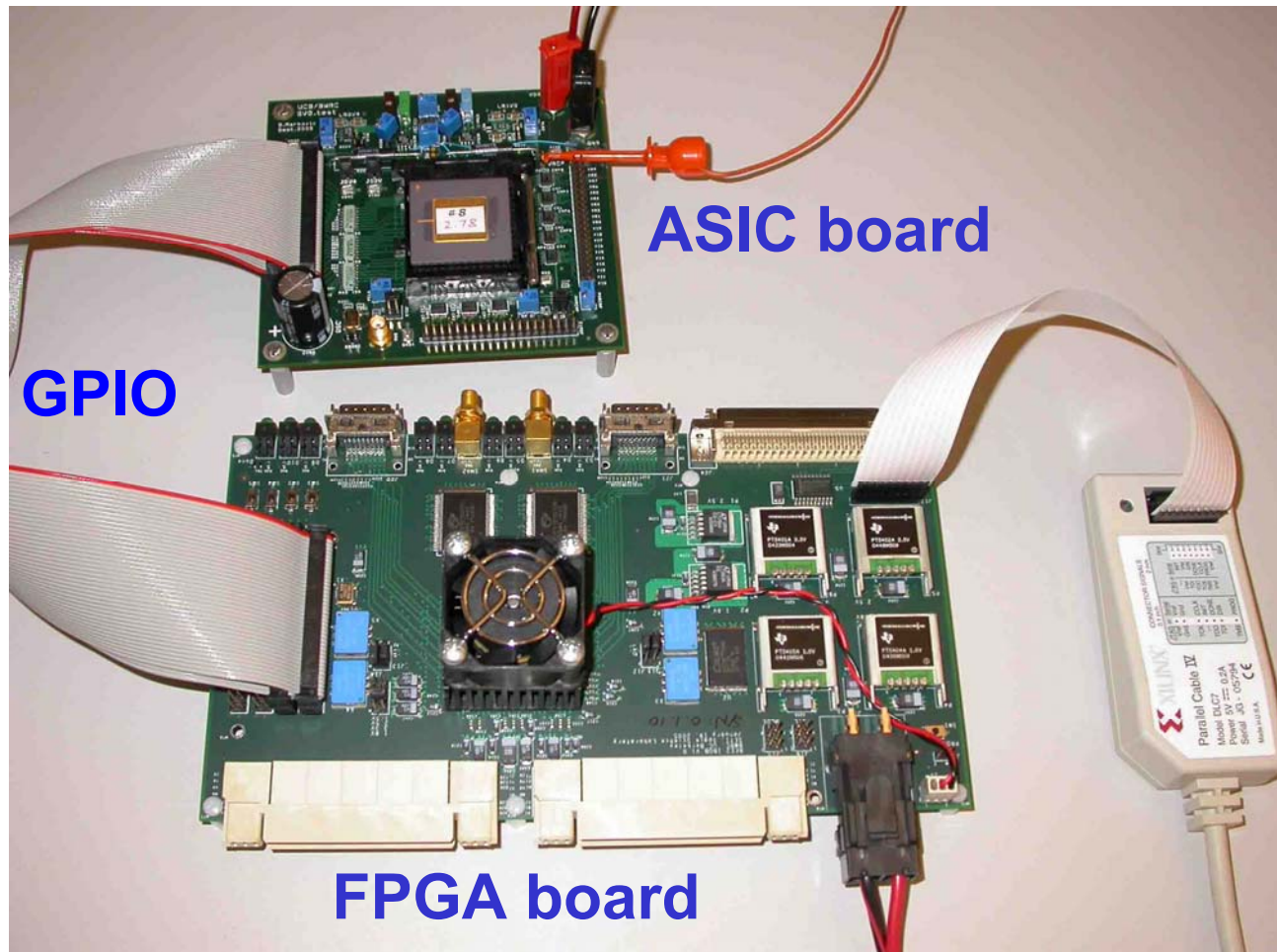
Simulink implicitly provides the testbench

Simulink I/O Test Model for the SVD



Emulation-based ASIC I/O test

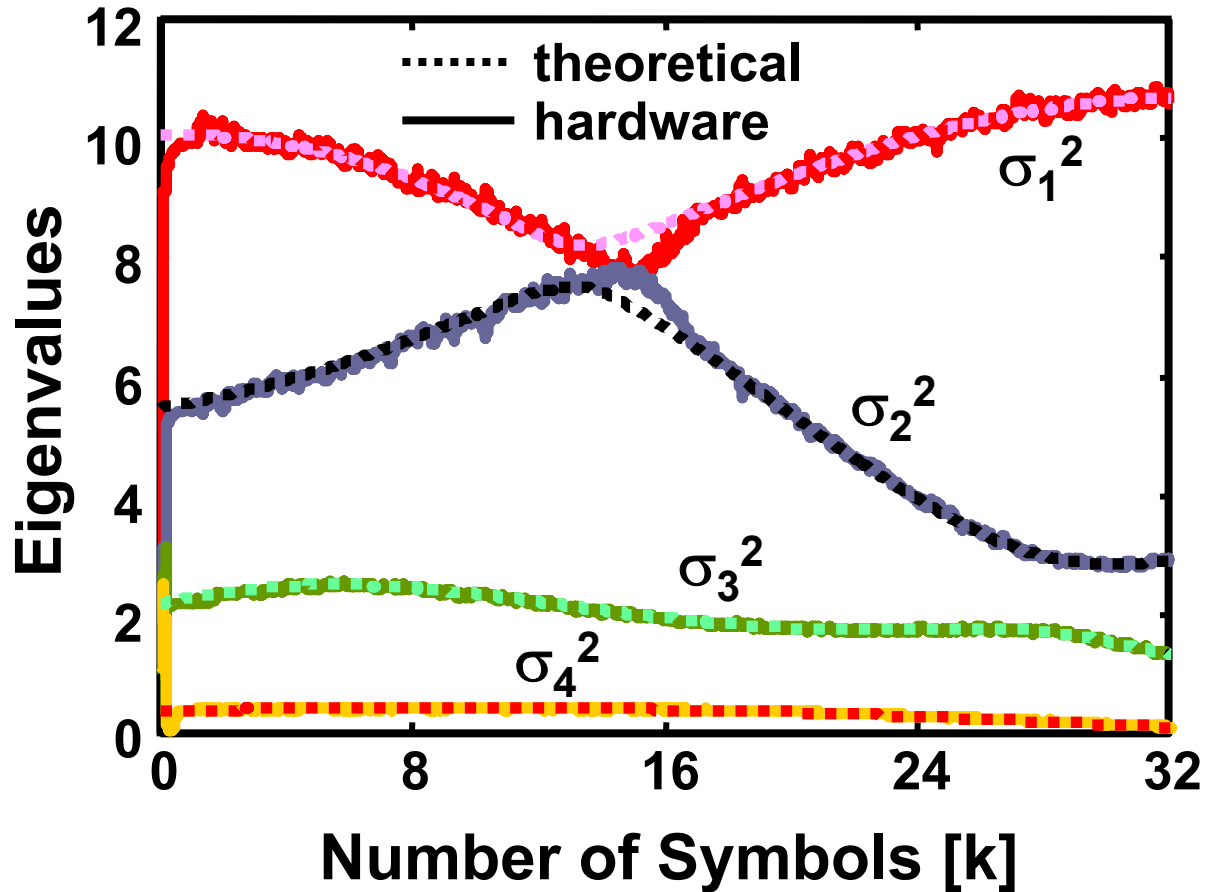
Experimental Setup



Real-time at-speed ASIC verification

Measured Functionality

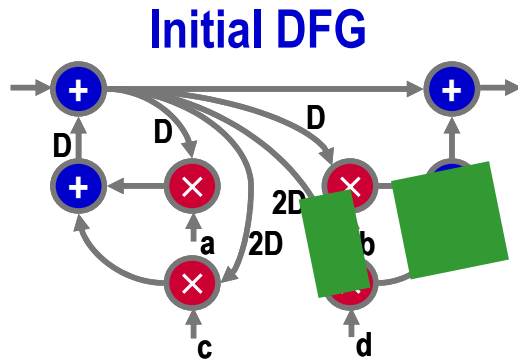
4x4 MIMO channel tracking



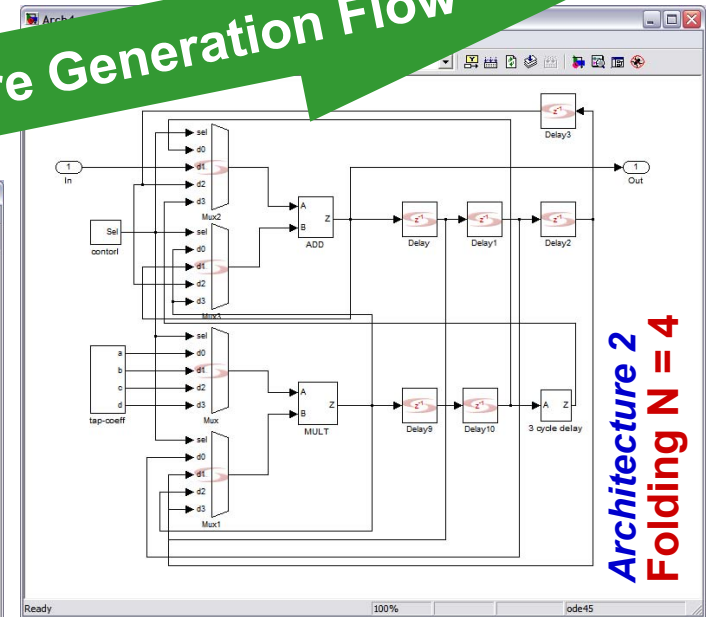
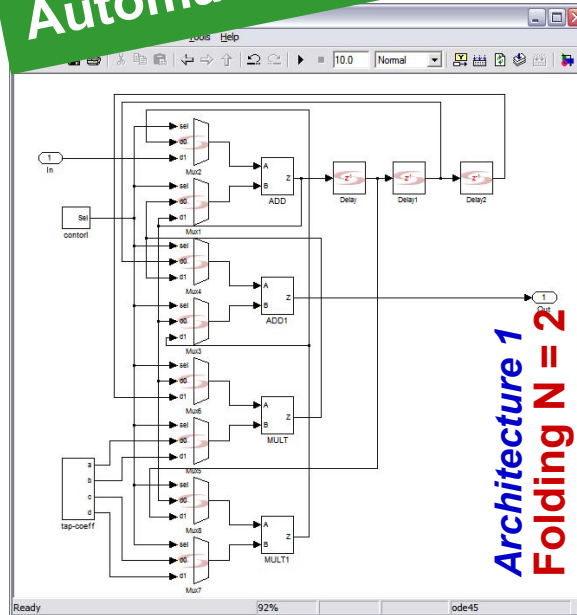
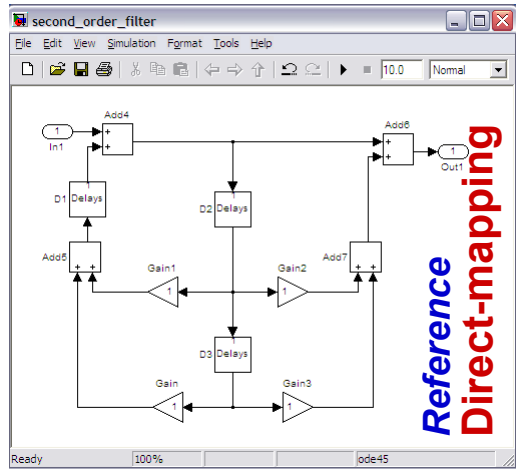
Up to 10 b/s/Hz with adaptive PSK

From Simulink to Optimized Hardware

Direct mapped DFG → Scheduler → Architecture Solutions → Hardware
 (Simulink) (C++ / MOSEK) (Simulink/SynDSP) (FPGA/ASIC)



Automated Architecture Generation Flow

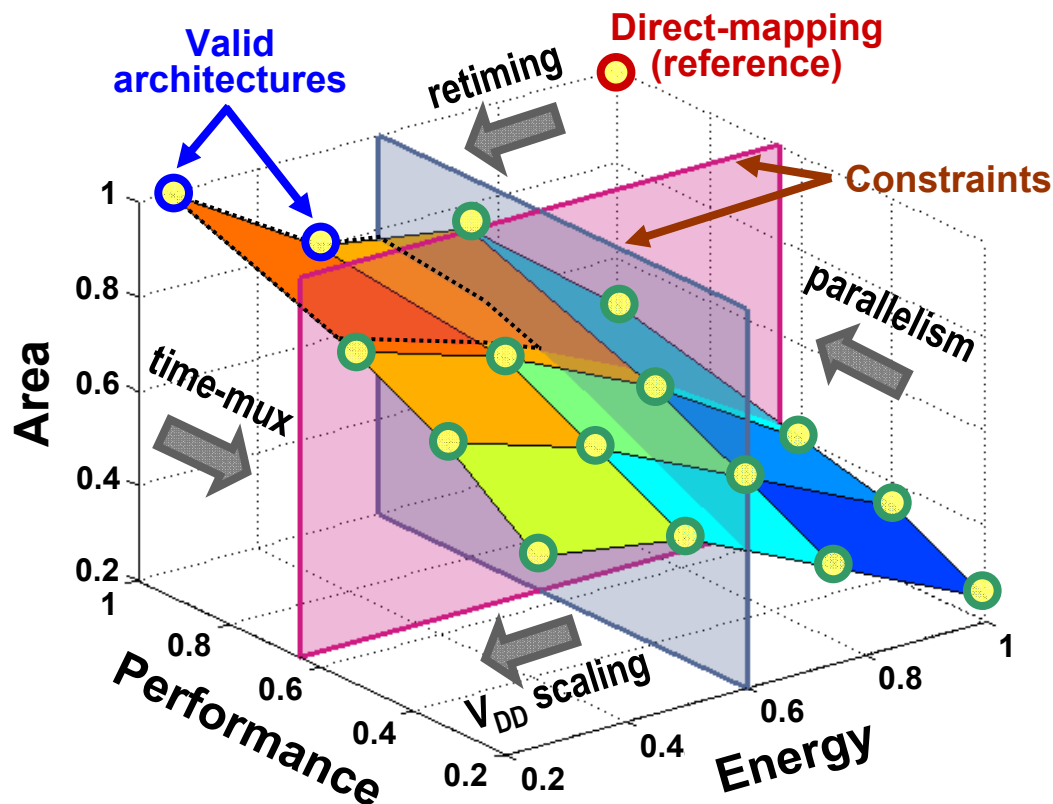


Resulting Simulink/SynDSP Architectures

ILP Scheduling & Bellman-Ford Retiming: optimal + reduced CPU time

Energy-Area-Performance Map

- ◆ Each point on the surface is an optimal architecture automatically generated in Simulink after modified ILP scheduling and retiming



- ◆ System designer can choose from feasible optimal solutions
- ◆ It is not just about functionality, but how good a solution is, and how many alternatives exist

Conclusions

- ◆ **Simulink provides level of abstraction needed for complete ASIC development**
 - Hardware emulation of algorithms
 - Technology-driven architecture selection
 - FPGA-based ASIC verification
 - Logic analysis can be fully ported onto FPGA
- ◆ **Energy-area-delay space is a compact way for comparing multiple architectural realizations**
 - ILP-based formulation automates architecture design
- ◆ **Complex algorithms in 90nm can achieve**
 - 2.1 GOPS/mW, 20 GOPS/mm²

References

◆ ASIC design and verification

- D. Markovic, V. Stojanovic, B. Nikolic, M.A. Horowitz, and R.W. Brodersen, "Methods for True Energy-Performance Optimization," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1282-1293, Aug. 2004.
- D. Markovic, R.W. Brodersen, and B. Nikolic, "A 70GOPS 34mW Multi-Carrier MIMO Chip in 3.5mm²," in *Proc. IEEE Int'l Symp. on VLSI Circuits (VLSI'06)*, June 2006, pp. 196-197.
- D. Markovic, B. Nikolic, R.W. Brodersen, "Power and Area Minimization for Multidimensional Signal Processing," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 922-934, April 2007.
- D. Markovic, C. Chang, B. Richards, H. So, B. Nikolic, and R.W. Brodersen, "ASIC Design and Verification in an FPGA Environment," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC'07)*, Sept. 2007, pp. 737-740.

◆ More publications available online

- www.ee.ucla.edu/~dejan

Acknowledgments

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