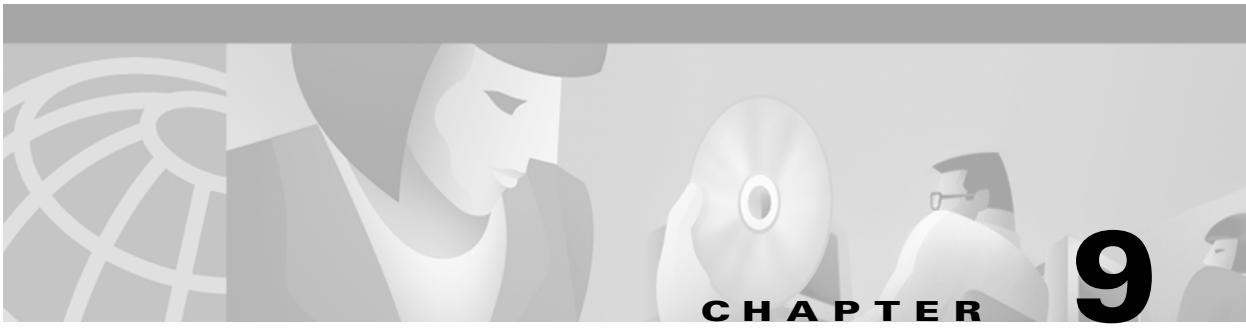


CHAPTER 9

Network Synchronization

MGX 8230 Clock Sources

The clock sources that are available for primary and secondary clock selection are

- Extracted received clock from the daughter card trunking interface (up to two ports)
- Derivative of an externally provided T1 or E1 clock
  - T1 clock rate 1.544 MHz +/- 50 ppm
  - E1 clock rate 2.048 MHz +/- 100 ppm
- Internal oscillator located on the PXM
- Clock provided via the backplane from one of the service modules

Synchronization and Timing Support

The PXM1 supports either a Stratum 3 or Stratum 4 enhanced clock.

The internal clock meets the Stratum 3 and Stratum 4 requirements as detailed in Table 9-1 and Table 9-2.

Table 9-1 Stratum 3 Requirements

Accuracy	Holdover Stability	Pull in Range
4.6xe-6	1xe-8/day	4.6xe-6

Table 9-2 Stratum 4 Requirements

Accuracy	Holdover Stability	Pull in Range
$32x10^{-6}$	no holdover	$32x10^{-6}$

Internal Holdover Capability

The MGX 8230 guarantees an 8 kHz clock speed during the time it switches over to other sources.

The MGX 8230 clock synchronization system meets the following criteria as specified Bellcore GR-1244-CORE, Section 2.6

- pull-in/hold-in range
- input tolerance requirements
- output signal requirements
- alarms, reports, and control commands

The MGX 8230 also supports clock synchronization system redundancy in compliance to GR-1244-CORE, Section 3.3.

External Timing Interfaces

The MGX 8230 accepts external timing from T1 and E1 interfaces. The PXM User Interface card that resides in the upper service bay provides the T1/E1 timing reference ports:

- The PXM-UI back card provides connections to external Stratum 4 clocking sources (see Figure 9-1). A RJ-45 connector labeled “T1 clock” is provided for external T1 clock input and an SMB connector labeled “E1 clock” is provided for E1 clock input.

- The PXM-UI-S3 back card provides connections for external Stratum 3 clocking sources (see Figure 9-2). A RJ-45 connector labeled CLK1 is provided for external T1 or E1 clock input.

Figure 9-1 PXM-UI Rear View

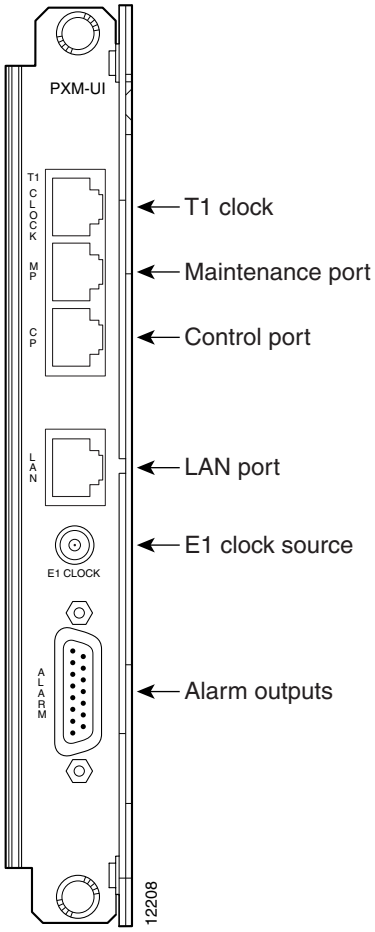
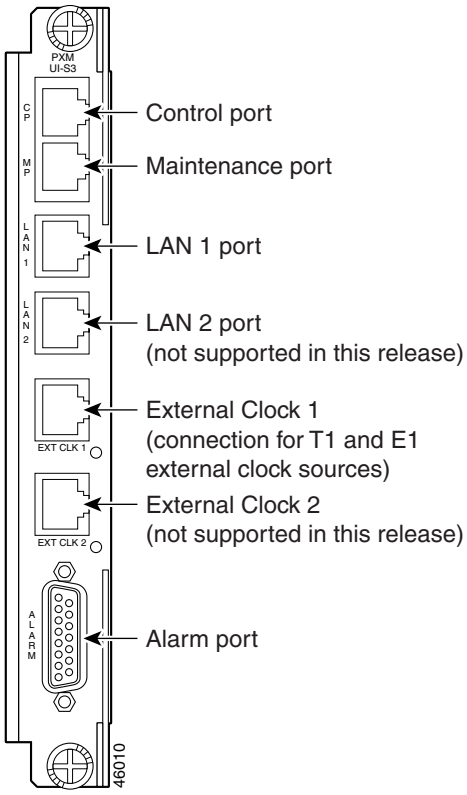


Figure 9-2 PXM-UI-S3 Rear View



E1 Interface Compliance

The E1 interface on the PXM back card has been designed to support both options according to G.703. As per G.703 Table 6, it supports an unframed HDB3 E1 (2048 KBps) signal. According to G.703 Table 10 (now calledTtable 11), it also supports a timing signal of 2048 kHz.

External Timing

MGX 8230 is capable of the following external timing and formats:

- Building Integrated Timing Source (BITS) as specified in Bellcore GR-1244-CORE.
- Minimum of two external timing references (inband and external).
- External timing is the DS1 reference in D4 (SF) format.
- Switching to the alternate timing reference.

The MGX 8230 Edge Concentrator is capable of receiving a minimum of two external timing references on separate physical interfaces. These are provisioned as the active (act) and alternate (alt). The terms act and alt are interchangeable depending on which reference is active, and providing timing reference for the system. The system also provides a DS1 reference for external timing in D4 (SF) format. At least two DS1 synchronization references, as specified in Bellcore GR-1244-CORE, Section 3.4, can be configured.

A switchover from the active clock source (primary or secondary) to the standby clock source will occur when the hardware detects a failure that warrants a switchover. The currently selected clock source is constantly monitored by the hardware to ensure that it is within tolerance.

If a failure in this selected clock is detected, the hardware gracefully switches over to the secondary clock source specified.

If both the primary and secondary sources have failed, the hardware will automatically output the clock generated internally on the card. Once the primary clock is within tolerance, the hardware will automatically switch back to it.

Regardless of whether the clock switchover is initiated by the user or by the hardware, the switchover meets the Accunet T1.5 Maximum Time Interval Error (MTIE) Specification.

When all timing references fail, as specified in Bellcore GR-1244-CORE, Section 3.4.1, the MGX 8230 can operate in self-timing or free-running mode, using an internal clock.

Revertive Clocking

Clocking can be either revertive or non-revertive.

- **Revertive**: If the node is configured such that the clock source fails (either due to a physical failure such as loss of signal, or due to the clock frequency drifting out of specification or a bad frequeny), the node abandons the clock source and finds an alternate clock source. Whenever the original clock source repairs, the node will automatically *revert* to using it.
- **Non-revertive**: The node behaves in exactly the same way as revertive except that whenever the original clock source repairs, the node does *not* automatically *revert* to the original clock source.

Whether a node is revertive or non-revertive depends upon the processor switching back card used and clocking source specified. Please refer to Table 9-3 to determine whether clocking is revertive or non-revertive in your network configuration.

Table 9-3 Revertive Clocking and PXM Back Card Support

Processor Switching Module Back Card	Using External Clock	Using Inband/Service Module Clock
PXM1-UI	For LoS: revertive	For LoS: revertive
	For bad freqeuncy/drift: revertive	For bad freqeuncy/drift: non-revertive
PXM-UI-S3	For LoS: revertive	For LoS: revertive
	For bad freqeuncy/drift: non-revertive	For bad freqeuncy/drift: non-revertive

Continuous Monitoring

The MGX 8230 recognizes the following DS1 impairments or conditions as failures:

- Loss of signal (LoS)
- Alarm Indication Signal (AIS)
- Out of frame (OoF)
- Frequency Offset, monitor frequency offset from BITS

Generating Alarms

Alarms are generated when a synchronization source, either active or standby, fails for some reason. Clocking failures do not affect any configuration or settings on either the PXM 1 or PXM45.

Software/Hardware Upgrades

Switch software upgrades do not cause changes in timing sources. A Y-cable is used to connect the external clock associated with both the active and standby processor cards. Part of the normal switch software upgrade process is a PXM switchover, the Y-cable will ensure clocking integrity to the external source.