



CHAPTER 4

Configuring a Supervisor Engine 32 PISA

This chapter describes how to configure a Supervisor Engine 32 PISA (Supervisor Engine 32 with a programmable intelligent services accelerator) in a Catalyst 6500 series switch. This chapter contains these sections:

- [Flash Memory on a Supervisor Engine 32 PISA, page 4-2](#)
- [Supervisor Engine 32 PISA Ports, page 4-2](#)
- [Configuring Full PISA EtherChannel Bandwidth, page 4-3](#)
- [Displaying PISA Platform Statistics, page 4-4](#)



Note

- For complete syntax and usage information for the commands used in this chapter, see the *Catalyst Supervisor Engine 32 PISA Cisco IOS Command Reference*, Release 12.2ZY, at this URL: <http://www.cisco.com/en/US/docs/switches/lan/catalyst6500/ios/12.2ZY/command/reference/cmdref.html>
 - This is the minimum required Supervisor Engine 32 PISA memory:
 - 512-MB DRAM on the Supervisor Engine 32
 - 1-GB DRAM on the PISA daughterboard
 - Supervisor Engine 32 PISA has a PFC3B and operates in PFC3B mode.
 - With a 3-slot or a 4-slot chassis, install the Supervisor Engine 32 PISA in either slot 1 or 2.
 - With a 6-slot or a 9-slot chassis, install the Supervisor Engine 32 PISA in either slot 5 or 6.
 - With a 13-slot chassis, install the Supervisor Engine 32 PISA in either slot 7 or 8.
 - Supervisor Engine 32 PISA does not support switch fabric connectivity.
 - For information about the hardware and software features supported by the Supervisor Engine 32 PISA, see the *Release Notes for Cisco IOS Release 12.2ZY on the Supervisor Engine 32 PISA* at this URL: http://www.cisco.com/en/US/docs/switches/lan/catalyst6500/ios/12.2ZY/release/notes/ol_13011.html
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Flash Memory on a Supervisor Engine 32 PISA

The Supervisor Engine 32 PISA has these flash memory devices:

- **disk0:**
 - One external CompactFlash Type II slot
 - Supports CompactFlash Type II flash PC cards
- **sup-bootdisk:**
 - Supervisor Engine 32 256-MB internal CompactFlash flash memory
 - From the Supervisor Engine 32 ROMMON, it is **bootdisk:**
- **bootdisk:**
 - PISA 256-MB internal CompactFlash flash memory
 - Not accessible from the Supervisor Engine 32 ROMMON

Supervisor Engine 32 PISA Ports

These sections describe the ports on a Supervisor Engine 32 PISA:

- [Supervisor Engine 32 PISA Management Ports, page 4-2](#)
- [Supervisor Engine 32 PISA Data Ports, page 4-2](#)

Supervisor Engine 32 PISA Management Ports

The console port for the Supervisor Engine 32 PISA port is an EIA/TIA-232 (RS-232) port. The Supervisor Engine 32 PISA also has two Universal Serial Bus (USB) 2.0 ports that currently are not enabled.

Supervisor Engine 32 PISA Data Ports

The WS-S32-10GE-PISA has these ports:

- Ports 1 and 2: XENPAK 10 Gigabit Ethernet
- Port 3: 10/100/1000 Mbps RJ-45



Note

- To avoid unexpected application of QoS to the [PISA EtherChannel](#), do not configure QoS on WS-S32-10GE-PISA ports.
- You can disable Port 3 and reallocate its port ASIC capacity to the PISA EtherChannel (see the [“Configuring Full PISA EtherChannel Bandwidth”](#) section on page 4-3 section).

The WS-S32-GE-PISA has these ports:

- Ports 1 through 8: Small form-factor pluggable (SFP) Gigabit Ethernet
- Port 9: 10/100/1000 Mbps RJ-45 port



Note

- To avoid unexpected application of QoS to the [PISA EtherChannel](#), do not configure QoS on WS-S32-GE-PISA ports.
- You can disable port 9 and reallocate its port ASIC capacity to the PISA EtherChannel (see the [“Configuring Full PISA EtherChannel Bandwidth”](#) section on page 4-3 section).

Configuring Full PISA EtherChannel Bandwidth

A Supervisor Engine 32 PISA automatically creates an EtherChannel (port channel interface 256) that the Supervisor Engine 32 and the PISA daughterboard use to communicate with each other. By default, the PISA EtherChannel bandwidth is 1 Gbps. To increase the PISA EtherChannel bandwidth, you can disable supervisor engine ports and reallocate the port ASIC capacity to the PISA EtherChannel.

To increase the PISA EtherChannel bandwidth, perform this task:

	Command	Purpose
Step 1	Router(config)# interface gigabitethernet slot/3	On a WS-S32-10GE-PISA, selects the Ethernet port to be configured.
	Or: Router(config)# interface gigabitethernet slot/[8 9]	On a WS-S32-GE-PISA, selects the Ethernet port to be configured. Note On a WS-S32-GE-PISA, you can allocate both ports 8 and 9 to the PISA EtherChannel.
Step 2	Router(config-if)# channel-group 256 mode on	Disables the port and allocates its port ASIC capacity to the PISA EtherChannel.
	Router(config-if)# no channel-group 256 mode on	Reverts to the default port ASIC capacity allocation.



Note

- You cannot enter any configuration under port channel interface 256.
- After the port becomes a member of the PISA EtherChannel, only the **no channel-group 256 mode on** command has any effect on the port until the port is no longer a member of the PISA EtherChannel. While the port is a member of the PISA EtherChannel, all port configuration commands except the **[no] channel-group 256 mode on** command are ignored.
- The PISA EtherChannel MTU size is 4,096 bytes.

This example shows how to allocate the port ASIC capacity of port 3 to the PISA EtherChannel on a WS-S32-10GE-PISA that is installed in slot 5:

```
Router# configure terminal
Router(config)# interface gigabitethernet 5/3
Router(config-if)# channel-group 256 mode on
Router(config-if)# end
```

This example shows how to allocate the port ASIC capacity of port 9 to the PISA EtherChannel on a WS-S32-GE-PISA that is installed in slot 5:

```
Router# configure terminal
Router(config)# interface gigabitethernet 5/9
Router(config-if)# channel-group 256 mode on
Router(config-if)# end
```

Displaying PISA Platform Statistics

To display platform statistics for the Supervisor Engine 32 PISA, perform this task:

Command	Purpose
Router# show platform pisa np <i>counter-type</i> counters	Displays platform statistics for the Supervisor Engine 32 PISA. <i>counter-type</i>—See Table 4-1 for the list of valid values.

[Table 4-1](#) shows the available counters.

Table 4-1 PISA Platform Counters

Counter-type	Description
me num	Microengine information (valid <i>num</i> values are from 0 to 15)
acl	ACL counter information
all	All Supervisor Engine 32 PISA-specific counters
all pps	Packets per second (pps) for all Supervisor Engine 32 PISA-specific counters
fpm	Flexible packet matching (FPM) counters
mqc	Modular QoS CLI information
nbar	Network-based application recognition (NBAR) counter information
rx	Receive engine counters
tx	Transmit engine counters

For examples of the **show platform pisa np** command output, see the *Catalyst Supervisor Engine 32 PISA Cisco IOS Command Reference*, Release 12.2ZY, at this URL:

<http://www.cisco.com/en/US/docs/switches/lan/catalyst6500/ios/12.2ZY/command/reference/cmdref.html>

To clear platform counters for the Supervisor Engine 32 PISA, perform this task:

Command	Purpose
Cisco IOS Release 12.2(33)ZYA and earlier releases Router# clear platform pisa ixp counters <i>counter-type</i>	Displays platform statistics for the Supervisor Engine 32 PISA. <i>counter-type</i>—See Table 4-1 for the list of valid values.
Cisco IOS Release 12.2(33)ZYA1 and later releases Router# clear platform pisa np <i>counter-type</i> counters	

This example shows how to clear the ACL counters in Cisco IOS Release 12.2(33)ZYA1 and later releases:

```
Router# clear platform pisa np acl counters
```

