



Per VC Error Display

The **show controllers atm** command was modified:

- To enable the output of CRC error counts on a per-VC basis
- To display only SAR controller information as the default output
- With new options for controlling the output

Supported Platforms

This feature is supported on the Cisco 6400 node route processor (NRP).

Supported Standards, MIBs, and RFCs

None

Configuration Tasks

None

Command Reference

- **show controllers atm**

show controllers atm

To display information on the physical ATM interface of the Cisco 6400 NRP, use the **show controllers atm 0/0/0** privileged EXEC command.

```
show controllers atm 0/0/0 [detailed | scheduler | vc vpi/vci]
```

Syntax	Description
0/0/0	<i>slot/subslot/port</i> entry for the physical ATM interface of the Cisco 6400 NRP
detailed	Output shows all available information
scheduler	Output shows SAR scheduler information
vc	Output shows information for the specified VC
<i>vpi/vci</i>	Virtual path identifier (VPI) and virtual channel identifier (VCI) of the VC

Defaults The default output shows only SAR controller information.

Command Modes Privileged EXEC

Command History	Release	Modification
	11.2 GS	This command was introduced.
	12.0(5)DA	This command was first supported on the Cisco 6260.
	12.0(5)XE	This command was first supported on the Cisco 7200 and 7500 series routers.
	12.0(5)T and 12.0(5)XK	This command was modified to support IMA groups on the Cisco 2600 and 3600 series routers.
	12.0(7)XE1	This command was first supported on the Cisco 7100 series routers.
	12.1(3) DC	This command was modified from its original version, with no display options, for the Cisco 6400 node route processor (NRP): <ul style="list-style-type: none"> • To enable the output of CRC error counts on a per-VC basis. • To display only SAR controller information as the default output. • With new options for controlling the output to include error counters on a per-VC basis.

Examples

In the following example, the output consists only of the SAR controller information:

```

NRP# show controllers atm 0/0/0
Interface ATM0/0/0
Hardware is ATM-SAR
PCI registers:
  bus_no=0, device_no=4
  CFID=0xA102104C, CFCs=0x02000006, CFRV=0x02030002, CFLT=0x0000FF00
  CFBA=0x4A000000, CFIT=0x02010100

*** TI1575 SAR at address 0x3A000000 ***
Receive/Transmit Statistics
rx_isrs:          0          rx_isr_pkts:   1          rx_isr_bufs:    0
rx_cells_ovf:    0          tx_cells_ovf:  0          hec_errors_ovf: 0
rx_unkn_prot:   314        rx_aal5_disc:  0          rx_pkt_ovf:     0
unkn_prot_ovf:  0          aal5_disc_ovf: 0          tx_count:       0
rx_crc_error:   0          rx_no_buf:     0          rx_timeout:     0
rx_abort:       0          rx_cong_cells: 0          rx_freeze:      0
rx_no_valbuf:   0          rx_bad_vc:    0          fallback_act:   0
tx_abort:       0          tx_no_desc:   0          tx_align:       0
tx_freeze:      0          disabled:     0          enabled:        0
tx_clones:      0          tx_xmt_paks:  3          teardown_vc:    0
tx_pend_count_negative: 0
tx_forced:      0          (0)
tx_max_queued:  6144        seg_ring_size: 32
tx output drops: 0
  pkt_too_big:  0          tx_pak_failed: 0
  idb_down:     0          invalid_pkt_type: 0
  invalid_vcd:  0          vc_ring_full:   0
  over_max_queued: 0          slot_owned_by_chip: 0
  vc_not_in_use: 0
invalid_addr_count: 0

PCI Statistics
detect_parity    0          system_error    0          master_abort    0
rx_target_abort  0          sig_target_abort 0          data_parity     0

Internal registers
config: 0x6037          status: 0x2000040          imask: 0xC381
ratcount: 0x800          globrat: 0x79          rxunkn: 0x10000010
txcompsize: 0x7FF          rxcompsize: 0x1FF          txsegsz: 0x1F
aal5discard:0x0          hecerrors: 0x0          unknp: 0x14C
rxcells: 0x1          txcells: 0x1B          schedsize: 0x1
txqueue: 0x80002009 (spinerr:0)          txpause: 0x0          chancount: 0x5
txcompring: 0x311A00C          rxcompring: 0x3114020

Structures common to all VCs
receive free buffer ring
  address: 0x3110820          buf size: 10          ring size: 63          sar_indx: 1          drv_indx: 1
receive completion ring
  addr: 0x3114000          indx: 1
transmit completion ring
  addr: 0x311A000          indx: 3

```

In the following example, the output consists of all available information:

```

NRP# show controllers atm 0/0/0 detailed
Interface ATM0/0/0
Hardware is ATM-SAR
PCI registers:
  bus_no=0, device_no=4
  CFID=0xA102104C, CFCS=0x02000006, CFRV=0x02030002, CFLT=0x0000FF00
  CFBA=0x4A000000, CFIT=0x02010100

*** TI1575 SAR at address 0x3A000000 ***
Receive/Transmit Statistics
rx_isrs:          0          rx_isr_pkts:    1          rx_isr_bufs:    0
rx_cells_ovf:    0          tx_cells_ovf:    0          hec_errors_ovf: 0
rx_unkn_prot:    514        rx_aal5_disc:    0          rx_pkt_ovf:     0
unkn_prot_ovf:  0          aal5_disc_ovf:  0          tx_count:       0
rx_crc_error:    0          rx_no_buf:       0          rx_timeout:     0
rx_abort:        0          rx_cong_cells:   0          rx_freeze:      0
rx_no_valbuf:    0          rx_bad_vc:       0          fallback_act:   0
tx_abort:        0          tx_no_desc:      0          tx_align:       0
tx_freeze:       0          disabled:        0          enabled:        0
tx_clones:       0          tx_xmt_paks:     3          teardown_vc:    0
tx_pend_count_negative: 0
tx_forced: 0          (0)
tx_max_queued:    6144        seg_ring_size:   32
tx output drops:  0
  pkt_too_big:    0          tx_pak_failed:   0
  idb_down:       0          invalid_pkt_type: 0
  invalid_vcd:    0          vc_ring_full:    0
  over_max_queued: 0          slot_owned_by_chip: 0
  vc_not_in_use:  0
invalid_addr_count: 0

PCI Statistics
detect_parity    0          system_error    0          master_abort    0
rx_target_abort  0          sig_target_abort 0          data_parity     0

Internal registers
config:          0x6037        status:          0x2000040    imask:           0xC381
ratcount:        0x800        globrat:         0x79          rxunkn:          0x10000010
txcompsize:      0x7FF        rxcompsize:     0x1FF        txsegsz:         0x1F
aal5discard:     0x0          hecerrors:      0x0          unknprot:        0x214
rxcells:         0x1          txcells:        0x1B          schedsize:       0x1
txqueue:         0x80002009 (spinerr:0)    txpause:        0x0          chancount:       0x5
txcompring:     0x311A00C    rxcompring:     0x3114020

Structures common to all VCs
receive free buffer ring
  address: 0x3110820  buf size: 10  ring size: 63  sar_indx: 1  drv_indx: 1
receive completion ring
  addr: 0x3114000  indx: 1
transmit completion ring
  addr: 0x311A000  indx: 3

*** VC information and associated 1575 structures ***
seg ring: 5          ringaddr: 0x311C400  ringindx:0      pendindx:0
tx dma: 5          ctrlring: 0xC47100  pktcnt: 0
rword10: 0x0          rword11: 0x0
rword20: 0x0          rword21: 0x0          rword22: 0x0          rword23: 0x0
pxmt 0          queued: 0
VCs mapped to this ring
vcd: 1          cellhdr: 0x1E00640  encap: 0          crcerror: 0
rx dma: 5          config: 0x24000000  ctrlrxring: 0x80000200  timecnt: 0xC8000

```

```

lookup: 2      channel: 5      vpvpci:      0x1E0064
seg ring: 6    ringaddr: 0x311C480    ringindx:0   pendindx:0
tx dma:  6    ctrlring: 0xC47120    pktcnt:      0
rword10: 0x0      rword11: 0x0
rword20: 0x0      rword21: 0x0      rword22: 0x0      rword23: 0x0
pxmt     0    queued:  0
VCs mapped to this ring
vcd:     2      cellhdr: 0x2800C80    encap:       0      crcerror: 0
rx dma:  6    config:  0x24000000    ctrlrxring: 0x80000400    timecnt: 0xC8000
lookup:  3    channel:  6      vpvpci:      0x2800C8
seg ring: 7    ringaddr: 0x311C500    ringindx:0   pendindx:0
tx dma:  7    ctrlring: 0xC47140    pktcnt:      0
rword10: 0x0      rword11: 0x0
rword20: 0x0      rword21: 0x0      rword22: 0x0      rword23: 0x0
pxmt     0    queued:  0
VCs mapped to this ring
vcd:     3      cellhdr: 0xA0      encap:       0      crcerror: 0
rx dma:  7    config:  0x24000000    ctrlrxring: 0x80000600    timecnt: 0xC8000
lookup:  0    channel:  7      vpvpci:      0xA
seg ring: 8    ringaddr: 0x311C580    ringindx:0   pendindx:0
tx dma:  8    ctrlring: 0xC47160    pktcnt:      0
rword10: 0x0      rword11: 0x0
rword20: 0x0      rword21: 0x0      rword22: 0x0      rword23: 0x0
pxmt     0    queued:  0
VCs mapped to this ring
vcd:     4      cellhdr: 0x500      encap:       0      crcerror: 0
rx dma:  8    config:  0x24000000    ctrlrxring: 0x80000800    timecnt: 0xC8000
lookup:  1    channel:  8      vpvpci:      0x50
seg ring: 9    ringaddr: 0x311C600    ringindx:3   pendindx:3
tx dma:  9    ctrlring: 0xC47183    pktcnt:      0
rword10: 0x663C0000    rword11: 0x33CE274
rword20: 0x0      rword21: 0x33CDFC4    rword22: 0x0      rword23: 0x0
pxmt     0    queued:  0
VCs mapped to this ring
vcd:     5      cellhdr: 0x3200640    encap:       0      crcerror: 0
rx dma:  9    config:  0x24000000    ctrlrxring: 0x80000A00    timecnt: 0xC8000
lookup:  4    channel:  9      vpvpci:      0x320064

```

*** TI1585/1585 Scheduler at address 0x3A040000 ***

Configuration/Statistics

```

line bw:  149760    min vc bw: 64      total slots: 2
free slots: 2

```

1585 internal registers

```

config:  0x227      status:  0x1E      imask:  0x0
clkfreq: 0x18FCA1    revnum:  0x0      acrlow:  0x80000000
acrok:   0x80000000

```

1585 connection config/status

```

scheduler id 5
  type: VBR      pcr: 353207    scr: 353207    mbs: 91
rtv: 0x100
scheduler id 6
  type: VBR      pcr: 353207    scr: 353207    mbs: 91
rtv: 0x100
scheduler id 7
  type: VBR      pcr: 353207    scr: 353207    mbs: 91
rtv: 0x100
scheduler id 8
  type: VBR      pcr: 353207    scr: 353207    mbs: 91
rtv: 0x100
scheduler id 9
  type: VBR      pcr: 353207    scr: 353207    mbs: 91
rtv: 0x100

```

In the following example, the output consists of only the SAR scheduler information:

```

NRP# show controllers atm 0/0/0 scheduler
Interface ATM0/0/0
Hardware is ATM-SAR
PCI registers:
  bus_no=0, device_no=4
  CFID=0xA102104C, CFCS=0x02000006, CFRV=0x02030002, CFLT=0x0000FF00
  CFBA=0x4A000000, CFIT=0x02010100

*** TI1585/1585 Scheduler at address 0x3A040000 ***
Configuration/Statistics
  line bw: 149760   min vc bw: 64   total slots: 2
  free slots: 2

1585 internal registers
config: 0x227      status: 0x1E      imask: 0x0
clkfreq: 0x18FCA1  revnum: 0x0      acrlow: 0x80000000
acrok: 0x80000000

1585 connection config/status
scheduler id 5
  type: VBR      pcr: 353207   scr: 353207   mbs: 91
rtv: 0x100
scheduler id 6
  type: VBR      pcr: 353207   scr: 353207   mbs: 91
rtv: 0x100
scheduler id 7
  type: VBR      pcr: 353207   scr: 353207   mbs: 91
rtv: 0x100
scheduler id 8
  type: VBR      pcr: 353207   scr: 353207   mbs: 91
rtv: 0x100
scheduler id 9
  type: VBR      pcr: 353207   scr: 353207   mbs: 91
rtv: 0x100

```

In the following example, the VC output consists only of information specific to VC 50/100:

```

NRP# show controllers atm 0/0/0 vc 50/100
Interface ATM0/0/0
Hardware is ATM-SAR
PCI registers:
  bus_no=0, device_no=4
  CFID=0xA102104C, CFCS=0x02000006, CFRV=0x02030002, CFLT=0x0000FF00
  CFBA=0x4A000000, CFIT=0x02010100

*** VC information and associated 1575 structures ***
seg ring: 9      ringaddr: 0x311C600   ringindx:3   pendindx:3
tx dma: 9      ctrlring: 0xC47183   pktcnt: 0
rword10: 0x663C0000  rword11: 0x33CE274
rword20: 0x0      rword21: 0x33CDFC4   rword22: 0x0      rword23: 0x0
pxmt 0      queued: 0
VCs mapped to this ring
vcd: 5      cellhdr: 0x3200640   encap: 0      crcerror: 0
rx dma: 9      config: 0x24000000   ctrlrxring: 0x80000A00   timecnt: 0xC8000
lookup: 4      channel: 9      vpivci: 0x320064

```

In the following example, the output displays CRC error counters for each configured VC:

```
NRP# show controllers atm 0/0/0 detailed | include crc
rx_crc_error: 0          rx_no_buf: 0          rx_timeout: 0
vcd: 1    cellhdr: 0x1E00640  encap: 0          crcerror: 0
vcd: 2    cellhdr: 0x2800C80  encap: 0          crcerror: 0
vcd: 3    cellhdr: 0xA0       encap: 0          crcerror: 0
vcd: 4    cellhdr: 0x500      encap: 0          crcerror: 0
vcd: 5    cellhdr: 0x3200640  encap: 0          crcerror: 0
```

Related Commands

Command	Description
show atm interface	Displays ATM-specific information about an ATM interface.
show atm pvc	Displays all ATM PVCs and traffic information.
show atm traffic	Displays current global ATM traffic information to and from all ATM networks connected to the router.
show atm vc	Displays the ATM layer connection information about the virtual connections.

Glossary

CRC—cyclic redundancy check. Error-checking technique in which the frame recipient calculates a remainder by dividing frame contents by a prime binary divisor and compares the calculated remainder to a value stored in the frame by the sending node.

SAR—segmentation and reassembly. One of the two sublayers of the AAL CPCS, responsible for dividing (at the source) and reassembling (at the destination) the PDUs passed from the CS. The SAR sublayer takes the PDUs processed by the CS and, after dividing them into 48-byte pieces of payload data, passes them to the ATM layer for further processing.

VC—virtual channel. Logical circuit created to ensure reliable communication between two network devices. A VC is defined by a VPI/VCI pair, and can be either permanent (PVC) or switched (SVC).