



CHAPTER 11

Overview of Gigabit Ethernet SPAs

This chapter provides an overview of the release history, supported features, Management Information Base (MIB) support, and architecture for the Gigabit Ethernet SPAs on the Cisco uBR10012 router.

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Release History

Release	Modification
12.2(33)SCB	Support for the following SPAs was introduced on the Cisco 10000 SIP-600 on the Cisco uBR10012 router: <ul style="list-style-type: none">• 1-Port 10-Gigabit Ethernet Shared Port Adapter, Version 2• 5-Port Gigabit Ethernet Shared Port Adapter, Version 2

Supported Features

Some of the significant hardware and software features supported by the Gigabit Ethernet SPAs on the Cisco uBR10012 router include:

- Autonegotiation (supported only on the Cisco 5-Port Gigabit Ethernet SPA)
- Speed negotiation
- Duplex negotiation
- Full-duplex operation
- EtherChannel bundles
- IEEE 802.1Q VLAN termination

- Up to 4000 VLANs per port and 8000 VLANs per SPA
- Jumbo frames support (9000 bytes)
- Support for command-line interface (CLI)-controlled OIR
- 802.3x flow control
- 802.3ad link bundling
- 802.1Q and QinQ for SIP oversubscription
- QinQ push/pop/swap functions
- QinQ configuration supports 448 outer VLAN tags
- 802.1p for SIP oversubscription
- Maximum transmission unit (MTU) up to 9180 bytes
- Up to 5000 MAC Accounting Entries for a SPA (source MAC Accounting on the ingress and Destination MAC Accounting on the egress)
- Power monitoring and diagnostics of SFP and XFP modules
- Ingress traffic classification based on IP Differentiated Services Code Point (DSCP) or IP precedence values, MPLS experimental (EXP) bits, VLAN 802.1Q priority bits, and IPv6 traffic-class bits
- Ingress IPv6 traffic classification based on IPv6 traffic-class bits
- Per-port byte and packet counters for policy drops, oversubscription drops, CRC error drops, packet sizes, unicast, multicast, and broadcast packets
- Per-VLAN byte and packet counters for policy drops, oversubscription drops, unicast, multicast, and broadcast packets

SPA Restrictions

In Cisco IOS Release 12.2(33)SCB, the Gigabit Ethernet SPAs have the following restrictions:

- When used as an uplink interface, the Cisco 1-port 10-Gigabit Ethernet SPA supports from 1 to 10 VLANs with priority queues and class based weighted-fair queues, based on QoS configuration and test scenarios. When QoS is applied at multiple VLAN 10-Gigabit Ethernet interfaces other than the main 10-Gigabit Ethernet interface, unexpected drops with nonpriority class queues may occur.
- As an access interface, the Cisco 1-port 10-Gigabit Ethernet SPA does not support oversubscription at the VLAN level when using QoS Model F.
- You cannot configure more than two active ports for sending and receiving packets on the Cisco 5-Port Gigabit Ethernet SPA.
- The following features are not supported:
 - IEEE 802.1 Q-in-Q VLAN tag switching
 - Bridge protocol data units (BPDU) filtering

Supported MIBs

The following MIBs are supported by the Gigabit Ethernet SPAs on the Cisco uBR10012 router:

- ENTITY-MIB (RFC 2737)

- CISCO-ENTITY-ASSET-MIB
- CISCO-ENTITY-FRU-CONTROL-MIB
- CISCO-ENTITY-ALARM-MIB
- CISCO-ENTITY-EXT-MIB
- CISCO-ENTITY-SENSOR-MIB
- IF-MIB
- ETHERLIKE-MIB (RFC 2665)
- Remote Monitoring (RMON)-MIB (RFC 1757)
- CISCO-CLASS-BASED-QOS-MIB
- Ethernet MIB/RMON

To locate and download MIBs for selected platforms, Cisco IOS releases, and feature sets, use Cisco MIB Locator found at the following URL:

<http://tools.cisco.com/ITDIT/MIBS/servlet/index>

If Cisco MIB Locator does not support the MIB information that you need, you can also obtain a list of supported MIBs and download MIBs from the Cisco MIBs page at the following URL:

<http://www.cisco.com/public/sw-center/netmgmt/cmtk/mibs.shtml>

To access Cisco MIB Locator, you must have an account on Cisco.com. If you have forgotten or lost your account information, send a blank e-mail to cco-locksmith@cisco.com. An automatic check will verify that your e-mail address is registered with Cisco.com. If the check is successful, account details with a new random password will be e-mailed to you. Qualified users can establish an account on Cisco.com by following the directions found at this URL:

<http://www.cisco.com/register>

This section describes the path of a packet in the ingress and egress directions through the Gigabit Ethernet SPAs. Each incoming and outgoing packet on the Gigabit Ethernet SPAs goes through the physical port (PHY) SFP optics, Media Access Controller (MAC), and ASIC devices.

Path of a Packet in the Ingress Direction

The following steps describe the path of an ingress packet through the Gigabit Ethernet SPAs:

1. The PHY SFP optics device receives incoming frames on a per-port basis from one of the laser optic interface connectors.
2. The PHY laser optics device processes the frame and sends it over the XAUI path to the MAC device.
3. The MAC device receives the frame, strips the CRCs, and sends the packet through the SPI 4.2 bus to the ASIC.
4. The ASIC takes the packet from the MAC devices and classifies the Ethernet information. CAM lookups based on etype, port, VLAN, and source and destination address information determine whether the packet is dropped or forwarded to the SPA interface. If the packet is forwarded to the SPA interface, an 8-byte SHIM header that is used for additional downstream packet processing is prepended to the packet.

Packet Path in the Egress Direction

The following steps describe the path of an egress packet from the SIP through the Gigabit Ethernet SPAs:

1. The packet is sent to the ASIC using the SPI 4.2 bus. The packets are received with Layer 2 and Layer 3 headers in addition to the packet data.
2. The ASIC uses port number, destination MAC address, destination address type, and VLAN ID to perform parallel CAM lookups. If the packet is forwarded, it is forwarded through the SPI 4.2 bus to the MAC device.
3. The MAC device forwards the packet to the PHY laser-optic interface, which transmits the packet.

Showing the SPA Hardware Type

To verify the SPA hardware type that is installed in your Cisco uBR10012 router, you can use the **show interfaces** command.

Table 11-1 shows the hardware description that appears in the **show** command output for each type of Gigabit Ethernet SPA that is supported on the Cisco uBR10012 router.

Table 11-1 SPA Hardware Descriptions in show Commands

SPA	Description in show interfaces Command
Cisco 1-port 10-Gigabit Ethernet SPA	Hardware is TenGigEther SPA
5-port Gigabit Ethernet SPA	Hardware is GigEther SPA

show interfaces Command

The following example shows output from the **show interfaces tengigabitethernet** command on a Cisco 1-port 10-Gigabit Ethernet SPA in slot 1, SPA subslot 3. The second line of the output identifies the type of SPA and its MAC address.

```
Router# show interfaces tenGigabitEthernet 1/3/0

GigabitEthernet1/3/0 is up, line protocol is up
  Hardware is TenGigEther SPA, address is 0005.00e7.2548 (bia 0005.00e7.2548)

  MTU 1500 bytes, BW 1000000 Kbit, DLY 10 usec,
    reliability 255/255, txload 1/255, rxload 1/255
  Encapsulation ARPA, loopback not set
  Keepalive not set
  Full Duplex, 1000Mbps, link type is auto, media type is SX
  output flow-control is unsupported, input flow-control is XON
  ARP type: ARPA, ARP Timeout 04:00:00
  Last input 00:00:00, output 00:00:00, output hang never
  Last clearing of "show interface" counters never
  Input queue: 0/75/0/0 (size/max/drops/flushes); Total output drops: 0
  Interface GigabitEthernet1/3/0 queueing strategy: PXF Class-based
  5 minute input rate 19000 bits/sec, 23 packets/sec
  5 minute output rate 17000 bits/sec, 23 packets/sec
    61860 packets input, 9470324 bytes, 0 no buffer
    Received 3151 broadcasts (0 IP multicasts)
    0 runts, 0 giants, 0 throttles
```

```
0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored
0 watchdog, 3151 multicast, 0 pause input
62413 packets output, 5726961 bytes, 0 underruns
0 output errors, 0 collisions, 0 interface resets
0 babbles, 0 late collision, 0 deferred
0 lost carrier, 0 no carrier, 0 pause output
0 output buffer failures, 0 output buffers swapped out
```

■ Showing the SPA Hardware Type