CHAPTER 14

Overview of the Serial SPAs

This chapter provides an overview of the release history, and feature and MIB support for the Cisco 7600 SIP-200 with the 2 and 4-Port T3/E3 SPAs, the 8-Port Channelized T1/E1 SPA, and the 2 or 4-Port CT3 SPA.

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Release History

Release	Modification
Cisco IOS Release 12.2(33)SXI	Support for the following hardware was introduced on the Cisco 7600 SIP-400 on the Catalyst 6500 Series switch: • 2-Port and 4-Port Clear Channel T3/E3 SPA • 2-Port and 4-Port Channelized T3 SPA • 8-Port Channelized T1/E1 SPA

Cisco IOS Release 12.2(33)SXH	Support for the following hardware was introduced on the Cisco 7600 SIP-200 on the Catalyst 6500 Series switch: • 1-Port Channelized OC-3/STM-1 SPA Support for the following hardware was introduced on the Cisco 7600 SIP-400 on the Catalyst 6500 Series switch: • 2-Port Channelized T3 SPA
Cisco IOS Release 12.2(18)SXE	Support for the following hardware was introduced on the Cisco 7600 SIP-200 on the Cisco 7600 series router and Catalyst 6500 series switch: • 2-Port T3/E3 SPA (SPA-2XT3/E3) • 4-Port T3/E3 SPA (SPA-4XT3/E3) • 8-Port T1/E1 SPA (SPA-8XCHT1/E1) • 2-Port CT3 SPA (SPA-2XCT3/DS0) • 4-Port CT3 SPA (SPA-4XCT3/DS0)

Supported Features

This section provides a list of some of the primary features supported by the SIP and SPA hardware and software.

Cisco 7600 SIP-200 and Cisco 7600 SIP-400 Features

The SIPs are carrier cards designed to process packets between different SPAs and the Catalyst 6500 Series switch switching fabric.

- Online insertion and removal (OIR)
- Supports up to four single-height or two double-height Shared Port Adaptors (SPAs).
- Field Programmable Gate Array (FPGA) upgrade support

  The SIPs support the standard FPD upgrade methods for the Catalyst 6500 Series switch. For more information about FPD support, see Chapter 31, “Upgrading Field-Programmable Devices.”

Restrictions

Note For other SIP-specific features and restrictions see also Chapter 3, “Overview of the SIPs and SSC”in this guide.

- On a 2-port or 4-port Channelized T3 SPA, when one of the T3 ports is configured as a DS3 Clear Channel interface and the other T3s are configured with a large number (greater than or equal to 400) of low-bandwidth channels (NxDS0, N=1,2,3 or 4), the DS3 Clear Channel interface is not able to run at 100 percent DS3 line rate when those low-bandwidth channels are idle (not transmitting or receiving packets). This issue does not occur if those low-bandwidth channels are not idle.
- On a 2-Port and 4-Port Channelized T3 SPA or 1-Port Channelized OC-3/STM-1 SPA, the maximum number of channels is limited to 1023 per SPA.

- On a 2-Port and 4-Port Channelized T3 SPA or 1-Port Channelized OC-3/STM-1 SPA, the maximum number of FIFO buffers is 4096. The FIFO buffers are shared among the interfaces; how they are shared is determined by speed. If all the FIFO buffers have been assigned to existing interfaces, a new interface cannot be created, and the "%Insufficient FIFOs to create channel group" error message is seen. Table 14-1 provides FIFO allocation information.

  To find the number of available FIFO buffers, use the **show controller t3** command:

```
Router# show controller t3 3/0/0

T3 3/0/0 is up.
  Hardware is SPA-4XCT3/DS0
  IO FPGA version: 2.6, HDLC Framer version: 0
  T3/T1 Framer(1) version: 2, T3/T1 Framer(2) version: 2
  SUBRATE FPGA version: 1.4
  HDLC controller available FIFO buffers 3112
```

Table 14-1 FIFO Allocation

Number of Timeslots	Number of FIFO Buffers
1-6 DS0	4
7-8 DS0	6
9 DS0	6
10-12 DS0	8
13-23 DS0	12
1-6 E1 TS	4
7-9 E1 TS	6
11-16 E1 TS	8
17-31E1 TS	16
T1	12
E1	16
DS3	336

SPA Features

The following is a list of some of the significant software features supported by the 2 and 4-Port T3/E3 SPA, the 8-Port Channelized T1/E1 SPA, the 1-Port Channelized OC-3/STM-1 SPA, and the 2 and 4-Port CT3 SPAs.

- Software selectable between T1, E1, E3, or T3 framing on each card (ports are configured as all T1, E1, T3, or E3). Applies to the 2 and 4-Port T3/E3 SPA and 8-Port Channelized T1/E1 SPA.
- Layer 2 encapsulation support:
  - Point-to-Point Protocol (PPP)
  - High-level Data Link Control (HDLC)
  - Frame Relay
- Internal or network clock (selectable per port)
- Online insertion and removal (OIR)

- Hot standby router protocol (HSRP)
- Alarm reporting-24-hour history maintained, 15-minute intervals on all errors
- 16- and 32-bit cyclic redundancy checks (CRC) supported (16-bit default)
- Local and remote loopback
- Bit error rate testing (BERT) pattern generation and detection per port

Note BERT is not supported on the 8-Port Channelized T1/E1 SPA.

- Dynamic provisioning— Dynamic provisioning allows for the addition of new customer circuits within a channelized interface without affecting other customers.
- FPD (field programmable device upgrades)
- End-to-end FRF.12 fragmentation support
- Link Fragmentation and Interleaving (LFI) support
- Compressed Real-Time Protocol (cRTP)—Supported on the Cisco 7600 SIP-200 with the 8-Port Channelized T1/E1 SPA, 2-Port and 4-Port Channelized T3 SPA, 2-Port and 4-Port Clear Channel T3/E3 SPA, and 1-Port Channelized OC-3/STM-1 SPA. For more information about configuring cRTP, see the "Configuring Compressed Real-Time Protocol" section on page 4-4.
- T1 Features
  - All ports can be fully channelized down to DS0
  - Data rates in multiples of 56 Kbps or 64 Kbps per channel
  - Maximum 1.536 Mbps for each T1 port
  - D4 (SF) and ESF support for each T1 port
  - ANSI T1.403 and AT&T TR54016 CI FDL support
  - Internal and receiver recovered clocking modes
  - Short haul and long haul CSU support
  - B8ZS and AMI line encoding

Note B8ZS and AMI line encoding are not configurable for TW on the 2-Port and 4-Port Channelized T3 SPA.

  - Support for Multilink Point-to-Point Protocol (MLPPP) for full T1s on the same SPA (hardware based) and across SPAs (software based).
  - Support for Multilink Frame Relay (MLFR)
- E1 Features
  - Maximum 1.984 Mbps for each E1 port in framed mode and a 2.048 Mbps in unframed E1 mode
  - All ports can be fully channelized down to DS0
  - Compliant with ITU G7.03, G.704, ETSI and ETS300156
  - Internal and receiver recovered clocking modes
  - HDB3 and AMI line encoding

  - Support for Multilink Point-to-Point Protocol (MLPPP) for full E1s on the same SPA (hardware based) and across SPAs (software based).
  - Support for Multilink Frame Relay (MLFR)
- E3 Features
  - Full duplex connectivity at E3 rate (34.368 MHz)
  - Supports G.751 or G.832 framing (software selectable)
  - High-density bipolar with three zones (HD3B) line coding
  - Compliant with E3 pulse mask
  - Line build-out: configured for up to 450 feet (135 m) of type 728A or equivalent coaxial cable
  - Loopback modes: DTE, local, dual, and network
  - E3 alarm/event detection (once per second polling)
    - Alarm indication signal (AIS)
    - Loss of frame (LOF)
    - Remote alarm indication (RAI)
  - Subrate and scrambling features for these DSU vendors:
    - Digital Link
    - ADC Kentrox
- T3 Features
  - Binary 3-zero substitution (B3ZS) line coding
  - Compliant with DS3 pulse mask per ANSI T1.102-1993
  - DS3 far-end alarm and control (FEAC) channel support
  - Full-duplex connectivity at DS-3 rate (44.736 MHz)
  - 672 DS0s per T3
  - Loopback modes: DTE, local, dual, and network
  - C-bit or M23 framing (software selectable)
  - Line build-out: configured for up to 450 feet (135 m) of type 734A or equivalent coaxial cable
  - DS-3 alarm/event detection (once per second polling)
    - Alarm indication signal (AIS)
    - Out of frame (OOF)
    - Far-end receive failure (FERF)
  - Generation and termination of DS3 Maintenance Data Link (MDL) in C-bit framing
  - Full FDL support and FDL performance monitoring
  - Subrate and scrambling features for these DSU vendors:
    - Digital Link
    - ADC Kentrox
    - Adtran
    - Verilink
    - Larscom

Note On a 2-port or 4-port Channelized T3 SPA, when one of the T3 ports is configured as a DS3 Clear Channel interface and the other T3s are configured with a large number (greater than or equal to 400) of low-bandwidth channels (NxDS0, N=1,2,3 or 4), the DS3 Clear Channel interface is not able to run at 100 percent DS3 line rate when those low-bandwidth channels are idle (not transmitting or receiving packets). This issue does not occur if those low-bandwidth channels are not idle.

Supported MIBs

The following MIBs are supported in Cisco IOS Release 12.2S for the serial SPAs on the Catalyst 6500 Series switch:

All serial SPAs:

- CISCO-ENTITY-ALARM-MIB
- CISCO-CLASS-BASED-QOS-MIB
- CISCO-ENVMON-MIB (For NPEs, NSEs, line cards, and SIPs only)
- CISCO-ENTITY-ASSET-MIB
- CISCO-ENTITY-FRU-CONTROL-MIB
- CISCO-ENTITY-SENSOR-MIB
- ENTITY-MIB
- IF-MIB
- RMON-MIB
- MPLS-LDP-MIB
- MPLS-LSR-MIB
- MPLS-TE-MIB
- MPLS-VPN-MIB

2 and 4-Port T3/E3 SPA:

- DS3/E3 MIB

8-Port Channelized T1/E1 SPA:

- DS1/E1 MIB

2 or 4-Port CT3 SPA:

- DS1-MIB
- DS3-MIB
- CISCO-FRAME-RELAY-MIB
- IANAifType-MIB
- RFC1381-MIB

To locate and download MIBs for selected platforms, Cisco IOS releases, and feature sets, use Cisco MIB Locator found at the following URL:

http://tools.cisco.com/ITDIT/MIBS/servlet/index

If Cisco MIB Locator does not support the MIB information that you need, you can also obtain a list of supported MIBs and download MIBs from the Cisco MIBs page at the following URL:

http://www.cisco.com/public/sw-center/netmgmt/cmtk/mibs.shtml

To access Cisco MIB Locator, you must have an account on Cisco.com. If you have forgotten or lost your account information, send a blank e-mail to cco-locksmith@cisco.com. An automatic check will verify that your e-mail address is registered with Cisco.com. If the check is successful, account details with a new random password will be e-mailed to you. Qualified users can establish an account on Cisco.com by following the directions found at this URL:

http://tools.cisco.com/RPF/register/register.do

Displaying the SPA Hardware Type

To verify the SPA hardware type that is installed in your Catalyst 6500 Series switch, you can use the **show diagbus** command or the **show interface** command (once the interface has been configured). There are several other commands on the Catalyst 6500 Series switch that also provide SPA hardware information.

Table 14-2 shows the hardware description that appears in the **show** command output for each type of SPA that is supported on the Catalyst 6500 Series switch.

Table 14-2 SPA Hardware Descriptions in show Commands

SPA	Description in show interfaces and show controllers commands
4-Port T3/E3 SPA	Hardware is SPA-4XT3/E3
2-Port T3/E3 SPA	Hardware is SPA-2XT3/E3
8-Port Channelized T1/E1 SPA	Hardware is SPA-T1E1
2-Port CT3 SPA	Hardware is 2 ports CT3 SPA
4-Port CT3 SPA	Hardware is 4 ports CT3 SPA

Example of the show interface Command

The following example shows output from the **show interface serial 5/0/0** command on a Catalyst 6500 Series switch with a 4-Port T3/E3 SPA installed in slot 5:

```
Serial5/0/0 is up, line protocol is up
Hardware is SPA-4XT3/E3[3/0]
MTU 4470 bytes, BW 44210 Kbit, DLY 200 usec,
reliability 248/255, txload 1/255, rxload 1/255
Encapsulation HDLC, crc 16, loopback not set
Keepalive set (10 sec)
Last input 00:00:06, output 00:00:07, output hang never
Last clearing of ''show interface'' counters 00:00:01
Input queue: 0/75/0/0 (size/max/drops/flushes); Total output drops: 0
Queueing strategy: fifo
Output queue: 0/40 (size/max)
5 minute input rate 0 bits/sec, 0 packets/sec
5 minute output rate 0 bits/sec, 0 packets/sec
0 packets input, 0 bytes, 0 no buffer
Received 0 broadcasts (0 IP multicast)
0 runts, 0 giants, 0 throttles
```

```
0 parity
0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored, 0 abort
0 packets output, 0 bytes, 0 underruns
0 output errors, 0 applique, 0 interface resets
0 output buffer failures, 0 output buffers swapped out
0 carrier transitions
```

The following example shows output from the **show interface serial 6/0/1** command on a Catalyst 6500 Series switch with a 8-Port Channelized T1/E1 SPA installed in slot 6:

```
Serial6/0/1:0 is up, line protocol is up
  Hardware is SPA-T1E1
  MTU 1500 bytes, BW 1536 Kbit, DLY 20000 usec,
     reliability 255/255, txload 1/255, rxload 1/255
  Encapsulation PPP, crc 16, loopback not set
  Keepalive set (10 sec)
  LCP Open, multilink Open
  Last input 00:00:03, output 00:00:03, output hang never
  Last clearing of "show interface" counters 5d17h
  Input queue: 0/75/0/0 (size/max/drops/flushes); Total output drops: 3194905708
  Queueing strategy: fifo
  Output queue: 0/40 (size/max)
  30 second input rate 0 bits/sec, 0 packets/sec
  30 second output rate 0 bits/sec, 0 packets/sec
     74223 packets input, 1187584 bytes, 0 no buffer
     Received 0 broadcasts (0 IP multicast)
     0 runts, 0 giants, 0 throttles
     0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored, 0 abort
     74227 packets output, 1187751 bytes, 0 underruns
     0 output errors, 0 collisions, 2 interface resets
     0 output buffer failures, 0 output buffers swapped out
     4 carrier transitions no alarm present
  Timeslot(s) Used:1-24, subrate: 64Kb/s, transmit delay is 0 flags
```

Example of the show controllers Command

The following example shows output from the **show controller serial** command on a Catalyst 6500 Series switch with a 4-Port T3/E3 SPA installed in slot 5:

```
Router# show controllers serial 5/0/2
Serial5/0/2 -
   Framing is c-bit, Clock Source is Line
   Bandwidth limit is 44210, DSU mode 0, Cable length is 10
   rx FEBE since last clear counter 0, since reset 0
   Data in current interval (807 seconds elapsed):
     0 Line Code Violations, 0 P-bit Coding Violation
     0 C-bit Coding Violation
     0 P-bit Err Secs, 0 P-bit Sev Err Secs
     0 Sev Err Framing Secs, 306 Unavailable Secs
     500 Line Errored Secs, 0 C-bit Errored Secs, 0 C-bit Sev Err Secs
  Data in Interval 1:
     0 Line Code Violations, 0 P-bit Coding Violation
     0 C-bit Coding Violation
     0 P-bit Err Secs, 0 P-bit Sev Err Secs
     0 Sev Err Framing Secs, 0 Unavailable Secs
     564 Line Errored Secs, 0 C-bit Errored Secs, 0 C-bit Sev Err Secs
  Data in Interval 2:
     0 Line Code Violations, 0 P-bit Coding Violation
     0 C-bit Coding Violation
     0 P-bit Err Secs, 0 P-bit Sev Err Secs
     0 Sev Err Framing Secs, 0 Unavailable Secs
     564 Line Errored Secs, 0 C-bit Errored Secs, 0 C-bit Sev Err Secs
```

```
[output omitted]
```

The following example shows output from the **show controllers** command on a Catalyst 6500 Series switch with a 8-Port Channelized T1/E1 SPA installed in slot 6:

```
Router# show controllers t1
T1 6/0/0 is up.
  Applique type is Channelized T1
  Cablelength is long gain36 0db
  No alarms detected.
  alarm-trigger is not set
  Framing is ESF, Line Code is B8ZS, Clock Source is Line.
  Data in current interval (394 seconds elapsed):
     0 Line Code Violations, 0 Path Code Violations
     0 Slip Secs, 0 Fr Loss Secs, 0 Line Err Secs, 0 Degraded Mins
     0 Errored Secs, 0 Bursty Err Secs, 0 Severely Err Secs, 0 Unavail Secs
  Total Data (last 24 hours)
     0 Line Code Violations, 0 Path Code Violations,
     0 Slip Secs, 0 Fr Loss Secs, 0 Line Err Secs, 0 Degraded Mins,
     0 Errored Secs, 0 Bursty Err Secs, 0 Severely Err Secs, 0 Unavail Secs
T1 6/0/1 is up.
  Applique type is Channelized T1
  Cablelength is long gain36 0db
  No alarms detected.
  alarm-trigger is not set
  Framing is ESF, Line Code is B8ZS, Clock Source is Line.
  Data in current interval (395 seconds elapsed):
     0 Line Code Violations, 0 Path Code Violations
     0 Slip Secs, 0 Fr Loss Secs, 0 Line Err Secs, 0 Degraded Mins
     0 Errored Secs, 0 Bursty Err Secs, 0 Severely Err Secs, 0 Unavail Secs
  Total Data (last 24 hours)
     0 Line Code Violations, 0 Path Code Violations,
     0 Slip Secs, 0 Fr Loss Secs, 0 Line Err Secs, 0 Degraded Mins,
     0 Errored Secs, 0 Bursty Err Secs, 0 Severely Err Secs, 0 Unavail Secs
```

The following example shows output from the **show controllers** command on a Catalyst 6500 Series switch with a 4-Port CT3 SPA installed in slot 3:

```
Router# show controllers t3
T3 3/1/2 is up.  Hardware is 4 ports CT3 SPA
  ATLAS FPGA version: 0, FREEDM336 version: 0
  TEMUX84(1) version: 0, TEMUX84(1) version: 0
  SUBRATE FPGA version: 0
  Applique type is Channelized T3
  No alarms detected.
  Framing is M23, Line Code is B3ZS, Clock Source is Internal
  Equipment customer loopback
  Data in current interval (146 seconds elapsed):
     0 Line Code Violations, 0 P-bit Coding Violation
     0 C-bit Coding Violation, 0 P-bit Err Secs
     0 P-bit Severely Err Secs, 0 Severely Err Framing Secs
     0 Unavailable Secs, 0 Line Errored Secs
     0 C-bit Errored Secs, 0 C-bit Severely Errored Secs
     0 Severely Errored Line Secs
     0 Far-End Errored Secs, 0 Far-End Severely Errored Secs
     0 CP-bit Far-end Unavailable Secs
     0 Near-end path failures, 0 Far-end path failures
     0 Far-end code violations, 0 FERF Defect Secs
     0 AIS Defect Secs, 0 LOS Defect Secs

  T1 1 is up
  timeslots: 1-24
  FDL per AT&T 54016 spec.
```

```
No alarms detected.
Framing is ESF, Clock Source is Internal
Data in current interval (104 seconds elapsed):
   0 Line Code Violations, 0 Path Code Violations
   0 Slip Secs, 0 Fr Loss Secs, 0 Line Err Secs, 0 Degraded Mins
   0 Errored Secs, 0 Bursty Err Secs, 0 Severely Err Secs
   0 Unavail Secs, 0 Stuffed Secs
   0 Near-end path failures, 0 Far-end path failures, 0 SEF/AIS Secs
Total Data (last 2 15 minute intervals):
   0 Line Code Violations,0 Path Code Violations,
   0 Slip Secs, 0 Fr Loss Secs, 0 Line Err Secs, 0 Degraded Mins,
   0 Errored Secs, 0 Bursty Err Secs, 0 Severely Err Secs
   0 Unavail Secs, 0 Stuffed Secs
   0 Near-end path failures, 0 Far-end path failures, 0 SEF/AIS Secs
```