CHAPTER 12

Overview of the POS SPAs

This chapter provides an overview of the release history, and feature and Management Information Base (MIB) support for the Packet over SONET (POS) SPAs on the Catalyst 6500 Series switch.

This chapter includes the following sections:

Release History

Release	Modification
Cisco IOS Release 12.2(33)SXI	Support for the 2-Port OC-48c/STM-16 POS SPA was introduced on the Cisco 7600 SIP-600 on the Catalyst 6500 series switch.
Cisco IOS Release 12.2(33)SXH	Support for the 1-Port OC-48 POS/RPR SPA with SFP Optics was introduced on the Cisco 7600 SIP-400 on the Catalyst 6500 series switch.
Cisco IOS Release 12.2(18)SXF10	Support for the 1-Port OC-48c/STM-16 POS SPA was introduced on the Cisco 7600 SIP-400 on the Catalyst 6500 series switch.
Cisco IOS Release 12.2(18)SXF2	Support for the 1-Port OC-192c/STM-64 POS/RPR VSR Optics SPA was introduced on the Cisco 7600 SIP-600 on the Cisco 7600 series router and Catalyst 6500 series switch.

Cisco IOS Release 12.2(18)SXF	Support for the following hardware was introduced on the Cisco 7600 series router and Catalyst 6500 series switch: • 1-Port OC-192c/STM-64 POS/RPR SPA • 1-Port OC-192c/STM-64 POS/RPR XFP SPA
Cisco IOS Release 12.2(18)SXE	Support for the following hardware was introduced on the Cisco 7600 series router and Catalyst 6500 series switch: • 2-Port OC-3c/STM-1 POS SPA • 4-Port OC-3c/STM-1 POS SPA • 1-Port OC-12c/STM-4 POS SPA

POS Technology Overview

Packet-over-SONET is a high-speed method of transporting IP traffic between two points. This technology combines the Point-to-Point Protocol (PPP) with Synchronous Optical Network (SONET) and Synchronous Digital Hierarchy (SDH) interfaces.

SONET is an octet-synchronous multiplex scheme defined by the American National Standards Institute (ANSI) standard (T1.1051988) for optical digital transmission at hierarchical rates from 51.840 Mbps to 2.5 Gbps (Synchronous Transport Signal, STS-1 to STS-48) and greater. SDH is an equivalent international standard for optical digital transmission at hierarchical rates from 155.520 Mbps (Synchronous Transfer Mode-1 [STM-1]) to 2.5 Gbps (STM-16) and greater.

SONET specifications have been defined for single-mode fiber and multimode fiber. The POS SPAs on the Catalyst 6500 Series switch allow transmission over both single-mode and multimode fiber at various optical carrier rates.

SONET/SDH transmission rates are integral multiples of 51.840 Mbps. The following transmission multiples are currently specified and used on the POS SPAs on the Catalyst 6500 Series switch:

- OC-3c/STM-1—155.520 Mbps
- OC-12c/STM-4—622.080 Mbps
- OC-48c/STM-16—2.488 Gbps
- OC-192c/STM-64—9.953 Gbps

Supported Features

This section provides a list of some of the primary features supported by the POS SPA hardware and software:

- Jumbo frames (up to 9216 bytes)
- Online insertion and removal (OIR) from the SIP, or OIR of the SIP with the SPA inserted
- Small form-factor pluggable (SFP) optics module OIR
- Field-programmable gate array (FPGA) upgrade support

The POS SPAs also support the following groups of features:

SONET/SDH Compliance Features

This section lists the SONET/SDH compliance features supported by the POS SPAs on the Catalyst 6500 Series switch:

- 1+1 SONET Automatic Protection Switching (APS) as per G.783 Annex A
- 1+1 SDH Multiplex Section Protection (MSP) as per G.783 Annex A
- American National Standards Institute (ANSI) T1.105
- ITU-T G.707, G.783, G.957, G.958
- Telcordia GR-253-CORE: SONET Transport Systems: Common Generic Criteria
- Telcordia GR-1244: Clocks for the Synchronized Network: Common Generic Criteria

SONET/SDH Error, Alarm, and Performance Monitoring Features

This section lists the SONET/SDH error, alarm, and performance monitoring features supported by the POS SPAs on the Catalyst 6500 Series switch:

- Signal failure bit error rate (SF-BER)
- Signal degrade bit error rate (SD-BER)
- Signal label payload construction (C2)
- Path trace byte (J1)
- Section:
  - Loss of signal (LOS)
  - Loss of frame (LOF)
  - Error counts for B1
  - Threshold crossing alarms (TCA) for B1
- Line:
  - Line alarm indication signal (LAIS)
  - Line remote defect indication (LRDI)
  - Line remote error indication (LREI)
  - Error counts for B2
  - Threshold crossing alarms (TCA) for B2
- Path:
  - Path alarm indication signal (PAIS)
  - Path remote defect indication (PRDI)

  - Path remote error indication (PREI)
  - Error counts for B3
  - Threshold crossing alarms (TCA) for B3
  - Loss of pointer (LOP)
  - New pointer events (NEWPTR)
  - Positive stuffing event (PSE)
  - Negative stuffing event (NSE)

SONET/SDH Synchronization Features

This section lists the SONET/SDH synchronization features supported by the POS SPAs on the Catalyst 6500 Series switch:

- Local (internal) timing (for inter-router connections over dark fiber or Wavelength Division Multiplex [WDM] equipment)
- Loop (line) timing (for connecting to SONET/SDH equipment)
- +/– 20 ppm clock accuracy over full operating temperature

WAN Protocol Features

This section lists the WAN protocols supported by the POS SPAs on the Catalyst 6500 Series switch:

- RFC 1661, *The Point-to-Point Protocol (PPP)*
- RFC 1662, *PPP in HDLC framing*
- RFC 2615, *PPP over SONET/SDH* (with 1+x43 self-synchronous payload scrambling)
- RFC 3518, *Point-to-Point Protocol (PPP) Bridging Control Protocol (BCP)*—See Table 12-1for BCP feature restrictions on the Catalyst 6500 series switch
- Cisco Protect Group Protocol over UDP/IP (Port 1972) for APS and MSP
- Multiprotocol Label Switching (MPLS)

Network Management Features

This section lists the network management features supported by the POS SPAs on the Catalyst 6500 Series switch:

- Simple Network Management Protocol (SNMP) Management Information Base (MIB) counters
- Local (diagnostic) loopback
- Network loopback
- NetFlow Data Export
- IP over the Section Data Communications Channel (SDCC) —See Table 12-1 for SDCC feature restrictions on the Catalyst 6500 series switch
- RFC 3592 performance statistics for timed intervals (current, 15-minute, multiple 15-minute, and 1-day intervals):

- Regenerator section
- Multiplex section
- Path errored seconds
- Severely errored seconds
- Severely errored framed seconds

Restrictions

Note For other SIP-specific features and restrictions see also Chapter 3, "Overview of the SIPs and SSC."

Table 12-1 provides information about POS feature compatibility and restrictions by SIP and SPA combination.

Table 12-1 POS Feature Compatibility and Restrictions by SIP and SPA Combination

Feature	Cisco 7600 SIP-200	Cisco 7600 SIP-400	Cisco 7600 SIP-600
Bridge Control Protocol (BCP)	2-Port and 4-Port OC-3c/STM-1 POS SPA—Supported.	• 1-Port OC-12c/STM-4 POS SPA—Supported. • 2-Port and 4-Port OC-3c/STM-1 POS SPA—Supported. • 1-Port OC-48c/STM-16 POS SPA—Supported.	Not supported on any POS SPAs.
Dynamic Packet Transport (DPT), which includes RPR/SRP	Not supported on any POS SPAs.	Not supported on any POS SPAs.	Not supported on any POS SPAs.
Frame Relay	Supported on all POS SPAs.	Supported on all POS SPAs.	Not supported on any POS SPAs.
Multilink PPP	Not supported on any OC-3 POS SPAs.	Not supported on any OC-3 POS SPAs.	Not supported on any OC-3 POS SPAs.
Section Data Communications Channel (SDCC)	• 2-Port OC-3c/STM-1 POS SPA—Supported. • 4-Port OC-3c/STM-1 POS SPA—SDCC is supported on up to two ports.	• 2-Port OC-3c/STM-1 POS SPA—Supported. • 4-Port OC-3c/STM-1 POS SPA—SDCC is supported on up to two ports. • 1-Port OC-12c/STM-4 POS SPA—Supported. • 1-Port OC-48c/STM-16 POS SPA—Not supported.	Not supported on any POS SPAs.

Supported MIBs

The following MIBs are supported in Cisco IOS Release 12.2(18)SXF2 for the 2-Port and 4-Port OC-3c/STM-1 POS SPA, 1-Port OC-12c/STM-4 POS SPA, 1-Port OC-192c/STM-64 POS/RPR SPA, 1-Port OC-192c/STM-64 POS/RPR XFP SPA, and 1-Port OC-192c/STM-64 POS/RPR VSR Optics SPA on the Catalyst 6500 Series switch:

- CISCO-APS-MIB
- CISCO-ENTITY-ASSET-MIB
- CISCO-ENTITY-FRU-CONTROL-MIB
- CISCO-ENVMON-MIB (For NPEs, NSEs, line cards, and MSCs only)
- CISCO-EXTENDED-ENTITY-MIB
- CISCO-OPTICAL-MIB
- ENTITY-MIB
- OLD-CISCO-CHASSIS-MIB
- IF-MIB
- SONET-MIB (RFC 2558, *Definitions of Managed Objects for SONET/SDH Interface Type*)

To locate and download MIBs for selected platforms, Cisco IOS releases, and feature sets, use Cisco MIB Locator found at the following URL:

http://tools.cisco.com/ITDIT/MIBS/servlet/index

If Cisco MIB Locator does not support the MIB information that you need, you can also obtain a list of supported MIBs and download MIBs from the Cisco MIBs page at the following URL:

http://www.cisco.com/public/sw-center/netmgmt/cmtk/mibs.shtml

To access Cisco MIB Locator, you must have an account on Cisco.com. If you have forgotten or lost your account information, send a blank e-mail to cco-locksmith@cisco.com. An automatic check will verify that your e-mail address is registered with Cisco.com. If the check is successful, account details with a new random password will be e-mailed to you. Qualified users can establish an account on Cisco.com by following the directions found at this URL:

http://tools.cisco.com/RPF/register/register.do

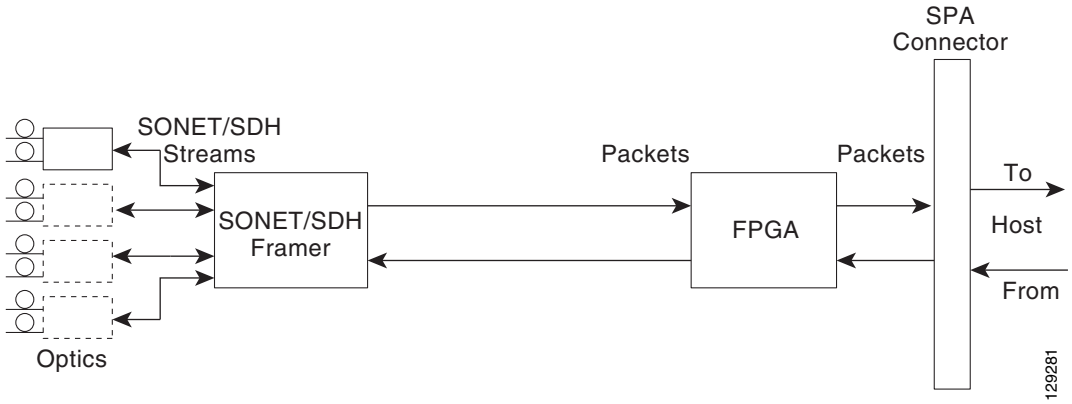
SPA Architecture

This section provides an overview of the architecture of the POS SPAs and describes the path of a packet in the ingress and egress directions. Some of these areas of the architecture are referenced in the SPA software and can be helpful to understand when troubleshooting or interpreting some of the SPA CLI and **show** command output.

4-Port OC-3c/STM-1 POS SPA Architecture

Figure 12-1 identifies some of the hardware devices that are part of the POS SPA architecture. The figure shows the four ports that are supported by the 4-Port OC-3c/STM-1 POS SPA only.

Figure 12-1 4-Port OC-3c/STM-1 POS SPA Architecture



Every incoming and outgoing packet on the 4-Port OC-3c/STM-1 POS SPA goes through the SONET/SDH framer and field-programmable gate array (FPGA) devices.

Path of a Packet in the Ingress Direction

The following steps describe the path of an ingress packet through the 4-Port OC-3c/STM-1 POS SPA:

1. The framer receives SONET/SDH streams from the SFP optics, extracts clocking and data, and processes the section, line, and path overhead.
2. The framer extracts the POS frame payload and verifies the frame size and frame check sequence (FCS).
3. The framer passes valid frames to the field-programmable gate array (FPGA) on the SPA.
4. The FPGA on the SPA transfers frames to the host through the SPI4.2 bus for further processing and switching.

Path of a Packet in the Egress Direction

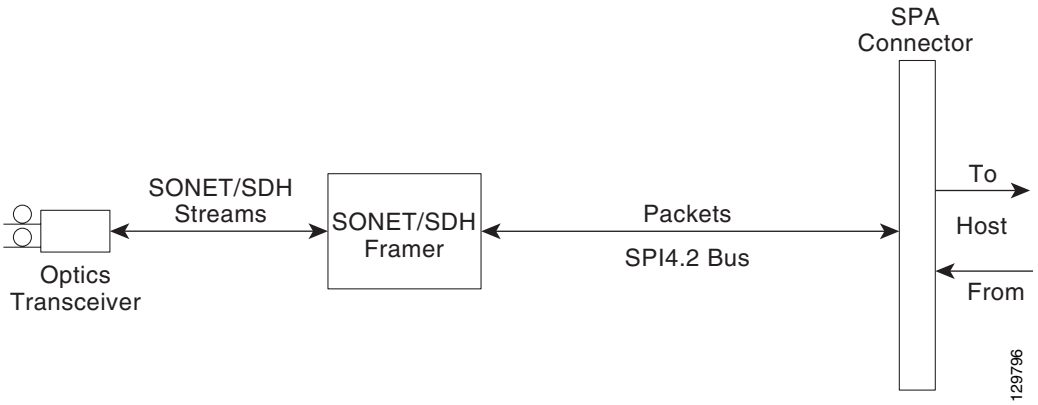
The following steps describe the path of an egress packet through the 4-Port OC-3c/STM-1 POS SPA:

1. The host sends packets to the FPGA on the SPA using the SPI4.2 bus.
2. The FPGA on the SPA stores the data in the appropriate channel's first-in first-out (FIFO) queue.
3. The FPGA on the SPA passes the packet to the framer.
4. The framer accepts the data and stores it in the appropriate channel queue.
5. The framer adds the FCS and SONET/SDH overhead.
6. The framer sends the data to the SFP optics for transmission onto the network.

1-Port OC-192c/STM-64 POS/RPR XFP SPA Architecture

Figure 12-2 identifies the primary hardware devices that are part of the POS SPA architecture. The figure shows a single optics transceiver supported by both of the POS SPAs. However, the 1-Port OC-192c/STM-64 POS/RPR SPA and 1-Port OC-192c/STM-64 POS/RPR VSR Optics SPA support fixed optics, while the 1-Port OC-192c/STM-64 POS/RPR XFP SPA supports XFP optics. The path of a packet remains the same except for where the optic transceiver support resides.

Figure 12-2 1-Port OC-192c/STM-64 POS/RPR XFP SPA Architecture



In POS mode, every incoming and outgoing packet on the OC-192 POS SPAs goes through the SONET/SDH framer and SPI4.2 interface.

Path of a Packet in the Ingress Direction

The following steps describe the path of an ingress packet through the 1-Port OC-192c/STM-64 POS/RPR XFP SPA:

1. The framer receives SONET/SDH streams from the XFP optics, extracts clocking and data, and processes the section, line, and path overhead.
2. The framer extracts the POS frame payload and verifies the frame size and frame check sequence (FCS).
3. The framer passes valid frames to the System Packet Level Interface 4.2 (SPI4.2) interface on the SPA.
4. The SPI4.2 interface transfers frames to the host through the SPI4.2 bus for further processing and switching.

Path of a Packet in the Egress Direction

The following steps describe the path of an egress packet through the 1-Port OC-192c/STM-64 POS/RPR XFP SPA:

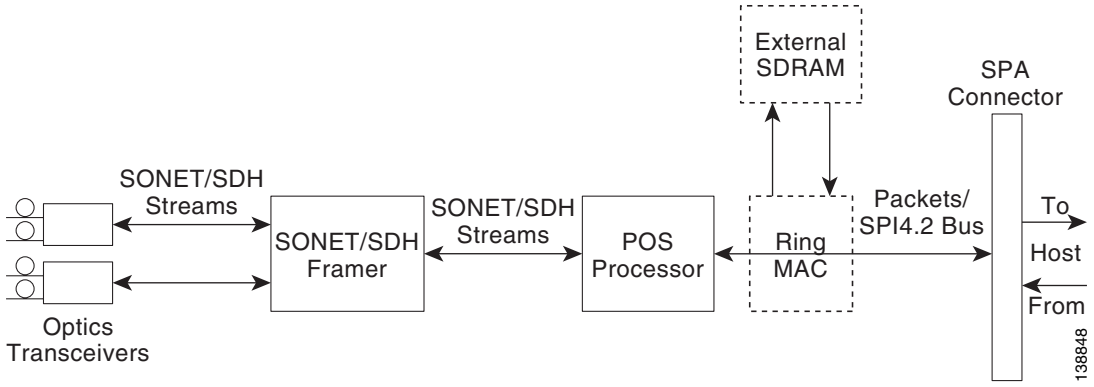
1. The host sends packets to the SPA using the SPI4.2 bus.
2. The SPA stores the data in the appropriate channel's first-in first-out (FIFO) queue.
3. The SPA passes the packet to the framer.
4. The framer accepts the data and stores it in the appropriate channel queue.

5. The framer adds the FCS and SONET/SDH overhead.
6. The framer sends the data to the XFP optics for transmission onto the network.

2-Port OC-48c/STM-16 POS SPA Architecture

Figure 12-3 identifies the primary hardware devices that are part of the 2-Port OC-48c/STM-16 POS SPA architecture.

Figure 12-3 2-Port OC-48c/STM-16 POS SPA Architecture



Path of a Packet in the Ingress Direction

The following steps describe the path of an ingress packet through the 2-Port OC-48c/STM-16 POS SPA:

1. The framer receives SONET/SDH streams from the SFP optics, extracts clocking and data, and processes the section, line, and path overhead.
2. The framer detects Loss of Signal (LOS), Loss of Frame (LOF), Severely Errored Frame (SEF), Line Alarm Indication Signal (AIS-L), Loss of Pointer (LOP), Line Remote Defect Indication Signal (Enhanced RDI-L), Path Alarm Indication Signal (AIS-P), Standard and Enhanced Path Remote Defect Indication Signal (RDI-P), Path Remote Error Indication (Enhanced REI-P). The framer extracts or inserts DCC bytes.
3. The framer processes the S1 synchronization status byte, the pointer action bytes (per Telcordia GR-253-CORE), and extracts or inserts DCC bytes.
4. The POS processor extracts the POS frame payload and verifies the frame size and frame check sequence (FCS).
5. The POS processor supports PPP, Frame Relay, or HDLC modes and optionally performs payload scrambling.
6. The POS processor passes valid frames to the System Packet Level Interface 4.2 (SPI4.2) interface on the SPA.
7. The SPI4.2 interface transfers frames to the host through the SPI4.2 bus for further processing and switching.

Path of a Packet in the Egress Direction

The following steps describe the path of an egress packet through the 2-Port OC-48c/STM-16 POS SPA:

1. The host sends packets to the SPA using the SPI4.2 bus.
2. The SPA stores the data in the appropriate SPI4 channel's first-in first-out (FIFO) queue.
3. The SPA passes the packet from the SPI4 interface to the POS processor where it is encapsulated in a POS frame and FCS is added.
4. The POS frame is sent to the SONET/SDH framer where it is placed into the SONET payload.
5. The framer adds the FCS and SONET/SDH overhead.
6. The framer sends the data to the SFP optics for transmission onto the network.

Displaying the SPA Hardware Type

To verify the SPA hardware type that is installed in your Catalyst 6500 Series switch, you can use the **show idprom** command. For other hardware information, you can also use the **show interfaces** or **show controllers** commands. There are several other commands on the Catalyst 6500 Series switch that also provide SPA hardware information. For more information about these commands, see the "Command Summary for POS SPAs" and the "SIP and SPA Commands" chapters in this guide.

Table 12-2 shows the hardware description that appears in the **show** command output for each type of SPA that is supported on the Catalyst 6500 Series switch.

Table 12-2 SPA Hardware Descriptions in show Commands

SPA	Description in show interfaces Command	Description in show idprom Command
2-Port OC-3c/STM-1 POS SPA	Hardware is Packet over Sonet	2-port OC3/STM1 POS Shared Port Adapter / SPA-2XOC3-POS
4-Port OC-3c/STM-1 POS SPA	Hardware is Packet over Sonet	4-port OC3/STM1 POS Shared Port Adapter / SPA-4XOC3-POS
1-Port OC-12c/STM-4 POS SPA	Hardware is Packet over Sonet	1-port OC12/STM4 POS Shared Port Adapter / SPA-1XOC12-POS
1-Port OC-48c/STM-16 POS SPA	Hardware is Packet over Sonet	1-port OC48/STM16 POS/RPR Shared Port Adapter / SPA-1XOC48POS/RPR
2-Port OC-48c/STM-16 POS SPA	Hardware is Packet over Sonet	2-port OC48/STM16 POS/RPR Shared Port Adapter / SPA-2XOC48POS/RPR
4-Port OC-48c/STM-16 POS SPA	Hardware is Packet over Sonet	4-port OC48/STM16 POS/RPR Shared Port Adapter / SPA-4XOC48POS/RPR

Table 12-2 SPA Hardware Descriptions in show Commands (continued)

SPA	Description in show interfaces Command	Description in show idprom Command
1-Port OC-192c/STM-64 POS/RPR SPA	Hardware is Packet over Sonet	1-port OC192/STM64 POS/RPR Shared Port Adapter / SPA-OC192POS-VSR / SPA-OC192POS-LR
1-Port OC-192c/STM-64 POS/RPR XFP SPA	Hardware is Packet over Sonet	1-port OC192/STM64 POS/RPR XFP Optics Shared Port Adapter / SPA-OC192POS-XFP

Example of the show idprom Command

The following example shows sample output for the **show idprom module detail** command for a 4-Port OC-3c/STM-1 POS SPA installed in subslot 3 of the SIP installed in slot 2 of the router:

```
Router# show idprom module 2/3 detail
IDPROM for SPA module #2/3
        (FRU is '4-port OC3/STM1 POS Shared Port Adapter')
        EEPROM version           : 4
        Compatible Type          : 0xFF
        Controller Type          : 1088
        Hardware Revision        : 0.230
        Boot Timeout             : 0 msecs
        PCB Serial Number        : PRTA0304155
        Part Number              : 73-9313-02
        73/68 Board Revision     : 04
        Fab Version              : 02
        RMA Test History         : 00
        RMA Number               : 0-0-0-0
        RMA History              : 00
        Deviation Number         : 0
        Product Identifier (PID) : SPA-4XOC3-POS
        Version Identifier (VID) : V01
.
.
.
```

Example of the show interfaces Command

The following example shows output from the **show interfaces pos** command on a Catalyst 6500 Series switch with a 4-Port OC-3c/STM-1 POS SPA installed in slot 5:

```
Router# show interfaces pos 5/0/1
POS5/0/1 is up, line protocol is up
  Hardware is Packet over Sonet
  Internet address is 10.5.5.5/8
  MTU 4470 bytes, BW 155000 Kbit, DLY 100 usec,
     reliability 96/255, txload 1/255, rxload 1/255
  Encapsulation HDLC, crc 16, loopback not set
  Keepalive not set
  Scramble disabled
  Last input 00:00:11, output 00:00:11, output hang never
  Last clearing of ''show interface'' counters 00:00:23
  Input queue: 0/75/0/0 (size/max/drops/flushes); Total output drops: 0
  Queueing strategy: fifo
```

```
Output queue: 0/40 (size/max)
5 minute input rate 0 bits/sec, 0 packets/sec
5 minute output rate 0 bits/sec, 0 packets/sec
5 packets input, 520 bytes
   Received 0 broadcasts (0 IP multicast)
   0 runts, 0 giants, 0 throttles
   0 parity
   0 input errors, 0 CRC, 0 frame, 0 overrun, 0 ignored, 0 abort
5 packets output, 520 bytes, 0 underruns
   0 output errors, 0 applique, 0 interface resets
   0 output buffer failures, 0 output buffers swapped out
   0 carrier transitions
```

Example of the show controllers Command

The following example shows output from the **show controllers pos** command on a Catalyst 6500 Series switch for the first interface (0) of a POS SPA installed in subslot 2 of a SIP installed in chassis slot 3:

```
Router# show controllers pos 3/2/0
POS3/2/0
SECTION
LOF = 0 LOS = 0 BIP(B1) = 0
LINE
AIS = 0 RDI = 0 FEBE = 0 BIP(B2) = 0
PATH
AIS = 0 RDI = 0 FEBE = 0 BIP(B3) = 0
PLM = 0 UNEQ = 0 TIM = 0 TIU = 0
LOP = 0 NEWPTR = 0 PSE = 0 NSE = 0

Active Defects: None
Active Alarms: None
Alarm reporting enabled for: SF SLOS SLOF B1-TCA B2-TCA PLOP B3-TCA

Framing: SONET
APS

COAPS = 0 PSBF = 0
State: PSBF_state = False
Rx(K1/K2): 00/00 Tx(K1/K2): 00/00
Rx Synchronization Status S1 = 00
S1S0 = 00, C2 = CF
Remote aps status (none); Reflected local aps status (none)
CLOCK RECOVERY
RDOOL = 0
State: RDOOL_state = False
PATH TRACE BUFFER: STABLE
Remote hostname : sip-sw-7600-2
Remote interface: POS3/2/1
Remote IP addr : 0.0.0.0
Remote Rx(K1/K2): 00/00 Tx(K1/K2): 00/00

BER thresholds: SF = 10e-3 SD = 10e-6
TCA thresholds: B1 = 10e-6 B2 = 10e-6 B3 = 10e-6

Clock source: internal
```