BIOS Parameters by Server Model

This appendix contains the following sections:

S3260 M3 Servers

Main Tab

Name	Description
Reboot Host Immediately checkbox	Upon checking, reboots the host server immediately. You must check the checkbox after saving changes.
TPM Support **set TPMAdminCtrl**	TPM (Trusted Platform Module) is a microchip designed to provide basic security-related functions primarily involving encryption keys. This option allows you to control the TPM Security Device support for the system. It can be one of the following: • **Disabled**—The server does not use the TPM. • **Enabled**—The server uses the TPM. **Note** We recommend that you contact your operating system vendor to make sure the operating system supports this feature.

Name	Description
Power ON Password Support drop-down	This token requires that you set a BIOS password before using the F2 BIOS configuration. If enabled, password needs to be validated before you access BIOS functions such as IO configuration, BIOS set up, and booting to an operating system using BIOS. It can be one of the following: • **Disabled**—Support is disabled. • **Enabled**—Support is enabled. **Note** This field is available only on some C-series servers.

Actions Area

Name	Description
Save button	Saves the settings for the BIOS parameters on all three tabs and closes the dialog box. If the **Reboot Host Immediately** check box is checked, the server is rebooted immediately and the new BIOS settings go into effect. Otherwise the changes are saved until the server is manually rebooted.
Reset button	Resets the values for the BIOS parameters on all three tabs to the settings that were in effect when this dialog box was first opened.
Restore Defaults button	Sets the BIOS parameters on all three tabs to their default settings.

Advanced Tab

Reboot Server Option

If you want to apply your changes at a later time, clear the **Reboot Host Immediately** check box. Cisco IMC stores the changes and applies them the next time the server reboots.

Note If there are existing BIOS parameter changes pending, Cisco IMC automatically overwrites the stored values with the current settings when you click **Save Changes**.

Processor Configuration Parameters

Name	Description
Intel Hyper-Threading Technology **set IntelHyperThread**	Whether the processor uses Intel Hyper-Threading Technology, which allows multithreaded software applications to execute threads in parallel within each processor. This can be one of the following: • **Disabled**—The processor does not permit hyperthreading. • **Enabled**—The processor allows for the parallel execution of multiple threads. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Number of Enabled Cores **set CoreMultiProcessing**	Allows you to disable one or more of the physical cores on the server. This can be one of the following: • **All**—Enables all physical cores. This also enables Hyper Threading on the associated logical processor cores. • **1** through ***n***—Specifies the number of physical processor cores that can run on the server. Each physical core has an associated logical core. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Execute Disable **set ExecuteDisable**	Classifies memory areas on the server to specify where application code can execute. As a result of this classification, the processor disables code execution if a malicious worm attempts to insert code in the buffer. This setting helps to prevent damage, worm propagation, and certain classes of malicious buffer overflow attacks. This can be one of the following: • **Disabled**—The processor does not classify memory areas. • **Enabled**—The processor classifies memory areas. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Intel VT **set IntelVT**	Whether the processor uses Intel Virtualization Technology (VT), which allows a platform to run multiple operating systems and applications in independent partitions. This can be one of the following: • **Disabled**—The processor does not permit virtualization. • **Enabled**—The processor allows multiple operating systems in independent partitions. **Note** If you change this option, you must power cycle the server before the setting takes effect.

Name	Description
Intel VT-d **set IntelVTD**	Whether the processor uses Intel Virtualization Technology for Directed I/O (VT-d). This can be one of the following: • **Disabled**—The processor does not use virtualization technology. • **Enabled**—The processor uses virtualization technology.
Intel VT-d Coherency Support **set CoherencySupport**	Whether the processor supports Intel VT-d Coherency. This can be one of the following: • **Disabled**—The processor does not support coherency. • **Enabled**—The processor uses VT-d Coherency as required.
Intel VT-d ATS Support **set ATS**	Whether the processor supports Intel VT-d Address Translation Services (ATS). This can be one of the following: • **Disabled**—The processor does not support ATS. • **Enabled**—The processor uses VT-d ATS as required.
CPU Performance **set CPUPerformance**	Sets the CPU performance profile for the server. The performance profile consists of the following options: • DCU Streamer Prefetcher • DCU IP Prefetcher • Hardware Prefetcher • Adjacent Cache-Line Prefetch This can be one of the following: • **Enterprise**—All options are enabled. • **High_Throughput**—Only the DCU IP Prefetcher is enabled. The rest of the options are disabled. • **HPC**—All options are enabled. This setting is also known as high performance computing. • **Custom**—All performance profile options can be configured from the BIOS setup on the server. In addition, the Hardware Prefetcher and Adjacent Cache-Line Prefetch options can be configured in the fields below.

Name	Description
Hardware Prefetcher **set HardwarePrefetch**	Whether the processor allows the Intel hardware prefetcher to fetch streams of data and instruction from memory into the unified second-level cache when necessary. This can be one of the following: • **Disabled**—The hardware prefetcher is not used. • **Enabled**—The processor uses the hardware prefetcher when cache issues are detected.
Adjacent Cache Line Prefetcher **set AdjacentCacheLinePrefetch**	Whether the processor fetches cache lines in even/odd pairs instead of fetching just the required line. This can be one of the following: • **Disabled**—The processor only fetches the required line. • **Enabled**— The processor fetches both the required line and its paired line.
DCU Streamer Prefetch **set DcuStreamerPrefetch**	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache. This can be one of the following: • **Disabled**—The processor does not try to anticipate cache read requirements and only fetches explicitly requested lines. • **Enabled**—The DCU prefetcher analyzes the cache read pattern and prefetches the next line in the cache if it determines that it may be needed.
DCU IP Prefetcher **set DcuIpPrefetch**	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache. This can be one of the following: • **Disabled**—The processor does not preload any cache data. • **Enabled**—The DCU IP prefetcher preloads the L1 cache with the data it determines to be the most relevant.
Direct Cache Access Support **set DirectCacheAccess**	Allows processors to increase I/O performance by placing data from I/O devices directly into the processor cache. This setting helps to reduce cache misses. This can be one of the following: • **Disabled**—Data from I/O devices is not placed directly into the processor cache. • **Enabled**—Data from I/O devices is placed directly into the processor cache.

BIOS Parameters by Server Model

Name	Description
Power Technology **set CPUPowerManagement**	Enables you to configure the CPU power management settings for the following options: • Enhanced Intel Speedstep Technology • Intel Turbo Boost Technology • Processor Power State C6 Power Technology can be one of the following: • **Custom**—The server uses the individual settings for the BIOS parameters mentioned above. You must select this option if you want to change any of these BIOS parameters. • **Disabled**—The server does not perform any CPU power management and any settings for the BIOS parameters mentioned above are ignored. • **Energy_Efficient**—The server determines the best settings for the BIOS parameters mentioned above and ignores the individual settings for these parameters.
Enhanced Intel Speedstep Technology **set EnhancedIntelSpeedStep**	Whether the processor uses Enhanced Intel SpeedStep Technology, which allows the system to dynamically adjust processor voltage and core frequency. This technology can result in decreased average power consumption and decreased average heat production. This can be one of the following: • **Disabled**—The processor never dynamically adjusts its voltage or frequency. • **Enabled**—The processor utilizes Enhanced Intel SpeedStep Technology and enables all supported processor sleep states to further conserve power. We recommend that you contact your operating system vendor to make sure the operating system supports this feature. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.

Name	Description
Intel Turbo Boost Technology **set IntelTurboBoostTech**	Whether the processor uses Intel Turbo Boost Technology, which allows the processor to automatically increase its frequency if it is running below power, temperature, or voltage specifications. This can be one of the following: • **Disabled**—The processor does not increase its frequency automatically. • **Enabled**—The processor utilizes Turbo Boost Technology if required. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Processor Power State C6 **set ProcessorC6Report**	Whether the BIOS sends the C6 report to the operating system. When the OS receives the report, it can transition the processor into the lower C6 power state to decrease energy usage while maintaining optimal processor performance. This can be one of the following: • **Disabled**—The BIOS does not send the C6 report. • **Enabled**—The BIOS sends the C6 report, allowing the OS to transition the processor to the C6 low power state. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Processor Power State C1 Enhanced **set ProcessorC1EReport**	Whether the CPU transitions to its minimum frequency when entering the C1 state. This can be one of the following: • **Disabled**—The CPU continues to run at its maximum frequency in C1 state. • **Enabled**—The CPU transitions to its minimum frequency. This option saves the maximum amount of power in C1 state.
Frequency Floor Override **set CpuFreqFloor**	Whether the CPU is allowed to drop below the maximum non-turbo frequency when idle. This can be one of the following: • **Disabled**— The CPU can drop below the maximum non-turbo frequency when idle. This option decreases power consumption but may reduce system performance. • **Enabled**— The CPU cannot drop below the maximum non-turbo frequency when idle. This option improves system performance but may increase power consumption.

Name	Description
P-STATE Coordination **set PsdCoordType**	Allows you to define how BIOS communicates the P-state support model to the operating system. There are 3 models as defined by the Advanced Configuration and Power Interface (ACPI) specification. • **HW_ALL**—The processor hardware is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a package). • **SW_ALL**—The OS Power Manager (OSPM) is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a physical package), and must initiate the transition on all of the logical processors. • **SW_ANY**—The OS Power Manager (OSPM) is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a package), and may initiate the transition on any of the logical processors in the domain. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Energy Performance **set CpuEngPerfBias**	Allows you to determine whether system performance or energy efficiency is more important on this server. This can be one of the following: • **Balanced_Energy** • **Balanced_Performance** • **Energy_Efficient** • **Performance**

Memory Configuration Parameters

Name	Description
Select Memory RAS **set SelectMemoryRAS**	How the memory reliability, availability, and serviceability (RAS) is configured for the server. This can be one of the following: • **Maximum_Performance**—System performance is optimized. • **Mirroring**—System reliability is optimized by using half the system memory as backup. • **Lockstep**—If the DIMM pairs in the server have an identical type, size, and organization and are populated across the SMI channels, you can enable lockstep mode to minimize memory access latency and provide better performance. This option offers better system performance than Mirroring and better reliability than Maximum Performance but lower reliability than Mirroring and lower system performance than Maximum Performance.
DRAM Clock Throttling **set DRAMClockThrottling**	Allows you to tune the system settings between the memory bandwidth and power consumption. This can be one of the following: • **Balanced**— DRAM clock throttling is reduced, providing a balance between performance and power. • **Performance**—DRAM clock throttling is disabled, providing increased memory bandwidth at the cost of additional power. • **Energy_Efficient**—DRAM clock throttling is increased to improve energy efficiency.
NUMA **set NUMAOptimize**	Whether the BIOS supports Non-Uniform Memory Access (NUMA). This can be one of the following: • **Disabled**—The BIOS does not support NUMA. • **Enabled**—The BIOS includes the ACPI tables that are required for NUMA-aware operating systems. If you enable this option, the system must disable Inter-Socket Memory interleaving on some platforms.

Name	Description
Low Voltage DDR Mode **set LvDDRMode**	Whether the system prioritizes low voltage or high frequency memory operations. This can be one of the following: • **Power_Saving_Mode**—The system prioritizes low voltage memory operations over high frequency memory operations. This mode may lower memory frequency in order to keep the voltage low. • **Performance_Mode**—The system prioritizes high frequency operations over low voltage operations.
DRAM Refresh rate **set DramRefreshRate**	Allows you to set the rate at which the DRAM cells are refreshed. This can be one of the following: • **1x**—DRAM cells are refreshed every 64ms. • **2x**—DRAM cells are refreshed every 32ms. • **3x**—DRAM cells are refreshed every 21ms. • **4x**—DRAM cells are refreshed every 16ms. • **Auto**—DRAM cells refresh rate is automatically chosen by the BIOS based on the system configuration. This is the recommended setting for this parameter.
Channel Interleaving **set ChannelInterLeave**	Whether the CPU divides memory blocks and spreads contiguous portions of data across interleaved channels to enable simultaneous read operations. This can be one of the following: • **Auto**—The CPU determines what interleaving is done. • **1_Way**—Some channel interleaving is used. • **2_Way** • **3_Way** • **4_Way**—The maximum amount of channel interleaving is used.
Rank Interleaving **set RankInterLeave**	Whether the CPU interleaves physical ranks of memory so that one rank can be accessed while another is being refreshed. This can be one of the following: • **Auto**—The CPU determines what interleaving is done. • **1_Way**—Some rank interleaving is used. • **2_Way** • **4_Way** • **8_Way**—The maximum amount of rank interleaving is used.

Name	Description
Patrol Scrub **set PatrolScrub**	Whether the system actively searches for, and corrects, single bit memory errors even in unused portions of the memory on the server. This can be one of the following: • **Disabled**—The system checks for memory ECC errors only when the CPU reads or writes a memory address. • **Enabled**—The system periodically reads and writes memory searching for ECC errors. If any errors are found, the system attempts to fix them. This option may correct single bit errors before they become multi-bit errors, but it may adversely affect performance when the patrol scrub is running.
Demand Scrub **set DemandScrub**	Whether the system corrects single bit memory errors encountered when the CPU or I/O makes a demand read. This can be one of the following: • **Disabled**— Single bit memory errors are not corrected. • **Enabled**— Single bit memory errors are corrected in memory and the corrected data is set in response to the demand read.
Altitude **set Altitude**	The approximate number of meters above sea level at which the physical server is installed. This can be one of the following: • **Auto**—The CPU determines the physical elevation. • **300_M**—The server is approximately 300 meters above sea level. • **900_M**—The server is approximately 900 meters above sea level. • **1500_M**—The server is approximately 1500 meters above sea level. • **3000_M**—The server is approximately 3000 meters above sea level.

QPI Configuration Parameters

Name	Description
QPI Link Frequency Select **set QPILinkFrequency**	The Intel QuickPath Interconnect (QPI) link frequency, in gigatransfers per second (GT/s). This can be one of the following: • **Auto**—The CPU determines the QPI link frequency. • **6.4_GT/s** • **7.2_GT/s** • **8.0_GT/s**
QPI Snoop Mode Drop-down list	The Intel QuickPath Interconnect (QPI) snoop mode. This can be one of the following: • **Auto**—The CPU automatically recognizes this as Early Snoop mode. • **Early Snoop**—The distributed cache ring stops can send a snoop probe or a request to another caching agent directly. This mode has lower latency and it is best for workloads that have shared data sets across threads and can benefit from a cache-to-cache transfer, or for workloads that are not NUMA optimized. • **Home Snoop**—The snoop is always spawned by the home agent (centralized ring stop) for the memory controller. This mode has a higher local latency than early snoop, but it provides extra resources for a larger number of outstanding transactions. • **Home Directory Snoop**— The home directory is an optional enabled feature that is implemented at both the HA and iMC logic in the processor. The goal of the directory is to filter snoops to the remote sockets and a node controller in scalable platforms and 2S and 4S configurations. • **Home Directory Snoop with OSB**— In the Opportunistic Snoop Broadcast (OSB) directory mode, the HA could choose to do speculative home snoop broadcast under very lightly loaded conditions even before the directory information has been collected and checked. • **Cluster on Die**—Enables Cluster On Die. When enabled LLC is split into two parts with an independent caching agent for each. This helps increase the performance in some workloads. This mode is available only for processors that have 10 or more cores. It is the best mode for highly NUMA optimized workloads.

SATA Configuration Parameters

Name	Description
SATA Mode **set SataMode**	Mode of operation of Serial Advanced Technology Attachment (SATA) Solid State Drives (SSD). • **Disabled**— All SATA ports is disabled, and drivers are not enumerated. • **AHCI Mode**—The default mode. Drives operate according to newer standard of Advance Host Controller Interface(AHCI).

USB Configuration Parameters

Name	Description
Legacy USB Support **set LegacyUSBSupport**	Whether the system supports legacy USB devices. This can be one of the following: • **Disabled**—USB devices are only available to EFI applications. • **Enabled**—Legacy USB support is always available. • **Auto**—Disables legacy USB support if no USB devices are connected.
Port 60/64 Emulation **set UsbEmul6064**	Whether the system supports 60h/64h emulation for complete USB keyboard legacy support. This can be one of the following: • **Disabled**—60h/64 emulation is not supported. • **Enabled**—60h/64 emulation is supported. You should select this option if you are using a non-USB aware operating system on the server.
All USB Devices **set AllUsbDevices**	Whether all physical and virtual USB devices are enabled or disabled. This can be one of the following: • **Disabled**—All USB devices are disabled. • **Enabled**—All USB devices are enabled.
USB Port: Rear **set UsbPortRear**	Whether the rear panel USB devices are enabled or disabled. This can be one of the following: • **Disabled**—Disables the rear panel USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled**—Enables the rear panel USB ports. Devices connected to these ports are detected by the BIOS and operating system.

Name	Description
USB Port: Internal **set UsbPortInt**	Whether the internal USB devices are enabled or disabled. This can be one of the following: • **Disabled**—Disables the internal USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled**—Enables the internal USB ports. Devices connected to these ports are detected by the BIOS and operating system.
USB Port: KVM **set UsbPortKVM**	Whether the vKVM ports are enabled or disabled. This can be one of the following: • **Disabled**—Disables the vKVM keyboard and/or mouse devices. Keyboard and/or mouse will not work in the vKVM window. • **Enabled**—Enables the vKVM keyboard and/or mouse devices.
USB Port: vMedia **set UsbPortVMedia**	Whether the virtual media devices are enabled or disabled. This can be one of the following: • **Disabled**—Disables the vMedia devices. • **Enabled**—Enables the vMedia devices.

PCI Configuration Parameters

Name	Description
PCI ROM CLP **set PciRomClp**	PCI ROM Command Line Protocol (CLP) controls the execution of different Option ROMs such as PxE and iSCSI that are present in the card. By default, it is disabled. • **Enabled**— Enables you to configure execution of different option ROMs such as PxE and iSCSI for an individual ports separately. • **Disabled**—The default option. You cannot choose different option ROMs. A default option ROM is executed during PCI enumeration.
ASPM Support **set ASPMSupport**	Allows you to set the level of ASPM (Active Power State Management) support in the BIOS. This can be one of the following: • **Disabled**—ASPM support is disabled in the BIOS. • **Force L0s**—Force all links to L0 standby (L0s) state. • **Auto**—The CPU determines the power state.

Serial Configuration Parameters

Name	Description
Out-of-Band Mgmt Port **set comSpcrEnable**	Allows you to configure the COM port 0 that can be used for Windows Emergency Management services. ACPI SPCR table is reported based on this setup option. This can be one of the following: • **Disabled**—Configures the COM port 0 as a general purpose port for use with the Windows Operating System. • **Enabled**—Configures the COM port 0 as a remote management port for Windows Emergency Management services.
Console Redirection **set ConsoleRedir**	Allows a serial port to be used for console redirection during POST and BIOS booting. After the BIOS has booted and the operating system is responsible for the server, console redirection is irrelevant and has no effect. This can be one of the following: • **Disabled**—No console redirection occurs during POST. • **COM_0**—Enables console redirection on COM port 0 during POST. • **COM_1**—Enables console redirection on COM port 1 during POST.
Terminal Type **set TerminalType**	What type of character formatting is used for console redirection. This can be one of the following: • **PC-ANSI**—The PC-ANSI terminal font is used. • **VT100**—A supported vt100 video terminal and its character set are used. • **VT100+**—A supported vt100-plus video terminal and its character set are used. • **VT-UTF8**—A video terminal with the UTF-8 character set is used. **Note** This setting must match the setting on the remote terminal application.

Name	Description
Bits per second **set BaudRate**	What BAUD rate is used for the serial port transmission speed. If you disable Console Redirection, this option is not available. This can be one of the following: • **9600**—A 9,600 BAUD rate is used. • **19200**—A 19,200 BAUD rate is used. • **38400**—A 38,400 BAUD rate is used. • **57600**—A 57,600 BAUD rate is used. • **115200**—A 115,200 BAUD rate is used. **Note** This setting must match the setting on the remote terminal application.
Flow Control **set FlowCtrl**	Whether a handshake protocol is used for flow control. Request to Send / Clear to Send (RTS/CTS) helps to reduce frame collisions that can be introduced by a hidden terminal problem. This can be one of the following: • **None**—No flow control is used. • **Hardware_RTS/CTS**—RTS/CTS is used for flow control. **Note** This setting must match the setting on the remote terminal application.

Name	Description
Putty KeyPad **set PuttyFunctionKeyPad**	Allows you to change the action of the PuTTY function keys and the top row of the numeric keypad. This can be one of the following: • **VT100**—The function keys generate **ESC OP** through **ESC O[.** • **LINUX**—Mimics the Linux virtual console. Function keys F6 to F12 behave like the default mode, but F1 to F5 generate **ESC [[A** through **ESC [[E**. • **XTERMR6**—Function keys F5 to F12 behave like the default mode. Function keys F1 to F4 generate **ESC OP** through ESC OS, which are the sequences produced by the top row of the keypad on Digital terminals. • **SCO**—The function keys F1 to F12 generate **ESC [M** through **ESC [X**. The function and shift keys generate **ESC [Y** through **ESC [j**. The control and function keys generate **ESC [k** through **ESC [v**. The shift, control and function keys generate **ESC [w** through **ESC [{**. • **ESCN**—The default mode. The function keys match the general behavior of Digital terminals. The function keys generate sequences such as **ESC [11~** and **ESC [12~**. • **VT400**—The function keys behave like the default mode. The top row of the numeric keypad generates **ESC OP** through **ESC OS**.
Redirection After BIOS POST **set RedirectionAfterPOST**	Whether BIOS console redirection should be active after BIOS POST is complete and control given to the OS bootloader. This can be one of the following: • **Always_Enable**—BIOS Legacy console redirection is active during the OS boot and run time. • **Bootloader**—BIOS Legacy console redirection is disabled before giving control to the OS boot loader.

LOM and PCIe Slots Configuration Parameters

Name	Description
CDN Support for VIC **set CdnEnable**	Whether the Ethernet Network naming convention is according to Consistent Device Naming (CDN) or the traditional way of naming conventions. This can be one of the following: • **Disabled**— CDN support for VIC cards is disabled. • **Enabled**— CDN support is enabled for VIC cards. **Note** CDN support for VIC cards work with Windows 2012 or the latest OS only.

Name	Description
All PCIe Slots OptionROM **set PcieOptionROMs**	Whether the server can use Option ROM present in the PCIe Cards. This can be one of the following: • **Disabled**—The Option ROM for all PCIe slots are not available. • **Enabled**—The Option ROMs for all the PCIe slots are available. • **UEFI_Only**—The Opiton ROMs for slot ***n*** are available for UEFI only. • **Legacy_Only**—The Option ROM for slot ***n*** are available for legacy only.
PCIe Slot:*n* OptionROM **set PcieSlot*n*OptionROM**	Whether the server can use the Option ROMs present in the PCIe Cards. This can be one of the following: • **Disabled**—The Option ROM for slot ***n*** is not available. • **Enabled**—The Option ROM for slot ***n*** is available. • **UEFI_Only**—The Option ROM for slot ***n*** is available for UEFI only. • **Legacy_Only**—The Option ROM for slot ***n*** is available for legacy only.
PCIe Mezzanine OptionROM **set PcieMezzOptionROM**	Whether the PCIe mezzanine slot expansion ROM is available to the server. This can be one of the following: • **Disabled**— The Option ROM for slot ***M*** is not available. • **Enabled**— The Option ROM for slot ***M*** is available. • **UEFI_Only**—The Option ROM for slot ***M*** is available for UEFI only. • **Legacy_Only**—The expansion slot for slot ***M*** is available for legacy only.
SIOC1 Link Speed **Set PcieSlot1LinkSpeed**	System IO Controller 1 (SIOC1) add-on slot 1 link speed. • **GEN1** — Link speed can reach up to first generation. • **GEN2** — Link speed can reach up to second generation. • **GEN3**— The default link speed. Link speed can reach up to third generation. • **Disabled** — Slot is disabled, and the card is not enumerated.

Name	Description
SIOC2 Link Speed **set PcieSlot2LinkSpeed**	System IO Controller 2 (SIOC2) add-on slot 2 link speed. • **GEN1** — Link speed can reach up to first generation. • **GEN2** — Link speed can reach up to second generation. • **GEN3**— The default link speed. Link speed can reach up to third generation. • **Disabled** — Slot is disabled, and the card is not enumerated.
Mezz Link Speed	Mezz link speed. This can be one of the following: • **GEN 1**— Link speed can reach up to first generation. • **GEN 2**— Link speed can reach up to second generation. • **GEN 3**—The default link speed. Link speed can reach up to third generation. • **Disabled**—Slot is disabled, and the card is not enumerated.

BIOS Configuration Dialog Box Button Bar

Important The buttons in this dialog box affect all BIOS parameters on all available tabs, not just the parameters on the tab that you are viewing.

Name	Description
Save Changes button	Saves the settings for the BIOS parameters on all three tabs and closes the dialog box. If the **Reboot Host Immediately** check box is checked, the server is rebooted immediately and the new BIOS settings go into effect. Otherwise the changes are saved until the server is manually rebooted.
Reset button	Restores the values for the BIOS parameters on all three tabs to the settings that were in effect when this dialog box was first opened.
Restore Defaults button	Sets the BIOS parameters on all three tabs to their default settings.

Server Management Tab

Server Management BIOS Parameters

Name	Description
FRB-2 Timer **set FRB-2**	Whether the FRB2 timer is used by Cisco IMC to recover the system if it hangs during POST. This can be one of the following: • **Disabled**—The FRB2 timer is not used. • **Enabled**—The FRB2 timer is started during POST and used to recover the system if necessary.
OS Watchdog Timer **set OSBootWatchdogTimer**	Whether the BIOS programs the watchdog timer with a specified timeout value. This can be one of the following: • **Disabled**—The watchdog timer is not used to track how long the server takes to boot. • **Enabled**—The watchdog timer tracks how long the server takes to boot. If the server does not boot within the length of time specified by the **set OSBootWatchdogTimerTimeout** command, the Cisco IMC logs an error and takes the action specified by the **set OSBootWatchdogTimerPolicy** command.
OS Watchdog Timer Timeout **set OSBootWatchdogTimerTimeOut**	If OS does not boot within the specified time, OS watchdog timer expires and system takes action according to timer policy. This can be one of the following: • **5_Minutes**—The OS watchdog timer expires 5 minutes after it begins to boot. • **10_Minutes**—The OS watchdog timer expires 10 minutes after it begins to boot. • **15_Minutes**—The OS watchdog timer expires 15 minutes after it begins to boot. • **20_Minutes**—The OS watchdog timer expires 20 minutes after it begins to boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.

Name	Description
OS Watchdog Timer Policy **set OSBootWatchdogTimerPolicy**	What action the system takes if the watchdog timer expires. This can be one of the following: • **Do_Nothing**—The server takes no action if the watchdog timer expires during OS boot. • **Power_Down**—The server is powered off if the watchdog timer expires during OS boot. • **Reset**—The server is reset if the watchdog timer expires during OS boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.

S3260 M4 Servers

Main Tab

Name	Description
Reboot Host Immediately checkbox	Upon checking, reboots the host server immediately. You must check the checkbox after saving changes.
TPM Support	TPM (Trusted Platform Module) is a microchip designed to provide basic security-related functions primarily involving encryption keys. This option allows you to control the TPM Security Device support for the system. It can be one of the following: • **Disabled**—The server does not use the TPM. • **Enabled**—The server uses the TPM. **Note** We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Power ON Password Support drop-down	This token requires that you set a BIOS password before using the F2 BIOS configuration. If enabled, password needs to be validated before you access BIOS functions such as IO configuration, BIOS set up, and booting to an operating system using BIOS. It can be one of the following: • **Disabled**—Support is disabled. • **Enabled**—Support is enabled.

Actions Area

Name	Description
Save button	Saves the settings for the BIOS parameters on all three tabs and closes the dialog box. If the **Reboot Host Immediately** check box is checked, the server is rebooted immediately and the new BIOS settings go into effect. Otherwise the changes are saved until the server is manually rebooted.
Reset button	Resets the values for the BIOS parameters on all three tabs to the settings that were in effect when this dialog box was first opened.
Restore Defaults button	Sets the BIOS parameters on all three tabs to their default settings.

Advanced Tab

Reboot Server Option

If you want your changes applied automatically after you click **Save Changes**, check the **Reboot Host Immediately** check box. Cisco IMC immediately reboots the server and applies your changes.

If you want to apply your changes at a later time, clear the **Reboot Host Immediately** check box. Cisco IMC stores the changes and applies them the next time the server reboots.

Note If there are existing BIOS parameter changes pending, Cisco IMC automatically overwrites the stored values with the current settings when you click **Save Changes**.

Processor Configuration Parameters

Name	Description
Intel Hyper-Threading Technology **set IntelHyperThread**	Whether the processor uses Intel Hyper-Threading Technology, which allows multithreaded software applications to execute threads in parallel within each processor. This can be one of the following: • **Disabled**—The processor does not permit hyperthreading. • **Enabled**—The processor allows for the parallel execution of multiple threads. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.

Name	Description
Number of Enabled Cores **set CoreMultiProcessing**	Allows you to disable one or more of the physical cores on the server. This can be one of the following: • **All**—Enables all physical cores. This also enables Hyper Threading on the associated logical processor cores. • **1** through ***n***—Specifies the number of physical processor cores that can run on the server. Each physical core has an associated logical core. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Execute Disable **set ExecuteDisable**	Classifies memory areas on the server to specify where application code can execute. As a result of this classification, the processor disables code execution if a malicious worm attempts to insert code in the buffer. This setting helps to prevent damage, worm propagation, and certain classes of malicious buffer overflow attacks. This can be one of the following: • **Disabled**—The processor does not classify memory areas. • **Enabled**—The processor classifies memory areas. We recommend that you contact your operating system vendor to make sure the operating system supports this feature.
Intel VT **set IntelVT**	Whether the processor uses Intel Virtualization Technology (VT), which allows a platform to run multiple operating systems and applications in independent partitions. This can be one of the following: • **Disabled**—The processor does not permit virtualization. • **Enabled**—The processor allows multiple operating systems in independent partitions. **Note** If you change this option, you must power cycle the server before the setting takes effect.
Intel VT-d **set IntelVTD**	Whether the processor uses Intel Virtualization Technology for Directed I/O (VT-d). This can be one of the following: • **Disabled**—The processor does not use virtualization technology. • **Enabled**—The processor uses virtualization technology.

Name	Description
Intel VT-d Interrupt Remapping **set InterruptRemap**	Whether the processor supports Intel VT-d Interrupt Remapping. This can be one of the following: • **Disabled**—The processor does not support remapping. • **Enabled**—The processor uses VT-d Interrupt Remapping as required.
Intel VT-d PassThrough DMA **set PassThroughDMA**	Whether the processor supports Intel VT-d Pass-through DMA. This can be one of the following: • **Disabled**—The processor does not support pass-through DMA. • **Enabled**—The processor uses VT-d Pass-through DMA as required.
Intel VT-d Coherency Support **set CoherencySupport**	Whether the processor supports Intel VT-d Coherency. This can be one of the following: • **Disabled**—The processor does not support coherency. • **Enabled**—The processor uses VT-d Coherency as required.
Intel VT-d ATS Support **set ATS**	Whether the processor supports Intel VT-d Address Translation Services (ATS). This can be one of the following: • **Disabled**—The processor does not support ATS. • **Enabled**—The processor uses VT-d ATS as required.

Name	Description
CPU Performance **set CPUPerformance**	Sets the CPU performance profile for the server. The performance profile consists of the following options: • DCU Streamer Prefetcher • DCU IP Prefetcher • Hardware Prefetcher • Adjacent Cache-Line Prefetch This can be one of the following: • **Enterprise**—All options are enabled. • **High_Throughput**—Only the DCU IP Prefetcher is enabled. The rest of the options are disabled. • **HPC**—All options are enabled. This setting is also known as high performance computing. • **Custom**—All performance profile options can be configured from the BIOS setup on the server. In addition, the Hardware Prefetcher and Adjacent Cache-Line Prefetch options can be configured in the fields below.
Hardware Prefetcher **set HardwarePrefetch**	Whether the processor allows the Intel hardware prefetcher to fetch streams of data and instruction from memory into the unified second-level cache when necessary. This can be one of the following: • **Disabled**—The hardware prefetcher is not used. • **Enabled**—The processor uses the hardware prefetcher when cache issues are detected.
Adjacent Cache Line Prefetcher **set AdjacentCacheLinePrefetch**	Whether the processor fetches cache lines in even/odd pairs instead of fetching just the required line. This can be one of the following: • **Disabled**—The processor only fetches the required line. • **Enabled**— The processor fetches both the required line and its paired line.

Name	Description
DCU Streamer Prefetch **set DcuStreamerPrefetch**	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache. This can be one of the following: • **Disabled**—The processor does not try to anticipate cache read requirements and only fetches explicitly requested lines. • **Enabled**—The DCU prefetcher analyzes the cache read pattern and prefetches the next line in the cache if it determines that it may be needed.
DCU IP Prefetcher **set DcuIpPrefetch**	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache. This can be one of the following: • **Disabled**—The processor does not preload any cache data. • **Enabled**—The DCU IP prefetcher preloads the L1 cache with the data it determines to be the most relevant.
Direct Cache Access Support **set DirectCacheAccess**	Allows processors to increase I/O performance by placing data from I/O devices directly into the processor cache. This setting helps to reduce cache misses. This can be one of the following: • **Disabled**—Data from I/O devices is not placed directly into the processor cache. • **Enabled**—Data from I/O devices is placed directly into the processor cache.
Power Technology **set CPUPowerManagement**	Enables you to configure the CPU power management settings for the following options: • Enhanced Intel Speedstep Technology • Intel Turbo Boost Technology • Processor Power State C6 Power Technology can be one of the following: • **Custom**—The server uses the individual settings for the BIOS parameters mentioned above. You must select this option if you want to change any of these BIOS parameters. • **Disabled**—The server does not perform any CPU power management and any settings for the BIOS parameters mentioned above are ignored. • **Energy_Efficient**—The server determines the best settings for the BIOS parameters mentioned above and ignores the individual settings for these parameters.

Name	Description
Enhanced Intel Speedstep Technology **set EnhancedIntelSpeedStep**	Whether the processor uses Enhanced Intel SpeedStep Technology, which allows the system to dynamically adjust processor voltage and core frequency. This technology can result in decreased average power consumption and decreased average heat production. This can be one of the following: • **Disabled**—The processor never dynamically adjusts its voltage or frequency. • **Enabled**—The processor utilizes Enhanced Intel SpeedStep Technology and enables all supported processor sleep states to further conserve power. We recommend that you contact your operating system vendor to make sure the operating system supports this feature. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Intel Turbo Boost Technology **set IntelTurboBoostTech**	Whether the processor uses Intel Turbo Boost Technology, which allows the processor to automatically increase its frequency if it is running below power, temperature, or voltage specifications. This can be one of the following: • **Disabled**—The processor does not increase its frequency automatically. • **Enabled**—The processor utilizes Turbo Boost Technology if required. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Processor C3 Report **set ProcessorC3Report**	Whether the BIOS sends the C3 report to the operating system. When the OS receives the report, it can transition the processor into the lower C3 power state to decrease energy usage while maintaining optimal processor performance. This can be one of the following: • **Disabled**—BIOS does not send C3 report. • **Enabled**—BIOS sends the C3 report, allowing the OS to transition the processor to the C3 low power state. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.

Name	Description
Processor C6 Report **set ProcessorC6Report**	Whether the BIOS sends the C6 report to the operating system. When the OS receives the report, it can transition the processor into the lower C6 power state to decrease energy usage while maintaining optimal processor performance. This can be one of the following: • **Disabled**—The BIOS does not send the C6 report. • **Enabled**—The BIOS sends the C6 report, allowing the OS to transition the processor to the C6 low power state. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Processor Power State C1 Enhanced **set ProcessorC1EReport**	Whether the CPU transitions to its minimum frequency when entering the C1 state. This can be one of the following: • **Disabled**—The CPU continues to run at its maximum frequency in C1 state. • **Enabled**—The CPU transitions to its minimum frequency. This option saves the maximum amount of power in C1 state.
P-STATE Coordination **set PsdCoordType**	Allows you to define how BIOS communicates the P-state support model to the operating system. There are 3 models as defined by the Advanced Configuration and Power Interface (ACPI) specification. • **HW_ALL**—The processor hardware is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a package). • **SW_ALL**—The OS Power Manager (OSPM) is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a physical package), and must initiate the transition on all of the logical processors. • **SW_ANY**—The OS Power Manager (OSPM) is responsible for coordinating the P-state among logical processors with dependencies (all logical processors in a package), and may initiate the transition on any of the logical processors in the domain. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.

Name	Description
Boot Performance Mode drop-down list **set BootPerformanceMode**	Allows the user to select the BIOS performance state that is set before the operating system handoff. This can be one of the following: • **Max Performance**—Processor P-state ratio is maximum • **Max Efficient**— Processor P-state ratio is minimum
Energy Performance Tuning **set PwrPerfTuning**	Allows you to choose BIOS or Operating System for energy performance bias tuning. This can be one of the following: • **OS**— Chooses OS for energy performance tuning. • **BIOS**— Chooses BIOS for energy performance tuning.
Energy Performance **set CpuEngPerfBias**	Allows you to determine whether system performance or energy efficiency is more important on this server. This can be one of the following: • **Balanced_Energy** • **Balanced_Performance** • **Energy_Efficient** • **Performance**

Name	Description
Package C State Limit **set PackageCStateLimit**	The amount of power available to the server components when they are idle. This can be one of the following: • **C0_state**—The server provides all server components with full power at all times. This option maintains the highest level of performance and requires the greatest amount of power. • **C1_state**—When the CPU is idle, the system slightly reduces the power consumption. This option requires less power than C0 and allows the server to return quickly to high performance mode. • **C3_state**—When the CPU is idle, the system reduces the power consumption further than with the C1 option. This requires less power than C1 or C0, but it takes the server slightly longer to return to high performance mode. • **C6_state**—When the CPU is idle, the system reduces the power consumption further than with the C3 option. This option saves more power than C0, C1, or C3, but there may be performance issues until the server returns to full power. • **C7_state**—When the CPU is idle, the server makes a minimal amount of power available to the components. This option saves the maximum amount of power but it also requires the longest time for the server to return to high performance mode. • **No_Limit**—The server may enter any available C state.
Extended APIC **set LocalX2Apic**	Allows you to enable or disable extended APIC support. This can be one of the following: • **XAPIC**—Enables APIC support. • **X2APIC**—Enables APIC and also enables Intel VT-d and Interrupt Remapping .
Workload Configuration **set WorkLdConfig**	Allows you to set a parameter to optimize workload characterization. This can be one of the following: • **Balanced**— Chooses balanced option for optimization. • **I/O Sensitive**— Chooses I/O sensitive option for optimization. **Note** We recommend you to set the workload configuration to **Balanced**.

Name	Description
CPU HWPM drop-down list **set HWPMEnable**	Enables the Hardware Power Management (HWPM) interface for better CPU performance and energy efficiency. This can be one of the following: • **Disabled**—The P-States are controlled the same way as on predecessor processor generations. • **Native Mode**—HWPM works with the operating system through a software interface. • **OOB Mode**—The CPU autonomously controls its frequency based on the operating system energy efficiency.
CPU Autonomous Cstate drop-down list **set AutonumousCstateEnable**	Enables CPU Autonomous C-State, which converts the HALT instructions to the MWAIT instructions. This can be one of the following: • **Disabled**—CPU Autonomous C-state is disabled. This is the default value. • **Enabled**—CPU Autonomous C-state is enabled.
Processor CMCI drop-down list **set CmciEnable**	Allows the CPU to trigger interrupts on corrected machine check events. The corrected machine check interrupt (CMCI) allows faster reaction than the traditional polling timer. This can be one of the following: • **Disabled**—Disables CMCI. • **Enabled**—Enables CMCI. This is the default value.

Memory Configuration Parameters

Name	Description
Select Memory RAS **set SelectMemoryRAS**	How the memory reliability, availability, and serviceability (RAS) is configured for the server. This can be one of the following: • **Maximum_Performance**—System performance is optimized. • **Mirroring**—System reliability is optimized by using half the system memory as backup. • **Lockstep**—If the DIMM pairs in the server have an identical type, size, and organization and are populated across the SMI channels, you can enable lockstep mode to minimize memory access latency and provide better performance. This option offers better system performance than Mirroring and better reliability than Maximum Performance but lower reliability than Mirroring and lower system performance than Maximum Performance.

Name	Description
NUMA **set NUMAOptimize**	Whether the BIOS supports Non-Uniform Memory Access (NUMA). This can be one of the following: • **Disabled**—The BIOS does not support NUMA. • **Enabled**—The BIOS includes the ACPI tables that are required for NUMA-aware operating systems. If you enable this option, the system must disable Inter-Socket Memory interleaving on some platforms.
Channel Interleaving **set ChannelInterLeave**	Whether the CPU divides memory blocks and spreads contiguous portions of data across interleaved channels to enable simultaneous read operations. This can be one of the following: • **Auto**—The CPU determines what interleaving is done. • **1_Way**—Some channel interleaving is used. • **2_Way** • **3_Way** • **4_Way**—The maximum amount of channel interleaving is used.
Rank Interleaving **set RankInterLeave**	Whether the CPU interleaves physical ranks of memory so that one rank can be accessed while another is being refreshed. This can be one of the following: • **Auto**—The CPU determines what interleaving is done. • **1_Way**—Some rank interleaving is used. • **2_Way** • **4_Way** • **8_Way**—The maximum amount of rank interleaving is used.
Patrol Scrub **set PatrolScrub**	Whether the system actively searches for, and corrects, single bit memory errors even in unused portions of the memory on the server. This can be one of the following: • **Disabled**—The system checks for memory ECC errors only when the CPU reads or writes a memory address. • **Enabled**—The system periodically reads and writes memory searching for ECC errors. If any errors are found, the system attempts to fix them. This option may correct single bit errors before they become multi-bit errors, but it may adversely affect performance when the patrol scrub is running.

Name	Description
Demand Scrub **set DemandScrub**	Whether the system corrects single bit memory errors encountered when the CPU or I/O makes a demand read. This can be one of the following: • **Disabled**— Single bit memory errors are not corrected. • **Enabled**— Single bit memory errors are corrected in memory and the corrected data is set in response to the demand read.
Altitude **set Altitude**	The approximate number of meters above sea level at which the physical server is installed. This can be one of the following: • **Auto**—The CPU determines the physical elevation. • **300_M**—The server is approximately 300 meters above sea level. • **900_M**—The server is approximately 900 meters above sea level. • **1500_M**—The server is approximately 1500 meters above sea level. • **3000_M**—The server is approximately 3000 meters above sea level.
Panic and High Watermark drop-down list **PanicHighWatermark**	When set to low, the memory controller does not postpone refreshes while **Memory Refresh Rate** is set to **1X Refresh**. This can be one of the following: • **Low**—Refresh rate is set to low. • **High** —Refresh rate is set to high.

QPI Configuration Parameters

Name	Description
QPI Link Frequency Select **set QPILinkFrequency**	The Intel QuickPath Interconnect (QPI) link frequency, in gigatransfers per second (GT/s). This can be one of the following: • **Auto**—The CPU determines the QPI link frequency. • **6.4_GT/s** • **7.2_GT/s** • **8.0_GT/s**

Name	Description
QPI Snoop Mode **set QpiSnoopMode**	The Intel QuickPath Interconnect (QPI) snoop mode. This can be one of the following: • **Home Snoop**—The snoop is always spawned by the home agent (centralized ring stop) for the memory controller. This mode has a higher local latency than early snoop, but it provides extra resources for a larger number of outstanding transactions. • **Cluster on Die**—Enables Cluster On Die. When enabled LLC is split into two parts with an independent caching agent for each. This helps increase the performance in some workloads. This mode is available only for processors that have 10 or more cores. It is the best mode for highly NUMA optimized workloads. • **Early Snoop**—The distributed cache ring stops can send a snoop probe or a request to another caching agent directly. This mode has lower latency and it is best for workloads that have shared data sets across threads and can benefit from a cache-to-cache transfer, or for workloads that are not NUMA optimized.

USB Configuration Parameters

Name	Description
Legacy USB Support **set LegacyUSBSupport**	Whether the system supports legacy USB devices. This can be one of the following: • **Disabled**—USB devices are only available to EFI applications. • **Enabled**—Legacy USB support is always available. • **Auto**—Disables legacy USB support if no USB devices are connected.
Port 60/64 Emulation **set UsbEmul6064**	Whether the system supports 60h/64h emulation for complete USB keyboard legacy support. This can be one of the following: • **Disabled**—60h/64 emulation is not supported. • **Enabled**—60h/64 emulation is supported. You should select this option if you are using a non-USB aware operating system on the server.
xHCI Mode **set PchUsb30Mode**	Whether the xHCI controller legacy support is enabled or disabled. This can be one of the following: • **Disabled**—Disables the xHCI controller legacy support. • **Enabled**—Enables the xHCI controller legacy support.

Name	Description
xHCI Legacy Support drop-down list **set UsbXhciSupport**	Whether the system supports legacy xHCI controller. This can be one of the following: • **Disabled**—Disables xHCI legacy support. • **Enabled**—Enables xHCI legacy support. This is the default value.
All USB Devices **set AllUsbDevices**	Whether all physical and virtual USB devices are enabled or disabled. This can be one of the following: • **Disabled**—All USB devices are disabled. • **Enabled**—All USB devices are enabled.
USB Port: Rear **set UsbPortRear**	Whether the rear panel USB devices are enabled or disabled. This can be one of the following: • **Disabled**—Disables the rear panel USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled**—Enables the rear panel USB ports. Devices connected to these ports are detected by the BIOS and operating system.
USB Port: KVM **set UsbPortKVM**	Whether the vKVM ports are enabled or disabled. This can be one of the following: • **Disabled**—Disables the vKVM keyboard and/or mouse devices. Keyboard and/or mouse will not work in the vKVM window. • **Enabled**—Enables the vKVM keyboard and/or mouse devices.
USB Port: vMedia **set UsbPortVMedia**	Whether the virtual media devices are enabled or disabled. This can be one of the following: • **Disabled**—Disables the vMedia devices. • **Enabled**—Enables the vMedia devices.

PCI Configuration Parameters

Name	Description
Memory Mapped I/O Above 4GB **set MemoryMappedIOAbove4GB**	Whether to enable or disable MMIO above 4GB or not. This can be one of the following: • **Disabled**—The server does not map I/O of 64-bit PCI devices to 4GB or greater address space. • **Enabled**—The server maps I/O of 64-bit PCI devices to 4GB or greater address space. **Note** PCI devices that are 64-bit compliant but use a legacy option ROM may not function correctly with this setting enabled.
Sriov **set SrIov**	Whether SR-IOV (Single Root I/O Virtualization) is enabled or disabled on the server. This can be one of the following: • **Disabled**—SR-IOV is disabled. • **Enabled**—SR-IOV is enabled.

Serial Configuration Parameters

Name	Description
Out-of-Band Mgmt Port **set comSpcrEnable**	Allows you to configure the COM port 0 that can be used for Windows Emergency Management services. ACPI SPCR table is reported based on this setup option. This can be one of the following: • **Disabled**—Configures the COM port 0 as a general purpose port for use with the Windows Operating System. • **Enabled**—Configures the COM port 0 as a remote management port for Windows Emergency Management services.
Console Redirection **set ConsoleRedir**	Allows a serial port to be used for console redirection during POST and BIOS booting. After the BIOS has booted and the operating system is responsible for the server, console redirection is irrelevant and has no effect. This can be one of the following: • **Disabled**—No console redirection occurs during POST. • **COM_0**—Enables console redirection on COM port 0 during POST. • **COM_1**—Enables console redirection on COM port 1 during POST.

Name	Description
Terminal Type **set TerminalType**	What type of character formatting is used for console redirection. This can be one of the following: • **PC-ANSI**—The PC-ANSI terminal font is used. • **VT100**—A supported vt100 video terminal and its character set are used. • **VT100+**—A supported vt100-plus video terminal and its character set are used. • **VT-UTF8**—A video terminal with the UTF-8 character set is used. **Note** This setting must match the setting on the remote terminal application.
Bits per second **set BaudRate**	What BAUD rate is used for the serial port transmission speed. If you disable Console Redirection, this option is not available. This can be one of the following: • **9600**—A 9,600 BAUD rate is used. • **19200**—A 19,200 BAUD rate is used. • **38400**—A 38,400 BAUD rate is used. • **57600**—A 57,600 BAUD rate is used. • **115200**—A 115,200 BAUD rate is used. **Note** This setting must match the setting on the remote terminal application.
Flow Control **set FlowCtrl**	Whether a handshake protocol is used for flow control. Request to Send / Clear to Send (RTS/CTS) helps to reduce frame collisions that can be introduced by a hidden terminal problem. This can be one of the following: • **None**—No flow control is used. • **Hardware_RTS/CTS**—RTS/CTS is used for flow control. **Note** This setting must match the setting on the remote terminal application.

Name	Description
Putty KeyPad **set PuttyFunctionKeyPad**	Allows you to change the action of the PuTTY function keys and the top row of the numeric keypad. This can be one of the following: • **VT100**—The function keys generate **ESC OP** through **ESC O[.** • **LINUX**—Mimics the Linux virtual console. Function keys F6 to F12 behave like the default mode, but F1 to F5 generate **ESC [[A** through **ESC [[E**. • **XTERMR6**—Function keys F5 to F12 behave like the default mode. Function keys F1 to F4 generate **ESC OP** through ESC OS, which are the sequences produced by the top row of the keypad on Digital terminals. • **SCO**—The function keys F1 to F12 generate **ESC [M** through **ESC [X**. The function and shift keys generate **ESC [Y** through **ESC [j**. The control and function keys generate **ESC [k** through **ESC [v**. The shift, control and function keys generate **ESC [w** through **ESC [{**. • **ESCN**—The default mode. The function keys match the general behavior of Digital terminals. The function keys generate sequences such as **ESC [11~** and **ESC [12~**. • **VT400**—The function keys behave like the default mode. The top row of the numeric keypad generates **ESC OP** through **ESC OS**.
Redirection After BIOS POST **set RedirectionAfterPOST**	Whether BIOS console redirection should be active after BIOS POST is complete and control given to the OS bootloader. This can be one of the following: • **Always_Enable**—BIOS Legacy console redirection is active during the OS boot and run time. • **Bootloader**—BIOS Legacy console redirection is disabled before giving control to the OS boot loader.

LOM and PCIe Slots Configuration Parameters

Name	Description
CDN Support for VIC **set CdnEnable**	Whether the Ethernet Network naming convention is according to Consistent Device Naming (CDN) or the traditional way of naming conventions. This can be one of the following: • **Disabled**— CDN support for VIC cards is disabled. • **Enabled**— CDN support is enabled for VIC cards. **Note** CDN support for VIC cards work with Windows 2012 or the latest OS only.

Name	Description
PCI ROM CLP **set PciRomClp**	PCI ROM Command Line Protocol (CLP) controls the execution of different Option ROMs such as PxE and iSCSI that are present in the card. By default, it is disabled. • **Enabled**— Enables you to configure execution of different option ROMs such as PxE and iSCSI for an individual ports separately. • **Disabled**—The default option. You cannot choose different option ROMs. A default option ROM is executed during PCI enumeration.
All PCIe Slots OptionROM **set PcieOptionROMs**	Whether the server can use Option ROM present in the PCIe Cards. This can be one of the following: • **Disabled**—The Option ROM for slot ***n*** is not available. • **Enabled**—The Option ROM for slot ***n*** is available. • **UEFI_Only**—The Option ROM for slot ***n*** is available for UEFI only. • **Legacy_Only**—The Option ROM for slot ***n*** is available for legacy only.
PCH SATA Mode **set SataModeSelect**	This options allows you to select the PCH SATA mode. This can be one of the following: • **AHCI**—Sets both SATA and sSATA controllers to AHCI mode. • **Disabled**—Disables both SATA and sSATA controllers. • **LSI SW Raid**— Sets both SATA and sSATA controllers to raid mode for LSI SW Raid
SBNVMe1 OptionROM **set SBNVMe1OptionROM**	Whether the server can use Option ROM present in SBNVMe1 controller. This can be one of the following: • **Disabled**—The Option ROM for SBNVMe1 controllers is not available. • **Enabled**—The Option ROMs for SBNVMe1 controller is available. • **UEFI_Only**—The Option ROMs for slot are available for UEFI only. • **Legacy_Only**—The Option ROM for slot are available for legacy only.

Name	Description
SIOC1 OptionROM **set SIOC1OptionROM**	Whether the server can use Option ROM present in System IO Controller 1 (SIOC1). This can be one of the following: • **Disabled**—The Option ROM for System IO Controller 1 (SIOC1) is not available. • **Enabled**—The Option ROMs for System IO Controller 1 (SIOC1) is available. • **UEFI_Only**—The Option ROMs for slot are available for UEFI only. • **Legacy_Only**—The Option ROM for slot are available for legacy only.
SIOC2 OptionROM **set SIOC2OptionROM**	Whether the server can use Option ROM present in System IO Controller 2 (SIOC2). This can be one of the following: • **Disabled**—The Option ROM for System IO Controller 2 (SIOC2) is not available. • **Enabled**—The Option ROMs for System IO Controller 2 (SIOC2) is available. • **UEFI_Only**—The Option ROMs for slot are available for UEFI only. • **Legacy_Only**—The Option ROM for slot are available for legacy only.
SBMezz1 OptionROM **set SBMezz1OptionROM**	Whether the server can use Option ROM present in SBMezz1 controller. This can be one of the following: • **Disabled**—The Option ROM for SBMezz1 controllers is not available. • **Enabled**—The Option ROMs for SBMezz1 controller is available. • **UEFI_Only**—The Option ROMs for slot are available for UEFI only. • **Legacy_Only**—The Option ROM for slot are available for legacy only.

Name	Description
SBMezz2 OptionROM drop-down list **set SBMezz2OptionROM**	Whether the server can use Option ROM that is available in the SBMezz2 controller. This can be one of the following: • **Disabled**—The Option ROM for SBMezz 2 controllers is not available. • **Enabled**—The Option ROM for SBMezz 2 controllers is available. • **UEFI Only**—The Option ROMs for slot are available for UEFI only. • **Legacy Only**—The Option ROMs for slot are available for legacy only.
IOESlot1 OptionROM **set IOESlot1OptionROM**	Whether option ROM is enabled on the IOE slot 1. This can be one of the following: • **Disabled**— Option ROM is disabled. • **Enabled**— Default value. Option ROM is enabled. • **UEFI Only**— slot 1 option ROM is available for UEFI only. • **Legacy Only**— slot 1 option ROM is available for legacy only.
IOEMezz1 OptionROM **set IOEMezz1OptionROM**	Whether option ROM is enabled on the IOE Mezz1. This can be one of the following: • **Disabled**— Option ROM is disabled. • **Enabled**— Default value. Option ROM is enabled. • **UEFI Only**— Mezz1 option ROM is available for UEFI only. • **Legacy Only**— Mezz1 option ROM is available for legacy only.
IOESlot2 OptionROM **set IOESlot2OptionROM**	Whether option ROM is enabled on the IOE slot 2. This can be one of the following: • **Disabled**— Option ROM is disabled. • **Enabled**— Default value. Option ROM is enabled. • **UEFI Only**— slot 2 option ROM is available for UEFI only. • **Legacy Only**— slot 2 option ROM is available for legacy only.

Name	Description
IOENVMe1 OptionROM **set IOENVMe1OptionROM**	Whether option ROM is enabled on the IOE NVMe1. This can be one of the following: • **Disabled**— Option ROM is disabled. • **Enabled**— Default value. Option ROM is enabled. • **UEFI Only**— Mezz1 option ROM is available for UEFI only. • **Legacy Only**— Mezz1 option ROM is available for legacy only.
IOENVMe2 OptionROM **set IOENVMe2OptionROM**	Whether option ROM is enabled on the IOE NVMe2. This can be one of the following: • **Disabled**— Option ROM is disabled. • **Enabled**— Default value. Option ROM is enabled. • **UEFI Only**— Mezz1 option ROM is available for UEFI only. • **Legacy Only**— Mezz1 option ROM is available for legacy only.
SBNVMe1 Link Speed **Set SBNVMe1LinkSpeed**	SBNVMe1 add-on slot 1 link speed. • **Auto**—Link speed is automatically assigned. • **GEN1**— Link speed can reach up to first generation. • **GEN2**—The default link speed. Link speed can reach up to second generation. • **GEN3**— Link speed can reach up to third generation. • **Disabled**—Slot is disabled, and the card is not enumerated.
SIOC1 Link Speed **Set PcieSlot1LinkSpeed**	System IO Controller 1 (SIOC1) add-on slot 1 link speed. • **GEN1** — Link speed can reach up to first generation. • **GEN2** — Link speed can reach up to second generation. • **GEN3**— The default link speed. Link speed can reach up to third generation. • **Disabled** — Slot is disabled, and the card is not enumerated.
SIOC2 Link Speed **set PcieSlot2LinkSpeed**	System IO Controller 2 (SIOC2) add-on slot 2 link speed. • **GEN1** — Link speed can reach up to first generation. • **GEN2** — Link speed can reach up to second generation. • **GEN3**— The default link speed. Link speed can reach up to third generation. • **Disabled** — Slot is disabled, and the card is not enumerated.

Name	Description
SBMezz1 Link Speed **set SBMezz1LinkSpeed**	SBMezz1 add-on slot 1 link speed. • **Auto**—Link speed is automatically assigned. • **GEN1**— Link speed can reach up to first generation. • **GEN2**—The default link speed. Link speed can reach up to second generation. • **GEN3**— Link speed can reach up to third generation. • **Disabled**—Slot is disabled, and the card is not enumerated.
SBMezz2 Link Speed drop-down list **set SBMezz2LinkSpeed**	Assigns SBMezz2 add-on slot 2 link speed. This can be one of the following: • **Auto**— Default value. Slot is enabled. • **GEN 1**— Link speed can reach up to first generation. • **GEN 2**— Link speed can reach up to second generation. • **GEN 3**— Link speed can reach up to third generation. • **Disabled**—Slot is disabled, and the card is not enumerated.
IOESlot1 Link Speed **set IOESlot1LinkSpeed**	Slot 1 link speed. This can be one of the following: • **Auto**— Default value. Slot is enabled. • **GEN 1**— Link speed can reach up to first generation. • **GEN 2**— Link speed can reach up to second generation. • **GEN 3**— Link speed can reach up to third generation. • **Disabled**—Slot is disabled, and the card is not enumerated.
IOEMezz1 Link Speed **set IOEMezz1LinkSpeed**	Mezz1 link speed. This can be one of the following: • **Auto**— Default value. Slot is enabled. • **GEN 1**— Link speed can reach up to first generation. • **GEN 2**— Link speed can reach up to second generation. • **GEN 3**— Link speed can reach up to third generation. • **Disabled**—Slot is disabled, and the card is not enumerated.

Name	Description
IOESlot2 Link Speed **set IOESlot2LinkSpeed**	Slot 2 link speed. This can be one of the following: • **Auto**— Default value. Slot is enabled. • **GEN 1**— Link speed can reach up to first generation. • **GEN 2**— Link speed can reach up to second generation. • **GEN 3**— Link speed can reach up to third generation. • **Disabled**—Slot is disabled, and the card is not enumerated.
IOENVMe1 Link Speed **set IOENVMe1LinkSpeed**	NVMe1 link speed. This can be one of the following: • **Auto**— Default value. Slot is enabled. • **GEN 1**— Link speed can reach up to first generation. • **GEN 2**— Link speed can reach up to second generation. • **GEN 3**— Link speed can reach up to third generation. • **Disabled**—Slot is disabled, and the card is not enumerated.
IOENVMe2 Link Speed **set IOENVMe2LinkSpeed**	NVMe2 link speed. This can be one of the following: • **Auto**— Default value. Slot is enabled. • **GEN 1**— Link speed can reach up to first generation. • **GEN 2**— Link speed can reach up to second generation. • **GEN 3**— Link speed can reach up to third generation. • **Disabled**—Slot is disabled, and the card is not enumerated.

BIOS Configuration Dialog Box Button Bar

Important The buttons in this dialog box affect all BIOS parameters on all available tabs, not just the parameters on the tab that you are viewing.

Name	Description
Save Changes button	Saves the settings for the BIOS parameters on all three tabs and closes the dialog box. If the **Reboot Host Immediately** check box is checked, the server is rebooted immediately and the new BIOS settings go into effect. Otherwise the changes are saved until the server is manually rebooted.
Reset Values button	Restores the values for the BIOS parameters on all three tabs to the settings that were in effect when this dialog box was first opened.

Name	Description
Restore Defaults button	Sets the BIOS parameters on all three tabs to their default settings.
Cancel button	Closes the dialog box without making any changes.

Server Management Tab

Server Management BIOS Parameters

Name	Description
FRB-2 Timer **set FRB-2**	Whether the FRB2 timer is used by Cisco IMC to recover the system if it hangs during POST. This can be one of the following: • **Disabled**—The FRB2 timer is not used. • **Enabled**—The FRB2 timer is started during POST and used to recover the system if necessary.
OS Watchdog Timer **set OSBootWatchdogTimer**	Whether the BIOS programs the watchdog timer with a specified timeout value. This can be one of the following: • **Disabled**—The watchdog timer is not used to track how long the server takes to boot. • **Enabled**—The watchdog timer tracks how long the server takes to boot. If the server does not boot within the length of time specified by the **set OSBootWatchdogTimerTimeout** command, the Cisco IMC logs an error and takes the action specified by the **set OSBootWatchdogTimerPolicy** command.
OS Watchdog Timer Timeout **set OSBootWatchdogTimerTimeOut**	If OS does not boot within the specified time, OS watchdog timer expires and system takes action according to timer policy. This can be one of the following: • **5_Minutes**—The OS watchdog timer expires 5 minutes after it begins to boot. • **10_Minutes**—The OS watchdog timer expires 10 minutes after it begins to boot. • **15_Minutes**—The OS watchdog timer expires 15 minutes after it begins to boot. • **20_Minutes**—The OS watchdog timer expires 20 minutes after it begins to boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.

Name	Description
OS Watchdog Timer Policy **set OSBootWatchdogTimerPolicy**	What action the system takes if the watchdog timer expires. This can be one of the following: • **Do_Nothing**—The server takes no action if the watchdog timer expires during OS boot. • **Power_Down**—The server is powered off if the watchdog timer expires during OS boot. • **Reset**—The server is reset if the watchdog timer expires during OS boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.

S3260 M5 Servers

I/O Tab

Note BIOS parameters listed in this tab may vary depending on the server.

Table 1: BIOS Parameters in I/O Tab

Name	Description
Reboot Host Immediately checkbox	Upon checking, reboots the host server immediately. You must check the checkbox after saving changes.
Legacy USB Support drop-down list **set UsbLegacySupport**	Whether the system supports legacy USB devices. This can be one of the following: • **Disabled**—USB devices are only available to EFI applications. • **Enabled**—Legacy USB support is always available.
Intel VT for directed IO drop-down list **set IntelVTD**	Whether the processor uses Intel Virtualization Technology (VT), which allows a platform to run multiple operating systems and applications in independent partitions. This can be one of the following: • **Disabled**—The processor does not permit virtualization. • **Enabled**—The processor allows multiple operating systems in independent partitions. **Note** If you change this option, you must power cycle the server before the setting takes effect.

Name	Description
Intel VTD coherency support drop-down list **set CoherencySupport**	Whether the processor supports Intel VT-d Coherency. This can be one of the following: • **Disabled**—The processor does not support coherency. • **Enabled**—The processor uses VT-d Coherency as required.
Intel VTD ATS support drop-down list **set ATS**	Whether the processor supports Intel VT-d Address Translation Services (ATS). This can be one of the following: • **Disabled**—The processor does not support ATS. • **Enabled**—The processor uses VT-d ATS as required.
PCIe RAS Support drop-down list	Whether PCIe RAS Support is available on the PCIe slot. This can be one of the following: • **Enabled**— PCIe RAS is available on the slot. • **Disabled**— PCIe RAS is not available on port.
All Onboard LOM Ports drop-down list	Whether all LOM ports are enabled or disabled. This can be one of the following: • **Enabled**— All LOM ports are enabled. • **Disabled**— All LOM ports are disabled.
LOM Port 0 OptionROM drop-down list	Whether Option ROM is available on the LOM port 0. This can be one of the following: • **Disabled**—Option ROM is not available on LOM port 0. • **Enabled**—Option ROM is available on LOM port 0.
LOM Port 1 OptionROM	Whether Option ROM is available on the LOM port 1. This can be one of the following: • **Disabled**—Option ROM is not available on LOM port 1. • **Enabled**—Option ROM is available on LOM port 1.
PCIe Slot *n***OptionROM**drop-down list	Whether the server can use the Option ROMs present in the PCIe Cards. This can be one of the following: • **Disabled**—Option ROM is not available on slot *n*. • **Enabled**—Option ROM is available on slot *n*.
MRAID OptionROM	Whether the server can use the RAID Option ROMs present in the PCIe card slot designated by *n*. This can be one of the following: • **Disabled**—Option ROM for slot *n* is not available. • **Enabled**—Option ROM for slot *n* is available.

Name	Description
MLOM Oprom drop-down list **set PcieSlotMLOMOptionROM**	This options allows you to control the Option ROM execution of the PCIe adapter connected to the MLOM slot. This can be one of the following: • **Disabled**—Does not execute Option ROM of the PCIe adapter connected to the MLOM slot. • **Enabled**—Executes Option ROM of the PCIe adapter connected to the MLOM slot.
HBA Oprom drop-down list **set PcieSlotHBAOptionROM**	This options allows you to control the Option ROM execution of the PCIe adapter connected to the HBA slot. This can be one of the following: • **Disabled**—Does not execute Option ROM of the PCIe adapter connected to the HBA slot. • **Enabled**—Executes Option ROM of the PCIe adapter connected to the HBA slot.
Front NVME1 Oprom drop-down list **set PcieSlotN1OptionROM**	This options allows you to control the Option ROM execution of the PCIe adapter connected to the SSD:NVMe1 slot. This can be one of the following: • **Disabled**—Does not execute Option ROM of the PCIe adapter connected to the SSD:NVMe1 slot. • **Enabled**—Executes Option ROM of the PCIe adapter connected to the SSD:NVMe1 slot
Front NVME2 Oprom drop-down list **set PcieSlotN2OptionROM**	This options allows you to control the Option ROM execution of the PCIe adapter connected to the SSD:NVMe2 slot. This can be one of the following: • **Disabled**—Does not execute Option ROM of the PCIe adapter connected to the SSD:NVMe2 slot. • **Enabled**—Executes Option ROM of the PCIe adapter connected to the SSD:NVMe2 slot
HBA Link Speed drop-down list **set PcieSlotHBALinkSpeed**	This option allows you to restrict the maximum speed of an adapter card installed in PCIe HBA slot. This can be one of the following: • **Disabled**—The maximum speed is not restricted. • **Auto**—System selects the maximum speed allowed. • **GEN1**—2.5GT/s (gigatransfers per second) is the maximum speed allowed. • **GEN2**—5GT/s is the maximum speed allowed. • **GEN3**—8GT/s is the maximum speed allowed.

Name	Description
MLOM Link Speed drop-down list **set PcieSlotMLOMLinkSpeed**	This option allows you to restrict the maximum speed of an adapter card installed in PCIe MLOM slot. This can be one of the following: • **Disabled**—The maximum speed is not restricted. • **Auto**—System selects the maximum speed allowed. • **GEN1**—2.5GT/s (gigatransfers per second) is the maximum speed allowed. • **GEN2**—5GT/s is the maximum speed allowed. • **GEN3**—8GT/s is the maximum speed allowed.
MRAID Link Speed drop-down list	This option allows you to restrict the maximum speed of an adapter card installed in MRAID slot. This can be one of the following: • **Disabled**—The maximum speed is not restricted. • **Auto**—System selects the maximum speed allowed. • **GEN1**—2.5GT/s (gigatransfers per second) is the maximum speed allowed. • **GEN2**—5GT/s is the maximum speed allowed. • **GEN3**—8GT/s is the maximum speed allowed.
PCIe Slot*n* Link Speed drop-down list **set PcieSlotnLinkSpeed**	System IO Controller *n* (SIOCn) add-on slot (designated by *n*) link speed. This can be one of the following: • **Disabled**—Slot is disabled, and the card is not enumerated. • **Auto**— The default link speed. Link speed is automatically assigned. • **GEN1**—Link speed can reach up to first generation. • **GEN2**—Link speed can reach up to second generation. • **GEN3**—Link speed can reach up to third generation.
Front NVME1 Link Speed drop-down list **set PcieSlotFrontNvme1LinkSpeed**	Link speed for NVMe front slot 1. This can be one of the following: • **Disabled**—Slot is disabled, and the card is not enumerated. • **Auto**—The default link speed. Link speed is automatically assigned. • **GEN1**—Link speed can reach up to first generation. • **GEN2**—Link speed can reach up to second generation. • **GEN3**—Link speed can reach up to third generation.

Name	Description
Front NVME2 Link Speed drop-down list **set PcieSlotFrontNvme2LinkSpeed**	Link speed for NVMe front slot 2. This can be one of the following: • **Disabled**—Slot is disabled, and the card is not enumerated. • **Auto**—The default link speed. Link speed is automatically assigned. • **GEN1**—Link speed can reach up to first generation. • **GEN2**—Link speed can reach up to second generation. • **GEN3**—Link speed can reach up to third generation.
Rear NVME1 Link Speed drop-down list **set PcieSlotRearNvme1LinkSpeed**	Link speed for NVMe rear slot 1. This can be one of the following: • **Disabled**—Slot is disabled, and the card is not enumerated. • **Auto**—The default link speed. Link speed is automatically assigned. • **GEN1**—Link speed can reach up to first generation. • **GEN2**—Link speed can reach up to second generation. • **GEN3**—Link speed can reach up to third generation.
Rear NVME2 Link Speed drop-down list **set PcieSlotRearNvme2LinkSpeed**	Link speed for NVMe rear slot 2. This can be one of the following: • **Disabled**—Slot is disabled, and the card is not enumerated. • **Auto**—The default link speed. Link speed is automatically assigned. • **GEN1**—Link speed can reach up to first generation. • **GEN2**—Link speed can reach up to second generation. • **GEN3**—Link speed can reach up to third generation.
VGA Priority drop-down list **set VgaPriority**	Allows you to set the priority for VGA graphics devices if multiple VGA devices are found in the system. This can be one of the following: • **OnBoard**—Priority is given to the onboard VGA device. BIOS post screen and OS boot are driven through the onboard VGA port. • **OffBoard**—Priority is given to the PCIE Graphics adapter. BIOS post screen and OS boot are driven through the external graphics adapter port. • **OnBoard VGA Disabled**—Priority is given to the PCIe Graphics adapter, and the onboard VGA device is disabled. The vKVM does not function when the onboard VGA is disabled.
P-SATA OptionROM drop-down list **set pSATA**	Allows you to select the PCH SATA optionROM mode. This can be one of the following: • **LSI SW Raid**— Sets both SATA and sSATA controllers to raid mode for LSI SW Raid. • **Disabled**— Disables both SATA and sSATA controllers.

Name	Description
M2.SATA OptionROM drop-down list **set SataModeSelect**	Mode of operation of Serial Advanced Technology Attachment (SATA) Solid State Drives (SSD). This can be one of the following: • **AHCI**— Sets both SATA and sSATA controllers to AHCI mode. • **LSI SW Raid**— Sets both SATA and sSATA controllers to raid mode for LSI SW Raid. • **Disabled**— Disables both SATA and sSATA controllers.
USB Port Rear drop-down list **set UsbPortRear**	Whether the rear panel USB devices are enabled or disabled. This can be one of the following • **Disabled**— Disables the rear panel USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled**— Enables the rear panel USB ports. Devices connected to these ports are detected by the BIOS and operating system.
USB Port Front drop-down list **set UsbPortFront**	Whether the front panel USB devices are enabled or disabled. This can be one of the following • **Disabled**— Disables the front panel USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled**— Enables the front panel USB ports. Devices connected to these ports are detected by the BIOS and operating system.
USB Port Internal drop-down list **set UsbPortInt**	Whether the internal USB devices are enabled or disabled. This can be one of the following • **Disabled**— Disables the internal USB ports. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled**— Enables the internal USB ports. Devices connected to these ports are detected by the BIOS and operating system.
USB Port KVM drop-down list **set UsbPortKVM**	Whether the vKVM ports are enabled or disabled. This can be one of the following • **Disabled**— Disables the vKVM keyboard and/or mouse devices. Keyboard and/or mouse will not work in the KVM window. • **Enabled**— Enables the vKVM keyboard and/or mouse devices.
USB Port Internal drop-down list	Whether the USB Port Internal is enabled or disabled. This can be one of the following • **Disabled**— Disables the USB Port Internal. Devices connected to these ports are not detected by the BIOS and operating system. • **Enabled**— Enables the USB Port Internal. Devices connected to these ports are detected by the BIOS and operating system.

Name	Description
IPV6 PXE Support drop-down list **set IPV6PXE**	Enables or disables IPv6 support for PXE. This can be one of the following • **disabled**—IPv6 PXE support is not available. • **enabled**—IPv6 PXE support is always available.
IPv4 HTTP Support	Enables or disables IPv4 support for HTTP. This can be one of the following • **disabled**—IPv4 HTTP support is not available. • **enabled**—IPv4 HTTP support is always available.
IPv6 HTTP Support	Enables or disables IPv6 support for HTTP. This can be one of the following • **disabled**—IPv6 PXE support is not available. • **enabled**—IPv6 PXE support is always available.
PCIe PLL SSC drop-down list **set PciePllSsc**	Enable this feature to reduce EMI interference by down spreading clock 0.5%. Disable this feature to centralize the clock without spreading. This can be one of the following: • **auto**—EMI interference is auto adjusted. **Disabled**—EMI interference is auto adjusted. • **ZeroPointFive**—EMI interference is reduced by down spreading the clock 0.5%.
IPV4 PXE Support drop-down list **set IPV4PXE**	Enables or disables IPv4 support for PXE. This can be one of the following • **disabled**—IPv4 PXE support is not available. • **enabled**—IPv4 PXE support is always available.
Network Stack drop-down list **set NetworkStack**	This option allows you to monitor IPv6 and IPv4. This can be one of the following • **disabled**—Network Stack support is not available. **Note** When disabled, the value set for **IPV4 PXE Support** does not impact the system. • **enabled**—Network Stack support is always available.
External SSC enable drop-down list **set EnableClockSpreadSpec**	This option allows you to reduce the EMI of your motherboard by modulating the signals it generates so that the spikes are reduced to flatter curves. This can be one of the following: • **Disabled**—Clock Spread Spectrum support is not available. • **Enabled**—Clock Spread Spectrum support is always available.

Name	Description
PCIe Slot MSTOR RAID OptionROM drop-down list **set PcieSlotMSTORRAIDOptionROM**	Whether the server can use the Option ROMs present in the PCIe MSTOR RAID. This can be one of the following: • **Disabled**—Option ROM is not available. • **Enabled**—Option ROM is available.

Server Management Tab

Note BIOS parameters listed in this tab may vary depending on the server.

Table 2: BIOS Parameters in Server Management Tab

Name	Description
Reboot Host Immediately checkbox	If the Reboot Host Immediately check box is checked, the server is rebooted immediately and the new BIOS settings go into effect. Otherwise the changes are saved until the server is manually rebooted.
OS Boot Watchdog Timer Policy drop-down list **set OSBootWatchdogTimerPolicy**	What action the system takes if the watchdog timer expires. This can be one of the following: • **Power Off**—The server is powered off if the watchdog timer expires during OS boot. • **Reset**—The server is reset if the watchdog timer expires during OS boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.
OS Watchdog Timer drop-down list **set OSBootWatchdogTimer**	Whether the BIOS programs the watchdog timer with a specified timeout value. This can be one of the following: • **Disabled**—The watchdog timer is not used to track how long the server takes to boot. • **Enabled**—The watchdog timer tracks how long the server takes to boot. If the server does not boot within the length of time specified in the **OS Boot Watchdog Timer Timeout** field, the Cisco IMC logs an error and takes the action specified in the **OS Boot Watchdog Policy** field.

Name	Description
OS Watchdog Timer Timeout drop-down list **set OSBootWatchdogTimerTimeOut**	If OS does not boot within the specified time, OS watchdog timer expires and system takes action according to timer policy. This can be one of the following: • **5 Minutes**—The OS watchdog timer expires 5 minutes after it begins to boot. • **10 Minutes**—The OS watchdog timer expires 10 minutes after it begins to boot. • **15 Minutes**—The OS watchdog timer expires 15 minutes after it begins to boot. • **20 Minutes**—The OS watchdog timer expires 20 minutes after it begins to boot. **Note** This option is only applicable if you enable the OS Boot Watchdog Timer.
Baud Rate drop-down list **set BaudRate**	What Baud rate is used for the serial port transmission speed. If you disable Console Redirection, this option is not available. This can be one of the following: • **9.6k**—A 9,600 Baud rate is used. • **19.2k**—A 19,200 Baud rate is used. • **38.4k**—A 38,400 Baud rate is used. • **57.6k**—A 57,600 Baud rate is used. • **115.2k**—A 115,200 Baud rate is used. This setting must match the setting on the remote terminal application.
Console Redirection drop-down list **set ConsoleRedir**	Allows a serial port to be used for console redirection during POST and BIOS booting. After the OS has booted, console redirection is irrelevant. This can be one of the following: • **Serial Port A**—Enables console redirection on serial port A during POST. • **Serial Port B**—Enables console redirection on serial port B during POST. • **Disabled**—No console redirection occurs during POST.

Name	Description
Adaptive Memory Training	When this option is **Enabled**: The Memory training will not happen in every boot but the BIOS will use the saved memory training result in every re-boot. Some exceptions when memory training happens in every boot are: BIOS update, CMOS reset, CPU or Memory configuration change, SPD or run-time uncorrectable error or the last boot has occurred more than 24 hours before. When this option is **Disabled**, the Memory training happens in every boot. Default value: **Enabled**. **Note** To disable the Fast Boot option, the end user must set the following tokens as mentioned below: Adaptive Memory Training to **Disabled** BIOS Techlog level to **Normal** OptionROM Launch Optimization to **Disabled**.
BIOS Techlog Level	This option denotes the type of messages in **BIOS tech log** file. The log file can be one of the following types: • **Minimum** - Critical messages will be displayed in the log file. • **Normal** - Warning and loading messages will be displayed in the log file. • **Maximum** - Normal and information related messages will be displayed in the log file. Default value: **Minimum**. **Note** This option is mainly for internal debugging purposes.

Name	Description
OptionROM Launch Optimization	When this option is **Enabled**, the OptionROMs only for the controllers present in the boot order policy will be launched. **Note** Some controllers such as Onboard storage controllers, Emulex FC adapters, and GPU controllers though not listed in the boot order policy will have the OptionROM launched. When this option is **Disabled**, all the OptionROMs will be launched. Default value: **Enabled**
CDN Control drop-down list **set cdnEnable**	Whether the Ethernet Network naming convention is according to Consistent Device Naming (CDN) or the traditional way of naming conventions. This can be one of the following: • **Disabled**— CDN support for VIC cards is disabled • **Enabled**— CDN support is enabled for VIC cards.
FRB 2 Timer drop-down list **set FRB-2**	Whether the FRB2 timer is used by Cisco IMC to recover the system if it hangs during POST. This can be one of the following: • **Disabled**—The FRB2 timer is not used. • **Enabled**—The FRB2 timer is started during POST and used to recover the system if necessary.
Flow Control drop-down list **set FlowCtrl**	Whether a handshake protocol is used for flow control. Request to Send / Clear to Send (RTS/CTS) helps to reduce frame collisions that can be introduced by a hidden terminal problem. This can be one of the following: • **None**—No flow control is used. • **RTS/CTS**—RTS/CTS is used for flow control. **Note** This setting must match the setting on the remote terminal application.

Name	Description
Terminal type drop-down list **set TerminalType**	What type of character formatting is used for console redirection. This can be one of the following: • **PC-ANSI**—The PC-ANSI terminal font is used. • **VT100**—A supported VT100 video terminal and its character set are used. • **VT100-PLUS**—A supported VT100-plus video terminal and its character set are used. • **VT-UTF8**—A video terminal with the UTF-8 character set is used.

Security Tab

Note BIOS parameters listed in this tab may vary depending on the server.

Table 3: BIOS Parameters in Security Tab

Name	Description
Reboot Host Immediately checkbox	**If the Reboot Host Immediately check box is checked, the server is rebooted immediately and the new BIOS settings go into effect. Otherwise the changes are saved until the server is manually rebooted.**
Trusted Platform Module State drop-down list **set TPMAdminCtrl**	Trusted Platform Module (TPM) is a microchip designed to provide basic security-related functions primarily involving encryption keys. This option allows you to control the TPM Security Device support for the system. It can be one of the following: • **Disabled**—The server does not use the TPM. • **Enabled**—The server uses the TPM. **Note** Contact your operating system vendor to make sure the operating system supports this feature.
SHA-1 PCR Bank	Enable or Disable SHA-1 PCR Bank. This can be one of the following: • **Disabled**—Support is disabled. • **Enabled**—Support is enabled.

Name	Description
Reboot Host Immediately checkbox	**If the Reboot Host Immediately check box is checked, the server is rebooted immediately and the new BIOS settings go into effect. Otherwise the changes are saved until the server is manually rebooted.**
SHA256 PCR Bank	Enable or Disable SHA256 PCR Bank. This can be one of the following: • **Disabled**—Support is disabled. • **Enabled**—Support is enabled.
Intel Trusted Execution Technology Support	Can be Enabled only when Trusted Platform Module (TPM) is Enabled. This can be one of the following: • **Disabled**—Support is disabled. • **Enabled**—Support is enabled.
Power ON Password drop-down list **set PowerOnPassword**	This token requires that you set a BIOS password before using the F2 BIOS configuration. If enabled, password needs to be validated before you access BIOS functions such as IO configuration, BIOS set up, and booting to an operating system using BIOS. It can be one of the following: • **Disabled**—Support is disabled. • **Enabled**—Support is enabled.

Processor Tab

Note BIOS parameters listed in this tab may vary depending on the server.

Table 4: BIOS Parameters in Processor Tab

Name	Description
Intel Virtualization Technology drop-down list **set IntelVT**	Whether the processor uses Intel Virtualization Technology (VT), which allows a platform to run multiple operating systems and applications in independent partitions. This can be one of the following: • **Disabled**—The processor does not permit virtualization. • **Enabled**—The processor allows multiple operating systems in independent partitions.
Extended APIC drop-down list **set LocalX2Apic**	Allows you to enable or disable extended APIC support. This can be one of the following: • **Enabled**—Enables APIC support • **Disabled**—Disables APIC support.
Processor C1E drop-down list **set ProcessorC1E**	Whether the CPU transitions to its minimum frequency when entering the C1 state. This can be one of the following: • **Disabled**—The CPU continues to run at its maximum frequency in C1 state. • **Enabled**—The CPU transitions to its minimum frequency. This option saves the maximum amount of power in C1 state. **Note** This option is available only on some C-Series servers.

Name	Description
Processor C6 Report drop-down list **set ProcessorC6Report**	Whether the BIOS sends the C6 report to the operating system. When the OS receives the report, it can transition the processor into the lower C6 power state to decrease energy usage while maintaining optimal processor performance. This can be one of the following: • **Disabled**—The BIOS does not send the C6 report. • **Enabled**—The BIOS sends the C6 report, allowing the OS to transition the processor to the C6 low power state. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter. **Note** This option is available only on some C-Series servers.
Execute Disable Bit drop-down list **set ExecuteDisable**	Classifies memory areas on the server to specify where application code can execute. As a result of this classification, the processor disables code execution if a malicious worm attempts to insert code in the buffer. This setting helps to prevent damage, worm propagation, and certain classes of malicious buffer overflow attacks. This can be one of the following: • **Disabled**—The processor does not classify memory areas. • **Enabled**—The processor classifies memory areas. **Note** Contact your operating system vendor to make sure the operating system supports this feature.

Name	Description
Turbo Mode drop-down list **set IntelTurboBoostTech**	Whether the processor uses Intel Turbo Boost Technology, which allows the processor to automatically increase its frequency if it is running below power, temperature, or voltage specifications. This can be one of the following: • **Disabled**—The processor does not increase its frequency automatically. • **Enabled**—The processor utilizes Turbo Boost Technology if required. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
EIST PSD Function drop-down list	EIST reduces the latency inherent with changing the voltage-frequency pair (P-state), thus allowing those transitions to occur more frequently. This allows for more granular, demand-based switching and can optimize the power-to-performance balance, based on the demands of the applications. This can be one of the following: • HW ALL: The processor is coordinates the P-state among logical processors dependencies. The OS keeps the P-state request up to date on all logical processors. • SW ALL: The OS Power Manager coordinates the P-state among logical processors with dependencies and initiates the transition on all of those Logical Processors.

Name	Description
SpeedStep (Pstates) drop-down list **set EnhancedIntelSpeedStep**	Whether the processor uses Enhanced Intel SpeedStep Technology, which allows the system to dynamically adjust processor voltage and core frequency. This technology can result in decreased average power consumption and decreased average heat production. This can be one of the following: • **Disabled**—The processor never dynamically adjusts its voltage or frequency. • **Enabled**—The processor utilizes Enhanced Intel SpeedStep Technology and enables all supported processor sleep states to further conserve power. We recommend that you contact your operating system vendor to make sure the operating system supports this feature. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
HyperThreading [ALL] drop-down list **set IntelHyperThread**	Whether the processor uses Intel Hyper-Threading Technology, which allows multithreaded software applications to execute threads in parallel within each processor. This can be one of the following: • **Disabled**—The processor does not permit hyperthreading. • **Enabled**—The processor allows for the parallel execution of multiple threads.
Cores Enabled drop-down list **set CoreMultiProcessing**	Allows you to disable one or more of the physical cores on the server. This can be one of the following: • **All**—Enables all physical cores. This also enables Hyper Threading on the associated logical processor cores. • **1 through 27**—Specifies the number of physical processor cores that can run on the server. Each physical core has an associated logical core. **Note** Contact your operating system vendor to make sure the operating system supports this feature.

Name	Description
Processor CMCI drop-down list **set ProcessorCMCI**	Allows the CPU to trigger interrupts on corrected machine check events. The corrected machine check interrupt (CMCI) allows faster reaction than the traditional polling timer. This can be one of the following: • **Disabled**—Disables CMCI. • **Enabled**—Enables CMCI. This is the default value.
Enhanced Intel SpeedStep Tech drop-down list **set EnhancedIntelSpeedStep**	Whether the processor uses Enhanced Intel SpeedStep Technology, which allows the system to dynamically adjust processor voltage and core frequency. This technology can result in decreased average power consumption and decreased average heat production. This can be one of the following: • **Disabled**—The processor never dynamically adjusts its voltage or frequency. • **Enabled**—The processor utilizes Enhanced Intel SpeedStep Technology and enables all supported processor sleep states to further conserve power. We recommend that you contact your operating system vendor to make sure the operating system supports this feature. **Note** **CPUPowerManagement** must be set to **Custom** or the server ignores the setting for this parameter.
Workload Configuration drop-down list **set WorkLdConfig**	This feature allows for workload optimization. The options are Balanced and I/O Sensitive: • **NUMA** • **UMA**
Sub NUMA Clustering drop-down list	Whether the CPU supports sub NUMA clustering, in which the tag directory and the memory channel are always in the same region. This can be one of the following: • **disabled**— Sub NUMA clustering does not occur. • **enabled**— Sub NUMA clustering occurs. • **auto** — The BIOS determines what Sub NUMA clustering is done.

Name	Description
Energy/Performance Bias Config	Displays the energy or performance bias configuration. This can be one of the following: • Balanced Performance • Performance • Balanced Power • Power
XPT Prefetch drop-down list	Whether XPT prefetch is used to enable a read request sent to the last level cache to issue a copy of that request to the memory controller prefetcher. This can be one of the following: • **disabled**—The CPU does not use the XPT Prefetch option. • **enabled**—The CPU enables the XPT prefetch option.
UPI Prefetch drop-down list	UPI prefetch is a mechanism to get the memory read started early on a DDR bus. This can be one of the following: • **disabled**—The processor does not preload any cache data. • **enabled**—The UPI prefetcher preloads the L1 cache with the data it determines to be the most relevant.

Name	Description
Energy Performance Bias Config drop-down list **set CpuEngPerfBias**	Allows you to determine whether system performance or energy efficiency is more important on this server. This can be one of the following: • — The server provides all server components with full power at all times. This option maintains the highest level of performance and requires the greatest amount of power. • — The server provides all server components with enough power to keep a balance between performance and power. • — The server provides all server components with enough power to keep a balance between performance and power. • — The server provides all server components with maximum power to keep reduce power consumption.
Power Performance Tuning drop-down list **set PwrPerfTuning**	Determines if the BIOS or Operating System can turn on the energy performance bias tuning. The options are BIOS and OS. • **bios**— Chooses BIOS for energy performance tuning. • **os**— Chooses OS for energy performance tuning.
LLC Prefetch drop-down list	Whether the processor uses the LLC Prefetch mechanism to fetch the date into the LLC. This can be one of the following: • **disabled**—The processor does not preload any cache data. • **enabled**—The LLC prefetcher preloads the L1 cache with the data it determines to be the most relevant.

Name	Description
Package C State **set package-c-state-limit-config package-c-state-limit**	The amount of power available to the server components when they are idle. This can be one of the following: • **no-limit**—The server may enter any available C state. • **auto** —The CPU determines the physical elevation. • —The server provides all server components with full power at all times. This option maintains the highest level of performance and requires the greatest amount of power. • —When the CPU is idle, the system reduces the power consumption further than with the C1 option. This requires less power than C1 or C0, but it takes the server slightly longer to return to high performance mode. • —When the CPU is idle, the system reduces the power consumption further than with the C3 option. This option saves more power than C0, C1, or C3, but there may be performance issues until the server returns to full power. • —When the CPU is idle, the system reduces the power consumption further than with the C3 option. This option saves more power than C0, C1, or C3, but there may be performance issues until the server returns to full power.
Hardware P-States drop-down list **set CpuHWPM**	Enables processor Hardware P-State. This can be one of the following: • **disabled**—HWPM is disabled. • **hwpm-native-mode**—HWPM native mode is enabled. • **hwpm-oob-mode**—HWPM Out-Of-Box mode is enabled. • **Native Mode with no Legacy** (only GUI)

Name	Description
Intel Speed Select drop-down list **set IntelSpeedSelect**	**Intel Speed Select** modes will allow users to run the CPU with different speed and cores. This can be one of the following: • **Base**— It will allow users to access maximum core and Thermal Design Power (TDP) ratio. • **Config 1**— It will allow users to access core and TDP ratio lesser than **Base**. • **Config 2**— It will allow users to access core and TDP ratio lesser than **Config 1**. Default value: **Base**.
Uncore Frequency Scaling drop-down list **set UFSDisable**	This feature allows you configure the scaling of uncore frequency of the processor. This can be one of the following: • **enabled**—Uncore frequency of the processor scales up or down based on the load. • **disabled**—Uncore frequency of the processor remains fixed. Refer Intel® Dear Customer Letter (DCL) to know the fixed higher and lower values for **Uncore Frequency Scaling**.
Configurable TDP Level drop-down list **set ConfigTDPLevel**	**Configurable TDP Level** feature allows adjustments in processor thermal design power values. By modifying the processor behavior and the performance levels, power consumption of a processor can be configured and TDP can be adjusted as the same time. Hence, a processor operates at higher or lower performance levels, depending on the available cooling capacities and desired power consumption. This can be one of the following: • **Normal** • **Level 1** • **Level 2** Refer Intel® Dear Customer Letter (DCL) to know the values for **TDP level**.

BIOS Parameters by Server Model

Name	Description
UPI Link Speed drop-down list **set QpiLinkSpeed**	**Note** **UPI Link Frequency Select** token is not applicable for single socket configuration. This feature allows you to configure the Intel Ultra Path Interconnect (UPI) link speed between multiple sockets. This can be one of the following: • **Auto**—This option configures the optimal link speed automatically. • **9.6 GT/s**—This option configures the optimal link speed at 9.6GT/s. • **10.4 GT/s**—This option configures the optimal link speed at 10.4GT/s
Energy Efficient Turbo drop-down list **set EnergyEfficientTurbo**	When energy efficient turbo is enabled, the optimal turbo frequency of the CPU turns dynamic based on CPU utilization. The power/performance bias setting also influences energy efficient turbo. This can be one of the following: • **Disabled**—Energy Efficient Turbo is disabled. • **Enabled**—Energy Efficient Turbo is enabled.
Processor EPP Enable	Displays the selected value for Processor EPP Enable. • **Disabled**—Processor EPP Enable is disabled. • **Enabled**—Processor EPP Enable is enabled.
Autonomous Core C-state drop-down list **set AutoCCState**	Enables CPU Autonomous C-State, which converts the HALT instructions to the MWAIT instructions. This can be one of the following: • **Disabled**—CPU Autonomous C-state is disabled. • **Enabled**—CPU Autonomous C-state is enabled.

Name	Description
Patrol Scrub drop-down list **set PatrolScrub**	Allows the system to actively search for, and correct, single bit memory errors even in unused portions of the memory on the server. This can be one of the following: • **Disabled**—The system checks for memory ECC errors only when the CPU reads or writes a memory address. • **Enabled**—The system periodically reads and writes memory searching for ECC errors. If any errors are found, the system attempts to fix them. This option may correct single bit errors before they become multi-bit errors, but it may adversely affect performance when the patrol scrub is running. • **Enable at End of POST**—The system checks for memory ECC errors after BIOS POST.
Processor EPP Profile drop-down list **set EPPProfile**	Allows you to determine whether system performance or energy efficiency is more important on this server. This can be one of the following: • Performance • Balanced Performance • Balanced Power • Power

Memory Tab

Note BIOS parameters listed in this tab may vary depending on the server.

Table 5: BIOS Parameters in Memory Tab

Name	Description
Reboot Host Immediately checkbox	Upon checking, reboots the host server immediately. You must check the checkbox after saving changes.

Name	Description
Select Memory RAS configuration drop-down list **set SelectMemoryRAS**	Determines how the memory reliability, availability, and serviceability (RAS) is configured for the server. This can be one of the following: • **Maximum Performance**—System performance is optimized. • **ADDDC Sparing**—Adaptive virtual lockstep is an algorithm implemented in the hardware and firmware to support the ADDDC mode. When selected, the system performance is optimized till the algorithm is activated. The algorithm is activated in case of DRAM device failure. Once the algorithm is activated, the virtual lockstep regions are activated to map out the failed region during run-time dynamically, and the performance impact is restricted at a region level. • **Mirror Mode 1LM**—System reliability is optimized by using half the system memory as backup. • **Partial Mirror Mode 1LM**—Partial DIMM Mirroring creates a mirrored copy of a specific region of memory cells, rather than keeping the complete mirror copy. Partial Mirroring creates a mirrored region in memory map with the attributes of a partial mirror copy. Up to 50% of the total memory capacity can be mirrored, using up to 4 partial mirrors.
Above 4G Decoding drop-down list **set MemoryMappedIOAbove4GB**	Enables or disables MMIO above 4GB or not. This can be one of the following: • **Disabled**—The server does not map I/O of 64-bit PCI devices to 4GB or greater address space. • **Enabled**—The server maps I/O of 64-bit PCI devices to 4GB or greater address space. **Note** PCI devices that are 64-bit compliant but use a legacy option ROM may not function correctly with this setting enabled.
DCPMM Firmware Downgrade drop-down list **set DCPMMFirmwareDowngrade**	Whether the BIOS supports downgrading the DCPMM firmware. This can be one of the following: • **Disabled**—Support is disabled. • **Enabled**—Support is enabled.

Name	Description
Partial Memory Mirror Mode drop-down list **set PartialMirrorModeConfig**	The partial memory size is either in percentage or in GB. This can be one of the following: • **Percentage**—The partial memory mirror is defined in percentage. • **Value in GB**—The partial memory mirror is defined in GB. • **Disabled**—Partial memory mirror is disabled.
Partial Mirror percentage field **set PartialMirrorPercent**	Percentage of memory to mirror above 4GB. Enter an integer between 0 and 50.
Partial Mirror1 Size in GB field **set PartialMirrorValue1**	Size of the first partial memory mirror in GB. Enter an integer between 0 and 65535. **Note** The combined memory size of all the partial mirror should not exceed 50% of the physical memory size.
Partial Mirror2 Size in GB field **set PartialMirrorValue2**	Size of the second partial memory mirror in GB. Enter an integer between 0 and 65535. **Note** The combined memory size of all the partial mirror should not exceed 50% of the physical memory size.
Partial Mirror3 Size in GB field **set PartialMirrorValue3**	Size of the third partial memory mirror in GB. Enter an integer between 0 and 65535. **Note** The combined memory size of all the partial mirror should not exceed 50% of the physical memory size.
Partial Mirror4 Size in GB field **set PartialMirrorValue4**	Size of the fourth partial memory mirror in GB. Enter an integer between 0 and 65535. **Note** The combined memory size of all the partial mirror should not exceed 50% of the physical memory size.
Memory Size Limit in GB field **set MemorySizeLimit**	Use this option to reduce the size of the physical memory limit in GB. Enter an integer between 0 and 65535.

Name	Description
NUMA drop-down list **set NUMAOptimize**	Whether the BIOS supports Non-Uniform Memory Access (NUMA). This can be one of the following: • **Disabled**—Support is disabled. • **Enabled**—Support is enabled.
BME DMA Mitigation drop-down list **set BmeDmaMitigation**	Allows you to disable the PCI BME bit to mitigate the threat from an unauthorized external DMA. This can be one of the following: • **Disabled**—PCI BME bit is disabled in the BIOS. • **Enabled**—PCI BME bit is enabled in the BIOS.
Select PPR Type drop-down list **set SelectPprType**	Cisco IMC supports **Hard-PPR**, which permanently remaps accesses from a designated faulty row to a designated spare row. This can be one of the following: • **Hard PPR**—Support is enabled. **Note** Hard PPR can be used only when **Memory RAS Configuration** is set to **ADDDC Sparing**. For other RAS selections, this setting should be set to **Disabled**. • **Disabled**—Support is disabled.
CR QoS drop-down list **CRQoS**	Enables you to select the CR QoS tuning. This can be one of the following: • **Recipe 1**—For QoS knobs and is recommended for 2-2-2 memory configuration in active directory. • **Recipe 2**—For QoS knobs and is recommended for other memory configuration in active directory. • **Recipe 3**—For QoS knobs and is recommended for 1 DIMM per channel configuration. • **Disabled**—**CR QoS** feature is disabled.

Name	Description
Snoopy mode for AD drop-down list **SnoopyModeForAD**	Enables new AD specific feature to avoid directory updates to DDRT memory from non-NUMA optimized workloads. This can be one of the following: • **Disabled**—Support is disabled. • **Enabled**—Support is enabled.
CR FastGo Config drop-down list **CrfastgoConfig**	Enables you to select CR QoS configuration profiles. This can be one of the following: • **Default** • **Option 1** • **Option 2** • **Option 3** • **Option 4** • **Option 5** • **Auto**
NVM Performance Setting drop-down list **NvmdimmPerformConfig**	Enables you to configure NVM baseline performance settings depending on the workload behavior. • **BW Optimized** • **Latency Optimized** • **Balanced Profile**
Snoopy mode for 2LM drop-down list **SnoopyModeFor2LM**	Enables you to avoid directory updates to far-memory from non-NUMA optimized workloads. This can be one of the following: • **Disabled**—Support is disabled. • **Enabled**—Support is enabled.

Name	Description
Memory Thermal Throttling Mode drop-down list **MemoryThermalThrottling**	This function is used for adjusting memory temperature. If memory temperature is excessively high after the function is enabled, the memory access rate is reduced and Baseboard Management Controller (BMC) adjusts the fan to cool down the memory to avoid any DIMM damage. This can be one of the following: • **Disabled**—Support is disabled. • **CLTT with PECI**—Enables Closed Loop Thermal Throttling with Platform Environment Control Interface.
Memory Refresh Rate drop-down list **MemoryRefreshRate**	Enables you to increase or decrease memory refresh rate. Increasing the DRAM refresh rate reduces the maximum number of activates (hammers) that can occur before the next refresh. This can be one of the following: • **1X Refresh**—Refresh rate is at minimum. • **2X Refresh** —Refresh is 2X faster.
Panic and High Watermark drop-down list **PanicHighWatermark**	When set to low, the memory controller does not postpone refreshes while **Memory Refresh Rate** is set to **1X Refresh**. This can be one of the following: • **Low**—Refresh rate is set to low. • **High** —Refresh rate is set to high.
Advanced Memory Test drop-down list **AdvancedMemTest**	**Note** This feature is applicable only to Samsung, Hynix and Micron DIMMs. You can enable advance DIMM testing during BIOS POST using this feature. This can be one of the following: • **Disabled**—Support is disabled. • **Enabled**—Support is enabled.
Enhanced Memory Test drop-down list	This can be one of the following: • **Auto**—Support is set to Auto. • **Disabled**—Support is disabled. • **Enabled**—Support is enabled.

Power/Performance Tab

Note BIOS parameters listed in this tab may vary depending on the server.

Table 6: BIOS Parameters in Power/Performance Tab

Name	Description
Reboot Host Immediately checkbox	Upon checking, reboots the host server immediately. You must check the checkbox after saving changes.
Hardware Prefetcher drop-down list **set HardwarePrefetch**	Whether the processor allows the Intel hardware prefetcher to fetch streams of data and instruction from memory into the unified second-level cache when necessary. This can be one of the following: • **Disabled**—The hardware prefetcher is not used. • **Enabled**—The processor uses the hardware prefetcher when cache issues are detected.
Adjacent Cache Line Prefetcher drop-down list **set AdjacentCacheLinePrefetch**	Whether the processor fetches cache lines in even or odd pairs instead of fetching just the required line. This can be one of the following: • **Disabled**—The processor only fetches the required line. • **Enabled**—The processor fetches both the required line and its paired line.
DCU Streamer Prefetch drop-down list **set DcuStreamerPrefetch**	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache. This can be one of the following: • **Disabled**—The processor does not try to anticipate cache read requirements and only fetches explicitly requested lines. • **Enabled**—The DCU prefetcher analyzes the cache read pattern and prefetches the next line in the cache if it determines that it may be needed.
DCU IP Prefetcher drop-down list **set DcuIpPrefetch**	Whether the processor uses the DCU IP Prefetch mechanism to analyze historical cache access patterns and preload the most relevant lines in the L1 cache. This can be one of the following: • **Disabled**—The processor does not preload any cache data. • **Enabled**—The DCU IP prefetcher preloads the L1 cache with the data it determines to be the most relevant.

Name	Description
CPU Performance drop-down list **set CPUPerformance**	Sets the CPU performance profile for the options listed above. This can be one of the following: • **Enterprise**—All options are enabled. • **HPC**—All options are enabled. This setting is also known as high performance computing. • **Hight Throughput**—Only the DCU IP Prefetcher is enabled. The rest of the options are disabled. • **Custom**—All performance profile options can be configured from the BIOS setup on the server. In addition, the Hardware Prefetcher and Adjacent Cache-Line Prefetch options can be configured as well.