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Open Source Used In Cisco Secure Endpoint Connector (Linux) 1.23.0

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1.3 libmnl 1.0.4

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References

* AOL

http://www.aleksey.com/pipermail/xmlsec/2003/005488.html http://www.aleksey.com/pipermail/xmlsec/attachments/20030729/0e25648e/attachment.htm

*

Cordys R&D BV http://www.aleksey.com/pipermail/xmlsec/2003/005581.html

* Cryptocom LTD http://www.aleksey.com/pipermail/xmlsec/2006/007410.html

1.5 jansson 2.11 1.5.1 Available under license :

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1.7 cre2 0.3.1

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Klib: a Generic Library in C

Overview

Klib is a standalone and lightweight C library distributed under [MIT/X11 license][1]. Most components are independent of external libraries, except the standard C library, and independent of each other. To use a component of this library, you only need to copy a couple of files to your source code tree without worrying about library dependencies.

Klib strives for efficiency and a small memory footprint. Some components, such as khash.h, kbtree.h, ksort.h and kvec.h, are among the most efficient implementations of similar algorithms or data structures in all programming languages, in terms of both speed and memory use.

A new documentation is available [here](http://attractivechaos.github.io/klib/) which includes most information in this README file.

Common components

* [khash.h][khash]: generic [hash table][2] with open addressing.

* [kbtree.h][kbtree]:

generic search tree based on [B-tree][3].

* [kavl.h][kavl]: generic intrusive [AVL tree][wiki-avl].

* [ksort.h][ksort]: generic sort, including [introsort][4], [merge sort][5], [heap sort][6], [comb sort][7], [Knuth shuffle][8] and the [k-small][9] algorithm.

* [kseq.h][kseq]: generic stream buffer and a [FASTA][10]/[FASTQ][11] format parser.

* kvec.h: generic dynamic array.

* klist.h: generic single-linked list and [memory pool][12].

* kstring.{h,c}: basic string library.

* kmath.{h,c}: numerical routines including [MT19937-64][13] [pseudorandom generator][14], basic [nonlinear programming][15] and a few special math functions.

* [ketopt.h][ketopt]: portable command-line argument parser with getopt_long-like API.

Components for more specific use cases

* ksa.c: constructing [suffix arrays][16] for strings with multiple sentinels, based on a revised [SAIS algorithm][17].

* knetfile.{h,c}: random access to remote files on HTTP or FTP.

* kopen.c: smart stream opening.

*

khmm.{h,c}: basic [HMM][18] library.

* ksw.(h,c}: Striped [Smith-Waterman algorithm][19].

* knhx.{h,c}: [Newick tree format][20] parser.

Methodology

For the implementation of generic [containers][21], klib extensively uses C macros. To use these data structures, we usually need to instantiate methods by expanding a long macro. This makes the source code look unusual or even ugly and adds difficulty to debugging. Unfortunately, for efficient generic programming in C that lacks [template][22], using macros is the only solution. Only with macros, we can write a generic container which, once instantiated, compete with a type-specific container in efficiency. Some generic libraries in C, such as [Glib][23], use the `void*` type to implement containers. These implementations are usually slower and use more memory than klib (see [this benchmark][31]).

To effectively use klib, it is important to understand how it achieves generic programming. We will use the hash table library as an example:

```
#include "khash.h"
KHASH_MAP_INIT_INT(m32, char)
                                           // instantiate structs and methods
int main() {
  int ret, is missing;
  khint tk;
  khash_t(m32) *h = kh_init(m32); // allocate a hash table
  k = kh_put(m32, h, 5, \&ret); // insert a key to the hash table
  if (!ret) kh del(m32, h, k);
  kh_value(h, k) = 10;
                            // set the value
  k = kh_get(m32, h, 10);
                               // query the hash table
  is_missing = (k == kh_end(h)); // test if the key is present
  k = kh_get(m32, h, 5);
  kh_del(m32, h, k);
                             // remove a key-value pair
  for (k = kh_begin(h); k != kh_end(h); ++k) // traverse
                           // test if a bucket contains data
     if (kh_exist(h, k))
 kh_value(h, k) = 1;
  kh_destroy(m32, h);
                               // deallocate the hash table
  return 0;
}
```

In this example, the second line instantiates a hash table with `unsigned` as

the key type and `char` as the value type. `m32` names such a type of hash table. All types and functions associated with this name are macros, which will be explained later. Macro `kh_init()` initiates a hash table and `kh_destroy()` frees it. `kh_put()` inserts a key and returns the iterator (or the position) in the hash table. `kh_get()` and `kh_del()` get a key and delete an element, respectively. Macro `kh_exist()` tests if an iterator (or a position) is filled with data.

An immediate question is this piece of code does not look like a valid C program (e.g. lacking semicolon, assignment to an _apparent_ function call and _apparent_ undefined `m32` 'variable'). To understand why the code is correct, let's go a bit further into the source code of `khash.h`, whose skeleton looks like:

```
#define KHASH_INIT(name, SCOPE, key_t, val_t, is_map, _hashf, _hasheq) \
  typedef struct \{ \setminus
   int n_buckets, size, n_occupied, upper_bound; \
   unsigned *flags; \setminus
  key_t *keys; \setminus
   val_t *vals; \setminus
  } kh ##name## t; \
  SCOPE inline kh_##name##_t *init_##name() { \
   return (kh_##name##_t*)calloc(1, sizeof(kh_##name##_t)); \
  } \
  SCOPE inline int get_##name(kh_##name##_t *h, key_t k) \
  ... \
  SCOPE inline void destroy ##name(kh ##name## t *h) { \
   if (h) { \
     free(h->keys); free(h->flags); free(h->vals); free(h); \
    } \
  }
 #define _int_hf(key) (unsigned)(key)
 #define _int_heq(a, b) (a == b)
 #define khash_t(name) kh_##name##_t
 #define kh_value(h, k) ((h)->vals[k])
 #define kh_begin(h, k) 0
 #define kh_end(h) ((h)->n_buckets)
 #define kh_init(name) init_##name()
 #define kh_get(name, h, k) get_##name(h, k)
 #define kh_destroy(name, h) destroy_##name(h)
 #define KHASH_MAP_INIT_INT(name, val_t) \
  KHASH_INIT(name, static, unsigned, val_t, is_map, _int_hf, _int_heq)
`KHASH_INIT()` is a huge macro defining all the structs and methods.
When this
macro is called, all the code inside it will be inserted by the [C
preprocess][37] to the place where it is called. If the macro is called
multiple times, multiple copies of the code will be inserted. To avoid naming
```

conflict of hash tables with different key-value types, the library uses [token

concatenation][36], which is a preprocessor feature whereby we can substitute part of a symbol based on the parameter of the macro. In the end, the C preprocessor will generate the following code and feed it to the compiler (macro `kh_exist(h,k)` is a little complex and not expanded for simplicity):

```
typedef struct {
  int n buckets, size, n occupied, upper bound;
  unsigned *flags;
  unsigned *keys;
  char *vals:
 } kh_m32_t;
 static inline kh_m32_t *init_m32() {
  return (kh_m32_t*)calloc(1, sizeof(kh_m32_t));
 }
 static inline int get_m32(kh_m32_t *h, unsigned k)
 static inline void destroy_m32(kh_m32_t *h) {
  if (h) {
 free(h->keys); free(h->flags); free(h->vals); free(h);
  }
 }
int main() {
int ret, is_missing;
khint tk;
kh_m32_t *h = init_m32();
k = put_m32(h, 5, &ret);
if (!ret) del_m32(h, k);
h - vals[k] = 10;
k = get_m 32(h, 10);
is_missing = (k == h->n_buckets);
k = get_m 32(h, 5);
del_m32(h, k);
for (k = 0; k != h > n_buckets; ++k)
 if (kh_exist(h, k)) h->vals[k] = 1;
destroy_m32(h);
return 0;
```

```
}
```

This is the C program we know.

From this example, we can see that macros and the C preprocessor plays a key role in klib. Klib is fast partly because the compiler knows the key-value type at the compile time and is able to optimize the code to the same level as type-specific code. A generic library written with `void*` will not get such performance boost.

Massively inserting code upon instantiation may remind us of C++'s slow compiling speed and huge binary size when STL/boost is in use. Klib is much better in this respect due to its small code size and component independency.

Inserting several hundreds lines of code won't make compiling obviously slower.

Resources

* Library documentation, if present, is available in the header files. Examples

can be found in the [test/][24] directory.

* **Obsolete** documentation of the hash table library can be found at

[SourceForge][25]. This README is partly adapted from the old documentation.

* [Blog post][26] describing the hash table library.

* [Blog post][27] on why using `void*` for generic programming may be inefficient.

* [Blog post][28] on the generic stream buffer.

* [Blog post][29] evaluating the performance of `kvec.h`.

* [Blog post][30] arguing B-tree may be a better data structure than a binary search tree.

* [Blog post][31] evaluating the performance of `khash.h` and `kbtree.h` among many other implementations. [An older version][33] of the benchmark is also available.

* [Blog post][34] benchmarking internal sorting algorithms and implementations.

* [Blog post][32]

on the k-small algorithm.

* [Blog post][35] on the Hooke-Jeeve's algorithm for nonlinear programming.

[1]: http://en.wikipedia.org/wiki/MIT_License

[2]: https://en.wikipedia.org/wiki/Hash_table

[3]: http://en.wikipedia.org/wiki/B-tree

[4]: http://en.wikipedia.org/wiki/Introsort

[5]: http://en.wikipedia.org/wiki/Merge_sort

[6]: http://en.wikipedia.org/wiki/Heapsort

[7]: http://en.wikipedia.org/wiki/Comb_sort

[8]: http://en.wikipedia.org/wiki/Fisher-Yates_shuffle

[9]: http://en.wikipedia.org/wiki/Selection_algorithm

[10]: http://en.wikipedia.org/wiki/FASTA_format

[11]: http://en.wikipedia.org/wiki/FASTQ_format

[12]: http://en.wikipedia.org/wiki/Memory_pool

[13]: http://en.wikipedia.org/wiki/Mersenne_twister

[14]: http://en.wikipedia.org/wiki/Pseudorandom_generator

[15]: http://en.wikipedia.org/wiki/Nonlinear_programming

[16]: http://en.wikipedia.org/wiki/Suffix_array

[17]: https://sites.google.com/site/yuta256/sais

[18]: http://en.wikipedia.org/wiki/Hidden_Markov_model

[19]: http://en.wikipedia.org/wiki/Smith-Waterman_algorithm

[20]:

http://en.wikipedia.org/wiki/Newick_format

[21]: http://en.wikipedia.org/wiki/Container_(abstract_data_type)

[22]: http://en.wikipedia.org/wiki/Template_(C%2B%2B)

[23]: http://en.wikipedia.org/wiki/GLib

[24]: https://github.com/attractivechaos/klib/tree/master/test

[25]: http://klib.sourceforge.net/

[26]: http://attractivechaos.wordpress.com/2008/09/02/implementing-generic-hash-library-in-c/

[27]: http://attractivechaos.wordpress.com/2008/10/02/using-void-in-generic-c-programming-may-be-inefficient/

[28]: http://attractivechaos.wordpress.com/2008/10/11/a-generic-buffered-stream-wrapper/

[29]: http://attractivechaos.wordpress.com/2008/09/19/c-array-vs-c-vector/

[30]: http://attractivechaos.wordpress.com/2008/09/24/b-tree-vs-binary-search-tree/

[31]: http://attractivechaos.wordpress.com/2008/10/07/another-look-at-my-old-benchmark/

[32]: http://attractivechaos.wordpress.com/2008/09/13/calculating-median/

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[36]: http://en.wikipedia.org/wiki/C_preprocessor#Token_concatenation

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[kbtree]:

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[khash]:

http://attractivechaos.github.io/klib/#Khash%3A%20generic%20hash%20table:%5B%5BKhash%3A%20generic%20hash%20table%5D%5D

[kseq]:

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[ksort]: http://attractivechaos.github.io/klib/#Ksort%3A%20sorting%2C%20shuffling%2C%20heap%20and%20k-small:%5B%5BKsort%3A%20sorting%2C%20shuffling%2C%20heap%20and%20k-small%5D%5D [kavl]:

http://attractivechaos.github.io/klib/#KAVL%3A%20generic%20intrusive%20AVL%20tree [ketopt]: http://attractivechaos.github.io/klib/#Ketopt%3A%20parsing%20command-line%20arguments

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tomb - support for clean goroutine termination in Go.

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1.13 llhttp 6.0.6 + P

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1.16 sqlite 3.39.3

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1.17 boost 1.81.0

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1.19 capnproto 0.10.4

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1.20 clamav 0.105.1 + P + 35922ef

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Julian Seward, Cambridge, UK. jseward@bzip.org bzip2/libbzip2 version 1.0.4 of 20 December 2006

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1.22 Ilvm 16.0.4 + P

1.22.1 Available under license :

; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py ; RUN: llc < %s -mtriple=aarch64-- | FileCheck %s

; A shuffle mask with all undef elements is always legal.

define <4 x i32> @PR41535(<2 x i32> %p1, <2 x i32> %p2) { ; CHECK-LABEL: PR41535: ; CHECK: // %bb.0: ; CHECK-NEXT: ext v0.8b, v0.8b, v1.8b, #4 ; CHECK-NEXT: mov v0.d[1], v0.d[0] ; CHECK-NEXT: ret %cat1 = shufflevector <2 x i32> %p1, <2 x i32> undef, <4 x i32> <i32 undef, i32 1, i32 undef, i32 undef, %cat2 = shufflevector <2 x i32> %p2, <2 x i32> undef, <4 x i32> <i32 0, i32 undef, i32 undef, i32 undef> %r = shufflevector <4 x i32> %cat1, <4 x i32> %cat2, <4 x i32> <i32 undef, i32 undef, i32 1, i32 4> ret <4 x i32> %r }

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit,avx512vbmi | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI

; Make sure CPUs default to prefer-256-bit. avx512vnni isn't interesting as it just adds an isel peephole for vpmaddwd+vpaddd

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cascadelake | FileCheck %s -- check-prefixes=CHECK,CHECK-AVX512

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cooperlake | FileCheck %s -- check-prefixes=CHECK,CHECK-AVX512

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=cannonlake | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI

;

RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=icelake-client | FileCheck %s -- check-prefixes=CHECK,CHECK-VBMI

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=icelake-server | FileCheck %s -- check-prefixes=CHECK,CHECK-VBMI

; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=tigerlake | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI

; This file primarily contains tests for specific places in X86ISelLowering.cpp that needed be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

define dso_local void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-

```
width"="256" {
; CHECK-LABEL: add256:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpaddd 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT: vpaddd (%rsi), %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:
vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%d = load < 16 x i 32 >, < 16 x i 32 >* %a
%e = load <16 x i32>, <16 x i32>* %b
\% f = add < 16 x i 32 > \% d, \% e
store <16 x i32> %f. <16 x i32>* %c
ret void
}
```

define dso_local void @add512(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vectorwidth"="512" { ; CHECK-LABEL: add512:

```
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT: vpaddd (%rsi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%d = load <16 x i32>, <16 x i32>* %a
%e = load <16 x i32>, <16 x i32>* %b
%f = add <16 x i32> %d, %e
store <16 x i32> %f, <16 x i32>* %c
ret void
```

}

define dso_local void @avg_v64i8_256(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="256" {

; CHECK-LABEL: avg_v64i8_256:

```
; CHECK: # %bb.0:
```

- ; CHECK-NEXT: vmovdqa (%rsi), %ymm0
- ; CHECK-NEXT: vmovdqa 32(%rsi), %ymm1
- ; CHECK-NEXT: vpavgb (%rdi), %ymm0,

%ymm0

; CHECK-NEXT: vpavgb 32(%rdi), %ymm1, %ymm1

- ; CHECK-NEXT: vmovdqu %ymm1, (%rax)
- ; CHECK-NEXT: vmovdqu %ymm0, (%rax)
- ; CHECK-NEXT: vzeroupper
- ; CHECK-NEXT: retq
- %1 = load <64 x i8>, <64 x i8>* %a

%2 = load <64 x i8>, <64 x i8>* %b

%3 = zext < 64 x i8 > %1 to < 64 x i32 >

%4 = zext < 64 x i8 > %2 to < 64 x i32 >

%5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32

%6 = add nuw nsw <64 x i32> %5, %4

%7 = lshr <64 x i32> %6, <i32 1, i32 1, i32

i 32 1, i 32 1

```
%8 = trunc <64 x i32> %7 to <64 x i8>
```

store <64 x i8> %8, <64 x i8>* undef, align 4

```
ret void
```

}

 $define \ dso_local \ void \ @avg_v64i8_512(<\!64 \ x \ i8>^* \ \%a, <\!64 \ x \ i8>^* \ \%b) \ "min-legal-vector-width"="512" \ \{a, a, b, a,$

; CHECK-LABEL: avg_v64i8_512:

; CHECK: # %bb.0:

```
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
```

- ; CHECK-NEXT: vpavgb (%rsi), %zmm0, %zmm0
- ; CHECK-NEXT: vmovdqu64 %zmm0, (%rax)
- ; CHECK-NEXT: vzeroupper
- ; CHECK-NEXT: retq

%1 = load <64 x i8>, <64 x i8>* %a

%2 = load <64 x i8>, <64 x i8>* %b

%3 = zext < 64 x i8 > %1 to < 64 x i32 >

%4 = zext < 64 x i8 > %2 to < 64 x i32 >

%5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32

1, i32 1,

```
%6 = add nuw nsw <64 x i32> %5, %4
```

%7 = lshr <64 x i32> %6, <i32 1, i32 1, i32

```
%8 = trunc <64 x i32> %7 to <64 x i8>
```

store <64 x i8> %8, <64 x i8>* undef, align 4

```
ret void
```

}

define dso_local void @pmaddwd_32_256(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="256" {

```
; CHECK-LABEL: pmaddwd_32_256:
; CHECK:
              # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmaddwd 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT: vpmaddwd (%rsi), %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
 %A = load <32 \text{ x i}16>, <32 \text{ x i}16>* %APtr
 B = load <32 \text{ x i} 16>, <32 \text{ x i} 16>* BPtr
 \%a = \text{sext} < 32 \text{ x i} 16 > \%A \text{ to } < 32 \text{ x i} 32 > 32 > 32 
 \%b = sext <32 x i16> %B to <32 x i32>
 \%m = mul nsw <32 x i32> %a, %b
 %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32
12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
 % even = shufflevector \langle 32 \times i 32 \rangle % m, \langle 32 \times i 32 \rangle undef, \langle 16 \times i 32 \rangle \langle i 32 1, i 32 3, i 32 5, i 32 7, i 32 9, i 32 \rangle
i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
 %ret = add <16 x i32> %odd, %even
 store <16 x i32> %ret, <16 x i32>* %CPtr
 ret void
}
define dso_local void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-
legal-vector-width"="512" {
; CHECK-LABEL: pmaddwd 32 512:
; CHECK:
              # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT: vpmaddwd (%rsi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
 %A = load <32 \text{ x i}16>, <32 \text{ x i}16>* %APtr
 B = load < 32 \text{ x i} 16 >, < 32 \text{ x i} 16 >* BPtr
 \%a = \text{sext} < 32 \text{ x i16} > \%A \text{ to } < 32 \text{ x i32} >
 \%b = sext <32 x i16> %B to <32 x i32>
 %m = mul nsw <32 x i32> %a, %b
 %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32
```

12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>

% even = shufflevector $\langle 32 x i 32 \rangle$ % m, $\langle 32 x i 32 \rangle$ undef, $\langle 16 \rangle$

x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>

```
%ret = add <16 x i32> % odd, % even
```

```
store <16 x i32> %ret, <16 x i32>* %CPtr
```

```
ret void
```

```
}
```

define dso_local void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="256" {

; CHECK-LABEL: psubus_64i8_max_256:

```
; CHECK: # %bb.0:
```

- ; CHECK-NEXT: vmovdqa (%rdi), %ymm0
- ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1

; CHECK-NEXT: vpsubusb 32(%rsi), %ymm1, %ymm1

; CHECK-NEXT: vpsubusb (%rsi), %ymm0, %ymm0

; CHECK-NEXT: vmovdqa %ymm0, (%rdx)

; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)

; CHECK-NEXT: vzeroupper

```
; CHECK-NEXT: retq
```

x = 10ad < 64 x i 8, < 64 x i 8, < 84 x i 8

%y = load < 64 x i 8 >, < 64 x i 8 >* %yptr

```
\% cmp = icmp ult <64 x i8> \% x, \% y
```

 $\%\,max$ = select <64 x i1> % cmp, <64 x i8> % y, <64 x i8> % x

%res = sub <64 x i8> % max, % y

store <64 x i8> %res, <64 x i8>* %zptr

```
ret void
```

```
}
```

```
define dso_local
```

void @psubus_64i8_max_512(<64 x i8>* % xptr, <64 x i8>* % yptr, <64 x i8>* % zptr) "min-legal-vector-width"="512" {

```
; CHECK-LABEL: psubus_64i8_max_512:
```

```
; CHECK: # %bb.0:
```

```
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
```

```
; CHECK-NEXT: vpsubusb (%rsi), %zmm0, %zmm0
```

```
; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
```

```
; CHECK-NEXT: vzeroupper
```

```
; CHECK-NEXT: retq
```

```
%x = load <64 x i8>, <64 x i8>* %xptr
```

```
%y = load <64 x i8>, <64 x i8>* %yptr
```

```
\% cmp = icmp ult <64 x i8> % x, % y
```

```
\text{\%}max = \text{select} < 64 \text{ x i1} > \text{\%} \text{cmp}, < 64 \text{ x i8} > \text{\%} \text{y}, < 64 \text{ x i8} > \text{\%} \text{x}
```

```
%res = sub <64 x i8> % max, % y
```

```
store <64 x i8> %res, <64 x i8>* %zptr
```

```
ret void
```

```
}
```

define dso_local i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {

```
; CHECK-LABEL: _Z9test_charPcS_i_256:
```

```
; CHECK: # %bb.0: # %entry
```

```
; CHECK-NEXT: movl %edx, %eax
```

```
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
```

```
; CHECK-NEXT: xorl %ecx, %ecx
```

; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1

; CHECK-NEXT: vpxor % xmm2, %xmm2, %xmm2 ; CHECK-NEXT: .p2align 4, 0x90 ; CHECK-NEXT: .LBB8_1: # % vector.body ; CHECK-NEXT: # =>This Inner Loop Header: Depth=1 ; CHECK-NEXT: vpmovsxbw 16(%rdi,%rcx), %ymm3 ; CHECK-NEXT: vpmovsxbw (%rdi,%rcx), %ymm4 ; CHECK-NEXT: vpmovsxbw 16(%rsi,%rcx), %ymm5 ; CHECK-NEXT: vpmaddwd %ymm3, %ymm5, %ymm3 ; CHECK-NEXT: vpaddd %ymm2, %ymm3, %ymm2 ; CHECK-NEXT: vpmovsxbw (%rsi,%rcx), %ymm3 ; CHECK-NEXT: vpmaddwd %ymm4, %ymm3, %ymm3 ; CHECK-NEXT: vpaddd %ymm1, %ymm3, %ymm1 ; CHECK-NEXT: addq \$32, %rcx ; CHECK-NEXT: cmpq %rcx, %rax ; CHECK-NEXT: jne .LBB8_1 ; CHECK-NEXT: # %bb.2: # %middle.block ; CHECK-NEXT: vpaddd %ymm0, %ymm1, %ymm1 ; CHECK-NEXT: vpaddd %ymm0, %ymm2, %ymm0 ; CHECK-NEXT: vpaddd %ymm0, %ymm1, %ymm0 ; CHECK-NEXT: vextracti128 \$1, %ymm0, %xmm1 ; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0 ; CHECK-NEXT: vpshufd $\{\{.*\#+\}\}$ xmm1 = xmm0[2,3,2,3] ; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0 ; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[1,1,1,1]; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0 ; CHECK-NEXT: vmovd %xmm0, %eax ; CHECK-NEXT: vzeroupper ; CHECK-NEXT: retq entry: %3 = zext i 32 %2 to i 64br label % vector.body vector.body: %index = phi i64 [%index.next, %vector.body], [0, %entry]

```
%index = phi 164 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
```

%12 = icmp eq i64 % index.next, %3 br i1 %12, label % middle.block, label % vector.body

middle.block:

%rdx.shuf1 = shufflevector <32 x i32> %11,

<32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20, i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 und

%bin.rdx1 = add <32 x i32> %11, %rdx.shuf1

%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i33 undef

%bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf

rdx.shuf15 = shufflevector <32 x i32> % bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,

i32 undef, i33 undef,

%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15

%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i33 undef,

%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17

%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i33 un

undef, i32 undef, i32

```
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
```

%13 = extractelement <32 x i32> %bin.rdx20, i32 0

ret i32 %13

```
}
```

define dso_local i32 @_Z9test_charPcS_i_512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="512" {

```
; CHECK-LABEL: _Z9test_charPcS_i_512:
```

```
; CHECK: # %bb.0: # %entry
```

```
; CHECK-NEXT: movl %edx, %eax
```

- ; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
- ; CHECK-NEXT: xorl %ecx, %ecx
- ; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
- ; CHECK-NEXT: .p2align 4, 0x90
- ; CHECK-NEXT: .LBB9_1: # %vector.body
- ; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
- ; CHECK-NEXT: vpmovsxbw (%rdi,%rcx), %zmm2
- ; CHECK-NEXT: vpmovsxbw (%rsi,%rcx), %zmm3
- ; CHECK-NEXT: vpmaddwd %zmm2, %zmm3, %zmm2

;

,	
CHECK-NEXT: addq \$32, %rcx	
; CHECK-NEXT: cmpq %rcx, %rax	
; CHECK-NEXT: jne .LBB9_1	
; CHECK-NEXT: # %bb.2: # %middle.block	
; CHECK-NEXT: vpaddd %zmm0, %zmm1, %zmm0	
; CHECK-NEXT: vextracti64x4 \$1, %zmm0, %ymm1	
; CHECK-NEXT: vpaddd %zmm1, %zmm0, %zmm0	
; CHECK-NEXT: vextracti128 \$1, % ymm0, % xmm1	
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0	
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[2,3,2,3]	
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0	
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[1,1,1,1]	
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0	
; CHECK-NEXT: vmovd %xmm0, %eax	
; CHECK-NEXT: vzeroupper	
; CHECK-NEXT: retq	
entry:	
%3 = zext i 32 %2 to i 64	
br label %vector.body	
vector.body:	
%index = phi i64 [%index.next, %vector.body], [0, %entry]	
%vec.phi = phi <32 x i32> [%11, %vector.body], [zeroinitializer, %entry]	
%4 = getelementptr inbounds i8, i8* $%0$, i64 $%$ index	
%5 = bitcast i8* %4 to <32 x i8>*	
% wide.load = load <32 x i8>, <32 x i8>* %5, align	
1	
%6 = sext < 32 x i8 > % wide.load to < 32 x i32 >	
%7 = getelementptr inbounds i8, i8* %1, i64 % index	
%8 = bitcast i8* %7 to <32 x i8>*	
% wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1	
%9 = sext < 32 x i8 > % wide.load14 to < 32 x i32 > 32	
%10 = mul nsw <32 x i 32 > %9, %6	
%11 = add nsw <32 x i32> %10, % vec.phi	
%index.next = add i64 %index, 32	
%12 = icmp eq i64 %index.next, %3	
br i1 %12, label %middle.block, label %vector.body	
middle.block:	
%rdx.shuf1 = shufflevector <32 x i32> $%11$, <32 x i32> undef, <32 x i32> <i32 16,="" 17,="" 18,="" 19,="" 20,<="" i32="" th=""><th></th></i32>	
i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i	
i32 undef, i32	

undef, i32 undef, i32 undef>

```
%bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
```

%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12,

i32 13, i32 14, i32 15, i32 undef, i33 undef, i33 undef, i34 undef, i35 undef

%bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf

%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i33 undef

```
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
```

%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i

```
i32 undef, i32 undef,
```

```
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i33 undef,
```

```
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
```

```
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
```

```
ret i32 %13
```

```
}
```

```
@a = dso_local global [1024 x i8] zeroinitializer, align 16
```

```
@b = dso_local global [1024 x i8] zeroinitializer, align 16
```

```
define dso_local i32 @sad_16i8_256()
```

```
"min-legal-vector-width"="256" {
; CHECK-LABEL: sad_16i8_256:
; CHECK:
           # %bb.0: # %entry
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: movq $-1024, %rax # imm = 0xFC00
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB10_1: # % vector.body
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-NEXT: vmovdqu a+1024(%rax), %xmm2
; CHECK-NEXT: vpsadbw b+1024(%rax), %xmm2, %xmm2
; CHECK-NEXT: vpaddd %ymm1, %ymm2, %ymm1
; CHECK-NEXT: addq $4, %rax
; CHECK-NEXT: jne .LBB10_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT: vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpshufd \{\{.*\#+\}\} xmm1 = xmm0[2,3,2,3]
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[1,1,1,1]
```

```
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vmovd %xmm0, %eax
; CHECK-NEXT: vzeroupper
; CHECK-NEXT:
          reta
entry:
  br label % vector.body
vector.body:
   %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
   %vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
   \%0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 % index
   \%1 = bitcast i8* \%0 to <16 x i8>*
   % wide.load = load <16 x i8>, <16 x i8>* %1, align 4
   \%2 = \text{zext} < 16 \text{ x i8} > \% \text{ wide.load to} < 16 \text{ x i32} >
   %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 % index
   \%4 = bitcast i8* \%3 to <16 x i8>*
   %wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
   \%5 = zext < 16 x i8 > \% wide.load1 to < 16 x i32 > 
   \%6 = \text{sub nsw} < 16 \text{ x i} 32 > \%2, \%5
   %7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, 
 1, i32 -1, i32 -1, i32 -1, i32 -1>
   \%8 = \text{sub nsw} < 16 \text{ x i} 32 > \text{zeroinitializer}, \%6
   \%9 = \text{select} < 16 \text{ x i} = 12 \%7, < 16 \text{ x i} = 32 \%6, < 16 \text{ x i} = 32 \%8
   \%10 = add nsw < 16 x i 32 > \%9, \% vec.phi
   \%index.next = add i64 %index.
   4
   %11 = icmp eq i64 % index.next, 1024
   br i1 %11, label %middle.block, label %vector.body
 middle.block:
   %rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32
 13, i32 14, i32 15, i32 undef, i32 undef
   \% bin.rdx = add <16 x i32> \% 10, \% rdx.shuf
   %rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32
 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 
i32 undef>
   \%bin.rdx2 = add <16 x i32> \%bin.rdx, \%rdx.shuf2
   %rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32
 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
 i32 undef, i32 undef>
   \%bin.rdx3 = add <16 x i32> \%bin.rdx2, \%rdx.shuf3
```

%rdx.shuf4 = shufflevector

<16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32

```
\%12 = extractelement < 16 x i 32 > \% bin.rdx4, i 32 0
```

ret i32 %12

```
}
```

define dso_local i32 @sad_16i8_512() "min-legal-vector-width"="512" { ; CHECK-LABEL: sad_16i8_512: ; CHECK: # %bb.0: # %entry ; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0 ; CHECK-NEXT: movq \$-1024, %rax # imm = 0xFC00 ; CHECK-NEXT: .p2align 4, 0x90 ; CHECK-NEXT: .LBB11_1: # % vector.body ; CHECK-NEXT: # =>This Inner Loop Header: Depth=1 ; CHECK-NEXT: vmovdqu a+1024(%rax), %xmm1 ; CHECK-NEXT: vpsadbw b+1024(%rax), %xmm1, %xmm1 ; CHECK-NEXT: vpaddd %zmm0, %zmm1, %zmm0 ; CHECK-NEXT: addq \$4, %rax ; CHECK-NEXT: jne .LBB11_1 ; CHECK-NEXT: # %bb.2: # %middle.block ; CHECK-NEXT: vextracti64x4 \$1, %zmm0, %ymm1 ; CHECK-NEXT: vpaddd %zmm1, %zmm0, %zmm0 ; CHECK-NEXT: vextracti128 \$1, % ymm0, % xmm1 ; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0 ; CHECK-NEXT: vpshufd $\{\{.*\#+\}\}$ xmm1 = xmm0[2,3,2,3] ; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0 ; CHECK-NEXT: vpshufd $\{\{.*\#+\}\}$ xmm1 = xmm0[1,1,1,1] ; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0 ; CHECK-NEXT: vmovd %xmm0, %eax ; CHECK-NEXT: vzeroupper ; CHECK-NEXT: retq entry: br label % vector.body vector.body: %index = phi i64 [0, %entry], [%index.next, %vector.body] %vec.phi = phi <16 x i32> [zeroinitializer, %entry], [%10, %vector.body] %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 % index%1 = bitcast i8* %0 to <16 x i8>*% wide.load = load <16 x i8>, <16 x i8>* %1, align 4 %2 = zext < 16 x i8 > % wide.load to < 16 x i32 >%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 % index %4 = bitcast i8* %3 to <16 x i8>*%wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4 %5 = zext < 16 x i8 > % wide.load1to <16 x i32> %6 = sub nsw <16 x i32> %2, %5 %7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, 1, i32 -1, i32 -1, i32 -1, i32 -1> %8 = sub nsw < 16 x i 32 > zeroinitializer, %6

%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8

```
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body
```

```
middle.block:
```

```
%rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32
  13, i32 14, i32 15, i32 undef, i32 undef
    %bin.rdx = add <16 x i32> %10, %rdx.shuf
    \frac{132}{3} % bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32
  undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 
 i32 undef>
       \%bin.rdx2 = add <16 x i32> \%bin.rdx. \%rdx.shuf2
    %rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32
  undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 
 i32 undef, i32 undef>
    \%bin.rdx3 = add <16 x i32> \%bin.rdx2, \%rdx.shuf3
    %rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32
  undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 
 i32 undef, i32 undef>
    %bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
    \%12 = extractelement <16 x i32> \% bin.rdx4, i32 0
   ret i32 %12
  }
 define dso_local void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
 ; CHECK-LABEL: sbto16f32 256:
; CHECK:
                                                                                      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
```

```
; CHECK-NEXT: vpmovm2d %k1, %ymm0
```

```
;
```

```
CHECK-NEXT: vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm1
```

```
; CHECK-NEXT: vcvtdq2ps %ymm1, %ymm1
```

```
; CHECK-NEXT: vmovaps %ymm1, (%rdi)
```

```
; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)
```

```
; CHECK-NEXT: vzeroupper
```

```
; CHECK-NEXT: retq
```

```
\text{\%mask} = \text{icmp slt} < 16 \text{ x i} 16 > \% \text{a}, zeroinitializer
```

```
\%1 = \text{sitofp} < 16 \text{ x il} > \% \text{ mask to} < 16 \text{ x float} >
```

```
store <16 x float> %1, <16 x float>* %res
```

```
ret void
```

```
}
```

```
define dso_local void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK: # %bb.0:
```

; CHECK-NEXT: vpmovw2m %ymm0, %k0 ; CHECK-NEXT: vpmovm2d %k0, %zmm0 ; CHECK-NEXT: vcvtdq2ps %zmm0, %zmm0 ; CHECK-NEXT: vmovaps %zmm0, (%rdi) ; CHECK-NEXT: vzeroupper ; CHECK-NEXT: retq %mask = icmp slt <16 x i16> %a, zeroinitializer %1 = sitofp <16 x i1> %mask to <16 x float> store <16 x float> %1, <16 x float>* %res ret void }

define dso_local void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {

; CHECK-LABEL: sbto16f64_256: ; CHECK: # %bb.0: ; CHECK-NEXT: vpmovw2m %ymm0, %k0 ; CHECK-NEXT: kshiftrw \$8, %k0, %k1 ; CHECK-NEXT: vpmovm2d %k1, %ymm0 ; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm1 ; CHECK-NEXT: vextracti128 \$1, %ymm0, %xmm0 ; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm0 ; CHECK-NEXT: vpmovm2d %k0, %ymm2 ; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm3 ; CHECK-NEXT: vextracti128 \$1, % ymm2, % xmm2 ; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm2 ; CHECK-NEXT: vmovaps %ymm2, 32(%rdi) ; CHECK-NEXT: vmovaps %ymm3, (%rdi) ; CHECK-NEXT: vmovaps %ymm0, 96(%rdi) ; CHECK-NEXT: vmovaps %ymm1, 64(%rdi) ; CHECK-NEXT: vzeroupper ; CHECK-NEXT: retq %mask = icmp slt <16 x i16> %a, zeroinitializer %1 = sitofp < 16 x il > % mask to < 16 x double >store <16 x double > %1, <16 x double > % res ret void }

define dso_local void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" { ; CHECK-LABEL: sbto16f64_512:

; CHECK: # %bb.0: ; CHECK-NEXT: vpmovw2m %ymm0, %k0 ; CHECK-NEXT: vpmovm2d %k0, %zmm0 ; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm1 ; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm0 ; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm0 ; CHECK-NEXT: vmovaps %zmm0, 64(%rdi)

```
; CHECK-NEXT: vmovaps %zmm1, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
```

}

define dso_local void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {

; CHECK-LABEL: ubto16f32_256:

- ; CHECK: # %bb.0:
- ; CHECK-NEXT: vpmovw2m %ymm0, %k0
- ; CHECK-NEXT: kshiftrw \$8, %k0, %k1
- ; CHECK-NEXT: vpmovm2d %k1, %ymm0
- ; CHECK-NEXT: vpsrld \$31, %ymm0, %ymm0
- ; CHECK-NEXT: vcvtdq2ps %ymm0, %ymm0

; CHECK-NEXT: vpmovm2d %k0, %ymm1

- ; CHECK-NEXT: vpsrld \$31, %ymm1, %ymm1
- ; CHECK-NEXT: vcvtdq2ps %ymm1, %ymm1
- ; CHECK-NEXT: vmovaps %ymm1,

```
(%rdi)
```

; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)

; CHECK-NEXT: vzeroupper

; CHECK-NEXT: retq

%mask = icmp slt <16 x i16> %a, zeroinitializer

%1 = uitofp <16 x i1> % mask to <16 x float>

```
store <16 x float> %1, <16 x float>* %res
```

```
ret void
```

```
}
```

 $define \ dso_local \ void \ @ubto16f32_512(<\!\!16 \ x \ i16\!\!> \%a, <\!\!16 \ x \ float\!\!> \ \%res) \ "min-legal-vector-width"="512" \ \{a, a, b, a,$

```
; CHECK-LABEL: ubto16f32_512:
```

```
; CHECK: # %bb.0:
```

; CHECK-NEXT: vpmovw2m %ymm0, %k0

; CHECK-NEXT: vpmovm2d %k0, %zmm0

; CHECK-NEXT: vpsrld \$31, %zmm0, %zmm0

; CHECK-NEXT: vcvtdq2ps %zmm0, %zmm0

```
; CHECK-NEXT: vmovaps %zmm0, (%rdi)
```

```
; CHECK-NEXT: vzeroupper
```

; CHECK-NEXT: retq

%mask = icmp slt <16 x i16> %a, zeroinitializer

```
\%1 = uitofp <16 x i1> \% mask to <16 x float>
```

store <16 x float> %1, <16 x float>* %res

```
ret void
```

}

define dso_local void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {

```
; CHECK-LABEL: ubto16f64_256:
          # %bb.0:
; CHECK:
; CHECK-NEXT: vpmovw2m
%ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT: vextracti128 $1, % ymm0, % xmm0
; CHECK-NEXT: vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm2
; CHECK-NEXT: vpsrld $31, %ymm2, %ymm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT: vextracti128 $1, % ymm2, % xmm2
; CHECK-NEXT: vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT: vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT: vmovaps %ymm3, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT: vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
\%1 = uitofp <16 x i1> \% mask to <16 x double>
store <16 \text{ x double} > \%1, <16 \text{ x double} > \% res
ret void
}
```

define dso_local void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" { ; CHECK-LABEL: ubto16f64_512:

; CHECK: # %bb.0:

; CHECK-NEXT:

vpmovw2m %ymm0, %k0

```
; CHECK-NEXT: vpmovm2d %k0, %zmm0
```

- ; CHECK-NEXT: vpsrld \$31, %zmm0, %zmm0
- ; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm1
- ; CHECK-NEXT: vextracti64x4 \$1, % zmm0, % ymm0

```
; CHECK-NEXT: vcvtdq2pd %ymm0, %zmm0
```

```
; CHECK-NEXT: vmovaps %zmm0, 64(%rdi)
```

```
; CHECK-NEXT: vmovaps % zmm1, (%rdi)
```

```
; CHECK-NEXT: vzeroupper
```

```
; CHECK-NEXT: retq
```

```
%mask = icmp slt <16 x i16> %a, zeroinitializer
```

```
\%1 = uitofp <16 x i1> \% mask to <16 x double>
```

```
store <16 x double> \%1, <16 x double>* %res
```

```
ret void
```

}

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-

```
width"="256" {
; CHECK-LABEL: test_16f32toub_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT: vpslld $31, %ymm1, %ymm1
; CHECK-NEXT: vpmovd2m %ymm1, %k0
; CHECK-NEXT: vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT: vpslld $31, %ymm1, %ymm1
; CHECK-NEXT: vpmovd2m %ymm1, %k1
; CHECK-NEXT: kunpckbw %k0, %k1, %k1
; CHECK-NEXT: vmovdqu16
%ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT: retq
\%a = load <16 x float>, <16 x float>* % ptr
\% mask = fptoui <16 x float> % a to <16 x i1>
% select = select <16 x i1> % mask, <16 x i16> % passthru, <16 x i16> zeroinitializer
ret <16 \text{ x i}16> % select
}
define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="512" {
; CHECK-LABEL: test_16f32toub_512:
; CHECK:
           # %bb.0:
; CHECK-NEXT: vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT: vpslld $31, %zmm1, %zmm1
; CHECK-NEXT: vpmovd2m %zmm1, %k1
; CHECK-NEXT: vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT: retq
\%a = load <16 x float>, <16 x float>* % ptr
\text{%mask} = \text{fptoui} < 16 \text{ x float} > \text{%a to} < 16 \text{ x il} >
% select = select <16 x i1> % mask, <16 x i16> % passthru, <16 x i16> zeroinitializer
ret <16 x i16> % select
}
define <16 x i16> @test_16f32tosb_256(<16 x float>* % ptr, <16 x i16> % passthru) "min-legal-vector-
width"="256" {
; CHECK-LABEL: test_16f32tosb_256:
; CHECK:
            # %bb.0:
; CHECK-NEXT:
  vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT: vpmovd2m %ymm1, %k0
; CHECK-NEXT: vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT: vpmovd2m %ymm1, %k1
; CHECK-NEXT: kunpckbw %k0, %k1, %k1
; CHECK-NEXT: vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT: retq
% a = load <16 x float>, <16 x float>* % ptr
\text{%mask} = \text{fptosi} < 16 \text{ x float} > \text{%a to} < 16 \text{ x il} >
```

```
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}
```

define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vectorwidth"="512" { ; CHECK-LABEL: test_16f32tosb_512: ; CHECK: # %bb.0: ; CHECK-NEXT: vcvttps2dq (%rdi), %zmm1 ; CHECK-NEXT: vpmovd2m %zmm1, %k1 ; CHECK-NEXT: vpmovd2m %zmm1, %k1 ; CHECK-NEXT: vmovdqu16 %ymm0, %ymm0 {%k1} {z} ; CHECK-NEXT: retq %a = load <16 x float>, <16 x float>* %ptr %mask = fptosi <16 x float> %a to <16 x i1> %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer ret <16 x i16> %select

}

define

```
dso_local void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: mul256:
; CHECK-AVX512:
                   # %bb.0:
; CHECK-AVX512-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-AVX512-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-AVX512-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-AVX512-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm5 =
ymm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT: vpmullw %ymm4, %ymm5, %ymm4
; CHECK-AVX512-NEXT: vmovdqa { { .*#+ } } ymm5 =
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm4, %ymm4
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm3 =
ymm3[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm1 =
ymm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT: vpmullw %ymm3, %ymm1, %ymm1
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm1, %ymm1
; CHECK-AVX512-NEXT: vpackuswb %ymm4, %ymm1, %ymm1
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm3 =
ymm2[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT: vpmullw %ymm3, %ymm4, %ymm3
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm3, %ymm3
```

```
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm2 =
ymm2[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT: vpmullw
%ymm2, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vpackuswb %ymm3, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-AVX512-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-AVX512-NEXT: vzeroupper
; CHECK-AVX512-NEXT: retq
; CHECK-VBMI-LABEL: mul256:
; CHECK-VBMI:
                  # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-VBMI-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-VBMI-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-VBMI-NEXT: vmovdga 32(%rsi), %ymm3
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm5 =
ymm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT: vpmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm3 =
ymm3[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm1 =
ymm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT: vpmullw %ymm3, %ymm1, %ymm1
; CHECK-VBMI-NEXT: vmovdqa {{.*#+}} ymm3 =
[0,2,4,6,8,10,12,14,32,34,36,38,40,42,44,46,16,18,20,22,24,26,28,30,48,50,52,54,56,58,60,62]
; CHECK-VBMI-NEXT: vpermt2b %ymm4, %ymm3, %ymm1
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm2[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm5 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT: vpmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm2 =
ymm2[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT:
  vpmullw %ymm2, %ymm0, %ymm0
; CHECK-VBMI-NEXT: vpermt2b %ymm4, %ymm3, %ymm0
; CHECK-VBMI-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-VBMI-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-VBMI-NEXT: vzeroupper
```

```
; CHECK-VBMI-NEXT: retq
%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void
```

}

define dso_local void @mul512(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="512" { ; CHECK-AVX512-LABEL: mul512:

; CHECK-AVX512: # %bb.0:

; CHECK-AVX512-NEXT: vmovdqa64 (%rdi), %zmm0

; CHECK-AVX512-NEXT: vmovdqa64 (%rsi), %zmm1

; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} zmm2 =

zmm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4 2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]

; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} zmm3 =

```
zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4 2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
```

```
;
```

CHECK-AVX512-NEXT: vpmullw %zmm2, %zmm3, %zmm2

; CHECK-AVX512-NEXT: vmovdqa64 {{.*#+}} zmm3 =

; CHECK-AVX512-NEXT: vpandq %zmm3, %zmm2, %zmm2

; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} zmm1 =

zmm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,32,33,33,34,34,35,35,36,3 6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]

```
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} zmm0 =
```

zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3

6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]

; CHECK-AVX512-NEXT: vpmullw %zmm1, %zmm0, %zmm0

; CHECK-AVX512-NEXT: vpandq %zmm3, %zmm0,

%zmm0

; CHECK-AVX512-NEXT: vpackuswb %zmm2, %zmm0, %zmm0

; CHECK-AVX512-NEXT: vmovdqa64 %zmm0, (%rdx)

; CHECK-AVX512-NEXT: vzeroupper

; CHECK-AVX512-NEXT: retq

```
;
```

; CHECK-VBMI-LABEL: mul512:

; CHECK-VBMI: #%bb.0:

; CHECK-VBMI-NEXT: vmovdqa64 (%rdi), %zmm0

; CHECK-VBMI-NEXT: vmovdqa64 (%rsi), %zmm1

; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} zmm2 =

2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]

; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} zmm3 =

```
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT: vpmullw %zmm2, %zmm3, %zmm2
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} zmm1 =
zmm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} zmm0 =
zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-VBMI-NEXT: vpmullw %zmm1, %zmm0, %zmm0
; CHECK-VBMI-NEXT: vmovdqa64 {{.*#+}} zmm1 =
46,96,98,100,102,104,106,108,110,48,50,52,54,56,58,60,62,112,114,116,118,120,122,124,126]
; CHECK-VBMI-NEXT: vpermi2b %zmm2, %zmm0, %zmm1
; CHECK-VBMI-NEXT: vmovdqa64 %zmm1, (%rdx)
; CHECK-VBMI-NEXT: vzeroupper
; CHECK-VBMI-NEXT: retq
\%d = load <64 x i8>, <64 x i8>* %a
\%e = load <64 x i8>. <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void
}
; This threw an assertion at one point.
define <4 x i32> @mload v4i32(<4
x i32> %trigger, <4 x i32>* %addr, <4 x i32> %dst) "min-legal-vector-width"="256" {
; CHECK-LABEL: mload_v4i32:
           # %bb.0:
; CHECK:
; CHECK-NEXT: vptestnmd %xmm0, %xmm0, %k1
; CHECK-NEXT: vpblendmd (%rdi), %xmm1, %xmm0 {%k1}
; CHECK-NEXT: retq
\%mask = icmp eq <4 x i32> % trigger, zeroinitializer
%res = call <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* %addr, i32 4, <4 x i1> %mask, <4 x i32>
%dst)
ret <4 x i32> %res
}
declare <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>*, i32, <4 x i1>, <4 x i32>)
define <16 x i32> @trunc_v16i64_v16i32(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i64_v16i32:
: CHECK:
           # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
; CHECK-NEXT: vmovdqa 96(%rdi), %ymm3
; CHECK-NEXT: vpmovqd %ymm0, %xmm0
; CHECK-NEXT: vpmovqd %ymm1, %xmm1
```

```
; CHECK-NEXT: vinserti128 $1, %xmm1, %ymm0, %ymm0
; CHECK-NEXT:
    vpmovqd %ymm2, %xmm1
; CHECK-NEXT: vpmovqd %ymm3, %xmm2
; CHECK-NEXT: vinserti128 $1, %xmm2, %ymm1, %ymm1
; CHECK-NEXT: retq
%a = load <16 x i64>, <16 x i64>* %x
%b = trunc <16 x i64> %a to <16 x i32>
ret <16 x i32> %b
}
```

```
define <\!\!16 \ x \ i8\!> @trunc\_v16i64\_v16i8(<\!\!16 \ x \ i64\!\!> \mbox{\ }\%x) \ nounwind \ "min-legal-vector-width" = "256" \ \{mbox{\ }\mbox{\ }\mb
```

```
; CHECK-LABEL: trunc_v16i64_v16i8:
```

; CHECK: # %bb.0:

```
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
```

```
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
```

```
; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
```

```
; CHECK-NEXT: vmovdqa 96(%rdi), %ymm3
```

```
; CHECK-NEXT: vpmovqb %ymm3, %xmm3
```

```
; CHECK-NEXT: vpmovqb %ymm2, %xmm2
```

```
; CHECK-NEXT: vpunpckldq { {.*#+} } xmm2 = xmm2[0], xmm3[0], xmm3[1]
```

```
; CHECK-NEXT: vpmovqb %ymm1, %xmm1
```

```
; CHECK-NEXT: vpmovqb %ymm0, %xmm0
```

```
; CHECK-NEXT: vpunpckldq { {.*#+} } xmm0 = xmm0[0], xmm1[0], xmm0[1], xmm1[1]
```

```
; CHECK-NEXT: vpunpcklqdq {{.*#+}} xmm0 = xmm0[0], xmm2[0]
```

```
; CHECK-NEXT: vzeroupper
```

```
; CHECK-NEXT: retq
```

```
%a = load <16 x i64>, <16
```

x i64>* %x

```
% b = trunc <16 x i64> % a to <16 x i8>
```

```
ret <16 x i8> %b
```

```
}
```

```
define <16 x i8> @trunc_v16i32_v16i8(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
  ; CHECK-LABEL: trunc_v16i32_v16i8:
  ; CHECK: # %bb.0:
  ; CHECK-NEXT: vmovdqa (%rdi), %ymm0
  ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
  ; CHECK-NEXT: vpmovdb %ymm1, %xmm1
  ; CHECK-NEXT: vpmovdb %ymm0, %xmm0
  ; CHECK-NEXT: vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm1[0]
  ; CHECK-NEXT: vzeroupper
  ; CHECK-NEXT: retq
  %a = load <16 x i32>, <16 x i32>* %x
  %b = trunc <16 x i32> %a to <16 x i8>
  ret <16 x i8> %b
```

```
}
```

```
define <8 x i8> @trunc_v8i64_v8i8(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i8:
; CHECK:
           # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmovqb %ymm1, %xmm1
; CHECK-NEXT: vpmovqb %ymm0, %xmm0
; CHECK-NEXT: vpunpckldq {{.*#+}} xmm0 = xmm0[0], xmm1[0], xmm0[1], xmm1[1]
; CHECK-NEXT: vzeroupper
CHECK-NEXT: retq
%a = load <8 x i64>, <8 x i64>* %x
\%b = trunc <8 x i64> % a to <8 x i8>
ret <8 x i8> %b
}
define <8 x i16> @trunc_v8i64_v8i16(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc v8i64 v8i16:
; CHECK:
           # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmovqw %ymm1, %xmm1
; CHECK-NEXT: vpmovqw %ymm0, %xmm0
; CHECK-NEXT: vpunpcklqdq {{.*#+}} xmm0 = xmm0[0], xmm1[0]
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <8 x i64>, <8 x i64>* %x
\%b = trunc <8 x i64> % a to <8 x i16>
ret <8 x i16> %b
}
define <8 x i32> @trunc_v8i64_v8i32_zeroes(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i32_zeroes:
; CHECK:
           # %bb.0:
; CHECK-NEXT: vpsrlq $48, 32(%rdi), %ymm0
; CHECK-NEXT: vpsrlq $48, (%rdi), %ymm1
; CHECK-NEXT: vpackusdw %ymm0, %ymm1, %ymm0
; CHECK-NEXT: vpermq \{\{.*\#+\}\} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT:
 retq
\%a = load < 8 \times i64 >, < 8 \times i64 >* \%x
%c = trunc < 8 x i64 > \%b to < 8 x i32 >
ret <8 x i32> %c
}
```

define <16 x i16> @trunc_v16i32_v16i16_zeroes(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" { ; CHECK-LABEL: trunc_v16i32_v16i16_zeroes:

```
; CHECK:
                                                              # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-NEXT: vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]
; CHECK-NEXT: vpermi2w 32(%rdi), %ymm1, %ymm0
; CHECK-NEXT: retq
   % a = load <16 x i32>, <16 x i32>* % x
   %b = lshr <16 x i32> %a, <i32 16, i32 
 16, i32 16, i32 16, i32 16, i32 16>
   %c = trunc < 16 x i 32 > \%b to < 16 x i 16 > 
  ret <16 x i16> %c
 }
define <32 x i8> @trunc v32i16 v32i8 zeroes(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_zeroes:
; CHECK-AVX512:
       # %bb.0:
; CHECK-AVX512-NEXT: vpsrlw $8, 32(%rdi), %ymm0
; CHECK-AVX512-NEXT: vpsrlw $8, (%rdi), %ymm1
; CHECK-AVX512-NEXT: vpackuswb %ymm0, %ymm1, %ymm0
; CHECK-AVX512-NEXT: vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-AVX512-NEXT: retq
; CHECK-VBMI-LABEL: trunc_v32i16_v32i8_zeroes:
; CHECK-VBMI:
                                                                                           # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-VBMI-NEXT: vmovdqa {{.*#+}} ymm0 =
[1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63]
; CHECK-VBMI-NEXT: vpermi2b 32(%rdi), %ymm1, %ymm0
; CHECK-VBMI-NEXT: retq
   \%a = load <32 \text{ x i} 16>, <32 \text{ x i} 16>* \% \text{ x}
   %b = lshr <32 x i16 > %a, <i16 8, i16 8, i16
i16 8, i1
   %c = trunc < 32 \text{ x i} 16 > \%b \text{ to } < 32 \text{ x i} 8 >
 ret <32 x i8> %c
 }
define <8 x i32> @trunc_v8i64_v8i32_sign(<8 x i64>*
  %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i32_sign:
: CHECK:
                                                              # %bb.0:
; CHECK-NEXT: vpsraq $48, 32(%rdi), %ymm0
; CHECK-NEXT: vpsraq $48, (%rdi), %ymm1
; CHECK-NEXT: vpmovqd %ymm1, %xmm1
; CHECK-NEXT: vpmovqd %ymm0, %xmm0
; CHECK-NEXT: vinserti128 $1, % xmm0, % ymm1, % ymm0
; CHECK-NEXT: retq
   \%a = load < 8 \times i64 >, < 8 \times i64 >* \%x
   %b = ashr <8 x i64> %a, <i64 48, i64 4
```

```
%c = trunc <8 x i64> %b to <8 x i32>
ret <8 x i32> %c
}
```

```
define <16 x i16> @trunc_v16i32_v16i16_sign(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i16_sign:
                                                     # %bb.0:
; CHECK:
; CHECK-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-NEXT: vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]
; CHECK-NEXT: vpermi2w 32(%rdi), %ymm1, %ymm0
; CHECK-NEXT: retq
  %a = load <16 x i32>, <16 x i32>* %x
  %b = ashr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16,
  i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16
  %c = trunc <16 x i32> %b to <16 x i16>
  ret <16 x i16> %c
 }
define <32 x i8> @trunc_v32i16_v32i8_sign(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_sign:
; CHECK-AVX512:
                                                                                        # %bb.0:
; CHECK-AVX512-NEXT: vpsrlw $8, 32(%rdi), %ymm0
; CHECK-AVX512-NEXT: vpsrlw $8, (%rdi), %ymm1
; CHECK-AVX512-NEXT: vpackuswb %ymm0, %ymm1, %ymm0
; CHECK-AVX512-NEXT: vpermq \{\{.*\#+\}\} ymm0 = ymm0[0,2,1,3]
; CHECK-AVX512-NEXT: retq
; CHECK-VBMI-LABEL: trunc_v32i16_v32i8_sign:
; CHECK-VBMI:
                                                                                # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-VBMI-NEXT: vmovdqa {{.*#+}} ymm0 =
[1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63]
; CHECK-VBMI-NEXT: vpermi2b 32(%rdi), %ymm1, %ymm0
; CHECK-VBMI-NEXT: retq
  \%a = load <32 \text{ x i} 16>, <32 \text{ x i} 16>* \% \text{ x}
  \%b = ashr <32 x i16> %a, <i16 8, i16
  8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, 
i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i1
  %c = trunc <32 x i16 > \%b to <32 x i8 >
  ret <32 x i8> %c
 }
define dso_local void @zext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-
width"="256" {
; CHECK-LABEL: zext_v16i8_v16i64:
; CHECK:
                                                    # %bb.0:
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm1 =
```

xmm0[0], zero, xmm0[1], zero, xmm0[2], zero, xmm0[3], zero, xmm0[4], zero, xmm0[5], zero, xmm0[6], zero, xmm0[7], zero, xmm0

o,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero

```
; CHECK-NEXT: vpshufd \{\{.*\#+\}\} xmm2 = xmm1[2,3,2,3]
```

; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm2 =

xmm2[0],zero,zero,zero,xmm2[1],zero,zero,zero,xmm2[2],zero,zero,zero,xmm2[3],zero,zero,zero

```
; CHECK-NEXT: vextracti128 $1, % ymm1, % xmm1
```

; CHECK-NEXT: vpshufd $\{\{.*\#+\}\}$ xmm3 = xmm1[2,3,2,3]

; CHECK-NEXT:

```
vpmovzxwq { {.*#+} } ymm3 =
```

```
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm1 =
```

```
; CHECK-NEXT: vpmovzxbq {{.*#+}} ymm0 =
```

```
; CHECK-NEXT: vmovdqa %ymm0, (%rdi)
```

```
; CHECK-NEXT: vmovdqa %ymm1, 64(%rdi)
```

```
; CHECK-NEXT: vmovdqa %ymm3, 96(%rdi)
```

; CHECK-NEXT: vmovdqa %ymm2, 32(%rdi)

```
; CHECK-NEXT: vzeroupper
```

```
; CHECK-NEXT: retq
```

```
\%a = zext < 16 x i8 > \%x to < 16 x i64 >
```

```
store <16 x i64> %a, <16 x i64>* %y
```

```
ret void
```

```
}
```

define dso_local void @sext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {

```
; CHECK-LABEL: sext_v16i8_v16i64:
```

```
; CHECK: # %bb.0:
```

```
; CHECK-NEXT: vpmovsxbw %xmm0, %ymm1
```

```
; CHECK-NEXT:
```

vpshufd { {.*#+} } xmm2 = xmm1[2,3,2,3]

```
; CHECK-NEXT: vpmovsxwq %xmm2, %ymm2
```

```
; CHECK-NEXT: vextracti128 $1, %ymm1, %xmm1
```

```
; CHECK-NEXT: vpshufd {{.*#+}} xmm3 = xmm1[2,3,2,3]
```

```
; CHECK-NEXT: vpmovsxwq %xmm3, %ymm3
```

```
; CHECK-NEXT: vpmovsxwq %xmm1, %ymm1
```

```
; CHECK-NEXT: vpmovsxbq %xmm0, %ymm0
```

```
; CHECK-NEXT: vmovdqa %ymm0, (%rdi)
```

```
; CHECK-NEXT: vmovdqa %ymm1, 64(%rdi)
```

```
; CHECK-NEXT: vmovdqa %ymm3, 96(%rdi)
```

```
; CHECK-NEXT: vmovdqa %ymm2, 32(%rdi)
```

; CHECK-NEXT: vzeroupper

```
; CHECK-NEXT: retq
```

```
a = sext < 16 x i8 > %x to < 16 x i64 >
```

```
store <16 x i64> %a, <16 x i64>* %y
```

```
ret void
```

}

```
define dso_local void @vselect_split_v8i16_setcc(<8 x i16> %s, <8 x i16> %t, <8 x i64>* %p, <8 x i64>* %q, <8
x i64>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v8i16_setcc:
; CHECK:
            # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqw %xmm1, %xmm0, %k1
; CHECK-NEXT: kshiftrb $4, %k1, %k2
CHECK-NEXT: vmovdqa64 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
\%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
\%a = icmp \ eq < 8 \ x \ i16 > \%s, \%t
\%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}
define dso_local void @vselect_split_v8i32_setcc(<8 x i32> %s, <8 x i32> %t, <8 x i64>* %p, <8 x i64>* %q, <8
x i64>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v8i32_setcc:
            # %bb.0:
; CHECK:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqd %ymm1, %ymm0, %k1
; CHECK-NEXT: kshiftrb $4, %k1, %k2
; CHECK-NEXT: vmovdqa64 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:
  vzeroupper
; CHECK-NEXT: retq
\%x = load <8 x i64>, <8 x i64>* %p
\%y = load <8 x i64>, <8 x i64>* %q
a = icmp \ eq < 8 \ x \ i32 > \% s, \% t
\%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}
```

define dso_local void @vselect_split_v16i8_setcc(<16 x i8> %s, <16 x i8> %t, <16 x i32>* %p, <16 x i32>* %q,

```
<16 x i32>* %r) "min-legal-vector-width"="256" {
```

```
; CHECK-LABEL: vselect_split_v16i8_setcc:
```

```
; CHECK: # %bb.0:
```

- ; CHECK-NEXT: vmovdqa (%rsi), %ymm2
- ; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
- ; CHECK-NEXT: vpcmpeqb %xmm1, %xmm0, %k1
- ; CHECK-NEXT: kshiftrw \$8, %k1, %k2
- ; CHECK-NEXT: vmovdqa32 32(%rdi), %ymm3 {%k2}
- ; CHECK-NEXT: vmovdqa32 (%rdi), %ymm2 {%k1}
- ; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
- ; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
- ; CHECK-NEXT: vzeroupper
- ; CHECK-NEXT: retq
- %x = load < 16 x i 32 >, <16 x i 32>* %p
- y = load < 16 x i 32, < 16 x i 32, < x i 32
- $\%a = icmp \ eq < 16 \ x \ i8 > \%s, \%t$
- %b = select <16 x i1>
- %a, <16 x i32> %x, <16 x i32> %y
- store <16 x i32> %b, <16 x i32>* %r

```
ret void
```

```
}
```

```
define dso_local void @vselect_split_v16i16_setcc(<16 x i16> %s, <16 x i16> %t, <16 x i32>* %p, <16 x i32>*
%q, <16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i16_setcc:
; CHECK:
            # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqw %ymm1, %ymm0, %k1
; CHECK-NEXT: kshiftrw $8, %k1, %k2
; CHECK-NEXT: vmovdqa32 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa32 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <16 x i32>, <16 x i32>* %p
%y = load <16 x i32>, <16 x i32>* %q
\%a = icmp eq <16 x i16> % s, % t
\%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
store <16 x i32> %b, <16 x i32>* %r
ret void
}
define <16 x i8> @trunc_packus_v16i32_v16i8(<16 x i32>* %p) "min-legal-vector-width"="256"
{
; CHECK-LABEL: trunc_packus_v16i32_v16i8:
```

; CHECK: # %bb.0: ; CHECK-NEXT: vmovdqa (%rdi), %ymm0 ; CHECK-NEXT: vpackusdw 32(%rdi), %ymm0, %ymm0 ; CHECK-NEXT: vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3] ; CHECK-NEXT: vpmovuswb %ymm0, %xmm0 ; CHECK-NEXT: vzeroupper ; CHECK-NEXT: retq %a = load <16 x i32>, <16 x i32>* %p %b = icmp slt <16 x i32> %a, <i32 255, i32 255, 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255> %c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> <i32 255, i32 255 %d = icmp sgt <16 x i32> %c, zeroinitializer %e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zeroinitializer %f = trunc <16 x i32> %e to <16 x i8> ret <16 x i8> %f

}

define dso_local void @trunc_packus_v16i32_v16i8_store(<16 x i32>* %p, <16 x i8>* %q) "min-legal-vector-width"="256"

{

; CHECK-LABEL: trunc_packus_v16i32_v16i8_store:

; CHECK: # %bb.0:

```
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
```

; CHECK-NEXT: vpackusdw 32(%rdi), %ymm0, %ymm0

; CHECK-NEXT: vpermq {{.*#+} ymm0 = ymm0[0,2,1,3]

; CHECK-NEXT: vpmovuswb %ymm0, (%rsi)

; CHECK-NEXT: vzeroupper

; CHECK-NEXT: retq

%a = load <16 x i32>, <16 x i32>* %p

%b = icmp slt <16 x i32> %a, <i32 255, i32 255,

```
%c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> <i32 255, i32 255, i32
```

 $%d = icmp \ sgt < 16 \ x \ i32 > \%c$, zeroinitializer

```
\%e = select <16 x i1> \%d, <16 x i32> \%c, <16 x i32> zeroinitializer
```

```
% f = trunc < 16 x i 32 > % e to < 16 x i 8 >
```

```
store <16 x i8> %f, <16 x i8>* %q
```

ret void

}

```
define <64 x i1> @v64i1_argument_return(<64 x
```

i1>%x) "min-legal-vector-width"="256" {

; CHECK-LABEL: v64i1_argument_return:

```
; CHECK: # %bb.0:
```

```
; CHECK-NEXT: retq
```

```
ret <64 x i1> % x
```

```
}
```

define dso_local void @v64i1_shuffle(<64 x i8>* %x, <64 x i8>* %y) "min-legal-vector-width"="256" {

; CHECK-LABEL: v64i1_shuffle: ; CHECK: # %bb.0: # %entry ; CHECK-NEXT: vmovdqa (%rdi), %ymm1 ; CHECK-NEXT: vmovdqa 32(%rdi), %ymm0 ; CHECK-NEXT: vptestnmb %ymm1, %ymm1, %k0 ; CHECK-NEXT: kshiftrd \$1, %k0, %k1 ; CHECK-NEXT: kshiftlq \$63, %k0, %k2 ; CHECK-NEXT: kshiftrq \$62, %k2, %k2 ; CHECK-NEXT: kshiftlq \$63, %k1, %k1 ; CHECK-NEXT: kshiftrq \$63, %k1, %k1 ; CHECK-NEXT: korg %k2, %k1, %k1 ; CHECK-NEXT: movq \$-5, %rax ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$3, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$61, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-9, %rax ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$2, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$60, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-17, %rax ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$5, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$59, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-33, %rax ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$4, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$58, %k2, %k2 ; CHECK-NEXT: korg %k2, %k1, %k1 ; CHECK-NEXT: movq \$-65, %rax ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$7, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$57, %k2, %k2

; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-129, %rax ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$6, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$56, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-257, %rax # imm = 0xFEFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$9, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$55, %k2, %k2 ; CHECK-NEXT: korg %k2, %k1, %k1 ; CHECK-NEXT: movq \$-513, %rax # imm = 0xFDFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$8, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$54, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-1025, %rax # imm = 0xFBFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$11, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$53, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-2049, %rax # imm = 0xF7FF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$10, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$52, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-4097, %rax # imm = 0xEFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$13, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$51, %k2, %k2 ; CHECK-NEXT: korg %k2, %k1, %k1 ; CHECK-NEXT: movq \$-8193, %rax # imm = 0xDFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1

; CHECK-NEXT: kshiftrd \$12, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$50, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-16385, %rax # imm = 0xBFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$15, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$49, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-32769, %rax # imm = 0xFFFF7FFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$14, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$48, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-65537, %rax # imm = 0xFFFEFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$17, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$47, %k2, %k2 ; CHECK-NEXT: korg %k2, %k1, %k1 ; CHECK-NEXT: movq \$-131073, %rax # imm = 0xFFFDFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$16, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$46, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-262145, %rax # imm = 0xFFFBFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$19, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$45, %k2, %k2 ; CHECK-NEXT: korg %k2, %k1, %k1 ; CHECK-NEXT: movq \$-524289, %rax # imm = 0xFFF7FFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$18, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$44, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1

; CHECK-NEXT: movq \$-1048577, %rax # imm = 0xFFEFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$21, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$43, %k2, %k2 ; CHECK-NEXT: korg %k2, %k1, %k1 ; CHECK-NEXT: movq \$-2097153, %rax # imm = 0xFFDFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$20, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$42, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movg \$-4194305, %rax # imm = 0xFFBFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$23, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrg \$41, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-8388609, %rax # imm = 0xFF7FFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$22, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$40, %k2, %k2 ; CHECK-NEXT: korg %k2, %k1, %k1 ; CHECK-NEXT: movq \$-16777217, %rax # imm = 0xFEFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$25, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$39, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movg \$-33554433, %rax # imm = 0xFDFFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$24, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$38, %k2, %k2 ; CHECK-NEXT: korg %k2, %k1, %k1 ; CHECK-NEXT: movq \$-67108865, %rax # imm = 0xFBFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$27, %k0, %k2

; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$37, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-134217729, %rax # imm = 0xF7FFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$26, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$36, %k2, %k2 ; CHECK-NEXT: korg %k2, %k1, %k1 ; CHECK-NEXT: movq \$-268435457, %rax # imm = 0xEFFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$29, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$35, %k2, %k2 ; CHECK-NEXT: korg %k2, %k1, %k1 ; CHECK-NEXT: movq \$-536870913, %rax # imm = 0xDFFFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$28, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrg \$34, %k2, %k2 ; CHECK-NEXT: korq %k2, %k1, %k1 ; CHECK-NEXT: movq \$-1073741825, %rax # imm = 0xBFFFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k1 ; CHECK-NEXT: kshiftrd \$31, %k0, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$33, %k2, %k2 ; CHECK-NEXT: korg %k2, %k1, %k1 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k1, %k2 ; CHECK-NEXT: vptestnmb %ymm0, %ymm0, %k1 ; CHECK-NEXT: kshiftrd \$30, %k0, %k0 ; CHECK-NEXT: kshiftlq \$63, %k0, %k0 ; CHECK-NEXT: kshiftrq \$32, %k0, %k0 ; CHECK-NEXT: korq %k0, %k2, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$1, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$31, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0

; CHECK-NEXT: movabsq \$-8589934593, %rax # imm = 0xFFFFFFDFFFFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftlq \$63, %k1, %k2 ; CHECK-NEXT: kshiftrq \$30, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$3, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$29, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$2, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$28, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$5, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$27, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: movabsg \$-137438953473, %rax # imm = 0xFFFFFDFFFFFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$4, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$26, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: movabsq \$-274877906945, %rax # imm = 0xFFFFFBFFFFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$7, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$25, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$6, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2

; CHECK-NEXT: kshiftrg \$24, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$9, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$23, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: movabsq \$-2199023255553, %rax # imm = 0xFFFFDFFFFFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$8, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$22, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: movabsq \$-4398046511105, ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$11, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$21, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$10, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrg \$20, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$13, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$19, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$12, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$18, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2

; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$15, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$17, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$14, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$16, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$17, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$15, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: movabsq \$-562949953421313, %rax # imm = 0xFFFDFFFFFFFFFFF ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$16, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$14, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$19, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$13, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$18, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$12, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: movabsq \$-4503599627370497, ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$21, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$11, %k2, %k2

; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$20, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$10, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$23, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$9, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$22, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$8, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$25, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$7, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$24, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$6, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$27, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$5, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0

; CHECK-NEXT: kshiftrd \$26, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$4, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$29, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$3, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$28, %k1, %k2 ; CHECK-NEXT: kshiftlq \$63, %k2, %k2 ; CHECK-NEXT: kshiftrq \$2, %k2, %k2 ; CHECK-NEXT: korg %k2, %k0, %k0 ; CHECK-NEXT: kmovq %rax, %k2 ; CHECK-NEXT: kandq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$31, %k1, %k2 ; CHECK-NEXT: kshiftlq \$62, %k2, %k2 ; CHECK-NEXT: korq %k2, %k0, %k0 ; CHECK-NEXT: kshiftrd \$30, %k1, %k1 ; CHECK-NEXT: kshiftlq \$1, %k0, %k0 ; CHECK-NEXT: kshiftrq \$1, %k0, %k0 ; CHECK-NEXT: kshiftlq \$63, %k1, %k1 ; CHECK-NEXT: korg %k1, %k0, %k1 ; CHECK-NEXT: vmovdqu8 %ymm1, (%rsi) {%k1} ; CHECK-NEXT: kshiftrq \$32, %k1, %k1 ; CHECK-NEXT: vmovdqu8 %ymm0, 32(%rsi) {%k1} ; CHECK-NEXT: vzeroupper ; CHECK-NEXT: retq entry: %a = load < 64 x i 8 >, < 64 x i 8 >* % x%b = icmp eq <64 x i8> %a, zeroinitializer % shuf = shufflevector <64 x i1> % b, <64 x i1> undef, <64 x i32> <i32 1, i32 0, i32 3, i32 2, i32 5, i32 4, i32 7, i32 6, i32 9, i32 8, i32 11, i32 10, i32 13, i32 12, i32 15, i32 14, i32 17, i32 16, i32 19, i32 18, i32 21, i32 20, i32 23, i32 22, i32 25, i 32 24, i 32 27, i 32 26, i 32 29, i 32 28, i 32 31, i 32 30, i 32 33, i 32 32, i 32 35, i 32 34, i 32 37, i 32 36, i 32 39, i 32 38, i 32 41, i 32 40, i 32 43, i 32 42, i 32 45, i 32 44, i 32 47, i 32 46, i 32 49, i 32 48, i 32 51, i 32 50, i 32 53, i 32 52, i 32 55, i 32 54, i32 57, i32 56, i32 59, i32 58, i32 61, i32 60, i32 63, i32 62> call void @llvm.masked.store.v64i8.p0v64i8(<64 x i8> %a, <64 x i8> % y, i32 1, <64 x i1> % shuf) ret void }

declare void @llvm.masked.store.v64i8.p0v64i8(<64 x i8>, <64 x i8>*, i32, <64 x i1>)

```
@mem64_dst = dso_local global i64 0, align 8
@mem64_src = dso_local global i64 0, align 8
define dso_local i32 @v64i1_inline_asm() "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_inline_asm:
; CHECK:
            # %bb.0:
; CHECK-NEXT: kmovq mem64 src(%rip), %k0
; CHECK-NEXT: #APP
; CHECK-NEXT: #NO_APP
; CHECK-NEXT: kmovq %k0, mem64 dst(%rip)
; CHECK-NEXT: movl -{ {[0-9]+}}(%rsp), %eax
; CHECK-NEXT: retq
\%1 = alloca i32, align 4
%2 = load i64, i64* @mem64_src, align
8
3 = \text{call i64 asm "", "=k,k,~{dirflag},~{fpsr},~{flags}"(i64 \% 2)
store i64 %3, i64* @mem64_dst, align 8
%4 = load i32, i32* %1, align 4
ret i32 %4
}
```

```
define dso_local void @cmp_v8i64_sext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-vector-width"="256" {
```

```
; CHECK-LABEL: cmp v8i64 sext:
; CHECK:
           # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT: vpcmpgtq 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT: vpcmpgtq (%rdi), %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
\%x = load <8 x i64>, <8 x i64>* % xptr
\%y = load <8 x i64>, <8 x i64>* % yptr
\% cmp = icmp slt <8 x i64> % x, % y
\% ext = sext <8 x i1> % cmp to <8 x i64>
store <8 x i64> % ext, <8 x i64>* % zptr
ret void
}
define dso_local void @cmp_v8i64_zext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-
vector-width"="256" {
; CHECK-LABEL: cmp_v8i64_zext:
CHECK:
          # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm0
```

; CHECK-NEXT: vmovdqa 32(%rsi), %ymm1

```
; CHECK-NEXT: vpcmpgtq 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT: vpcmpgtq (%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpsrlq $63, %ymm1, %ymm1
; CHECK-NEXT: vpsrlq $63, %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
\%x = load <8 x i64>, <8 x i64>* % xptr
\%y = load <8 x i64>, <8 x i64>* % yptr
\% cmp = icmp slt <8 x i64> % x, % y
\% ext = zext <8 x i1> % cmp to <8 x i64>
store <8 x i64> % ext, <8 x i64>* % zptr
ret void
}
define <16 \text{ x} i8> @var_rotate_v16i8(<16 \text{ x} i8> %a, <16 \text{ x} i8> %b) nounwind "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: var rotate v16i8:
; CHECK-AVX512:
                     # %bb.0:
; CHECK-AVX512-NEXT: vpand {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm1, %xmm1
; CHECK-AVX512-NEXT: vpmovzxbw {{.*#+}} ymm1 =
```

```
xmm1[0],zero,xmm1[1],zero,xmm1[2],zero,xmm1[3],zero,xmm1[4],zero,xmm1[5],zero,xmm1[6],zero,xmm1[7],zero,xmm1[8],zero,xmm1[9],zero,xmm1[10],zero,xmm1[11],zero,xmm1[12],zero,xmm1[13],zero,xmm1[14],zero,xmm1[15],zero
```

;

```
CHECK-AVX512-NEXT: vpmovzxbw {{.*#+}} ymm0 =
xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],zero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[7],xero,xmm0[
o,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xmm0[14],zero,xm
m0[15],zero
; CHECK-AVX512-NEXT: vpshufb {{.*#+}} ymm0 =
ymm0[0,0,2,2,4,4,6,6,8,8,10,10,12,12,14,14,16,16,18,18,20,20,22,22,24,24,26,26,28,28,30,30]
; CHECK-AVX512-NEXT: vpsllvw %ymm1, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vpsrlw $8, % ymm0, % ymm0
; CHECK-AVX512-NEXT: vpmovwb %ymm0, %xmm0
; CHECK-AVX512-NEXT: vzeroupper
; CHECK-AVX512-NEXT: retq
; CHECK-VBMI-LABEL: var_rotate_v16i8:
; CHECK-VBMI:
                                                                                                          # %bb.0:
; CHECK-VBMI-NEXT: # kill: def $xmm0 killed $xmm0 def $ymm0
; CHECK-VBMI-NEXT: vmovdqa {{.*#+}} ymm2 =
[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15]
 CHECK-VBMI-NEXT: vpand {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm1, %xmm1
; CHECK-VBMI-NEXT: vpermb %ymm0, %ymm2, %ymm0
; CHECK-VBMI-NEXT: vpmovzxbw {{.*#+}} ymm1 =
xmm1[0],zero,xmm1[1],zero,xmm1[2],zero,xmm1[3],zero,xmm1[4],zero,xmm1[5],zero,xmm1[6],zero,xmm1[7],zer
o,xmm1[8],zero,xmm1[9],zero,xmm1[10],zero,xmm1[11],zero,xmm1[12],zero,xmm1[13],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xmm1[14],zero,xm
```

m1[15],zero

; CHECK-VBMI-NEXT: vpsllvw %ymm1, %ymm0, %ymm0

; CHECK-VBMI-NEXT: vpsrlw \$8, %ymm0, %ymm0

; CHECK-VBMI-NEXT: vpmovwb %ymm0, %xmm0

; CHECK-VBMI-NEXT: vzeroupper

```
; CHECK-VBMI-NEXT: retq
```

%b8 = sub <16 x i8> <i8 8, i8 8, i8

```
\$ shl = shl <16 x i8> %a, %b
```

\$ lshr = lshr < 16 x i8 > % a, % b8

% or = or <16 x i8> % shl, % lshr

ret <16 x i8> % or

```
}
```

define <32 x i8> @var_rotate_v32i8(<32 x i8> %a, <32 x i8> %b) nounwind "min-legal-vector-width"="256" { ; CHECK-LABEL: var_rotate_v32i8:

; CHECK:

%bb.0:

; CHECK-NEXT: vpand {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm1, %ymm1

; CHECK-NEXT: vpxor %xmm2, %xmm2, %xmm2

; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm3 =

ymm1[8],ymm2[8],ymm1[9],ymm2[9],ymm1[10],ymm2[10],ymm1[11],ymm2[11],ymm1[12],ymm2[12],ymm1[13],ymm2[13],ymm1[14],ymm2[14],ymm1[15],ymm2[15],ymm1[24],ymm2[24],ymm1[25],ymm2[25],ymm1[26],ym m2[26],ymm1[27],ymm2[27],ymm1[28],ymm2[28],ymm1[29],ymm2[29],ymm1[30],ymm2[30],ymm1[31],ymm2[31]

; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm4 =

ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]

; CHECK-NEXT: vpsllvw %ymm3, %ymm4, %ymm3

; CHECK-NEXT: vpsrlw \$8, %ymm3, %ymm3

; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm1 =

ymm1[0],ymm2[0],ymm1[1],ymm2[1],ymm1[2],ymm2[2],ymm1[3],ymm2[3],ymm1[4],ymm2[4],ymm1[5],ymm2[5],ymm1[6],ymm2[6],ymm1[7],ymm2[7],ymm1[16],ymm2[16],ymm1[17],ymm2[17],ymm1[18],ymm2[18],ymm1[19],ymm2[19],ymm1[20],ymm1[21],ymm2[21],ymm1[22],ymm2[22],ymm1[23],ymm2[23]

; CHECK-NEXT:

```
vpunpcklbw \{\{.*\#+\}\} ymm0 =
```

ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]

; CHECK-NEXT: vpsllvw %ymm1, %ymm0, %ymm0

; CHECK-NEXT: vpsrlw \$8, %ymm0, %ymm0

; CHECK-NEXT: vpackuswb %ymm3, %ymm0, %ymm0

; CHECK-NEXT: retq

%b8 = sub <32 x i8> <i8 8, i8 8, i8

\$ shl = shl <32 x i8> % a, % b

%lshr = lshr <32 x i8> % a, % b8

% or = or <32 x i8> % shl, % lshr

ret <32 x i8 > % or

```
}
```

define <32 x i8> @splatvar_rotate_v32i8(<32 x i8> %a, <32 x i8> %b) nounwind "min-legal-vector-width"="256"

{

```
; CHECK-LABEL: splatvar_rotate_v32i8:
```

; CHECK: # %bb.0:

; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm2 =

```
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
```

```
; CHECK-NEXT: vpand {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm1, %xmm1
```

```
; CHECK-NEXT:
```

vpsllw %xmm1, %ymm2, %ymm2

```
; CHECK-NEXT: vpsrlw $8, % ymm2, % ymm2
```

```
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm0 =
```

ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]

; CHECK-NEXT: vpsllw %xmm1, %ymm0, %ymm0

- ; CHECK-NEXT: vpsrlw \$8, % ymm0, % ymm0
- ; CHECK-NEXT: vpackuswb %ymm2, %ymm0, %ymm0
- ; CHECK-NEXT: retq

%splat = shufflevector <32 x i8> %b, <32 x i8> undef, <32 x i32> zeroinitializer

```
\% splat8 = sub < 32 x i8 > < i8 8, i8 8,
```

```
8, i8 8>, %splat
```

\$ shl = shl < 32 x i8 > \$a, \$ splat

\$ lshr = lshr < 32 x i8 > % a, % splat8

% or = or <32 x i8> % shl, % lshr

ret <32 x i8> % or

```
}
```

```
define <32 x i8> @constant_rotate_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
```

; CHECK-LABEL: constant_rotate_v32i8:

; CHECK: # %bb.0:

; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm1

= ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]

```
; CHECK-NEXT: vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm1, %ymm1
```

; CHECK-NEXT: vpsrlw \$8, % ymm1, % ymm1

```
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm0 =
```

```
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
```

```
; CHECK-NEXT: vpsllvw { {\.?LCPI[0-9]+_[0-9]+} }(%rip), %ymm0, %ymm0
```

; CHECK-NEXT: vpsrlw \$8, %ymm0, %ymm0

; CHECK-NEXT: vpackuswb %ymm1, %ymm0, %ymm0

```
; CHECK-NEXT: retq
```

%shl = shl <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 7, i8 6, i8 5, i8 4, i8 3, i8 2, i8 1, i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 7, i8 6, i8 5, i8 4, i8 3, i8 2, i8 1>

```
%lshr = lshr <32 x i8> %a, <i8 8, i8 7, i8 6, i8 5, i8 4, i8 3, i8 2, i8 1, i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 7, i8 6, i8 5, i8 4, i8 3, i8 2, i8 1, i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7>
```

```
% or = or <32 x i8> % shl, % lshr
```

ret <32 x i8> %or

}

define <32 x i8> @splatconstant_rotate_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {

; CHECK-LABEL: splatconstant_rotate_v32i8:

; CHECK: # %bb.0:

; CHECK-NEXT: vpsllw \$4, %ymm0, %ymm1

; CHECK-NEXT: vpsrlw \$4, %ymm0, %ymm0

; CHECK-NEXT: vpternlogq \$216, {{\.?LCPI[0-9]+_[0-9]+}}(%rip){1to4}, %ymm1, %ymm0

; CHECK-NEXT: retq

%shl = shl <32 x i8> %a, <i8 4, i8 4

%lshr = lshr <32 x i8> %a, <i8 4, i8 4, i8

% or = or <32 x i8> % shl, % lshr

ret <32 x i8> % or

}

define <32 x i8> @splatconstant_rotate_mask_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" { ; CHECK-LABEL: splatconstant_rotate_mask_v32i8:

;

CHECK: # %bb.0:

; CHECK-NEXT: vpsllw \$4, %ymm0, %ymm1

; CHECK-NEXT: vpsrlw \$4, %ymm0, %ymm0

; CHECK-NEXT: vpternlogq \$216, {{\.?LCPI[0-9]+}}(%rip){1to4}, %ymm1, %ymm0

; CHECK-NEXT: vpand {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm0, %ymm0

; CHECK-NEXT: retq

%shl = shl <32 x i8> %a, <i8 4, i8 4

%lshr = lshr <32 x i8> %a, <i8 4, i8 4, i8

%rmask = and <32 x i8> %lshr, <i8 55, i8 55,

%lmask = and <32 x i8> %shl, <i8 33, i8 33,

% or = or <32 x i8> % lmask, % rmask

ret <32 x i8> % or

}

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; RUN: opt -passes=consthoist -S -o - %s | FileCheck %s

target datalayout = "e-m:e-p:32:32-i64:64-v128:64:128-a:0:32-n32-S64"

target triple = "thumbv6m-none--musleabi"

; Check that for i8 type, the maximum legal offset is 31.

; Also check that an constant used as value to be stored rather than

; pointer in a store instruction is hoisted.

; CHECK: foo_i8

; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874720 to i32

; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32

; CHECK-DAG: %[[C3:const[0-9]?]] = bitcast i32 805873720 to i32

; CHECK-DAG: %[[C4:const[0-9]?]] = bitcast i32 805873688 to i32

; CHECK: %0 = inttoptr i32 %[[C2]] to ptr

; CHECK-NEXT: %1 = load volatile i8, ptr %0

; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4

; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to ptr

; CHECK-NEXT: %3 = load volatile i8, ptr %2

; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 31

; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to ptr

; CHECK-NEXT: %5 = load volatile

i8, ptr %4

; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to ptr

; CHECK-NEXT: %7 = load volatile i8, ptr %6

; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 7

; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to ptr

; CHECK-NEXT: %9 = load volatile i8, ptr %8

; CHECK-NEXT: %10 = inttoptr i32 %[[C4]] to ptr

; CHECK-NEXT: store i8 %9, ptr %10

; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C4]], 31

; CHECK-NEXT: %11 = inttoptr i32 %[[M4]] to ptr

; CHECK-NEXT: store i8 %7, ptr %11

; CHECK-NEXT: %12 = inttoptr i32 %[[C3]] to ptr

; CHECK-NEXT: store i8 %5, ptr %12

; CHECK-NEXT: %[[M5:const_mat[0-9]?]] = add i32 %[[C3]], 7

; CHECK-NEXT: %13 = inttoptr i32 %[[M5]] to ptr

; CHECK-NEXT: store i8 %3, ptr %13

; CHECK-NEXT: %[[M6:const_mat[0-9]?]] = add i32 %[[C1]], 80

; CHECK-NEXT: %14 = inttoptr i32 %[[M6]] to ptr

; CHECK-NEXT: store ptr %14, ptr @goo

```
define void @foo_i8() {
entry:
%0 = load volatile i8, ptr inttoptr (i32 805874688 to ptr)
%1 = load volatile
i8, ptr inttoptr (i32 805874692 to ptr)
%2 = load volatile i8, ptr inttoptr (i32 805874719 to ptr)
%3 = load volatile i8, ptr inttoptr (i32 805874720 to ptr)
%4 = load volatile i8, ptr inttoptr (i32 805874727 to ptr)
store i8 %4, ptr inttoptr(i32 805873688 to ptr)
store i8 %3, ptr inttoptr(i32 805873719 to ptr)
store i8 %2, ptr inttoptr(i32 805873720 to ptr)
store i8 %1, ptr inttoptr(i32 805873727 to ptr)
store ptr inttoptr(i32 805874800 to ptr), ptr @goo
ret void
}
```

; Check that for i16 type, the maximum legal offset is 62.

; CHECK: foo_i16

; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874752 to i32

; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32

; CHECK: %0 = inttoptr i32 %[[C2]] to ptr

; CHECK-NEXT: %1 = load volatile i16, ptr %0, align 2

; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4

; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to ptr

; CHECK-NEXT: %3 = load volatile i16, ptr %2, align 2

; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add

i32 %[[C2]], 32

; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to ptr

; CHECK-NEXT: %5 = load volatile i16, ptr %4, align 2

; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C2]], 62

; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to ptr

; CHECK-NEXT: %7 = load volatile i16, ptr %6, align 2

; CHECK-NEXT: %8 = inttoptr i32 %[[C1]] to ptr

; CHECK-NEXT: %9 = load volatile i16, ptr %8, align 2

; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 22

; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to ptr

; CHECK-NEXT: %11 = load volatile i16, ptr %10, align 2

define void @foo_i16() {

entry:

%0 =load volatile i16, ptr inttoptr (i32 805874688 to ptr), align 2

%1 = 10 volatile i16, ptr inttoptr (i32 805874692 to ptr), align 2

%2 =load volatile i16, ptr inttoptr (i32 805874720 to ptr), align 2

%3 = load volatile i16, ptr inttoptr (i32 805874750 to ptr), align 2

%4 = load volatile i16, ptr inttoptr (i32 805874752 to ptr), align 2

%5 = load volatile i16, ptr inttoptr (i32 805874774 to ptr), align

```
2
ret void
}
```

```
; Check that for i32 type, the maximum legal offset is 124.
; CHECK: foo_i32
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to ptr
; CHECK-NEXT: %1 = load volatile i32, ptr %0, align 4
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to ptr
; CHECK-NEXT: %3 = load volatile i32, ptr %2, align 4
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 124
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to ptr
; CHECK-NEXT: %5 = load volatile i32, ptr %4, align 4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to ptr
; CHECK-NEXT: %7 = load volatile i32, ptr %6, align 4
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 8
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to ptr
; CHECK-NEXT: %9 = load volatile i32, ptr %8, align 4
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 12
; CHECK-NEXT: %10 = inttoptr
i32 %[[M4]] to ptr
; CHECK-NEXT: %11 = load volatile i32, ptr %10, align 4
define void @foo_i32() {
entry:
\%0 = 1000 volatile i32, ptr inttoptr (i32 805874688 to ptr), align 4
%1 = load volatile i32, ptr inttoptr (i32 805874692 to ptr), align 4
%2 = load volatile i32, ptr inttoptr (i32 805874812 to ptr), align 4
%3 = load volatile i32, ptr inttoptr (i32 805874816 to ptr), align 4
%4 = load volatile i32, ptr inttoptr (i32 805874824 to ptr), align 4
%5 = load volatile i32, ptr inttoptr (i32 805874828 to ptr), align 4
ret void
}
                      _____
clang-tidy High-Integrity C++ Files
```

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Any file referencing a High-Integrity C++ Coding guideline:

HIC++ Coding Standard as created by PRQA.

Please see http://www.codingstandard.com/section/conditions-of-use/ for more information.

; RUN: llc -march=hexagon < %s ; REQUIRES: asserts

; The two loads based on %struct.0, loading two different data types ; cause LSR to assume type "void" for the memory type. This would then ; cause an assert in isLegalAddressingMode. Make sure we no longer crash.

```
target triple = "hexagon"
```

```
%struct.0 = type { ptr, i8, %union.anon.0 }
%union.anon.0 = type { ptr }
```

define hidden fastcc void @fred() unnamed_addr #0 {
 entry:

br i1 undef, label % while.end, label % while.body.lr.ph

```
while.body.lr.ph:
br label %while.body
```

; preds = %entry

; preds = % while.body

```
while.body: ; preds = %exit.2, %while.body.lr.ph
%lsr.iv = phi ptr [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
switch i32 undef, label %exit [
i32 1, label %sw.bb.i
i32 2, label %sw.bb3.i
```

```
]
```

```
sw.bb.i:
unreachable
```

```
; preds = % while.body
```

```
unreachable
```

sw.bb3.i:

```
exit:
```

```
; preds = % while.body
switch i32 undef, label %exit.2 [
i32 1, label %sw.bb.i17
i32 2, label %sw.bb3.i20
```

```
]
```

```
sw.bb.i17: ; preds = %.exit
%0 = load i32, ptr %lsr.iv, align 4
unreachable
```

```
sw.bb3.i20: ; preds = %exit
%1 = load ptr, ptr %lsr.iv, align 4
unreachable
```

```
exit.2: ; preds = % exit
```

%cgep22 = getelementptr %struct.0, ptr %lsr.iv, i32 1 br label %while.body

```
while.end: ; preds = %entry
ret void
}
```

attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" } ; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --include-generatedfuncs

```
; RUN: opt -S -passes=verify,
iroutliner -ir-outlining-no-cost <\%\,s | FileCheck \%\,s
```

; This test checks that debug info is recognized as able to be extracted along

; with the other instructions, but is not included in the consolidated function.

define void @function1() !dbg !6 {

entry:

%a = alloca i32, align 4, !dbg !17

call void @llvm.dbg.value(metadata ptr %a, metadata !9, metadata !DIExpression()), !dbg !17 %b = alloca i32, align 4, !dbg !18

call void @llvm.dbg.value(metadata ptr %b, metadata !11, metadata !DIExpression()), !dbg !18 %c = alloca i32, align 4, !dbg !19

```
call void @llvm.dbg.value(metadata ptr %c, metadata !12, metadata !DIExpression()), !dbg !19 store i32 2, ptr %a, align 4, !dbg !20
```

```
store i32 3, ptr %b, align 4, !dbg !21
```

```
store i32 4, ptr %c, align 4, !dbg !22
```

```
%al = load i32, ptr %a, align 4, !dbg !23
```

call void @llvm.dbg.value(metadata i32 %al,

metadata !13, metadata !DIExpression()), !dbg !23

```
%bl = load i32, ptr %b, align 4, !dbg !24
```

call void @llvm.dbg.value(metadata i32 %bl, metadata !15, metadata !DIExpression()), !dbg !24 %cl = load i32, ptr %c, align 4, !dbg !25

call void @llvm.dbg.value(metadata i32 %cl, metadata !16, metadata !DIExpression()), !dbg !25 ret void, !dbg !26

}

define void @function2() !dbg !27 {
entry:

%a = alloca i32, align 4, !dbg !35

call void @llvm.dbg.value(metadata ptr %a, metadata !29, metadata !DIExpression()), !dbg !35 %b = alloca i32, align 4, !dbg !36

```
call void @llvm.dbg.value(metadata ptr %b, metadata !30, metadata !DIExpression()), !dbg !36 %c = alloca i32, align 4, !dbg !37
```

```
call void @llvm.dbg.value(metadata ptr %c, metadata !31, metadata !DIExpression()), !dbg !37 store i32 2, ptr %a, align 4, !dbg !38
```

```
store i32 3, ptr %b, align 4, !dbg !39
```

```
store i32 4, ptr %c, align 4, !dbg !40
```

```
%al = load i32, ptr %a, align 4, !dbg !41
```

call void @llvm.dbg.value(metadata i32 %al, metadata !32, metadata !DIExpression()), !dbg !41 %bl = load i32, ptr %b, align 4, !dbg !42 call void @llvm.dbg.value(metadata i32 %bl, metadata !33, metadata !DIExpression()), !dbg !42 %cl = load i32, ptr %c, align 4, !dbg !43 call void @llvm.dbg.value(metadata i32 %cl, metadata !34, metadata !DIExpression()), !dbg !43 ret void, !dbg !44 }

; Function Attrs: nounwind readnone speculatable willreturn declare void @llvm.dbg.value(metadata, metadata, metadata) #0

attributes #0 = { nounwind readnone speculatable willreturn }

!llvm.dbg.cu = !{ !0} !llvm.debugify = !{ !3, !4} !llvm.module.flags = !{ !5}

!0 = distinct !DICompileUnit(language: DW_LANG_C, file: !1, producer: "debugify", isOptimized: true, runtimeVersion: 0, emissionKind: FullDebug, enums: !2)

- !1 = !DIFile(filename: "legal-debug.ll", directory: "/")
- $!2 = !{}$
- $!3 = !{i32 20}$
- !4 = !{i32 12}
- !5 = !{i32 2, !"Debug Info Version", i32 3}

!6 = distinct !DISubprogram(name: "function1", linkageName: "function1", scope:

null, file: !1, line: 1, type: !7, scopeLine: 1, spFlags: DISPFlagDefinition | DISPFlagOptimized, unit: !0, retainedNodes: !8)

- !7 = !DISubroutineType(types: !2)
- !8 = !{!9, !11, !12, !13, !15, !16}
- !9 = !DILocalVariable(name: "1", scope: !6, file: !1, line: 1, type: !10)
- !10 = !DIBasicType(name: "ty64", size: 64, encoding: DW_ATE_unsigned)
- !11 = !DILocalVariable(name: "2", scope: !6, file: !1, line: 2, type: !10)
- !12 = !DILocalVariable(name: "3", scope: !6, file: !1, line: 3, type: !10)
- !13 = !DILocalVariable(name: "4", scope: !6, file: !1, line: 7, type: !14)
- !14 = !DIBasicType(name: "ty32", size: 32, encoding: DW_ATE_unsigned)
- !15 = !DILocalVariable(name: "5", scope: !6, file: !1, line: 8, type: !14)
- !16 = !DILocalVariable(name: "6", scope: !6, file: !1, line: 9, type: !14)
- !17 = !DILocation(line: 1, column: 1, scope: !6)
- !18 = !DILocation(line: 2, column: 1, scope: !6)
- !19 = !DILocation(line: 3, column: 1, scope: !6)
- !20 = !DILocation(line: 4, column: 1, scope: !6)
- !21 = !DILocation(line:
- 5, column: 1, scope: !6)
- !22 = !DILocation(line: 6, column: 1, scope: !6)
- !23 = !DILocation(line: 7, column: 1, scope: !6)
- !24 = !DILocation(line: 8, column: 1, scope: !6)

```
!25 = !DILocation(line: 9, column: 1, scope: !6)
```

```
!26 = !DILocation(line: 10, column: 1, scope: !6)
```

!27 = distinct !DISubprogram(name: "function2", linkageName: "function2", scope: null, file: !1, line: 11, type: !7, scopeLine: 11, spFlags: DISPFlagDefinition | DISPFlagOptimized, unit: !0, retainedNodes: !28)

```
!28 = !{!29, !30, !31, !32, !33, !34}
```

- !29 = !DILocalVariable(name: "7", scope: !27, file: !1, line: 11, type: !10)
- !30 = !DILocalVariable(name: "8", scope: !27, file: !1, line: 12, type: !10)
- !31 = !DILocalVariable(name: "9", scope: !27, file: !1, line: 13, type: !10)
- !32 = !DILocalVariable(name: "10", scope: !27, file: !1, line: 17, type: !14)
- !33 = !DILocalVariable(name: "11", scope: !27, file: !1, line: 18, type: !14)
- !34 = !DILocalVariable(name: "12", scope: !27, file: !1, line: 19, type: !14)

!35 = !DILocation(line:

```
11, column: 1, scope: !27)
```

- !36 = !DILocation(line: 12, column: 1, scope: !27)
- !37 = !DILocation(line: 13, column: 1, scope: !27)
- !38 = !DILocation(line: 14, column: 1, scope: !27)
- !39 = !DILocation(line: 15, column: 1, scope: !27)
- !40 = !DILocation(line: 16, column: 1, scope: !27)
- !41 = !DILocation(line: 17, column: 1, scope: !27)
- !42 = !DILocation(line: 18, column: 1, scope: !27)
- !43 = !DILocation(line: 19, column: 1, scope: !27)
- !44 = !DILocation(line: 20, column: 1, scope: !27)
- ; CHECK-LABEL: @function1(

; CHECK-NEXT: entry:

; CHECK-NEXT: [[A:%.*]] = alloca i32, align 4, !dbg [[DBG17:![0-9]+]]

```
; CHECK-NEXT: call void @llvm.dbg.value(metadata ptr [[A]], metadata [[META9:![0-9]+]], metadata
```

!DIExpression()), !dbg [[DBG17]]

```
; CHECK-NEXT: [[B:%.*]] = alloca i32, align 4, !dbg [[DBG18:![0-9]+]]
```

```
; CHECK-NEXT: call void @llvm.dbg.value(metadata ptr [[B]], metadata [[META11:![0-9]+]], metadata !DIExpression()), !dbg [[DBG18]]
```

```
; CHECK-NEXT: [[C:%.*]] = alloca
```

i32, align 4, !dbg [[DBG19:![0-9]+]]

```
; CHECK-NEXT: call void @llvm.dbg.value(metadata ptr [[C]], metadata [[META12:![0-9]+]], metadata !DIExpression()), !dbg [[DBG19]]
```

```
; CHECK-NEXT: call void @outlined_ir_func_0(ptr [[A]], ptr [[B]], ptr [[C]]), !dbg [[DBG20:![0-9]+]]
```

```
; CHECK-NEXT: ret void, !dbg [[DBG21:![0-9]+]]
```

;

; CHECK-LABEL: @function2(

; CHECK-NEXT: entry:

; CHECK-NEXT: [[A:%.*]] = alloca i32, align 4, !dbg [[DBG30:![0-9]+]]

; CHECK-NEXT: call void @llvm.dbg.value(metadata ptr [[A]], metadata [[META24:![0-9]+]], metadata !DIExpression()), !dbg [[DBG30]]

; CHECK-NEXT: [[B:%.*]] = alloca i32, align 4, !dbg [[DBG31:![0-9]+]]

```
; CHECK-NEXT: call void @llvm.dbg.value(metadata ptr [[B]], metadata [[META25:![0-9]+]], metadata !DIExpression()), !dbg [[DBG31]]
```

; CHECK-NEXT: [[C:%.*]] = alloca i32, align 4, !dbg [[DBG32:![0-9]+]]

; CHECK-NEXT: call void @llvm.dbg.value(metadata ptr [[C]], metadata [[META26:![0-9]+]], metadata

```
!DIExpression()), !dbg [[DBG32]]
```

```
CHECK-NEXT: call void @outlined_ir_func_0(ptr [[A]], ptr [[B]], ptr [[C]]), !dbg [[DBG33:![0-9]+]]
; CHECK-NEXT: ret void, !dbg [[DBG34:![0-9]+]]
; CHECK: @outlined_ir_func_0(ptr [[TMP0:%.*]], ptr [[TMP1:%.*]], ptr [[TMP2:%.*]])
; CHECK:
             entry_to_outline:
; CHECK-NEXT: store i32 2, ptr [[TMP0]], align 4
; CHECK-NEXT: store i32 3, ptr [[TMP1]], align 4
; CHECK-NEXT: store i32 4, ptr [[TMP2]], align 4
; CHECK-NEXT: [[AL:%.*]] = load i32, ptr [[TMP0]], align 4
; CHECK-NEXT: [[BL:%.*]] = load i32, ptr [[TMP1]], align 4
; CHECK-NEXT: [[CL:%.*]] = load i32, ptr [[TMP2]], align 4
; CHECK-NEXT: br label [[ENTRY_AFTER_OUTLINE_EXITSTUB:%.*]]
; RUN: opt < %s -passes=argpromotion -S | FileCheck %s
; CHECK-LABEL: define i32 @foo() #0 {
; CHECK-NEXT: %.val = load <32 x half>, ptr undef, align 4
; CHECK-NEXT: call void @bar(<32 x half> %.val)
; CHECK-NEXT: ret i32 0
; CHECK-NEXT: }
; CHECK-LABEL: define internal void @bar(<32 x half> %.0.val) #0 {
; CHECK-NEXT:
                   ret void
; CHECK-NEXT: }
; CHECK: attributes #0 = { uwtable "min-legal-vector-width"="512" }
define i32 @foo() #0 {
call void @bar(ptr undef)
ret i32 0
}
define internal void @bar(ptr) #0 {
\%2 = \text{load} < 32 \text{ x half}, ptr \%0, align 4
ret void
}
attributes #0 = { uwtable "min-legal-vector-width"="0" }
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```

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! RUN: %python %S/../test_errors.py %s %flang -fopenmp -Werror

! OpenMP Version 5.0

! 2.19.4.4 firstprivate Clause

! 2.19.4.5 lastprivate Clause
! 2.19.6.1 copyin Clause
! 2.19.6.2 copyprivate Clause
! If the list item is a polymorphic variable with the allocatable attribute,
! the behavior is unspecified.

subroutine firstprivate()
class(*), allocatable, save :: x

!PORTABILITY: If a polymorphic variable with allocatable attribute 'x' is in FIRSTPRIVATE clause, the behavior is unspecified !\$omp parallel firstprivate(x) call sub() !\$omp end parallel

end

subroutine lastprivate()
class(*), allocatable, save :: x

!PORTABILITY: If a polymorphic variable with allocatable attribute 'x' is in LASTPRIVATE clause, the behavior
is unspecified
!\$omp do lastprivate(x)
do i = 1, 10
call sub()

enddo !\$omp end do

end

subroutine copyin()
class(*), allocatable, save :: x
!\$omp threadprivate(x)

!PORTABILITY: If a polymorphic variable with allocatable attribute 'x'
is in COPYIN clause, the behavior is unspecified
!\$omp parallel copyin(x)
 call sub()
!\$omp end parallel

end

subroutine copyprivate()
class(*), allocatable, save :: x
!\$omp threadprivate(x)

PORTABILITY: If a polymorphic variable with allocatable attribute 'x' is in COPYPRIVATE clause, the behavior is unspecified

!\$omp single copyprivate(x)
 call sub()
!\$omp end single

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py

; RUN: llc -march=amdgcn -mcpu=fiji < % s | FileCheck -enable-var-scope --check-prefixes=GCN,GCN-SAFE,VI,VI-SAFE % s

; RUN: llc -enable-no-signed-zeros-fp-math -march=amdgcn -mcpu=fiji < %s | FileCheck -enable-var-scope -- check-prefixes=GCN,GCN-NSZ,VI,VI-NSZ %s

; -----; rcp tests

define half @v_fneg_rcp_f16(half %a) #0 {

; GCN-LABEL: v_fneg_rcp_f16:

```
; GCN: ; %bb.0:
```

; GCN-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)

; GCN-NEXT: v_rcp_f16_e64 v0, -v0

; GCN-NEXT: s_setpc_b64 s[30:31]

%rcp = call half @llvm.amdgcn.rcp.f16(half %a)

%fneg = fneg half %rcp

ret half %fneg

```
}
```

define half @v_fneg_rcp_fneg_f16(half %a) #0 {

```
; GCN-LABEL: v_fneg_rcp_fneg_f16:
         ; %bb.0:
; GCN:
; GCN-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; GCN-NEXT:
  v_rcp_f16_e32 v0, v0
; GCN-NEXT: s_setpc_b64 s[30:31]
\% fneg.a = fneg half %a
%rcp = call half @llvm.amdgcn.rcp.f16(half %fneg.a)
%fneg = fneg half %rcp
ret half % fneg
}
define { half, half } @v_fneg_rcp_store_use_fneg_f16(half %a) #0 {
; GCN-LABEL: v_fneg_rcp_store_use_fneg_f16:
; GCN:
        ; %bb.0:
; GCN-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; GCN-NEXT: v_rcp_f16_e32 v2, v0
; GCN-NEXT: v_xor_b32_e32 v1, 0x8000, v0
; GCN-NEXT: v_mov_b32_e32 v0, v2
; GCN-NEXT: s_setpc_b64 s[30:31]
\% fneg.a = fneg half %a
%rcp = call half @llvm.amdgcn.rcp.f16(half %fneg.a)
%fneg = fneg half %rcp
%insert.0 = insertvalue { half, half } poison, half %fneg, 0
%insert.1 = insertvalue { half, half } %insert.0, half %fneg.a, 1
ret { half, half } %insert.1
}
define { half, half } @v_fneg_rcp_multi_use_fneg_f16(half %a, half %c) #0 {
; GCN-LABEL: v_fneg_rcp_multi_use_fneg_f16:
; GCN:
          ; %bb.0:
; GCN-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; GCN-NEXT:
  v_rcp_f16_e32 v2, v0
; GCN-NEXT: v_mul_f16_e64 v1, -v0, v1
```

```
; GCN-NEXT: v_mov_b32_e32 v0, v2
; GCN-NEXT: s_setpc_b64 s[30:31]
%fneg.a = fneg half %a
%rcp = call half @llvm.amdgcn.rcp.f16(half %fneg.a)
%fneg = fneg half %rcp
%use1 = fmul half %fneg.a, %c
%insert.0 = insertvalue { half, half } poison, half %fneg, 0
%insert.1 = insertvalue { half, half } %insert.0, half %use1, 1
ret { half, half } %insert.1
}
```

```
; sin tests
```

_____ define half @v_fneg_amdgcn_sin_f16(half %a) #0 { ; GCN-LABEL: v_fneg_amdgcn_sin_f16: ; %bb.0: ; GCN: ; GCN-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0) ; GCN-NEXT: v sin f16 e64 v0, -v0 ; GCN-NEXT: s_setpc_b64 s[30:31] % sin = call half @llvm.amdgcn.sin.f16(half %a) % fneg = fneg half % sin ret half %fneg } :-----vintrp tests define { float, float } @v_fneg_interp_p1_f16(float %a, float %b) #0 { ; SI-LABEL: v_fneg_interp_p1_f16: ; %bb.0: ; SI: ; SI-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0) ; SI-NEXT: v_mul_f16_e64 v1, v0, -v1 ; SI-NEXT: s mov b32 m0, 0 ; SI-NEXT: v_interp_p1_f16 v0, v1, attr0.x ; SI-NEXT: v_interp_p1_f16 v1, v1, attr0.y ; SI-NEXT: s_setpc_b64 s[30:31] ; GCN-LABEL: v_fneg_interp_p1_f16: ; GCN: ; %bb.0: ; GCN-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0) ; GCN-NEXT: v_mul_f32_e64 v1, v0, -v1 ; GCN-NEXT: s_mov_b32 m0, 0 ; GCN-NEXT: s_setreg_imm32_b32 hwreg(HW_REG_MODE, 2, 2), 3 ; GCN-NEXT: v_interp_p1ll_f16 v0, v1, attr0.x ; GCN-NEXT: v_interp_p1ll_f16 v1, v1, attr0.y ; GCN-NEXT: s_setpc_b64 s[30:31] %mul = fmul float %a, %b %fneg = fneg float %mul %intrp0 = call float @llvm.amdgcn.interp.p1.f16(float %fneg, i32 0, i32 0, i1 false, i32 0) %intrp1 = call float @llvm.amdgcn.interp.p1.f16(float %fneg, i32 1, i32 0, i1 false, i32 0) %insert.0 = insertvalue { float, float } poison, float %intrp0, 0 %insert.1 = insertvalue { float, float } %insert.0, float %intrp1, 1 ret { float, float } % insert.1 }

define { half, half } @v_fneg_interp_p2_f16(float %a, float %b) #0 {

```
; SI-LABEL: v_fneg_interp_p2_f16:
     ; %bb.0:
; SI:
; SI-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; SI-NEXT: v_mul_f16_e64 v2, v0, -v1
; SI-NEXT: v_mov_b32_e32 v1, 4.0
; SI-NEXT: v_mov_b32_e32 v0, 4.0
; SI-NEXT: s mov b32 m0, 0
; SI-NEXT: v_interp_p2_f16 v0, v2, attr0.x
; SI-NEXT: v_interp_p2_f16 v1, v2, attr0.y
; SI-NEXT: s_setpc_b64 s[30:31]
; GCN-LABEL: v_fneg_interp_p2_f16:
; GCN:
         ; %bb.0:
; GCN-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
; GCN-NEXT: v_mul_f32_e64 v1, v0, -v1
; GCN-NEXT: v_mov_b32_e32 v2, 4.0
; GCN-NEXT: s_mov_b32 m0, 0
; GCN-NEXT: s setreg imm32 b32
hwreg(HW_REG_MODE, 2, 2), 3
; GCN-NEXT: v_interp_p2_f16 v0, v1, attr0.x, v2
; GCN-NEXT: v_interp_p2_f16 v1, v1, attr0.y, v2
; GCN-NEXT: s_setpc_b64 s[30:31]
% mul = fmul float % a, % b
\%fneg = fneg float \%mul
%intrp0 = call half @llvm.amdgcn.interp.p2.f16(float 4.0, float %fneg, i32 0, i32 0, i1 false, i32 0)
%intrp1 = call half @llvm.amdgcn.interp.p2.f16(float 4.0, float %fneg, i32 1, i32 0, i1 false, i32 0)
%insert.0 = insertvalue { half, half } poison, half %intrp0, 0
%insert.1 = insertvalue { half, half } %insert.0, half %intrp1, 1
ret { half, half } %insert.1
}
: ------
```

; arithmetic.fence tests

;-----

; FIXME: Legalization/promote is broken define half @v_fneg_arithmetic_fence_f16(half %a) #0 { ; GCN-LABEL: v_fneg_arithmetic_fence_f16: ; GCN: ; %bb.0: ; GCN-NEXT: ;ARITH_FENCE ; GCN-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0) ; GCN-NEXT: v_xor_b32_e32 v0, 0x8000, v0 ; GCN-NEXT: s_setpc_b64 s[30:31] %fence = call half @llvm.arithmetic.fence.f16(half %a) %fneg = fneg half %fence ret half %fneg } define half @v_fneg_arithmetic_fence_fmul_f16(half %a, half %b) #0 {

```
; GCN-LABEL: v_fneg_arithmetic_fence_fmul_f16:
```

```
; GCN: ; %bb.0:
```

```
; GCN-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
```

```
; GCN-NEXT: v_mul_f16_e32 v0, v0, v1
```

```
; GCN-NEXT: ;ARITH_FENCE
```

```
; GCN-NEXT: v_xor_b32_e32 v0, 0x8000, v0
```

```
; GCN-NEXT: s_setpc_b64 s[30:31]
```

```
%mul = fmul half %a, %b
```

% fence = call half @llvm.arithmetic.fence.f16(half %mul)

```
%fneg = fneg half %fence
```

ret half %fneg

```
}
```

declare half @llvm.amdgcn.rcp.f16(half) #1

declare half @llvm.amdgcn.sin.f16(half) #1

declare half @llvm.arithmetic.fence.f16(half) #1

declare float @llvm.amdgcn.interp.p1.f16(float, i32, i32, i1, i32) #0

declare half @llvm.amdgcn.interp.p2.f16(float, float, i32, i32, i1, i32) #0

```
attributes #0 = { nounwind
```

"denormal-fp-math-f32"="preserve-sign,preserve-sign" }

attributes #1 = { nounwind readnone }

attributes #2 = { nounwind "unsafe-fp-math"="true" }

```
attributes #3 = { nounwind "no-signed-zeros-fp-math"="true" }
```

attributes #4 = { nounwind "amdgpu-ieee"="false" "denormal-fp-math-f32"="preserve-sign,preserve-sign" }

;; NOTE: These prefixes are unused and the list is autogenerated. Do not add tests below this line:

; GCN-NSZ: {{.*}}

```
; GCN-SAFE: {{.*}}
```

; VI: {{.*}}

; VI-NSZ: {{.*}}

; VI-SAFE: {{.*}}

; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature -- check-attributes --check-globals

```
; RUN: opt -aa-pipeline=basic-aa -passes=attributor -attributor-manifest-internal -attributor-max-iterations-verify - attributor-annotate-decl-cs -attributor-max-iterations=10 -S < \%s | FileCheck \%s --check-prefixes=CHECK,TUNIT ; RUN: opt -aa-pipeline=basic-aa -passes=attributor-cgscc -attributor-manifest-internal -attributor-annotate-decl-cs - S < \%s | FileCheck \%s --check-prefixes=CHECK,CGSCC
```

; Test that we only promote arguments when the caller/callee have compatible

; function attrubtes.

target triple = "x86_64-unknown-linux-gnu"

; This should promote

define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr %arg, ptr readonly %arg1) #0 {

;

; CHECK: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable

```
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
```

CHECK-SAME: (ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR0:[0-9]+]] {

```
; CHECK-NEXT: bb:
```

```
; CHECK-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; CHECK-NEXT: store <8 x i64> [[TMP0]], ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, ptr % arg1
store <8 x i64> %tmp, ptr %arg
ret void
}
```

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr %arg) #0 {

;

; TUNIT: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable

```
; TUNIT-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
```

```
; TUNIT-SAME: (ptr nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR0]] {
```

; TUNIT-NEXT: bb:

; TUNIT-NEXT:

[[TMP:%.*]] = alloca <8 x i64>, align 32

; TUNIT-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32

; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 32 dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5:[0-9]+]]

; TUNIT-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64

```
; TUNIT-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR6:[0-9]+]]
```

; TUNIT-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64

; TUNIT-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2

; TUNIT-NEXT: ret void

```
;
```

; CGSCC: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable

; CGSCC-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512

; CGSCC-SAME: (ptr nocapture

nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]]) #[[ATTR0]] {

; CGSCC-NEXT: bb:

; CGSCC-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

; CGSCC-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32

; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 64

```
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5:[0-9]+]]
; CGSCC-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; CGSCC-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr
noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]])
#[[ATTR6:[0-9]+]]
; CGSCC-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64
; CGSCC-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CGSCC-NEXT: ret void
:
bb:
\%tmp = alloca <8 x i64>, align 32
\%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr
align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}
; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr %arg, ptr
readonly %arg1) #1 {
; CHECK: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite)
uwtable
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR1:[0-9]+]] {
; CHECK-NEXT: bb:
; CHECK-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; CHECK-NEXT: store <8 x i64> [[TMP0]], ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1_PRIV]], align
64
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64
; CHECK-NEXT: ret void
·
bb:
\%tmp = load <8 x i64>, ptr % arg1
store <8 x i64> % tmp, ptr % arg
ret void
}
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr % arg) #1 {
; TUNIT: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite)
uwtable
```

```
; TUNIT-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
```

```
; TUNIT-SAME: (ptr nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR1]] {
```

; TUNIT-NEXT: bb:

; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

; TUNIT-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32

; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 32 dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]

; TUNIT-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64

; TUNIT-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr

noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTP61]

#[[ATTR6]]

; TUNIT-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64

; TUNIT-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2

; TUNIT-NEXT: ret void

```
;
```

; CGSCC: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable

; CGSCC-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256

; CGSCC-SAME: (ptr nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]]) #[[ATTR1]] {

; CGSCC-NEXT: bb:

; CGSCC-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

; CGSCC-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32

; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]

; CGSCC-NEXT:

```
[[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
```

; CGSCC-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr

noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR6]]

; CGSCC-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64

; CGSCC-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2

; CGSCC-NEXT: ret void

```
,
bb:
```

```
\%tmp = alloca <8 x i64>, align 32
```

```
\%tmp2 = alloca <8 x i64>, align 32
```

call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)

 $call \ fastcc \ void \ @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr \ \% tmp2, ptr \ \% tmp))$

%tmp4 = load <8 x i64>, ptr %tmp2, align 32

store <8 x i64> %tmp4, ptr %arg, align 2

ret void

}

; This should promote

define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr %arg, ptr readonly %arg1) #1 {

;

; CHECK: Function Attrs: inlinehint nofree

```
norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR1]] {
; CHECK-NEXT: bb:
; CHECK-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; CHECK-NEXT: store <8 x i64> [[TMP0]], ptr [[ARG1 PRIV]], align 64
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64
: CHECK-NEXT: ret void
bb:
\%tmp = load <8 x i64>, ptr % arg1
store <8 x i64> % tmp, ptr % arg
ret void
}
define void @avx512 legal512 prefer512 call avx512 legal512 prefer256(ptr % arg) #0 {
; TUNIT: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite)
uwtable
; TUNIT-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
TUNIT-SAME: (ptr nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR0]] {
; TUNIT-NEXT: bb:
; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 32
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; TUNIT-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; TUNIT-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr
noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]])
#[[ATTR6]]
; TUNIT-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64
; TUNIT-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; TUNIT-NEXT: ret void
; CGSCC: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite)
uwtable
; CGSCC-LABEL:
define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CGSCC-SAME: (ptr nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
#[[ATTR0]] {
; CGSCC-NEXT: bb:
; CGSCC-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
```

```
; CGSCC-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; CGSCC-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr
noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]])
#[[ATTR6]]
; CGSCC-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64
; CGSCC-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CGSCC-NEXT: ret void
bb:
%tmp
= alloca <8 x i64>, align 32
\%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}
; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr % arg, ptr
readonly %arg1) #0 {
; CHECK: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite)
uwtable
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR0]] {
; CHECK-NEXT: bb:
; CHECK-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; CHECK-NEXT: store <8 x i64> [[TMP0]], ptr [[ARG1_PRIV]],
align 64
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64
; CHECK-NEXT: ret void
:
bb:
\%tmp = load <8 x i64>, ptr % arg1
store <8 x i64> %tmp, ptr %arg
ret void
}
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr % arg) #1 {
; TUNIT: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite)
uwtable
```

```
; TUNIT-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
```

```
; TUNIT-SAME: (ptr nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR1]] {
```

; TUNIT-NEXT: bb:

; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

; TUNIT-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32

; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 32 dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]

; TUNIT-NEXT: [[TMP0:%.*]] = load

<8 x i64>, ptr [[TMP]], align 64

; TUNIT-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr

noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR6]]

; TUNIT-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64

; TUNIT-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2

; TUNIT-NEXT: ret void

;

; CGSCC: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable

; CGSCC-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512

; CGSCC-SAME: (ptr nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]]) #[[ATTR1]] {

; CGSCC-NEXT: bb:

; CGSCC-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

; CGSCC-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32

; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)

[[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]

; CGSCC-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64

; CGSCC-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr

noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR6]]

; CGSCC-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64

; CGSCC-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2

; CGSCC-NEXT: ret void

```
bb:
```

%tmp = alloca <8 x i64>, align 32

%tmp2 = alloca <8 x i64>, align 32

call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)

 $call \ fastcc \ void \ @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr \ \% tmp2, ptr \ \% tmp))$

%tmp4 = load <8 x i64>, ptr %tmp2, align 32

store <8 x i64> %tmp4, ptr %arg, align 2

ret void

}

; This should not promote

define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr %arg, ptr readonly %arg1) #1 {

;

; CHECK: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite)

uwtable

```
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], ptr noalias nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR1]] {
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1]], align 64
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64
; CHECK-NEXT: ret void
bb:
\%tmp = load <8 x i64>, ptr % arg1
store < 8 \times 164 > \% tmp, ptr % arg
ret void
}
define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr % arg) #2 {
; TUNIT: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite)
uwtable
; TUNIT-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
TUNIT-SAME: (ptr nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR2:[0-9]+]] {
; TUNIT-NEXT: bb:
; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 32
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; TUNIT-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr
noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], ptr noalias nocapture
nofree noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR6]]
; TUNIT-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64
; TUNIT-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; TUNIT-NEXT: ret void
; CGSCC: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem:
readwrite) uwtable
; CGSCC-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CGSCC-SAME: (ptr nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
#[[ATTR2:[0-9]+]] {
; CGSCC-NEXT: bb:
; CGSCC-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; CGSCC-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr
noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], ptr noalias nocapture
```

```
; CGSCC-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64
; CGSCC-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align
2
; CGSCC-NEXT: ret void
bb:
\%tmp = alloca <8 x i64>, align 32
\%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}
; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr %arg, ptr
readonly %arg1) #2 {
; CHECK: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite)
uwtable
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], ptr noalias nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR2:[0-9]+]] {
; CHECK-NEXT:
 bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1]], align 64
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64
; CHECK-NEXT: ret void
·
bb:
\%tmp = load <8 x i64>, ptr % arg1
store <8 x i64> %tmp, ptr %arg
ret void
}
define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr % arg) #1 {
; TUNIT: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite)
uwtable
; TUNIT-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; TUNIT-SAME: (ptr nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR1]] {
; TUNIT-NEXT: bb:
; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 32
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
```

; TUNIT-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], ptr noalias nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR6]]

; TUNIT-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64

; TUNIT-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2

; TUNIT-NEXT: ret void

;

; CGSCC: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable

; CGSCC-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256

; CGSCC-SAME: (ptr nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]]) #[[ATTR1]] {

; CGSCC-NEXT: bb:

; CGSCC-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

; CGSCC-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32

; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP]],

i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]

; CGSCC-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], ptr noalias nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR6]]

; CGSCC-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64

; CGSCC-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2

; CGSCC-NEXT: ret void

```
;
```

bb:

```
\%tmp = alloca <8 x i64>, align 32
```

%tmp2 = alloca <8 x i64>, align 32

```
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
```

call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr %tmp2, ptr %tmp) %tmp4 = load <8 x i64>, ptr %tmp2, align 32

store <8 x i64> %tmp4, ptr %arg, align 2

ret void

}

; This should promote

```
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr %arg,
ptr readonly %arg1) #3 {
```

;

; CHECK: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable

```
; CHECK-LABEL: define { { [^@]+ } } @ callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
```

; CHECK-SAME: (ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)

```
[[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR3:[0-9]+]] {
```

; CHECK-NEXT: bb:

; CHECK-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64

```
; CHECK-NEXT: store <8 x i64> [[TMP0]], ptr [[ARG1_PRIV]], align 64
```

; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1_PRIV]], align 64

```
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64
; CHECK-NEXT: ret void
bb:
\%tmp = load <8 x i64>, ptr % arg1
store <8 x i64> % tmp, ptr % arg
ret void
}
define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr %arg) #4 {
; TUNIT: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite)
uwtable
TUNIT-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; TUNIT-SAME: (ptr nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR3]] {
; TUNIT-NEXT: bb:
; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 32
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; TUNIT-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; TUNIT-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr noalias
nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]])
#[[ATTR6]]
; TUNIT-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64
; TUNIT-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; TUNIT-NEXT: ret void
; CGSCC: Function Attrs: inlinehint nofree norecurse nosync
nounwind willreturn memory(argmem: readwrite) uwtable
; CGSCC-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CGSCC-SAME: (ptr nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])
#[[ATTR3]] {
; CGSCC-NEXT: bb:
; CGSCC-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
; CGSCC-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; CGSCC-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr noalias
nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]])
#[[ATTR6]]
; CGSCC-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64
; CGSCC-NEXT: store <8 x i64> [[TMP4]], ptr
[[ARG]], align 2
; CGSCC-NEXT: ret void
:
```

bb:

```
\%tmp = alloca <8 x i64>, align 32
\%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> % tmp4, ptr % arg, align 2
ret void
}
; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr %arg, ptr readonly
%arg1) #4 {
; CHECK: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite)
uwtable
; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR3]] {
; CHECK-NEXT: bb:
; CHECK-NEXT: [[ARG1 PRIV:%.*]] = alloca <8 x i64>, align 64
; CHECK-NEXT:
  store <8 x i64> [[TMP0]], ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1_PRIV]], align 64
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]], align 64
; CHECK-NEXT: ret void
bb:
\%tmp = load <8 x i64>, ptr % arg1
store <8 x i64> % tmp, ptr % arg
ret void
}
define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr % arg) #3 {
; TUNIT: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite)
uwtable
; TUNIT-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; TUNIT-SAME: (ptr nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR3]] {
; TUNIT-NEXT: bb:
; TUNIT-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; TUNIT-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly align 32
dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
TUNIT-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
; TUNIT-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr noalias
nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]])
```

```
#[[ATTR6]]
```

```
; TUNIT-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64
```

```
; TUNIT-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
```

; TUNIT-NEXT: ret void

```
;
```

; CGSCC: Function Attrs: inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable

; CGSCC-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256

; CGSCC-SAME: (ptr nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]])

```
#[[ATTR3]] {
```

; CGSCC-NEXT: bb:

; CGSCC-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

; CGSCC-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32

; CGSCC-NEXT: call void @llvm.memset.p0.i64(ptr noalias nocapture nofree noundef nonnull writeonly

```
align 64 dereferenceable(64) [[TMP]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR5]]
```

```
; CGSCC-NEXT: [[TMP0:%.*]] = load <8 x i64>, ptr [[TMP]], align 64
```

```
; CGSCC-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR6]]
```

; CGSCC-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 64

; CGSCC-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2

```
; CGSCC-NEXT: ret void
```

```
;
```

bb:

```
%tmp = alloca <8 x i64>, align 32
```

```
%tmp2 = alloca <8 x i64>, align 32
```

```
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
```

```
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr %tmp2, ptr %tmp)
```

```
\%tmp4 = load <8 x i64>, ptr %tmp2, align 32
```

```
store <8 x i64> %tmp4, ptr %arg, align 2
```

```
ret void
```

```
}
```

; Function Attrs: argmemonly nounwind declare void @llvm.memset.p0.i64(ptr nocapture writeonly, i8, i64, i1) #5

```
attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
```

attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }

```
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
```

```
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
```

```
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
```

```
attributes #5 = { argmemonly nounwind }
```

;.

; TUNIT: attributes #[[ATTR0]] = { inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="512" "target-features"="+avx512vl" }

; TUNIT: attributes #[[ATTR1]] = { inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx512vl" } ; TUNIT: attributes #[[ATTR2]] = { inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable "min-legal-vector-width"="256" "prefer-vector-width"="256" "target-features"="+avx512vl" } ; TUNIT: attributes #[[ATTR3]] = { inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx512vl" } ; TUNIT: attributes #[[ATTR3]] = { inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx2" } ; TUNIT: attributes #[[ATTR4:[0-9]+]] = { nocallback nofree nounwind willreturn memory(argmem: write) } ; TUNIT: attributes #[[ATTR5]] = { willreturn }

; TUNIT: attributes #[[ATTR6]] = { nofree nosync nounwind willreturn }

;.

; CGSCC: attributes #[[ATTR0]] = { inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable

"min-legal-vector-width"="512" "prefer-vector-width"="512" "target-features"="+avx512vl" }

; CGSCC: attributes #[[ATTR1]] = { inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx512vl" } ; CGSCC: attributes #[[ATTR2]] = { inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable "min-legal-vector-width"="256" "prefer-vector-width"="256" "target-features"="+avx512vl" } ; CGSCC: attributes #[[ATTR3]] = { inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx512vl" } ; CGSCC: attributes #[[ATTR3]] = { inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx512vl" } ; CGSCC: attributes #[[ATTR3]] = { inlinehint nofree norecurse nosync nounwind willreturn memory(argmem: readwrite) uwtable "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx2" } ; CGSCC: attributes #[[ATTR4:[0-9]+]] = { nocallback nofree nounwind willreturn memory(argmem: write) }

; CGSCC: attributes #[[ATTR5]] = { willreturn }

; CGSCC: attributes #[[ATTR6]] = { nounwind willreturn }

```
;.
```

; RUN: opt %s -passes=inline -S | FileCheck %s

```
define internal void @innerSmall() "min-legal-vector-width"="128" { ret void
```

}

```
define internal void @innerLarge() "min-legal-vector-width"="512" { ret void
```

}

define internal void @innerNoAttribute() {
 ret void

```
}
```

; We should not add an attribute during inlining. No attribute means unknown.

; Inlining doesn't change the fact that we don't know anything about this

; function.

```
define void @outerNoAttribute() {
```

call void @innerLarge()

```
ret void
}
```

```
define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
call void @innerLarge()
ret void
}
define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
call void @innerSmall()
ret void
}
; We should remove the attribute after inlining since the callee's
; vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
call void @innerNoAttribute()
ret void
}
; CHECK: define void @outerNoAttribute()
{
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }
; RUN: opt -mtriple=aarch64-linux-gnu -mattr=+sve -passes=scalarize-masked-mem-intrin -S < %s | FileCheck %s
; Testing that masked scatters operating on scalable vectors that are
; packed in SVE registers are not scalarized.
; CHECK-LABEL: @masked scatter nxv4i32(
; CHECK: call void @llvm.masked.scatter.nxv4i32
define void @masked_scatter_nxv4i32(<vscale x 4 x i32> %data, <vscale x 4 x ptr> %ptrs, <vscale x 4 x i1>
%masks) {
call void @llvm.masked.scatter.nxv4i32(<vscale x 4 x i32> %data, <vscale x 4 x ptr> %ptrs, i32 0, <vscale x 4 x
i1 > \% masks)
ret void
}
; Testing that masked scatters operating on scalable vectors of FP
; data that is packed in SVE registers are not scalarized.
; CHECK-LABEL: @masked_scatter_nxv2f64(
; CHECK: call void @llvm.masked.scatter.nxv2f64
define void @masked_scatter_nxv2f64(<vscale x 2 x double> %data, <vscale x 2 x ptr> % ptrs, <vscale x 2 x i1>
%masks) {
```

```
call void @llvm.masked.scatter.nxv2f64(<vscale x 2 x double>%data, <vscale x 2 x ptr>%ptrs,
```

```
i32 0, <vscale x 2 x i1> % masks)
```

ret void

}

- ; Testing that masked scatters operating on scalable vectors of FP
- ; data that is unpacked in SVE registers are not scalarized.

; CHECK-LABEL: @masked_scatter_nxv2f16(

; CHECK: call void @llvm.masked.scatter.nxv2f16

define void @masked_scatter_nxv2f16(<vscale x 2 x half> %data, <vscale x 2 x ptr> %ptrs, <vscale x 2 x i1> %masks) {

call void @llvm.masked.scatter.nxv2f16(<vscale x 2 x half> %data, <vscale x 2 x ptr> %ptrs, i32 0, <vscale x 2 x i1> %masks)

ret void

}

; Testing that masked scatters operating on 64-bit fixed vectors are

; scalarized because NEON doesn't have support for masked scatter ; instructions.

; instructions.

; CHECK-LABEL: @masked_scatter_v2f32(

; CHECK-NOT: @llvm.masked.scatter.v2f32(

define void @masked_scatter_v2f32(<2 x float> %data, <2 x ptr> %ptrs, <2 x i1> %masks) { call void @llvm.masked.scatter.v2f32(<2 x float> %data, <2 x ptr> %ptrs, i32 0, <2 x i1> %masks) ret void

}

; Testing that masked scatters operating on 128-bit

fixed vectors are

; scalarized because NEON doesn't have support for masked scatter

; instructions and because we are not targeting fixed width SVE.

; CHECK-LABEL: @masked_scatter_v4i32(

; CHECK-NOT: @llvm.masked.scatter.v4i32(

```
define void @masked_scatter_v4i32(<4 x i32> %data, <4 x ptr> %ptrs, <4 x i1> %masks) {
```

call void @llvm.masked.scatter.v4i32(<4 x i32> %data, <4 x ptr> %ptrs, i32 0, <4 x i1> %masks) ret void

}

declare void @llvm.masked.scatter.nxv4i32(<vscale x 4 x i32> %data, <vscale x 4 x ptr> %ptrs, i32 %align, <vscale x 4 x i1> %masks)

declare void @llvm.masked.scatter.nxv2f64(<vscale x 2 x double> %data, <vscale x 2 x ptr> %ptrs, i32 %align, <vscale x 2 x i1> %masks)

declare void @llvm.masked.scatter.nxv2f16(<vscale x 2 x half> %data, <vscale x 2 x ptr> %ptrs, i32 %align, <vscale x 2 x i1> %masks)

declare void @llvm.masked.scatter.v2f32(<2 x float> %data, <2 x ptr> %ptrs, i32 %align, <2 x i1> %masks) declare void @llvm.masked.scatter.v4i32(<4 x i32> %data, <4 x

ptr> %ptrs, i32 %align, <4 x i1> %masks)

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```

```
static_library("BSD-Archive") {
  output_name = "lldbPluginObjectContainerBSDArchive"
  configs += [ "//llvm/utils/gn/build:lldb_code" ]
  deps = [
    "//lldb/source/Core",
    "//lldb/source/Host",
    "//lldb/source/Symbol",
    "//llvm/lib/Support",
  ]
  sources = [ "ObjectContainerBSDArchive.cpp" ]
}
```

; RUN: opt -mtriple=aarch64-linux-gnu -mattr=+sve -passes=scalarize-masked-mem-intrin -S < %s | FileCheck %s

; Testing that masked gathers operating on scalable vectors that are ; packed in SVE registers are not scalarized.

; CHECK-LABEL: @masked_gather_nxv4i32(; CHECK: call <vscale x 4 x i32> @llvm.masked.gather.nxv4i32 define <vscale x 4 x i32> @masked_gather_nxv4i32(<vscale x 4 x ptr> %ld, <vscale x 4 x i1> %masks, <vscale x 4 x i32> %passthru) { %res = call <vscale x 4 x i32> @llvm.masked.gather.nxv4i32(<vscale x 4 x ptr> %ld, i32 0, <vscale x 4 x i1> %masks, <vscale x 4 x i32> %passthru) ret <vscale x 4 x i32> %passthru) ret <vscale x 4 x i32> %res } ; Testing that masked gathers operating on scalable vectors of FP data ; that is packed in SVE registers are not scalarized.

```
; CHECK-LABEL: @masked_gather_nxv2f64(
; CHECK: call <vscale x 2 x double> @llvm.masked.gather.nxv2f64
define <vscale x 2 x double> @masked_gather_nxv2f64(<vscale x 2 x ptr> %ld, <vscale x 2 x i1> %masks, <vscale
x 2 x double> %passthru)
{
%res = call <vscale x 2 x double> @llvm.masked.gather.nxv2f64(<vscale x 2 x ptr> %ld, i32 0, <vscale x 2 x i1>
%masks, <vscale x 2 x double> %passthru)
ret <vscale x 2 x double> %passthru)
ret <vscale x 2 x double> %res
}
```

; Testing that masked gathers operating on scalable vectors of FP data ; that is unpacked in SVE registers are not scalarized.

; CHECK-LABEL: @masked_gather_nxv2f16(; CHECK: call <vscale x 2 x half> @llvm.masked.gather.nxv2f16 define <vscale x 2 x half> @masked_gather_nxv2f16(<vscale x 2 x ptr> %ld, <vscale x 2 x i1> %masks, <vscale x 2 x half> %passthru) { %res = call <vscale x 2 x half> @llvm.masked.gather.nxv2f16(<vscale x 2 x ptr> %ld, i32 0, <vscale x 2 x i1> %masks, <vscale x 2 x half> %passthru) ret <vscale x 2 x half> %passthru) ret <vscale x 2 x half> %res }

; Testing that masked gathers operating on 64-bit fixed vectors are ; scalarized because NEON doesn't have support for masked gather

; instructions.

```
; CHECK-LABEL: @masked_gather_v2f32(
; CHECK-NOT: @llvm.masked.gather.v2f32(
define <2 x float> @masked_gather_v2f32(<2
x ptr> %ld, <2 x i1> %masks, <2 x float> %passthru) {
%res = call <2 x float> @llvm.masked.gather.v2f32(<2 x ptr> %ld, i32 0, <2 x i1> %masks, <2 x float> %passthru)
```

; Testing that masked gathers operating on 128-bit fixed vectors are

; scalarized because NEON doesn't have support for masked gather

; instructions and because we are not targeting fixed width SVE.

; CHECK-LABEL: @masked_gather_v4i32(

; CHECK-NOT: @llvm.masked.gather.v4i32(

 $define <4 \ x \ i32 > @masked_gather_v4i32(<4 \ x \ ptr> \% ld, <4 \ x \ i1 > \% masks, <4 \ x \ i32 > \% passthru) \{$

%res = call <4 x i32> @llvm.masked.gather.v4i32(<4 x ptr> %ld, i32 0, <4 x i1> %masks, <4 x i32> %passthru) ret <4 x i32> %res

```
}
```

declare <vscale x 4 x i32> @llvm.masked.gather.nxv4i32(<vscale x 4 x ptr> %ptrs, i32 %align, <vscale x 4 x i1> %masks, <vscale x 4 x i32> %passthru)

declare <vscale x 2 x double> @llvm.masked.gather.nxv2f64(<vscale x 2 x ptr> %ptrs, i32 %align, <vscale x 2 x i1> %masks, <vscale x 2 x double>

%passthru)

declare <vscale x 2 x half> @llvm.masked.gather.nxv2f16(<vscale x 2 x ptr> %ptrs, i32 %align, <vscale x 2 x i1> %masks, <vscale x 2 x half> %passthru)

declare <2 x float> @llvm.masked.gather.v2f32(<2 x ptr> %ptrs, i32 %align, <2 x i1> %masks, <2 x float> %passthru)

declare <4 x i32> @llvm.masked.gather.v4i32(<4 x ptr> %ptrs, i32 %align, <4 x i1> %masks, <4 x i32> %passthru) # RUN: llc -O0 -mtriple=m68k -start-after=prologepilog -verify-machineinstrs %s -o - | FileCheck %s

name: is-pcrel-register-operand-legal body: | bb.0.entry: ; CHECK: move.1 (0,%pc,%a0), (%a1)

; CHECK: move.1 (%a0), (0,%pc,%a1)

MOV32jk \$a1, 0, \$a0, implicit-def \$ccr

MOV32kj 0, \$a1, \$a0, implicit-def \$ccr

; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py

; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s

define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {

; CHECK-LABEL: test_sitofp_fixed:

; CHECK: ; %bb.0:

; CHECK-NEXT: sshll2.2d v4, v2, #0

```
; CHECK-NEXT: sshll2.2d v5, v0, #0
```

```
; CHECK-NEXT: sshll2.2d v6, v1, #0
```

```
; CHECK-NEXT: sshll2.2d v7, v3, #0
```

```
; CHECK-NEXT: sshll.2d v0, v0, #0
```

```
; CHECK-NEXT: sshll.2d v16, v1, #0
```

```
; CHECK-NEXT: sshll.2d v17, v2, #0
```

```
; CHECK-NEXT: sshll.2d v18, v3, #0
```

```
; CHECK-NEXT: scvtf.2d v1, v5, #6
; CHECK-NEXT: scvtf.2d v0, v0, #6
; CHECK-NEXT: scvtf.2d v3, v6, #6
; CHECK-NEXT: scvtf.2d v2, v16, #6
; CHECK-NEXT: scvtf.2d v5, v4, #6
; CHECK-NEXT: scvtf.2d v4, v17, #6
; CHECK-NEXT: scvtf.2d v7, v7, #6
; CHECK-NEXT: scvtf.2d v6, v18, #6
; CHECK-NEXT: ret
```

% flt = sitofp <16 x i32> % in to <16 x double>

%res = fdiv <16 x double> %flt, <double 64.0, double 64.0>

ret <16 x double> % res

}

; This one is small enough to satisfy isSimple, but still illegally large.

define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {

; CHECK-LABEL: test_sitofp_fixed_shortish:

; CHECK: ; %bb.0:

; CHECK-NEXT: scvtf.2d v0, v0, #6

; CHECK-NEXT: scvtf.2d v1, v1, #6

; CHECK-NEXT: ret

%flt = sitofp <4 x i64> %in to <4 x double> %res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0> ret <4 x double> %res } Ptyprocess is under the ISC license, as code derived from Pexpect. http://opensource.org/licenses/ISC

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py

; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s

;

; D31946

; Check that we dont end up with the ""LLVM ERROR: Cannot select" error.

; Additionally ensure that the output code actually put fp128 values in SSE registers.

declare fp128 @llvm.fabs.f128(fp128) declare fp128 @llvm.copysign.f128(fp128, fp128)

define fp128 @TestSelect(fp128 %a, fp128 %b) { ; CHECK-LABEL: TestSelect: ; CHECK: # %bb.0: ; CHECK-NEXT: pushq %rbx ; CHECK-NEXT: .cfi_def_cfa_offset 16 ; CHECK-NEXT: subg \$32, %rsp ; CHECK-NEXT: .cfi_def_cfa_offset 48 ; CHECK-NEXT: .cfi_offset %rbx, -16 ; CHECK-NEXT: movaps %xmm1, {{[-0-9]+}}(%r{{[sb]}}p) # 16-byte Spill ; CHECK-NEXT: movaps %xmm0, (%rsp) # 16-byte Spill ; CHECK-NEXT: callq __gttf2@PLT ; CHECK-NEXT: movl %eax, %ebx ; CHECK-NEXT: movaps (%rsp), %xmm0 # 16-byte Reload ; CHECK-NEXT: movaps {{[-0-9]+}}(%r{{[sb]}}p), %xmm1 # 16-byte Reload ; CHECK-NEXT: callq __subtf3@PLT ; CHECK-NEXT: testl %ebx, %ebx ; CHECK-NEXT: jg .LBB0_2 ; CHECK-NEXT: #%bb.1: ; CHECK-NEXT: xorps %xmm0, %xmm0 ; CHECK-NEXT: .LBB0_2: ; CHECK-NEXT: addg \$32, %rsp ; CHECK-NEXT: .cfi_def_cfa_offset 16 ; CHECK-NEXT: popq %rbx ; CHECK-NEXT: .cfi_def_cfa_offset 8 ; CHECK-NEXT: retq %cmp = fcmp ogt fp128 %a, %b % sub = fsub fp128 %a, %b ret fp128 %res } define fp128 @TestFabs(fp128 %a) { ; CHECK-LABEL: TestFabs: ; CHECK: # %bb.0: ; CHECK-NEXT: andps {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm0 ; CHECK-NEXT: retq %res = call fp128 @llvm.fabs.f128(fp128 %a) ret fp128 %res } define fp128 @TestCopysign(fp128 %a, fp128 %b) { ; CHECK-LABEL: TestCopysign:

; CHECK: # %bb.0:

```
; CHECK-NEXT: andps {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm1
; CHECK-NEXT: andps {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm0
; CHECK-NEXT:
 orps %xmm1, %xmm0
; CHECK-NEXT: retq
%res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
ret fp128 %res
}
define fp128 @TestFneg(fp128 %a) {
; CHECK-LABEL: TestFneg:
; CHECK:
          # %bb.0:
; CHECK-NEXT: pushq %rax
; CHECK-NEXT: .cfi_def_cfa_offset 16
; CHECK-NEXT: movaps %xmm0, %xmm1
; CHECK-NEXT: callq __multf3@PLT
; CHECK-NEXT: xorps { {\.?LCPI[0-9]+_[0-9]+} }(%rip), %xmm0
; CHECK-NEXT: popq %rax
; CHECK-NEXT: .cfi_def_cfa_offset 8
; CHECK-NEXT: retq
\%mul = fmul fp128 %a, %a
ret fp128 %res
}
_____
```

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py ; RUN: llc -march=amdgcn -mcpu=fiji < %s | FileCheck -check-prefixes=VI %s

; FIXME: This one should fold to rcp

define half @select_fneg_posk_src_rcp_f16(i32 %c, half %x, half %y) {

```
; VI-LABEL: select_fneg_posk_src_rcp_f16:
```

```
; VI: ; %bb.0:
```

```
; VI-NEXT: s_waitcnt vmcnt(0) expcnt(0) lgkmcnt(0)
```

```
; VI-NEXT: v_rcp_f16_e32 v1, v1
```

```
; VI-NEXT: v_mov_b32_e32 v2, 0xc000
```

```
; VI-NEXT: v_cmp_eq_u32_e32 vcc, 0, v0
```

```
; VI-NEXT: v_cndmask_b32_e32 v0, v2, v1, vcc
```

```
; VI-NEXT: v_xor_b32_e32 v0, 0x8000, v0
```

```
; VI-NEXT: s_setpc_b64 s[30:31]
```

% cmp = icmp eq i32 % c, 0

%rcp = call half @llvm.amdgcn.rcp.f16(half %x)

%fneg = fneg half %rcp

% select = select i1 % cmp, half % fneg, half 2.0

ret half %select

```
}
```

declare half @llvm.amdgcn.rcp.f16(half) #0

attributes #0 = { nocallback nofree nosync nounwind speculatable willreturn memory(none) } ; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --include-generatedfuncs

; RUN: opt -S -passes=verify, iroutliner -ir-outlining-no-cost < % s | FileCheck % s

; This test checks that we do outline indirect calls when it is not specified ; that we should not.

declare void @f1(ptr, ptr); declare void @f2(ptr, ptr); define void @function1(ptr %func) { entry: %a = alloca i32, align 4 %b = alloca i32, align 4 %c = alloca i32, align 4store i32 2, ptr %a, align 4 store i32 3, ptr %b, align 4 store i32 4, ptr %c, align 4 call void %func() %al = load i32, ptr %a %bl = load i32, ptr %b %cl = load i32, ptr %c ret void } define void @function2(ptr %func) { entry: %a = alloca i32, align 4%b = alloca i32, align 4 %c = alloca i32, align 4store i32 2, ptr %a, align 4 store i32 3, ptr %b, align 4 store i32 4, ptr %c, align 4 call void %func() %al = load i32, ptr %a %bl = load i32, ptr %b %cl = load i32, ptr %c ret void } CHECK-LABEL: @function1(; CHECK-NEXT: entry: ; CHECK-NEXT: [[A:%.*]] = alloca i32, align 4 ; CHECK-NEXT: [[B:%.*]] = alloca i32, align 4 ; CHECK-NEXT: [[C:%.*]] = alloca i32, align 4 ; CHECK-NEXT: call void @outlined_ir_func_0(ptr [[A]], ptr [[B]], ptr [[C]], ptr [[FUNC:%.*]])

```
;
; CHECK-LABEL: @function2(
; CHECK-NEXT: entry:
; CHECK-NEXT: [[A:%.*]] = alloca i32, align 4
; CHECK-NEXT: [[B:%.*]] = alloca i32, align 4
; CHECK-NEXT: [[C:%.*]] = alloca i32, align 4
; CHECK-NEXT: call void @outlined_ir_func_0(ptr [[A]], ptr [[B]], ptr [[C]], ptr [[FUNC:%.*]])
; CHECK-NEXT: ret void
; CHECK-LABEL: define internal void @outlined_ir_func_0(
; CHECK-NEXT: newFuncRoot:
; CHECK-NEXT: br label [[ENTRY_TO_OUTLINE:%.*]]
             entry_to_outline:
; CHECK:
; CHECK-NEXT: store i32 2, ptr [[TMP0:%.*]], align 4
; CHECK-NEXT: store i32 3, ptr [[TMP1:%.*]], align 4
; CHECK-NEXT: store i32 4, ptr [[TMP2:%.*]], align 4
; CHECK-NEXT:
  call void [[TMP3:%.*]]()
; CHECK-NEXT: [[AL:%.*]] = load i32, ptr [[TMP0]], align 4
; CHECK-NEXT: [[BL:%.*]] = load i32, ptr [[TMP1]], align 4
; CHECK-NEXT: [[CL:%.*]] = load i32, ptr [[TMP2]], align 4
; CHECK-NEXT: br label [[ENTRY_AFTER_OUTLINE_EXITSTUB:%.*]]
; CHECK:
             entry_after_outline.exitStub:
; CHECK-NEXT: ret void
:
; RUN: llc < %s -mtriple=s390x-linux-gnu -mcpu=zEC12 -verify-machineinstrs | FileCheck %s
; Test that early if conversion produces LOCR with operands of the right
; register classes.
define void @autogen_SD4739(ptr) {
; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
BB:
%L34 = load i8, ptr %0
%Cmp56 = icmp sgt i8 undef, %L34
br label %CF246
CF246:
                               ; preds = %CF246, %BB
%S1163 = select i1 %Cmp56, i8 %L34, i8 undef
br i1 undef, label %CF246, label %CF248
CF248:
                               ; preds = %CF248, %CF246
store i8 %Sl163, ptr %0
br label %CF248
}
```

; RUN: llc -march=hexagon -hexagon-hvx-widen=32 < %s | FileCheck %s

; Truncating a type-to-be-widenened to a legal type (v8i8).

; Check that this compiles successfully.

; CHECK-LABEL: f0:

; CHECK: dealloc_return

```
target datalayout = "e-m:e-p:32:32:32-a:0-n16:32-i64:64:64-i32:32:32-i16:16:16-i1:8:8-f32:32:32-f64:64:64-
v32:32:32-v64:64:64-v512:512:512-v1024:1024:1024-v2048:2048:2048"
target triple = "hexagon"
```

define dllexport void @f0(ptr %a0) local_unnamed_addr #0 {
 b0:

%v0 = load i8, ptr undef, align 1

%v1 = zext i8 % v0 to i16

%v2 = add i16 0, %v1

%v3 = icmp sgt i16 %v2, 1

%v4 = select i1 %v3, i16 %v2, i16 1

```
%v5 = udiv i16 -32768, %v4
```

%v6 = zext i16 %v5 to i32

%v7 = insertelement <8 x i32> undef, i32 %v6, i32 0

%v8 = shufflevector < 8 x i32 > %v7, < 8 x i32 > undef, < 8 x i32 > zeroinitializer

```
%v9 = load < 8 \times i16, ptr undef, align 2
```

```
%v10 = sext < 8 x i16 > %v9 to < 8 x i32 >
```

%v11 = mul nsw <8 x i32> %v8, %v10

%v12 = add nsw <8 x i32> %v11, <i32 16384, i32 16384, i32 16384,

```
i32 16384, i32 16384, i32 16384, i32 16384, i32 16384>
```

%v13 = lshr <8 x i32> %v12, <i32 15, i32 15, i

```
%v14 = trunc < 8 x i32 > %v13 to < 8 x i8 >
```

%v15 = getelementptr inbounds i8, ptr %a0, i32 undef

store <8 x i8> %v14, ptr %v15, align 1

ret void

}

```
attributes #0 = { "target-features"="+hvx,+hvx-length128b" }
; NOTE: Assertions have been autogenerated by utils/update_analyze_test_checks.py
; RUN: opt < %s -passes="print<cost-model>" 2>&1 -disable-output -mtriple=x86_64-apple-macosx10.8.0 -
mattr=+avx2 | FileCheck %s --check-prefixes=VEC256,AVX
; RUN: opt < %s -passes="print<cost-model>" 2>&1 -disable-output -mtriple=x86_64-apple-macosx10.8.0 -
mattr=+avx512vl,+prefer-256-bit | FileCheck %s --check-prefixes=VEC256,AVX512VL256
```

; RUN: opt < %s -passes="print<cost-model>" 2>&1 -disable-output -mtriple=x86_64-apple-macosx10.8.0 - mattr=+avx512vl,-prefer-256-bit | FileCheck %s --check-prefixes=AVX512VL512

```
; RUN: opt < %s -passes="print<cost-model>" 2>&1 -disable-output -mtriple=x86_64-apple-macosx10.8.0 -
mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-prefixes=VEC256,SKX256
; RUN: opt < %s -passes="print<cost-model>" 2>&1 -disable-output -mtriple=x86_64-apple-macosx10.8.0 -
mattr=+avx512vl,+avx512bw,+avx512dq,-prefer-256-bit | FileCheck %s --check-prefixes=SKX512
```

define

void @zext256() "min-legal-vector-width"="256" {

; AVX-LABEL: 'zext256'

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %A = zext < 8 x i16> undef to <8 x i64>; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %B = zext < 8 x i32> undef to <8 x i64>; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext < 16 x i8> undef to <16 x i32>; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext < 16 x i16> undef to <16 x i32>; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext < 16 x i16> undef to <16 x i32>; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext < 16 x i16> undef to <16 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %E = zext <32 x i8> undef to <32 x i16> ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; AVX512VL256-LABEL: 'zext256'

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %A = zext < 8 x i 16> undef to < 8 x i 64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: B = zext < 8 x i 32> undef to <8 x i64>

; AVX512VL256-NEXT: Cost

Model: Found an estimated cost of 2 for instruction: %C = zext <16 x i8> undef to <16 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext < 16 x i 16 > undef to < 16 x i 32 >

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext < 32 x i8> undef to <32 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; AVX512VL512-LABEL: 'zext256'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: B = zext < 8 x i 32> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext < 16 x i 16> undef to <16 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction:

&E = zext <32 x i8 > undef to <32 x i16 >

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; SKX256-LABEL: 'zext256'

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %A = zext <8 x i16> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: B = zext < 8 x i 32> undef to < 8 x i 64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = zext < 16 x i8> undef to <16 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext < 16 x i 16 > undef to < 16 x i 32 > i 32 >

; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

; SKX512-LABEL: 'zext256'

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext < 8 x i 16> undef to < 8 x i 64>

; SKX512-NEXT: Cost Model: Found an estimated

cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext < 16 x i8> undef to <16 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

 $\%A = zext <\!\!8 \ x \ i16\!\!>$ undef to $<\!\!8 \ x \ i64\!\!>$

B = zext < 8 x i 32> undef to < 8 x i 64>

%C = zext < 16 x i8 > undef to < 16 x i32 >

D = zext < 16 x i 16 undef to < 16 x i 32

&E = zext < 32 x i8 > undef to < 32 x i16 >

ret void

}

define void @zext512() "min-legal-vector-width"="512" {

; AVX-LABEL: 'zext512'

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %A = zext <8 x i16> undef to <8 x i64> ; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %B = zext <8 x i32>

undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext < 16 x i8> undef to <16 x i32>; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext < 16 x i16> undef to <16 x i32>i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %E = zext <32 x i8> undef to <32 x i16> ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; AVX512VL256-LABEL: 'zext512'

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext < 8 x i 16> undef to < 8 x i 64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: $B = zext < 8 \times i32$ undef to $< 8 \times i64$

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext < 16 x i8> undef to <16 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext < 16 x i 16 > undef to < 16 x i 32 >

; AVX512VL256-NEXT: Cost Model: Found an estimated cost

of 3 for instruction: &E = zext < 32 x i8 > undef to < 32 x i16 >

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; AVX512VL512-LABEL: 'zext512'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to

<8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64> ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext < 16 x i is undef to <16 x i32> ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32> ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16> : AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void ; SKX256-LABEL: 'zext512' ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64> ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64> ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32> ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext < 16 x i 16> undef to < 16 xi32>; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16> ; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void ; SKX512-LABEL: 'zext512' ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext < 8 x i 16> undef to < 8 xi64> ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64> ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32> ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to $<16 \times i32>$; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16> ; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void %A = zext < 8 x i16 > undef to < 8 x i64 >B = zext < 8 x i 32 > undef to < 8 x i 64 >%C = zext < 16 x i8 > undef to < 16 x i32 >%D = zext < 16 x i 16 > undef to < 16 x i 32 >%E = zext <32 x i8> undef to <32 x i16> ret void } define void @sext256() "min-legal-vector-width"="256" { ; AVX-LABEL: 'sext256' ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %A = sext <8 x i8> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %B = sext <8 x i16> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %C = sext <8 x i32> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: D = sext < 16 x i undef to < 16 x i 32>

; AVX-NEXT: Cost Model: Found

an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %F = sext <32 x i8> undef to <32 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

; AVX512VL256-LABEL: 'sext256'

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %A = sext <8 x i8> undef to <8 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: $B = \text{sext} < 8 \times 16$ undef to $< 8 \times 164$

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext < 8 x i 32 > undef to < 8 x i 64 >

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: $D = \text{sext} < 16 \text{ x i8} > \text{undef to} < 16 \text{ x i32} > 10 \text$

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext < 16 x i 16 > undef to < 16 x i 32 >

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; AVX512VL512-LABEL: 'sext256'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: $B = \text{sext} < 8 \times \text{i16} > \text{undef to} < 8 \times \text{i64} >$

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext < 8 x i 32 > undef to < 8 x i 64 >

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; SKX256-LABEL: 'sext256'

; SKX256-NEXT: Cost Model: Found an

estimated cost of 2 for instruction: %A = sext <8 x i8> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = sext <8 x i16> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = sext <16 x i8> undef to <16 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x

i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; SKX512-LABEL: 'sext256'

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64> ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>

; SKX512-NEXT: Cost

Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

%A = sext <8 x i8> undef to <8 x i64> %B = sext <8 x i16> undef to <8 x i64> %C = sext <8 x i32> undef to <8 x i64> %D = sext <16 x i8> undef to <16 x i32>

&E = sext < 16 x i 16 > undef to < 16 x i 32 >

%F = sext <32 x i8> undef to <32 x i16>

ret void

```
}
```

define void @sext512() "min-legal-vector-width"="512" {

; AVX-LABEL: 'sext512'

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %A = sext <8 x i8> undef to <8 x i64> ; AVX-NEXT: Cost Model: Found

an estimated cost of 4 for instruction: %B = sext <8 x i16> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %C = sext < 8 x i32> undef to <8 x i64> ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext < 16 x i8> undef to <16 x i32> ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext < 16 x i16> undef to <16 x i32> ; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %F = sext < 32 x i8> undef to <32 x i16> ; AVX-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %F = sext < 32 x i8> undef to <32 x i16> ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; AVX512VL256-LABEL: 'sext512'

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: B = sext < 8 x i 16> undef to < 8 x i 64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext < 8 x i 32 > undef to < 8 x i 64 >

; AVX512VL256-NEXT:

Cost Model: Found an estimated cost of 1 for instruction: %D = sext < 16 x i8 > undef to < 16 x i32 > 16 x i8 > 16

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; AVX512VL512-LABEL: 'sext512'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: $B = \text{sext} < 8 \times 16$ > undef to $< 8 \times 164>$

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext < 8 x i 32 > undef to < 8 x i 64 >

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext < 16 x i8 > undef to < 16 x i32 >

; AVX512VL512-NEXT: Cost Model: Found an estimated cost

of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; SKX256-LABEL: 'sext512'

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64> ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext < 8 x i 32 > undef to < 8 x i 64 > i

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: $%D = \text{sext} < 16 \text{ x} \text{ i8} > \text{undef to} < 16 \text{ x} \text{ i32} > 16 \text{ s} \text{ i32} > 16 \text{$

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>

; SKX256-NEXT: Cost

Model: Found an estimated cost of 0 for instruction: ret void

;

; SKX512-LABEL: 'sext512'

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64> ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x

i64>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext < 8 x i 32 > undef to < 8 x i 64 >

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x

```
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
%A = sext < 8 x i8 > undef to < 8 x i64 >
B = \text{sext} < 8 \times \text{i16} \text{-} \text{undef to} < 8 \times \text{i64}
%C = sext < 8 \times i32 > undef to < 8 \times i64 >
D = \text{sext} < 16 \text{ x i8}
undef to <16 \text{ x i} 32>
\&E = \text{sext} < 16 \text{ x i} 16 > \text{undef to} < 16 \text{ x i} 32 >
\%F = sext <32 x i8> undef to <32 x i16>
ret void
}
define void @trunc256() "min-legal-vector-width"="256" {
; VEC256-LABEL: 'trunc256'
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = trunc <8 x i64> undef to <8 x
i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %B = trunc <8 x i64> undef to <8 x
i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %C = trunc <8 x i64> undef to <8 x
i8>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = trunc < 16 x i 32 > undef to < 16 x
i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: \%E = trunc <16 x i32> undef to <16 x
i8>
; VEC256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: \%F = trunc <32 x i16> undef to <32 x
i8>
; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
; AVX512VL512-LABEL: 'trunc256'
AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = trunc <8 x i64> undef to
<8 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = trunc <8 x i64> undef to
<8 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = trunc <8 x i64> undef to
<8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc <16 x i32> undef
to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: \%E = trunc <16 x i32> undef to
<16 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: \%F = trunc <32 x i16> undef to
<32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
; SKX512-LABEL: 'trunc256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = trunc <8 x i64> undef to <8 x
i32>
```

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = trunc < 8 x i64 > undef to < 8 x i16 >; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = trunc <8 x i64> undef to <8 x i8> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc < 16 x i 32 > undef to < 16 xi16> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %E = trunc <16 x i32> undef to <16 x i8>; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %F = trunc <32 x i16> undef to <32 x i8> ; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void $%A = trunc < 8 \times i64 > undef to < 8 \times i32 >$ $B = \text{trunc} < 8 \times \text{i}64 > \text{undef to} < 8 \times \text{i}16 >$ $%C = trunc < 8 \times i64 > undef to < 8 \times i8 >$ %D = trunc < 16 x i 32 > undef to < 16 x i 16 > 16 x i 16 x i 16 > 16 x i 16 x i 16 x i 16 > 16 x i 16 > 16 x i 16&E = trunc < 16 x i 32 > undef to < 16 x i 8 >%F = trunc <32 x i16> undef to <32 x i8> ret void } define i32 @zext256_vXi1() "min-legal-vector-width"="256" { ; AVX-LABEL: 'zext256_vXi1' ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64> ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64> ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64> ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32> ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32> ; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32> ; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32> ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16> ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16> ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: % V8i16 = zext <8 x i1> undef to <8 x i16> ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16> ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>

; AVX512VL256-LABEL: 'zext256_vXi1'

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: % V4i64 = zext <4 x i1> undef to <4 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>

; AVX512VL256-NEXT:

Cost Model: Found an estimated cost of 5 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 12 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated

cost of 12 for instruction: %V16i8 = zext < 16 x i1 > undef to < 16 x i8 >

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 25 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 50 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; AVX512VL512-LABEL: 'zext256_vXi1'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: % V2i64 = zext <2 x i1> undef to <2 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: % V4i64 = zext <4 x i1> undef to <4 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of

2 for instruction: %V4i32 = zext < 4 x i1 > undef to < 4 x i32 >

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext < 16 x i1 > undef to < 16 x i32 >

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = zext < 16 x i1 > undef to < 16 x i16 >

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: % V2i8

= zext <2 x i1> undef to <2 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: % V4i8 = zext <4 x i1> undef to <4 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 19 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; SKX256-LABEL: 'zext256_vXi1'

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>

SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32> ; SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = zext < 16 x i1 > undef to < 16 x i16 >; SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i 8 >; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>; SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef ; SKX512-LABEL: 'zext256 vXi1' ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext < 2 x i1 > undef to < 2 x i64 >; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x

i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext

<4 x i1> undef to <4 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>

; SKX512-NEXT: Cost Model: Found an estimated

cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

% V2i64 = zext <2 x i1> undef to <2 x i64> % V4i64 = zext <4 x i1> undef to <4 x i64> % V8i64 = zext <8 x i1> undef to <8 x i64>

% V2i32 = zext <2 x i1> undef to <2 x i32> % V4i32 = zext <4 x i1> undef to <4 x i32> % V8i32 = zext <8 x i1> undef to <8 x i32> % V16i32 = zext <16 x i1> undef to <16 x i32>

```
%V2i16 = zext <2 x i1> undef to <2 x i16>
%V4i16 = zext <4 x i1> undef to <4 x i16>
```

```
%V8i16 = zext <8 x i1> undef to <8 x i16>
```

V16i16 = zext < 16 x i1 > undef to < 16 x i16 >

```
%V32i16 = zext <32 x i1> undef to <32 x i16>
```

```
% V2i8 = zext <2 x i1> undef to <2 x i8>
% V4i8 = zext <4 x i1> undef to <4 x i8>
% V8i8 = zext <8 x i1> undef to <8 x i8>
% V16i8 = zext <16 x i1> undef to <16 x i8>
% V32i8 = zext <32 x i1> undef to <32 x i8>
% V64i8 = zext <64 x i1> undef to <64 x i8>
```

```
ret i32 undef
```

```
}
```

define i32 @sext256_vXi1()

"min-legal-vector-width"="256" {

; AVX-LABEL: 'sext256_vXi1'

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost

of 4 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8> ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for

instruction: % V4i8 = sext <4 x i1> undef to <4 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8> ; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; AVX512VL256-LABEL: 'sext256_vXi1'

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64 ; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef

to <4 x i64>

; AVX512VL256-NEXT:

Cost Model: Found an estimated cost of 3 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: % V2i32 = sext <2 x i1> undef to <2 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction:

%V4i16 = sext <4 x i1> undef to <4 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 20 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: % V4i8 = sext <4 x i1> undef to <4 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>

;

AVX512VL256-NEXT: Cost Model: Found an estimated cost of 21 for instruction: %V32i8 = sext < 32 x i1 > undef to < 32 x i8 >

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 42 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; AVX512VL512-LABEL: 'sext256_vXi1'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32

; AVX512VL512-NEXT: Cost Model: Found an estimated

cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext < 16 x i1 > undef to < 16 x i32 >

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: % V4i16 = sext <4 x i1> undef to <4 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 15 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>

; AVX512VL512-NEXT:

Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; SKX256-LABEL: 'sext256_vXi1'

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to $< 8 \times i32 >$; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = sext < 16 x i 1 > undef to<16 x i32> ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16 ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16> ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16> : SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16> ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i16 = sext < 32 x i1 > undef to<32 x i16> ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %18 = sext i1 undef to i8 ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8> ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8> ; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i 8 >; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef ; SKX512-LABEL: 'sext256_vXi1' ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64 ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64> ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64> ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64> ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32 ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32> ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32> ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32> ; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>

; SKX512-NEXT: Cost Model:

Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>

;

SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

%I64 = sext i1 undef to i64

%V2i64 = sext <2 x i1> undef to <2 x i64>

%V4i64 = sext < 4 x i1 > undef to < 4 x i64 >

V8i64 = sext < 8 x i1 > undef to < 8 x i64 >

%I32 = sext i1 undef to i32 %V2i32 = sext <2 x i1> undef to <2 x i32> %V4i32 = sext <4 x i1> undef to <4 x i32> %V8i32 = sext <8 x i1> undef to <8 x i32> %V16i32 = sext <16 x i1> undef to <16 x i32>

```
%I16 = sext i1 undef to i16
%V2i16 = sext <2 x i1> undef to <2 x i16>
%V4i16 = sext <4 x i1> undef to <4 x i16>
%V8i16 = sext <8 x i1> undef to <8 x i16>
%V16i16 = sext <16 x i1> undef to <16 x i16>
%V32i16 = sext <32 x i1> undef to <32 x i16>
```

```
%I8 = sext i1 undef to i8
%V2i8 = sext <2
x i1> undef to <2 x i8>
%V4i8 = sext <4 x i1> undef to <4 x i8>
```

% V8i8 = sext <8 x i1> undef to <8 x i8> % V16i8 = sext <16 x i1> undef to <16 x i8> % V32i8 = sext <32 x i1> undef to <32 x i8> % V64i8 = sext <64 x i1> undef to <64 x i8>

ret i32 undef

}

define i32 @trunc_vXi1() "min-legal-vector-width"="256" {

; AVX-LABEL: 'trunc_vXi1'

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 46 for instruction: %V64i64

= trunc <64 x i64> undef to <64 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 17 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 34 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>

; AVX-NEXT: Cost Model: Found an

estimated cost of 0 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 18 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1> ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1> ; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1> ; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>

;

AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: % V64i8 = trunc <64 x i8> undef to <64 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; AVX512VL256-LABEL: 'trunc_vXi1'

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc < 2 x i64 > undef to < 2 x i1 >

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: V4i64 = trunc <4 x i64 > undef to <4 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: % V8i64 = trunc <8 x i64> undef to <8 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 22 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 44 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>

; AVX512VL256-NEXT:

Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: $V4i32 = trunc < 4 \times i32 > undef to < 4 \times i1 >$

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = trunc < 16 x i32 > undef to < 16 x i1 >

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 16 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = trunc <2 x i16 undef to <2 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: V4i16 = trunc <4 x i16 undef to <4 x i1>

; AVX512VL256-NEXT: Cost Model: Found

an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: V16i16 = trunc < 16 x i16 > undef to < 16 x i1 >

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 16 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 32 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = trunc <2 x i8> undef

to <2 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: % V4i8 = trunc <4 x i8> undef to <4 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: % V8i8 = trunc <8 x i8> undef to <8 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated

cost of 17 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 34 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; AVX512VL512-LABEL: 'trunc_vXi1'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: % V16i64 = trunc <16 x i64> undef to <16 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 22 for instruction: % V32i64 = trunc <32 x i64> undef to <32 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost

of 44 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: % V2i16 = trunc <2 x i16> undef to <2 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction:

%V4i16 = trunc <4 x i16> undef to <4 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 14 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1> ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x il>; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = trunc <8 x i8> undef to $<8 \times 1^{>}$; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1> ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 15 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1> ; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef ; SKX256-LABEL: 'trunc_vXi1' ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i l >; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i l >; SKX256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x il>; SKX256-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x il>SKX256-NEXT: Cost Model: Found an estimated cost of 47 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i 1 >; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 19 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: % V2i8 = trunc <2 x i8> undef to <2 x i1>; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: % V8i8 = trunc <8 x i8> undef to <8 x i1> : SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1> ; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef ; SKX512-LABEL: 'trunc_vXi1' ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i l >; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i l >; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i l >; SKX512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x il>; SKX512-NEXT: Cost Model: Found an estimated cost of 47 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i l >; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i l >; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>; SKX512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: % V2i8 = trunc <2 x i8> undef to <2 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1> : SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1> ; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef %V2i64 = trunc <2 x i64> undef to <2 x i1> %V4i64 = trunc <4 x i64> undef to <4 x i1> %V8i64 = trunc <8 x i64> undef to <8 x i1> %V16i64 = trunc < 16 x i64 > undef to < 16 x i1 >V32i64 = trunc <32 x i64 > undef to <32 x i1>%V64i64 = trunc < 64 x i64 > undef to < 64 x i1 > $V_{2i32} = trunc < 2 x i 32 > undef to < 2 x i 1>$ V4i32 = trunc < 4 x i32 > undef to < 4 x i1 >%V8i32 = trunc <8 x i32> undef to <8 x i1> V16i32 = trunc < 16 x i32 > undef to < 16 x i1 >%V32i32 = trunc <32 x i32> undef to <32 x i1> %V64i32 = trunc < 64 x i32 > undef to < 64 x i1 >%V2i16 = trunc <2 x i16> undef to <2 x i1> %V4i16 = trunc <4 x i16> undef to <4 x i1> %V8i16 = trunc <8 x i16> undef to <8 x i1> %V16i16 = trunc<16 x i16> undef to <16 x i1> %V32i16 = trunc <32 x i16> undef to <32 x i1> %V64i16 = trunc < 64 x i16 > undef to < 64 x i1>%V2i8 = trunc <2 x i8> undef to <2 x i1> %V4i8 = trunc <4 x i8> undef to <4 x i1>

```
% V8i8 = trunc <8 x i8> undef to <8 x i1>
%V16i8 = trunc < 16 x i8 > undef to < 16 x i1 >
%V32i8 = trunc < 32 x i8 > undef to < 32 x i1 >
%V64i8 = trunc < 64 x i8 > undef to < 64 x i1 >
ret i32 undef
}
; RUN: llc -O3 -mtriple=powerpc-unknown-linux-gnu -mcpu=e500 -mattr=spe < %s | FileCheck %s
; PowerPC SPE is a rare in-tree target that has the FP TO SINT node marked
; as Legal.
; Verify that fptosi(42.1) isn't simplified when the rounding mode is
; unknown.
; Verify that no gross errors happen.
; CHECK-LABEL: @f20
; COMMON: cfdctsiz
define i32 @f20(double %a) strictfp {
entry:
%result = call i32 @llvm.experimental.constrained.fptosi.i32.f64(double 42.1,
                            metadata !"fpexcept.strict")
                            strictfp
ret i32 % result
}
```

@llvm.fp.env = thread_local global i8 zeroinitializer, section "llvm.metadata" declare i32 @llvm.experimental.constrained.fptosi.i32.f64(double, metadata) Copyright (c) 2019 Intel Corporation. All rights reserved.

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add_lldb_library(lldbPluginObjectContainerBSDArchive PLUGIN ObjectContainerBSDArchive.cpp

LINK_LIBS lldbCore lldbHost lldbSymbol LINK_COMPONENTS Support)

5 1 1

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; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature -- scrub-attributes

; RUN: opt -S -passes=argpromotion < %s | FileCheck %s

; Test that we only promote arguments when the caller/callee have compatible

; function attrubtes.

target triple = "x86_64-unknown-linux-gnu"

```
; This should promote
```

```
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr %arg, ptr readonly %arg1) #0 {
```

```
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; CHECK-SAME: (ptr [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], ptr [[ARG]]
```

```
; CHECK-NEXT: ret void
```

;

```
bb:
%tmp = load <8 x i64>, ptr %arg1
store <8 x i64> %tmp, ptr %arg
ret void
```

```
}
```

```
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr %arg) #0 {
    ; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
    ; CHECK-SAME:
    (ptr [[ARG:%.*]])
    ; CHECK-NEXT: bb:
    ; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
    ; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
    ; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, ptr [[TMP]]
    ; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr
    [[TMP2]], <8 x i64> [[TMP_VAL]])
    ; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
    ; CHECK-NEXT: ret void
    ; CHECK-NEXT: ret void
```

```
bb:
```

```
\%tmp = alloca <8 x i64>, align 32
\%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> % tmp4, ptr % arg, align 2
ret void
}
; This should promote
define
internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr %arg, ptr readonly
%arg1) #1 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], ptr [[ARG]]
; CHECK-NEXT: ret void
bb:
\%tmp = load <8 x i64>, ptr % arg1
store <8 x i64> % tmp, ptr % arg
ret void
}
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr % arg) #1 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, ptr [[TMP]]
; CHECK-NEXT: call fastcc
void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr [[TMP2]], <8 x i64>
[[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CHECK-NEXT: ret void
:
bb:
\%tmp = alloca <8 x i64>, align 32
\%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
```

```
ret void
}
```

; This should promote

```
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr % arg, ptr
readonly %arg1) #1 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1 VAL]],
ptr [[ARG]]
; CHECK-NEXT: ret void
bb:
\%tmp = load <8 x i64>, ptr % arg1
store <8 x i64> %tmp, ptr %arg
ret void
}
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr % arg) #0 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, ptr [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CHECK-NEXT: ret void
:
bb:
```

```
\%tmp = alloca <8 x i64>, align 32
```

```
\%tmp2 = alloca <8 x i64>, align
```

```
32
```

call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)

```
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(ptr %tmp2, ptr %tmp)
\%tmp4 = load <8 x i64>, ptr %tmp2, align 32
```

```
store <8 x i64> %tmp4, ptr %arg, align 2
```

```
ret void
```

```
}
```

; This should promote

define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr %arg, ptr readonly % arg1) #0 {

; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512

```
; CHECK-SAME: (ptr [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], ptr [[ARG]]
; CHECK-NEXT: ret void
bb:
\%tmp = load <8 x i64>, ptr % arg1
store <8 x i64> % tmp, ptr % arg
ret void
}
define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr % arg) #1 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (ptr [[ARG:%.*]])
; CHECK-NEXT:
 bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, ptr [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CHECK-NEXT: ret void
bb:
\%tmp = alloca <8 x i64>, align 32
\%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}
; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr
% arg, ptr readonly % arg1) #1 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]], ptr readonly [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1]]
; CHECK-NEXT: store <8 x i64> [[TMP]], ptr [[ARG]]
; CHECK-NEXT: ret void
;
bb:
\%tmp = load <8 x i64>, ptr % arg1
```

```
store <8 x i64> %tmp, ptr %arg
ret void
}
```

```
define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr % arg) #2 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr
[[TMP2]], ptr [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
: CHECK-NEXT: ret void
:
bb:
\%tmp = alloca <8 x i64>, align 32
\%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}
; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr % arg, ptr
readonly % arg1) #2 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]], ptr readonly [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, ptr [[ARG1]]
; CHECK-NEXT: store <8 x i64>
[[TMP]], ptr [[ARG]]
; CHECK-NEXT: ret void
:
bb:
\%tmp = load <8 x i64>, ptr % arg1
store <8 x i64> %tmp, ptr %arg
ret void
}
define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr % arg) #1 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]])
: CHECK-NEXT: bb:
```

```
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr
[[TMP2]], ptr [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CHECK-NEXT: ret void
:
bb:
\%tmp = alloca <8 x i64>, align 32
\%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64
32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}
; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr %arg, ptr readonly
%arg1) #3 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], ptr [[ARG]]
; CHECK-NEXT: ret void
bb:
\%tmp = load <8 x i64>, ptr % arg1
store <8 x i64> %tmp, ptr %arg
ret void
}
define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr %arg) #4 {
; CHECK-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:
  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, ptr [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(ptr
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
```

```
; CHECK-NEXT: ret void
bb:
\%tmp = alloca <8 x i64>, align 32
\%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee avx2 legal256 prefer256 call avx2 legal512 prefer256(ptr %tmp2, ptr %tmp)
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}
; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr %arg, ptr readonly
%arg1) #4 {
CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], ptr [[ARG]]
; CHECK-NEXT: ret void
•
bb:
\%tmp = load <8 x i64>, ptr % arg1
store <8 x i64> % tmp, ptr % arg
ret void
}
define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr % arg) #3 {
; CHECK-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (ptr [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: call void @llvm.memset.p0.i64(ptr align 32 [[TMP]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, ptr [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load
<8 x i64>, ptr [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], ptr [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
\%tmp = alloca <8 x i64>, align 32
\%tmp2 = alloca <8 x i64>, align 32
call void @llvm.memset.p0.i64(ptr align 32 %tmp, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(ptr %tmp2, ptr %tmp)
```

```
%tmp4 = load <8 x i64>, ptr %tmp2, align 32
store <8 x i64> %tmp4, ptr %arg, align 2
ret void
}
; If the arguments are scalar, its ok to promote.
define internal i32 @scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr %X, ptr %Y)
#2 {
; CHECK-LABEL: define
{{[^@]+}}@scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (i32 [[X_VAL:%.*]], i32 [[Y_VAL:%.*]])
; CHECK-NEXT: [[C:%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
; CHECK-NEXT: ret i32 [[C]]
%A = load i32, ptr %X
\%B = load i32, ptr %Y
%C = add i 32 %A, %B
ret i32 %C
}
define i32 @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr
%B) #2 {
; CHECK-LABEL: define {{[^@]+}}@scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (ptr [[B:%.*]])
; CHECK-NEXT: [[A:%.*]] = alloca i32
; CHECK-NEXT: store i32 1, ptr [[A]]
; CHECK-NEXT: [[A_VAL:%.*]] = load i32, ptr [[A]]
; CHECK-NEXT: [[B_VAL:%.*]] = load i32, ptr [[B]]
; CHECK-NEXT: [[C:%.*]] = call i32
@scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32 [[A_VAL]], i32 [[B_VAL]])
; CHECK-NEXT: ret i32 [[C]]
%A = alloca i32
store i32 1, ptr %A
%C = call i32 @scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(ptr %A, ptr %B)
ret i32 %C
}
; If the arguments are scalar, its ok to promote.
define internal i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr %X, ptr %Y)
#2 {
; CHECK-LABEL: define
{{[^@]+}}@scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (i32 [[X_VAL:%.*]],
i32 [[Y_VAL:%.*]])
; CHECK-NEXT: [[C:%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
; CHECK-NEXT: ret i32 [[C]]
:
```

```
%A = load i32, ptr %X
\%B = load i32, ptr \%Y
%C = add i 32 %A, %B
ret i32 %C
}
define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr %B) #2 {
; CHECK-LABEL: define {{[^@]+}}@scalar_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (ptr [[B:%.*]])
; CHECK-NEXT: [[A:%.*]] = alloca i32
; CHECK-NEXT: store i32 1, ptr [[A]]
; CHECK-NEXT: [[A_VAL:%.*]] = load i32, ptr [[A]]
; CHECK-NEXT: [[B_VAL:%.*]] = load i32, ptr [[B]]
; CHECK-NEXT: [[C:%.*]] = call i32
@scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32 [[A_VAL]], i32 [[B_VAL]])
; CHECK-NEXT: ret i32 [[C]]
%A = alloca i32
store i32 1, ptr %A
%C = call i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(ptr %A, ptr %B)
ret i32 %C
}
; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0.i64(ptr
nocapture writeonly, i8, i64, i1) #5
attributes \#0 = \{ inline hint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="512" }
attributes #1 = \{ inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="256" }
attributes #2 = \{ inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="256" "prefer-vector-width"="256" }
```

```
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
```

```
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
```

```
attributes #5 = { argmemonly nounwind }
```

1.23 ragel 6.10

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```
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```

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1.24 curl 8.3.0

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1.25 bcc 0.28.0

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